Redundant Three-Phase AC to DC Converter using Single-Phase CUK Rectifier Module with Minimized DC Bus Capacitance

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Abstract— **This paper presents a redundant three-phase ac to dc converter using single-phase CUK rectifier module with nearly power factor and minimized dc bus capacitance based on power balance control technique. The focus of the proposed control strategy is to reduce the dc bus capacitance value under condition step load change from 10% (75W) to 100% (750W). Using power balance control technique does minimized dc bus capacitance, inductor current sharing, redundant operation, high power factor and tight dc bus voltage works on the principle of modular three-phase rectifier with parallel single-phase CUK rectifier module. Simulation results are used to illustrate the operation and performance features of the modular three-phase rectifiers.**

I. INTRODUCTION

Increasing demand for high power converters in telecommunication, and computer power supplies drives the need for higher flexibility in control, increased level of system integration, and more reliability, besides achieving high levels of performance [1]. In recent years, the low harmonic current in line side is required by the legislation of regulations for controlling harmonics [2]-[5]. The power range of the switching mode power supplies (SMPS) market starts from a few watts to some kilowatts. In the kilowatt range, the telecommunication power supplies form the major part of the SMPS market [6]-[7]. The supply voltage of most telecommunication switching equipment is 48V [8]-[12]. This voltage value is a universal standard for telecommunications equipment, and is well defined both by the European Telecommunications Standards Institute (ETSI) and the American National Standards Institute (ANSI). A 48V dc power supply system consists of a number of paralleled rectifiers that connected to one or more battery strings also connected in parallel. Generally, the power levels of the rectifier modules involved in telecommunication applications are 750W or 1,500W [13]-[15].

The conventional dc 48 V output power supply for the telecommunication system have the three-phase PWM rectifier in the first in order to obtain the sinusoidal input current waveforms [16]-[20]. In addition to this, the conventional power supplies have the dc to dc converter which is isolated between input side and output one in second steps to obtain the dc -48 V. As described above, the conventional power supply is proposed of two power converter; three-phase PWM rectifier [21]-[25] and dc to dc converter. For this reason, the conventional power supply cause the low power efficiency and high cost. Also, a dc capacitor smoothing the intermediate voltage together with a voltage detector to control this voltage is required. To solve this problem, the power conversion system which has CUK converter is has been already proposed. Using the CUK converter, this power conversion system can convert three-phase ac input power into the isolated dc output power.

However, the capacitor technology has been getting more and more attention in industry application. The dc bus capacitor is the most important passive component in a telecommunication system. Conventional designs have been using a set of electrolytic bulk capacitors to smooth dc bus voltage.

So, the first issue of this paper presents a three-phase ac to dc converter using CUK rectifier module which can directly convert 3-phase ac input into the dc -48 V output with minimized dc bus capacitor. The proposed rectifier consists of three power converter which is connected in 3-phase line to neutral. Controlled the duty factor of each active switch, the proposed rectifier occur the sinusoidal waveforms with power factor of unity. The benefit of the proposed control strategy is excellent power factor correction, good inductor current sharing and fast dynamic transient response with minimized dc bus capacitance. Significant results are (1) size reduction, (2) cost reduction, and (3) transient response improvement.

In the second issue, redundant rectifiers meet two needs: battery recharging after mains outage and continued operation if one rectifier fails. The design concept and the feasible performance evaluations of the redundant three-phase ac to dc converter using single-phase isolated CUK rectifier module is discussed.

The objectives of this paper are: minimized dc bus capacitance, redundancy (n+1), inductor current sharing, nearly unity power factor, low harmonic distortion, and improve dynamic transient response. Simulation results are presented. It's in agreement with the theoretical analysis.

II. Reduction of DC Bus Capacitance With Three-Phase AC to DC Converter Based on Power Balance Control Technique

Fig. 1 shows power circuit of the modular three-phase ac to dc converter. In this topology, three identical single-phase isolated CUK rectifier modules are used. They are connected in parallel on a common dc bus to feed the dc load. The rectifier is termed as Y-connected. A power balance control technique is employed to give a fast dynamic transient response. The objectives of the proposed control strategy are to eliminate harmonics, inductor current sharing, regulated dc output voltage and meet the transient response requirements of step load change and minimized dc bus capacitance.

A. Average Small-Signal Analysis

The average small signal model of the modular three-phase ac to dc converter using CUK rectifier module based on power balance control technique is :

$$3V_{gi}\,I_{L1i} = V_o I_o \tag{1}$$

V_{gi} is RMS value of the rectifier voltage, I_{L1i} is RMS value of the inductor current, V_o is average output voltage and I_o is average output current. The peak value of the inductor current is

$$\hat{I}_{L1i} = \frac{K_2 V_o I_{load}}{3V_{gi}} \tag{2}$$

$$\hat{I}_{Lref1i} = \hat{I}_{L1i} + I_{VR} \tag{3}$$

$\hat{I}_{Lref1i}$ is peak value of the inductor reference current, $\hat{I}_{L1i}$ is peak value of the inductor current, I_{VR} is correcting signal from PI regulator and K_2 is conversion gain of inductor current. The inductor reference current is :

$$i_{Lref11} = \hat{I}_{Lref11}\left|\sin(\omega t)\right| \tag{4}$$

$$i_{Lref12} = \hat{I}_{Lref12}\left|\sin(\omega t - 120^\circ)\right| \tag{5}$$

$$i_{Lref13} = \hat{I}_{Lref13}\left|\sin(\omega t - 240^\circ)\right| \tag{6}$$

The dynamic equation at common dc bus is

$$\sum_{i=1}^{3} I_{L2i} = C_2 \frac{dV_o}{dt} + I_{load} \tag{7}$$

Where the $\bar{V}$ means steady-state value and $\tilde{v}$ means small-signal value. Applying the perturbations in (1), (2), (3), and (7), and performing the small-signal approximation ($\tilde{v}\,.\,\tilde{v}=0$) results in :

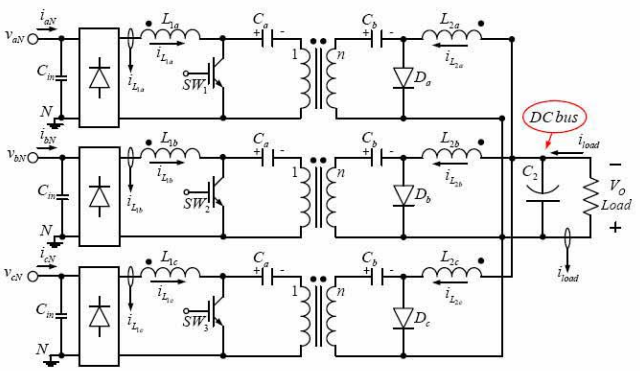

Fig. 1. Modular three-phase ac to dc converter using isolated CUK rectifier module with minimized dc bus capacitance based on power balance control technique.

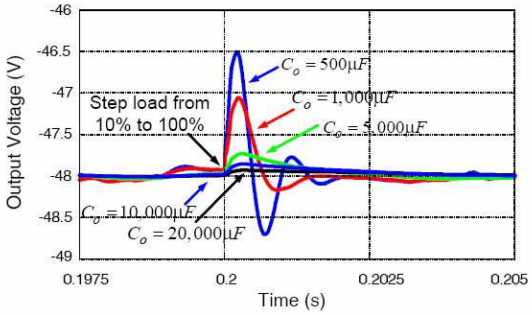

Fig. 2. Simulation result of transient response at common dc bus capacitor when step load change from 10% (75 W) to 100% (750 W).

$$\tilde{i}_o = \frac{3K_1\bar{\hat{I}}_{Lref1i}}{\bar{V}_o}\tilde{v}_{gi} + \frac{3K_1\bar{V}_{gi}}{\bar{V}_o}\tilde{\hat{i}}_{Lref1i} - \frac{\bar{I}_o}{\bar{V}_o}\tilde{v}_o \tag{8}$$

$$\tilde{i}_o = C_2\frac{d\tilde{v}_o}{dt} + \tilde{i}_{load} \tag{9}$$

$$\tilde{i}_{Lref1i} = \tilde{i}_{L1i} + \tilde{i}_{VR} \tag{10}$$

$$\tilde{\hat{i}}_{L1i} = \frac{K_2\bar{V}_o}{3\bar{V}_{gi}}\tilde{i}_{load} + \frac{K_2\bar{I}_{load}}{3\bar{V}_{gi}}\tilde{v}_o - \frac{K_2\bar{V}_o\bar{I}_{load}}{3\left(\bar{V}_{gi}\right)^2}\tilde{v}_{gi} \tag{11}$$

The transfer function of the proposed system is :

$$\frac{\tilde{v}_o}{\tilde{v}_{oref}} = \frac{3G_{VR}\bar{V}_{gi}K_1}{\bar{V}_o C_2 S + 3G_{VR}\bar{V}_{gi}K_1 k_{fb}} \tag{12}$$

Here, a PI regulator is

$$G_{VR}(s) = \frac{k_p\left(S+\omega_Z\right)}{S} \tag{13}$$

The proposed topology transfer function is :

$$PTF = \frac{3\bar{V}_{gi}K_1 k_{fb}}{(\bar{V}_o C_2)S} \tag{14}$$

Open loop transfer function is :

$$OLTF = \frac{3G_{VR}(s)\bar{V}_{gi}K_1 k_{fb}}{(\bar{V}_o C_2)S} \tag{15}$$

B. Performance of Three-Phase Rectifier with Minimized DC Bus Capacitance Base on Power Balance Control Technique

An average small-signal model of the modular three-phase rectifier has been shown in Eq. (12). The simulation result of the proposed system is considered. Analysis of steady-state and transient operation of the proposed system is presented. The control strategy provides a fast transient response under load disturbances condition. Such a fast response, in turn, minimizes the overshoot, droop and the settling time of the output voltage. The control strategy also provides the desired current sharing between the paralleled isolated CUK converters even during transients.

The proposed system which consists of a modular 250W CUK dc to dc converter with diode front end rectifier and a single dc bus capacitor. It was simulated for different dc bus capacitance values. A rated operation of 750W output power and -48V of dc output voltage with 220V of ac line-to-neutral voltage are assumed. The dc bus voltage is measured for the feedback control purposes. In addition, in order to improve dynamic response in the dc voltage control, load current and input voltage is also measured and added to the inductor current amplitude reference as load feedforward. The simulated results are discussed below. The steady state and dynamic performance of proposed topology is shown in Fig. 2 to Fig. 6. As a dynamic response example, Fig. 2 shows the simulation results of a sudden load change requiring changing over from 75W to 750W (ΔP_O = 0.675 kW) for various output capacitance value (500 μF, 1,000 μF, 5,000 μF, 10,000 μF and 20,000 μF). Figure 2 shows that the Δ_{Vdroop} of output voltage at the common dc bus capacitor is reduced when the power balance control technique is employed. By utilizing feedfoward, the low bandwidth of the voltage control loop is well compensated and the dc-link voltage is hardly disturbed. Transient response analysis for this paper is based upon Δ_{Vdroop} , $\Delta_{Vovershoot}$ and settling time of output voltage for the dc bus capacitor chosen as various values. The influence of its value is shown in Fig. 3. The Δ_{Vdroop} and $\Delta_{Vovershoot}$ is typically unsymmetrical. The $\Delta_{Vovershoot}$ is higher than Δ_{Vdroop} for C_2 < 1,000 μF. However, for high values of dc bus capacitor with 1,500 μF ≤ C_2 ≤ 20,000μF, the Δ_{Vdroop} and $\Delta_{Vovershoot}$ is nearly equal and Δt of the settling time is 1.2 ms.

Fig 4 and Fig 5 shows the comparison of $\pm\Delta v_O$ and settling time of dc bus voltage due to the step load change from 100% to 10% and vice versa. The output voltage waveforms represent the results corresponding to value of capacitor output at 700 μF, 800 μF, 900 μF, 1,000 μF, and 2,000 μF respectively. The comparison between the results indicates that the small voltage dips and less variant in response trajectories are yielded by applying power balance control technique. Although the smaller value of output capacitor is chosen, the better control is obtained, the compromise between control performance and output capacitor should be considered. Thus C_2= 1,500 μF will be adopted in the common dc bus capacitor at load terminal.

Simulation results of the proposed system with a nominal output power of P_O = 750W operating at balanced and unbalanced three-phase mains (220V line to neutral voltage) are shown in Fig. 6. The simulation does analyze the following modules and load condition : 0…100ms: symmetric mains, 100…200ms: two-phase supply (main phase a loss), 200…300ms: return of the missing main phase, 300…400ms: one-module loss (in phase a), 400…500ms: step load change from 100% to 10% under one-module loss (in phase a) and 500…600ms: step load change from 10% to 100% under one-module loss (in phase a).

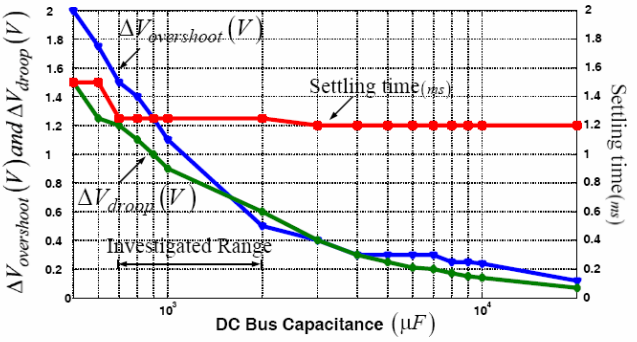

Fig. 3. The Δ_{Vdroop} (V), $\Delta_{Vovershoot}$ (V) and Settling time (ms) comparison of DC bus capacitor components.

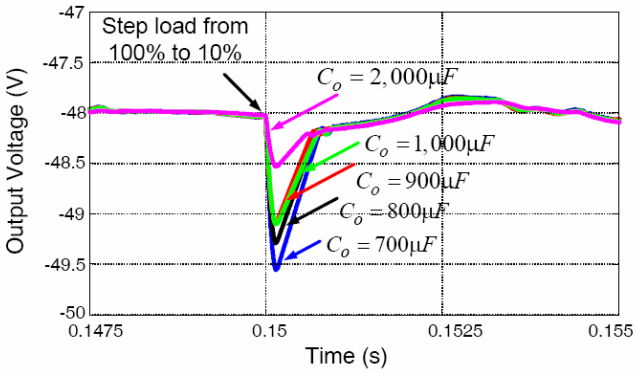

Fig. 4. The transient performance indexes at different values of a common dc bus capacitor when step load change from 10% (75 W) to 100 %.(750 W).

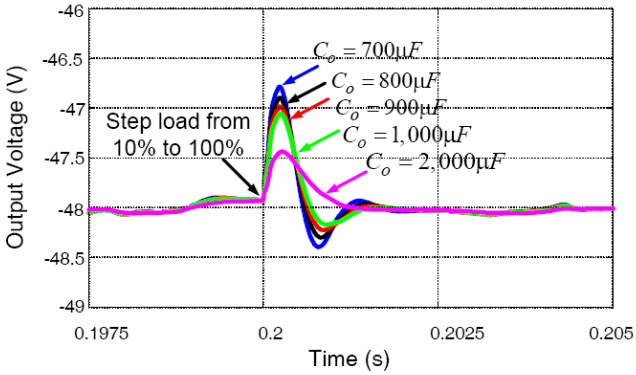

Fig. 5. The transient performance indexes at different values of a common dc bus capacitor when step load change from 100% (750 W) to 10% (75 W).

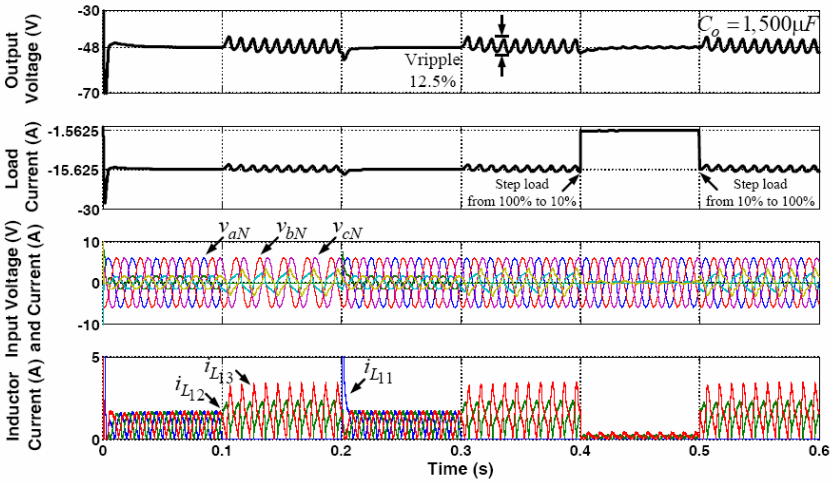

Fig. 6. Time behavior of the dc output voltage v_o , the load current i_{load} , the line to neutral voltages v_{xN} (x=a,b,c) , the individual line current i_{sx} (x=a,b,c) and the individual inductor current i_{lj} (j=$1,2,3$) for symmetric mains condition, mains phase a loss, power module # in phase a fault and a load step from 100% (750 W) to 10% (75 W) and vice versa under power module in phase a fault.

At t = 100 ms, the loss of the main phase a does occur. The calculation of the rms value of the main line to neutral voltage does require a minimal calculation time of t_A = 10 ms, resulting in a temporarily false value of the input phase current. These wrong value do cause a significant drop of the output voltage (v_o) and load current (i_{load}) during the time period t = 100…110 ms. As soon as the rms value is calculated correctly the rapid fall of the output voltage is stopped due to the PI controller increased value of the reference inductor current. A detailed view on the return of the missing phase a at t = 200 ms is given in Fig. 6. The phase currents i_{saN} , i_{sbN} and i_{scN} do increase very rapidly because of the values of the correcting signal. The behavior for a loss of module in phase a shown in Fig. 6 within the time interval t = 300…600 ms. Again the delayed calculation of the peak values of the inductor current does cause a drop of the dc output capacitor voltage within the time interval t = 300…320 ms. A load variation within the time interval t = 400…500 ms. The simulation result of transient response of the output voltage and current waveforms at load change from 750 W to 75 W and vice versa are shown in Fig. 6 (C_2 = 1,500 μF). A load dump at t=400 ms is completely handled by the power balance control technique. However, it has been found from this study that the three-phase connection of three-phase rectifier modules under loss condition of module in phase a offers drawback such as : very large output voltage ripple at the common dc bus capacitor (v_{ripple}=12.5%), this significantly increases capacitor heating and does not improves its operating life, high THD_i and low power factor. So, redundancy is required when continuous operation of the system is required in mission critical applications.

III. Redundant Operation

Redundancy (n+1) : in determining the number of the modules it should be taken into account that for the reason of safety at least two rectifier modules must be installed (n≥2). It is an additional requirement that the power supply system must meet the requirement of the telecommunications load even in the case of a module fault.

There are a number of ways to construct redundant or fault-tolerant power systems. The most common method is to have at least one supply with sufficient output power to fully satisfy the system's power requirements. Then, a redundant power supply of the exact same ratings is provided as a "back-up" in the event one of the three supplies fails. This forms a basic n+1 redundant and fault-tolerant power system (3+1 system). "n" equals the number of supplies required to fully three-phase ac to dc converter and "+1" equals one back-up or redundant supply that will take over for a failed supply. "n" must consist of three power supplies, each providing 33.3% of the total load power with "+1" supply having the same power rating as the others. One advantage of this type of power system (3+1) is that under normal operating conditions each of the three main power supplies are only providing 33.3% of the total system power, thus reducing the thermal stress on each supply, and improving the reliability of the distributed power system.

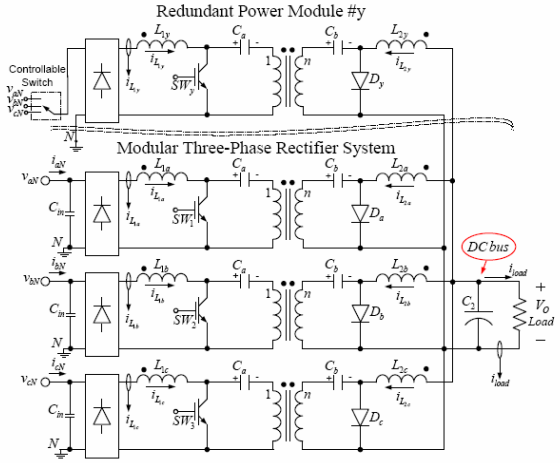

Fig. 7. Redundant three-phase ac to dc converter using single-phase CUK rectifier module with minimized dc bus capacitor (Number of module 3+y) based on power balance control technique.

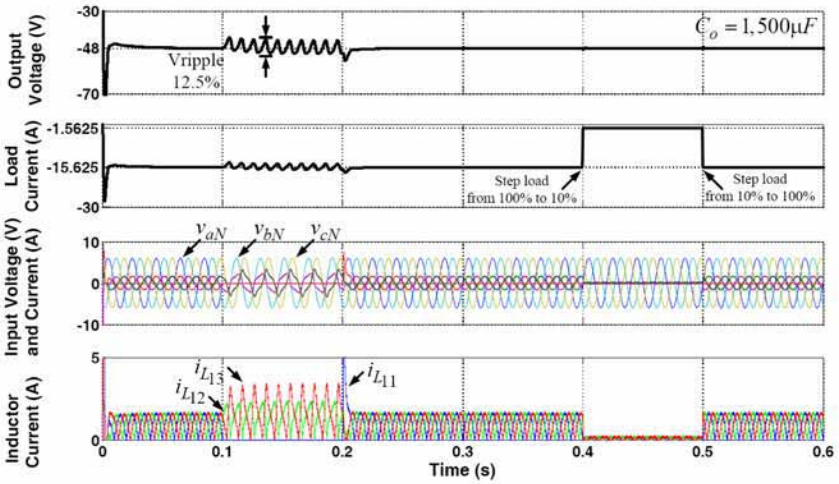

Fig. 8. Time behavior of the dc output voltage v_o , the load current i_{load} , the line to neutral voltages v_{xN} $(x=a,b,c)$, the individual line current i_{sx} $(x=a,b,c)$ and the individual inductor current i_{Lj} $(j=1,2,3)$ for symmetric mains condition, mains phase a loss, power module # in phase a fault and a load step from 100% (750 W) to 10% (75 W) and vice versa under redundant power system condition.

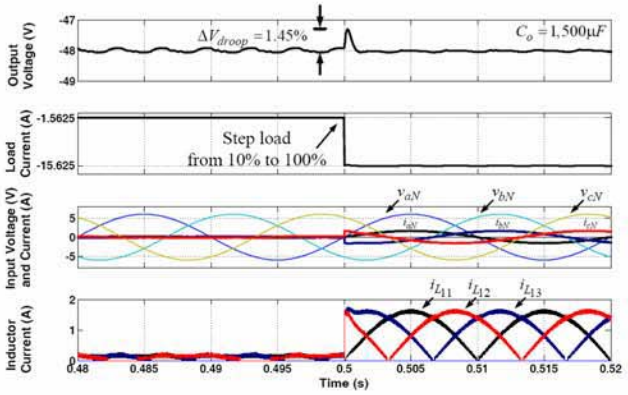

Fig. 9. Closed up of transient responses when i_{load} is changed from -1.5625 A (75 W) to -15.625 A (750 W). [v_o : output voltage (1 V/div), i_L : inductor current (1 A/div), i_{sN} : line current (5 A/div), v_{sN} : line to neutral voltage (300 V/div) and t : time (5ms/div)] with a common dc bus capacitor at 1,500 µF based on power balance control technique.

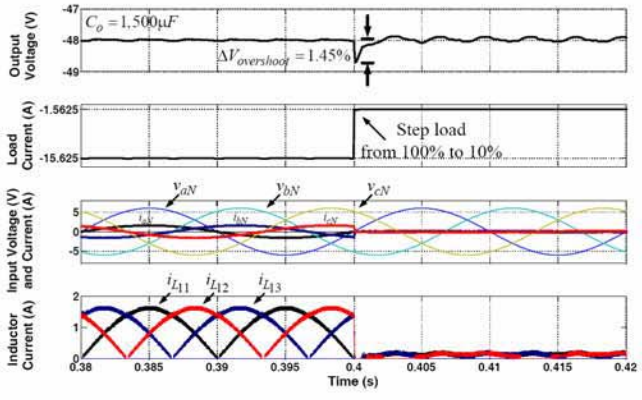

Fig. 10. Closed up of transient responses when i_{load} is changed from -15.625 A (750 W) to -1.5625 A (75 W). [v_o : output voltage (1 V/div), i_L : inductor current (1 A/div), i_{sN} : line current (5 A/div), v_{sN} : line to neutral voltage (300 V/div) and t : time (5ms/div)] with a common dc bus capacitor at 1,500 µF based on power balance control technique.

Performance characteristics of the redundant three-phase ac to dc converter using isolated single-phase CUK rectifier module with minimized dc bus capacitance based on power balance control technique are given in Figs. 8-10 illustrating the steady state and transient behavior at different loads under balance condition.

The simulation results of the proposed system in Fig. 7 with operating at balanced and unbalanced three-phase mains under redundant power system condition are shown in Fig. 8. The simulation does analyze the following modules and load conditions : 0…100ms : symmetric mains, 100…200ms : two-phase supply (main phase a loss), 200…300ms : return of the missing main phase, 300…600ms : at this time redundant power system condition has been began (one-module loss in phase a), 400…500ms: step load change from 100% to 10% and 500…600ms: step load change from 10% to 100%.

Fig. 9 shows the source voltage, 3-phase currents, individual inductor current, load current and dc bus voltage when step load change from 10% (75 W) to 100% (750 W). The source currents respond very quickly and settle to steady state value within a 1.2 ms. The individual inductor current increases almost instantaneously to feed the increased load current demand by taking the energy instantaneously from dc bus capacitor. Output voltage recovers within 1.2 ms. Source currents always remain sinusoidal and power factor nearly unity. Fig. 10 shows similar results as in Fig. 9 for sudden decrease of load. The proposed topology power supplied from source is decreased form 100 % (750 W) to 10% (75 W). Source currents settle to steady state value within 1.2 ms demonstrating the excellent transient response of the DC bus voltage rises only to 48.696 V but reaches the steady state value within 1.2 ms. Source currents remain always nearly sinusoidal under all operating conditions. The proposed topology meets the requirements of harmonic components of source current and maintains the source currents sinusoidal in transient and steady state conditions. The performance of the proposed control algorithm of the proposed topology is found

to be excellent and the source current is practically sinusoidal and in phase with the source voltage. The fast response of the proposed topology ensures that the proposed topology is not overburdened during transient conditions. The voltage ripple is quite small in dc bus capacitor voltage and may be reduced further by increasing the capacitor value. $\Delta V_{overshoot}$ in dc bus voltage is observed to be $\approx$ 1.45 % during transients which may be controlled by the design to a lower value but at the expense of increased value of dc bus capacitor.

In summary, we have discussed how you can provide increased reliability by connecting one or more power supplies in parallel. We have also covered how to construct an n+1 redundant and fault-tolerant power system and the features required of the supplies in order to accomplish this with the greatest amount of reliability and ease of system maintenance.

IV. Conclusions

Analysis, design and simulation of the redundant three-phase ac to dc converter using single-phase isolated CUK rectifier module with nearly unity power factor and minimized dc bus capacitor are studies. It's operated based on power balance control technique. The proposed control strategy provides fast transient response and good inductor current sharing. In order to improve dynamic response in the dc voltage control, load current and input voltage is also measured and added to the inductor current loop. The condition under mains failure (loss of one main phase), module loss and heavily step load change has been presented.

In this case, DC bus capacitor $C_2 = 1{,}500\ \mu F$ according to Δ_{Vdroop} , $\Delta_{Vovershoot}$ and settling time of output voltage. The proposed method is based on the reliability and electrical performance for these rectifiers. This paper has demonstrated that, with a minimized dc bus capacitor, excellent power factor correction, module load sharing under load transients can be achieved. Reliability is also increased due to the redundant operation system.

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References

[1] B. Singh, B.N. Singh, A. Chandra, K. Al-Haddad, A. Pandey, D.P. Kothari, "A review of single-phase improved power quality AC-DC converters," *IEEE Trans. Ind. Electron.,* vol. 50, Issue 5, pp. 962 – 981, Oct. 2003.

[2] W. Stefanutti, P. Mattavelli, G. Spiazzi, P. Tenti, "Digital Control of Single-Phase Power Factor Preregulators Based on Current and Voltage Sensing at Switch Terminals," *IEEE Trans. Power Electron.*, vol. 21, Issue: 5, pp. 1356- 1363, Sept. 2006.

[3] Yungtaek Jang; M.M. Jovanovic, Kung-Hui Fang; Yu-Ming Chang, "High-power-factor soft-switched boost converter," *IEEE Trans. Power Electron.*, vol. 21 Issue: 1, pp. 98- 104, Jan. 2006.

[4] Min Chen and Jian Sun, "Low-Frequency Input Impedance Modeling of Boost Single-Phase PFC Converters," *IEEE Trans. Power Electron.*, vol. 22, Issue: 4, pp. 1402-1409, July 2007.

[5] L. Huber, Irving, M.M. Jovanovic, "Open-Loop Control Methods for Interleaved DCM/CCM Boundary Boost PFC Converters," *IEEE Trans. Power Electron.*, vol. 23, Issue 4, Page(s): 1649-1657, July 2008.

[6] Jingquan Chen, D. Maksimovic, R.W. Erickson, "Analysis and design of a low-stress buck-boost converter in universal-input PFC applications," *IEEE Trans. Power Electron.*, vol. 21, Issue: 2, pp. 320- 329, March 2006.

[7] R. Zane, D. Maksimovic, "Nonlinear-carrier control for high-power-factor rectifiers based on up-down switching converters," *IEEE Trans. Power Electron.*, vol. 13, Issue 2, pp. 213 – 221, March 1998.

[8] Ching-Jung Tseng and Chern-Lin Chen; "A novel ZVT PWM Cuk power-factor corrector," *IEEE Ind. Electron.,* vol. 46, Issue 4, pp. 780 – 787, Aug. 1999.

[9] S. Buso, G. Spiazzi, D. Tagliavia, "Simplified control technique for high-power-factor flyback Cuk and Sepic rectifiers operating in CCM," *IEEE Trans. Ind. Appl.,* vol. 36, Issue 5, Page(s):1413 – 1418, Sept.-Oct. 2000.

[10] M. Brkovic and S. Cuk, "Input current shaper using Cuk converter," in *Proc. IEEE INTELEC Conf.*, 1992, pp. 532-539.

[11] G. Ranganathan and L. Umanand, "Power factor improvement using DCM Cuk converter with coupled inductor," in *Proc. IEE Electric Power Applications Conf.*, 1999, pp. 231-236.

[12] D.S.L. Simonetti, J. Sebastian, F.S. dos Reis, and J. Uceda, "Design criteria for SEPIC and Cuk converters as power factor preregulators in discontinuous conduction mode," *IEEE PEMC Conf.*, pp. 283-288, 1992,

[13] A. Newton, T.C. Green, and D. Andrew, "AC/DC Power Factor Correction Using Interleaved Boost & CUK Converters," *IEE PEVSD Conf.*, pp. 293-298, 2000.

[14] S. Kim and P.N. Enjeti, "Control of multiple single-phase PFC modules with a single low-cost DSP," *IEEE Trans. Ind. Appl.*, vol. 39, pp. 1379-1385, Sept.-Oct 2003.

[15] Sangsun Kim and P.N. Enjeti, "A parallel-connected single phase power factor correction approach with improved efficiency," *IEEE Trans. Power Electron.*, vol. 19, Issue 1, pp. 87 – 93, Jan. 2004.

[16] B. Singh, S. Gairola, B.N. Singh, A. Chandra, K. Al-Haddad, "Multipulse AC–DC Converters for Improving Power Quality: A Review," *IEEE Trans. Power Electron.*, vol. 23 Issue: 1, pp. 260-281, Jan. 2008.

[17] B. Singh, B.N. Singh, A. Chandra, K. Al-Haddad, A. Pandey, D.P. Kothari, "A review of three-phase improved power quality AC-DC converters," *IEEE Trans. Ind. Electron.,* vol.51, Issue 3, pp. 641 – 660, June 2004.

[18] G. Spiazzi and F.C. Lee, "Implementation of Single-Phase Boost Power-Factor-Correction Circuits in Three-Phase Applications," *IEEE Trans. Ind. Electron.* vol. 44, no. 3, pp. 365-371, June 1997.

[19] H.M. Suryawanshi, M.R. Ramteke, K.L. Thakre, V.B. Borghate, "Unity-Power-Factor Operation of Three-Phase AC–DC Soft Switched Converter Based On Boost Active Clamp Topology in Modular Approach," *IEEE Trans. Ind. Electron.* vol. 23 Issue: 1, pp. 229-236, Jan. 2008.

[20] X.H. Wu, S.K. Panda, J.X. Xu, "Analysis of the Instantaneous Power Flow for Three-Phase PWM Boost Rectifier Under Unbalanced Supply Voltage Conditions," *IEEE Trans.Power Electron.* vol. 23 Issue : 4, pp. 1679-1691, July 2008.

[21] P. Xiao, K.A. Corzine, G.K. Venayagamoorthy, "Multiple Reference Frame-Based Control of Three-Phase PWM Boost Rectifiers under Unbalanced and Distorted Input Conditions," *IEEE Trans. Power Electron.,* vol. 23, Issue: 4, pp. 2006-2017, July 2008.

[22] T. Nussbaumer, J.W. Kolar, "Improving mains current quality for three-phase three-switch buck-type PWM rectifiers," *IEEE Trans. Power Electron.,* vol. 21, Issue 4, Page(s): 967- 973, July 2006.

[23] T. Nussbaumer, M. Baumann, J.W. Kolar, "Comprehensive Design of a Three-Phase Three-Switch Buck-Type PWM Rectifier," *IEEE Trans. Power Electron.,* vol. 22, Issue: 2, pp. 551-562, March 2007.

[24] Lung-Sheng Yang; Tsorng-Juu Liang; Jiann-Fuh Chen, "Analysis and Design of a Novel Three-Phase AC–DC Buck-Boost Converter," *IEEE Trans. Power Electron.,* vol. 23, Issue 2, pp. 707-714 March 2008.

[25] Y.K. Eric Ho, S.Y.R. Hui, and Yim-Shu Lee, "Characterization of Single-Stage Three-Phase Power-Factor-Correction Circuit Using Modular Single-Phase PWM DC-to-DC Converters," *IEEE Trans. Power Electron.*, vol.15, pp. 62-71, January 2000.

IEEE 13th European Conference on Power Electronics and Applications, 2009. EPE '09. 2009 , Page(s): 1-10

Analysis, Design and Implementation of a Three-Phase AC to DC Converter Using Single-Phase Isolated CUK Rectifier Modules with Small DC Bus Capacitor

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Keywords

«DC power supply», «Harmonics», «Power factor correction», «Power supply», «Switched-mode power supply».

Abstract

The paper presents an implementation and control of a high power-factor and fast dynamic transient response of the modular three-phase ac to dc converter using three CUK rectifier modules with a small dc bus capacitor. The methodology aims at finding the small dc bus capacitor which meets the desired system performance, with power balance control technique. Modeling a modular three-phase rectifier system is considered as the first step in the optimal sizing procedure. In this paper, mathematical average small-signal model for characterizing modular three-phase rectifier is proposed. Design of an analog controller for a small dc bus capacitor based modular three-phase rectifier is presented. The controller senses the parameters of the proposed system, and makes decisions about reject load and input voltage disturbances. The second step consists in minimize the sizing of the dc bus capacitor according to the transient response of dc bus output voltage and the delivered energy of capacitor concepts. Considering various types and capacities of dc bus capacitor, which can meet the desired system performance, are obtained by changing the type and size of the dc bus capacitors. The proposed system with the dc bus capacitor 470 μF gives the optimal choice. A 750W laboratory prototype with 470 μF is implemented and tested to verify the feasibility of the proposed system. The experimental results show that the proposed system, meet the desired system performance. Therefore the system choice plays an important role in cost reduction.

Introduction

Among various PFC converters, a modular three-phase ac to dc converter composed of three modified single-phase single-switch modules with a single dc bus capacitor has been proposed for medium and high-power applications in distributed power system (DPS) [1]-[3]. A single dc bus capacitor, C_O is connected at the output terminal for filtering the output voltage ripples. It can be used as dc bus for distributing power to load converter. Compared to the conventional six-switch topology [4]-[5], this type of three-phase PFC converter features a simple and robust configuration.

Capacitors are available today may be made in five basic technologies and used across a broad spectrum of application. The currently commercially available technologies are listed below : 1) ceramic; 2) aluminum electrolytic; 3) tantalum electrolytic; 4) film (polymeric); 5) film (mica and paper). Electrolytic capacitor technology, providing moderate energy and power density, but has relatively high losses and is polarity dependent, and therefore primarily used in dc circuits. Typical applications are moderate to large capacitors at up to 600 V, mainly for dc applications involving filtering and rectified circuits. When a capacitor is selected to perform properly in an electronic circuit, its characteristics are optimized to provide the designer with a well-defined level of reliability for the component throughout the design lifetime of the circuit. The selection of a capacitor design requires the matching of available capacitor characteristics and parameters to the application needs. In addition to the basic capacitance value and voltage rating, specifying all the characteristics allows the supplier to provide the most cost-effective capacitor for a given application.

In general, dc bus capacitors are installed in switching power supply systems for voltage regulation, power factor correction, and reactive power control. This process involves determining capacitor size, type, location, voltage constraints, load variation and control method. The main effort usually is to determine capacitor size for voltage regulation. The dc bus in any distributed power system is normally equipped with an electrolytic capacitor, which provides decoupling between the rectifier and the load converter. However, the dc bus capacitor is a large, heavy, and expensive component. Moreover, the dc bus capacitor is the prime factor of degradation of system reliability. This problem is well recognized by the industry. Manufacturers of low cost and high volume systems are looking for ways to reduce the size and cost of this electrolytic capacitor.

This paper presents a three-phase ac to dc converter using single-phase isolated CUK rectifier module with nearly unity-power factor and reduce dc bus capacitor. This research project has attempted the development of a power balance control technique that will allow the use of a smaller dc-link capacitor without affecting the output performance of the converter.

The proposed method implemented in three-phase ac to dc converter applications will result in the following advantages:

- High power factor, modularity, fast dynamic transient response, small capacitor size, reduced converter weight and volume.
- Significant improvement in system reliability by the use of a smaller link capacitor.
- Power balance control technique to simplify the design procedure of the dc bus voltage regulator, to provide fast transient response, high performance, and increased reliability.
- An analog controller insensitive to environment, simple control strategy, offering stable operation under most operating conditions. It is easy to understand and to implement.

Proposed system

Fig. 1 shows a modular three-phase ac to dc converter using single-phase single-switch isolated CUK rectifier modules. The power circuit is formed by an input-side Y-connected of three power modules with parallel connected at dc bus voltage. The capacitor C_O is shared by three power modules. The control strategy consists of single output voltage loop control and three inductor current calculators.

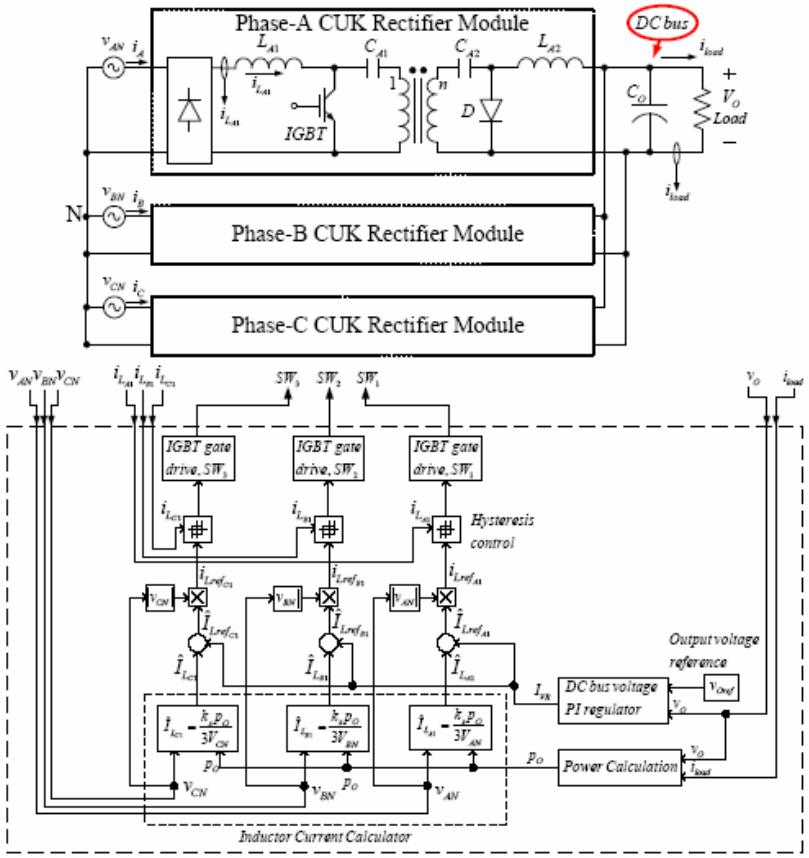

Fig. 1: Three-phase ac to dc converter using three single-phase isolated CUK rectifier modules with small dc bus capacitor.

Selecting the value of the dc bus capacitor

Traditional PFC converter, the relationship between the energy of bulk capacitors and the hold-up time, this given as:

$$C_{O,\min} = \frac{2P_O T_{hld}}{V_O^2 - V_{O,\min}^2} \tag{1}$$

Where, P_O is the power of the dc-dc converter; V_O is normal operation voltage of the bulk capacitors; $V_{O,min}$ is the minimum operation input voltage for the dc-dc converter at the latter stage. Typically, with a proper design, ripple voltage and current in the capacitor will not be an issue. By choosing T_{hld} = 2 ms, $\Delta v_o = \pm 5\%$, one can find $C_{O,min}$ = 10,683 μF. In order to guarantee minimum capacitance requirement is satisfied, thus assuring minimum hold up time.

$$C_O = \frac{C_{O,\min}}{1 - \Delta C_{tol}} = 13{,}353\ \mu\text{F} \tag{2}$$

Pick C_O = 13,600 μF. Table I shows the design results of a 750 W, -48 V, a three-phase ac to dc converter using isolated CUK rectifier modules.

Average small signal model

The analytical model derivation is based on the power stage schematic shown in Fig. 1 where the ideal switches and zero equivalent series resistance in the capacitors are assumed.

$$\sum_{i=A}^{C} V_{gi} I_{L1i} = V_O I_O \tag{3}$$

When, $i = A$, B and C, V_{gi} is rectifier voltage, I_{L1i} is inductor current, V_O is dc output voltage, I_o is average output current over a half-line cycle. The peak value of the inductor current is

$$\hat{I}_{L1i} = \frac{K_2 V_O I_{load}}{3V_{gi}} \tag{4}$$

$$\hat{I}_{Lref1i} = \hat{I}_{L1i} + I_{VR} \tag{5}$$

$\hat{I}_{Lref1i}$ is peak value of the inductor reference current, $\hat{I}_{L1i}$ is peak value of the inductor current, I_{VR} is correcting signal of PI controller, K_2 is conversion gain of inductor current. The dynamic equation of the output voltage is

$$\sum_{i=A}^{C} I_{Oi} = C_O \frac{dV_O}{dt} + I_{load} \tag{6}$$

I_{load} is the load current. Applying the perturbations in (1), (2), (3), and (6), and performing the small-signal approximation ($\tilde{v}\,.\,\tilde{v} = 0$). Therefore, the output voltage can be expressed as

$$\tilde{v}_o = T_C \tilde{v}_{Oref} + T_A \tilde{v}_{g_i} - Z_O \tilde{i}_{load} \tag{7}$$

When, applying Mason gain formula.

$$\frac{\tilde{v}_O}{\tilde{v}_{Oref}} = \frac{G_2 Z_L G_{VR}}{1 + k_{fb} G_2 Z_L G_{VR} + G_3 Z_L - G_2 Z_L F_2} \tag{8}$$

Therefore, the gain K_2 can be expressed as:

$$K_2 = K_1^{-1} = \sqrt{2} \tag{9}$$

The transfer function of Fig.1 can be obtained from the average small-signal model proposed:

$$\frac{\tilde{v}_O}{\tilde{v}_{Oref}} = \frac{3G_{VR}\overline{V}_{gi}K_1}{\overline{V}_O C_2 S + 3G_{VR}\overline{V}_{gi}K_1 k_{fb}} \tag{10}$$

K_1 is RMS gain, k_{fb} is feedback gain. Here, a PI controller is chosen for voltage regulation

$$G_{VR}(s) = \frac{k_p\left(S + \omega_Z\right)}{S} \tag{11}$$

$G_{VR}(s)$ is PI controller, k_p is the gain of controller, ω_Z is the location of the zero.

Experimental verification

Performance evaluation of the modular three-phase rectifier system

A 750 W laboratory prototype was implemented and tested to verify the feasibility of the proposed control strategy. The specifications of the laboratory prototype are listed in table I. Steady state input currents of the proposed system with three different values of dc bus capacitor (C_O = 150 μF, 1,000 μF and 13,600 μF) are shown in Fig. 2. They are nearly sinusoidal. The measured power-factors are 0.99 and total harmonic distortions (THD) are lower than 3%, respectively. They have been illustrated that the proposed system can achieved a high power-factor and low THD_i.

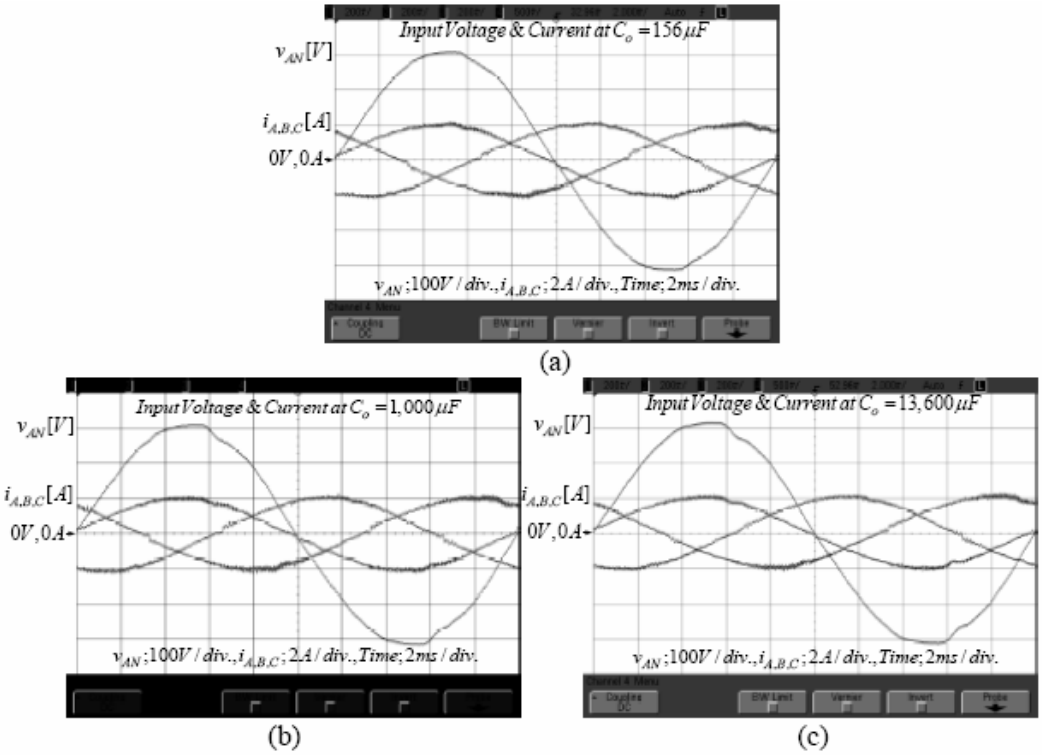

Fig. 2: Steady state condition of the modular three-phase rectifier with C_O = 150 μF, 1,000 μF and 13,600 μF.

Table I: Design results for the laboratory prototype

Characteristic/Symbol	Value
Input Chokes / L_{A1},L_{B1},L_{C1}	5.069 mH, 5.068 mH, 5.066 mH
Output Chokes / L_{A2},L_{B2},L_{C2}	1.066 mH, 1.086 mH, 1.044 mH
Output Capacitor / C_O	156 μF (min), 13,600 μF (max)
Input voltage / v_{AN}, v_{BN}, v_{CN}	220 V
Line frequency	50 Hz
Switching frequency	≈20-30 kHz
Rated module	250 W/ module
Total output power	750 W
Output voltage	-48 V
n	0.5
Storage capacitor/ C_A, C_B, C_C	0.68 μF

The experimental results of the proposed system operating at step load change from 75 W to 750 W and vice versa under three different output capacitors (156 μF, 1,000 μF and 13,600 μF) are shown in Fig. 3. The comparison between the results indicates that the small voltage dips and less variant in response trajectories are yielded by applying power balance control technique. The main performance features of the proposed system for input power-factor (PF) and input current total harmonic distortion (THD_i) are plotted in Fig. 4 as a function of the different dc capacitor size ($C_{O,min}$ = 150 μF to $C_{O,max}$ = 13,600 μF) at rated input and output voltage and output power (220V, -48 V and 750 W). They are measured with the Digital power meter YOKOGAWA model 2531A.

The following can be concluded:

- Power-factor is nearly unity, greater than 0.99 for all difference values of output capacitor,
- Input current THD_i remains low, lower than 3% (750 W), for fifteen values of output capacitor.

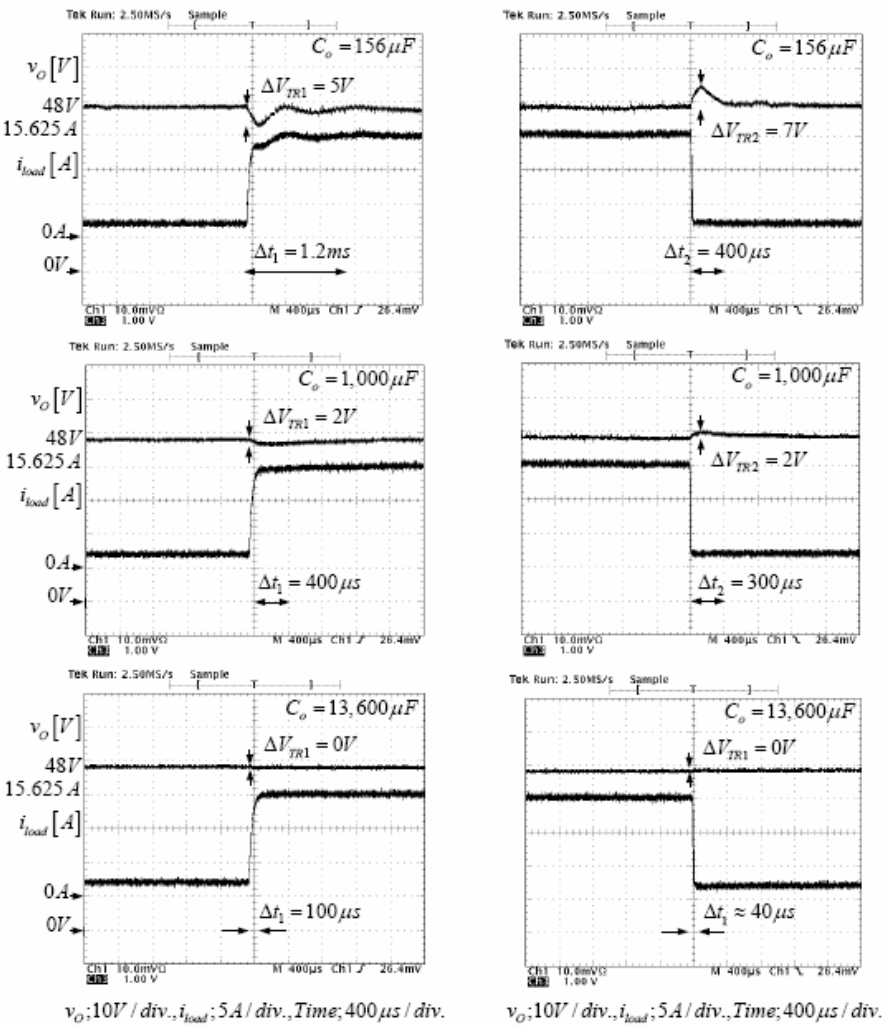

Fig. 3 : Transient condition of the modular three-phase ac to dc converter: dc bus voltage and load current at step load change from 10% (75 W) to 100% (750 W) and vice versa (parameter of PI controller k_p = 1 and ω_z = 150 with power balance control technique).

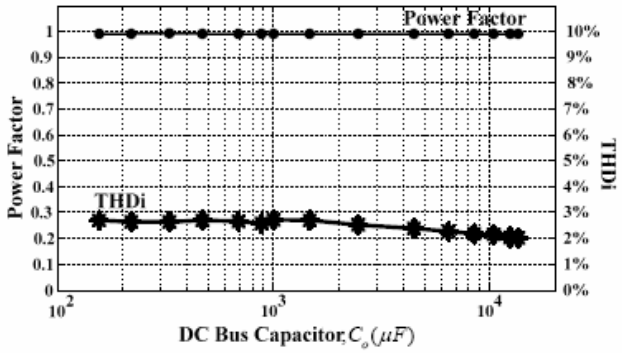

Fig. 4 : Steady state condition of the proposed system with $C_{O,min}$ = 156 μF to $C_{O,max}$ = 13,600 μF.

The influence of its value on ΔV_{droop}, $\Delta V_{overshoot}$, Δt_{droop}, and $\Delta t_{overshoot}$ is shown in Fig. 5. As expected the Δt_{droop} decreases as the capacitance increases, down to 100μs for $C_O \geq$ 4,000 μF, and the ΔV_{droop}, $\Delta V_{overshoot}$ decreases as well. The voltage $\Delta V_{overshoot}$ is higher than ΔV_{droop} for $C_O <$ 700 μF. At low values of dc bus capacitor with $C_O <$ 1,000 μF, sum of ΔV_{droop} and $\Delta V_{overshoot}$ is larger than 5%. However, for high values of dc bus capacitor with 4,000 μF $\leq C_O \leq$ 13,600 μF, the ΔV_{droop} and $\Delta V_{overshoot}$ are nearly zero and Δt_{droop} is nearly zero as well. If we define optimal range of dc bus capacitor is $C_{O,optR}$. The $\%\Delta V_{droop} \leq \%\Delta V_{transpec}$ (5%) is the system recovers faster. For the optimal range of dc bus capacitor with 470 μF $\leq C_O \leq$ 1,000 μF, the $\%\Delta V_{droop}$ is lower than 5% and Δt of the settling time is very small (≈ 400 μs).

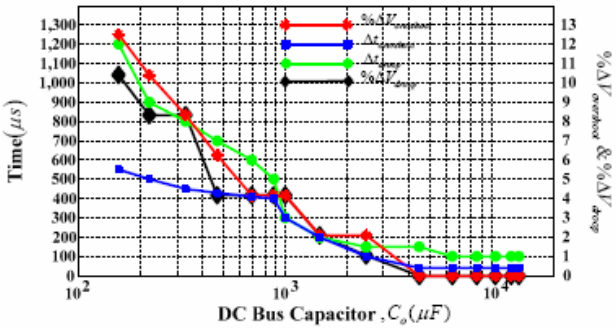

Fig. 5: Performance as a function of step load change from 75 W (10%) to 750 W (10%) and vice versa (v_s = 220 V and v_o = -48 V).

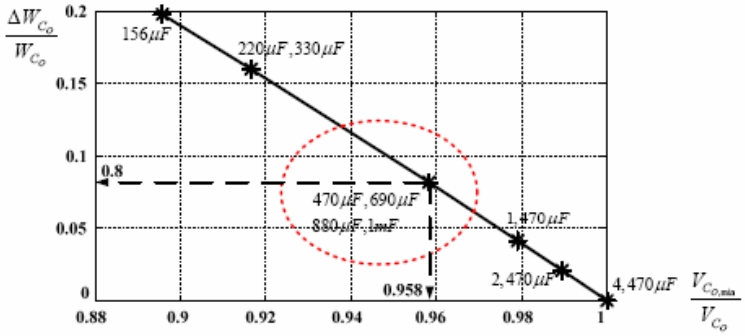

Fig. 6: Normalized delivered energy from the energy storage capacitor during hold-up time ΔW_{CO} /W_{CO} as a function of normalized minimum energy-storage capacitor voltage $V_{CO,min}$ /V_{CO} for different C_O.

In this paper, requirements are 400 μs or 500 μs at nominal input voltage. The less restrictive option can be usually complied with a 0.62 μF/W capacitor (i.e., a 750 W application wound need a 470 μF). The most restrictive option can be complied with 1.3 μF/W. When, ΔW_{Co} is the amount of delivered energy to the output during hold-up time and W_{Co} is the total stored energy in C_O at V_{Co}. As seen from Fig. 6, only 8% of the stored energy is delivered to the load during the hold-up time if $V_{Co,min}$ is selected to be 0.958 V_{Co} ($C_{O,opt}$ = 470 μF).

Steady-state and dynamic response of the proposed system with small dc bus capacitor

The dynamic responses of the modular three-phase rectifier corresponding to conventional control and proposed control are shown in Fig. 7. It shows the experimental result of the output voltage to a load step between 24 W and 750 W with and without power balance control technique, for two different PI controller conditions (k_p=1 and ω_z=50, k_p=1 and ω_z=150). The waveforms shown in Fig. 7(a) and Fig. 7(b) pertain to a step change in load between 24 W and 750 W under rated input voltage condition with k_p=1 and ω_z=50. The upper trace of Fig. 7 (a) is the dc bus voltage and the lower one in Fig. 7 (a) is the load current during the transient. It can be seen that the output voltage waveform has a large dip and a longer settle time, indicating a poor dynamic performance. Fig. 7 (b) shows that, during the transient, the output voltage waveform (upper trace) recovery quickly without voltage dip, indicate very good dynamic performance. This demonstrates that the load disturbance is effectively removed from the voltage-feedback loop. The settling time of the transients without power balance control is 60 ms and the one with power balance control is about 1 ms. Fig. 7 (c) and Fig. 7 (d) correspond to a step change in load between 750 W and 24 W. Fig. 7 (c) is the waveform of dc bus voltage and load current. It can be seen that the dc bus voltage response is improved due to the increased k_p and ω_z. The dc bus voltage waveform in Fig. 7 (d) is greatly improved. It recovers very quickly without voltage dip at all. The settling time of the transients without power balance control is 20 ms and the one with power balance control is about 1 ms. The response is upper 20 times faster with the proposed power balance control than without power balance control in both cases (k_p=1 and ω_z=50, k_p=1 and ω_z=150).

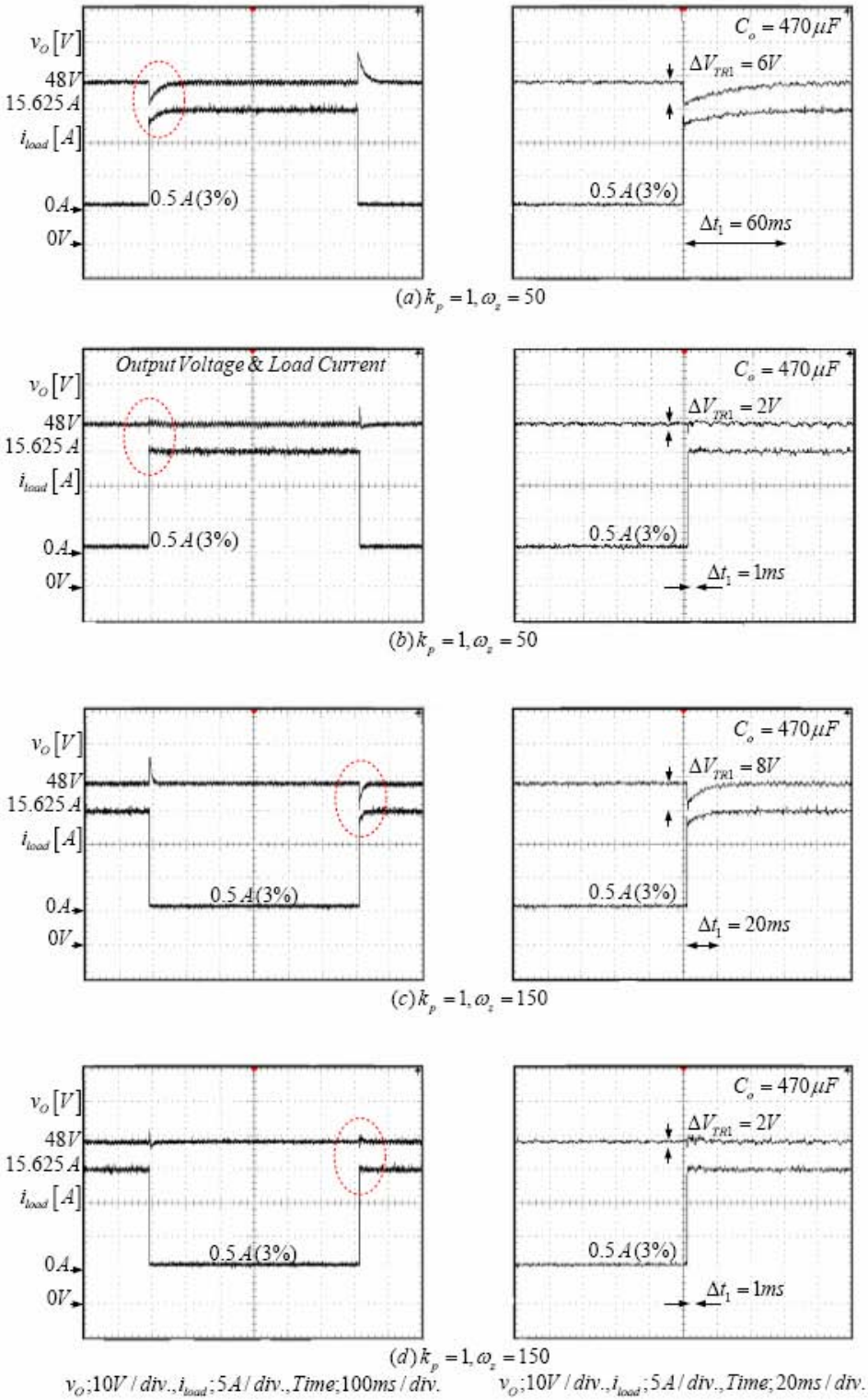

Fig. 7: Waveforms of dc bus voltage and load current when the load steps from 3% to 100% and vice versa : (a) and (c) without power balance control technique; (b) and (d) with power balance control technique.

It is quite obvious that a system having a fast voltage loop exhibits better dynamic responses over the one having a slow voltage loop. It is experimentally shown that the rectifier system with the conventional controller also exhibits similar dynamic performances as those shown in Fig. 7(b) and Fig 7(d), when its voltage-loop bandwidth is design with k_p=1, ω_z=50 and k_p=1, ω_z=150 based on power balance control technique.

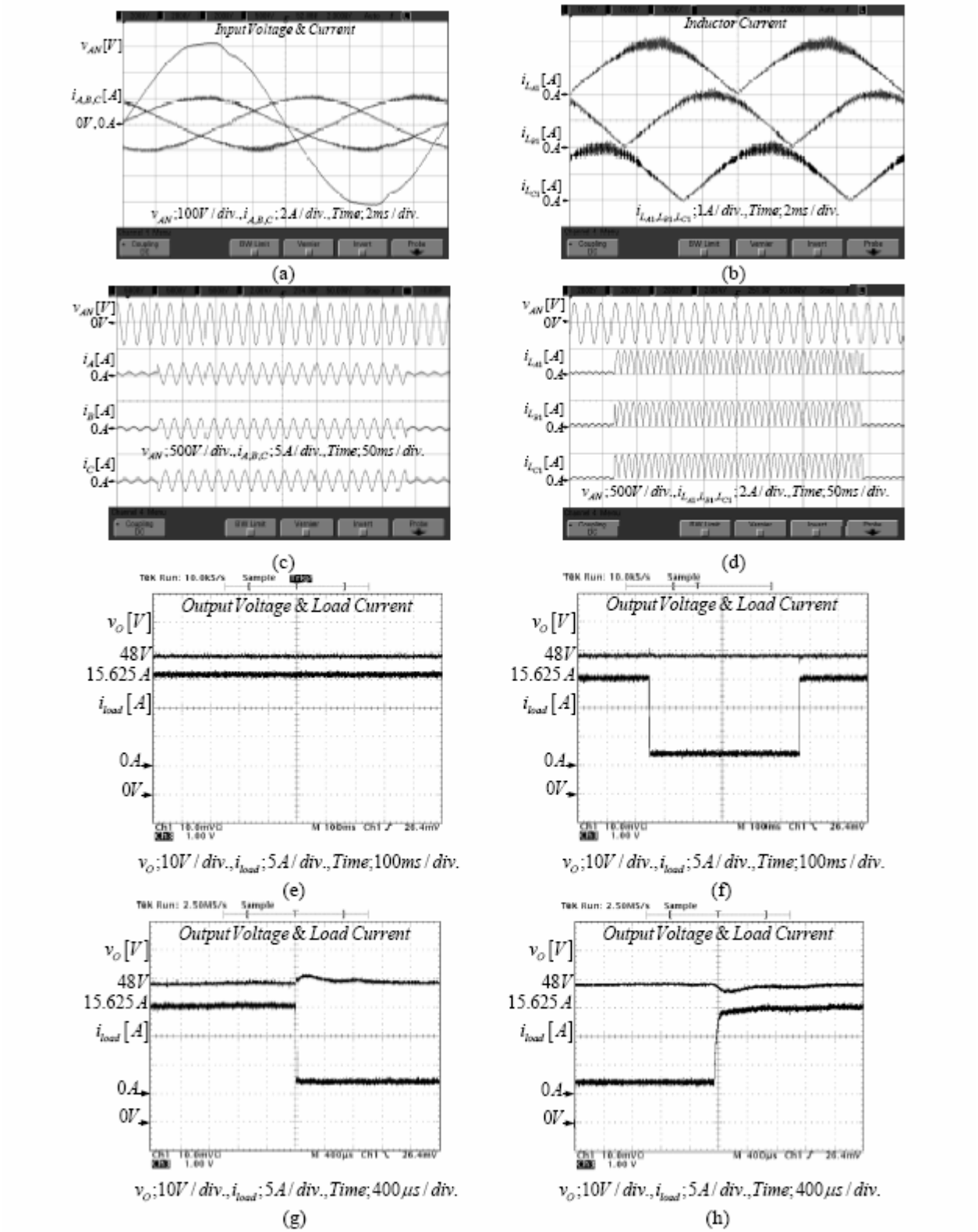

Fig. 8 : Experimental steady state and transient response of the modular three-phase rectifier with small dc bus capacitor (C_O = 470 μF): source voltage and line current, inductor current, dc bus voltage and load current.

Steady state and transient response of the proposed system are shown in Fig. 8 (a)–(h), respectively. The parameters PI controllers are: k_p = 1 and ω_z = 150. The steady-state input characteristics of the rectifier for output power of 750 W are shown in Fig. 8 (a). Line current is in phase with their relative voltages. It has been illustrated that the proposed system can achieved a high power factor. Since i_A is

proportional to v_{AN} under this control method, the distortion shown in i_A is due to the corresponding distortion in v_{AN}. Fig. 8 (b) shows the steady state of three-individual inductor current waveforms at full load. It can be noted that the inductor currents are almost balanced. The transient response of the three-input line currents and three-individual inductor currents at load step change from 75 to 750W and vice versa are shown in Fig. 8 (c) and Fig. 8 (d). For the given range of output power, the power factor is close to unity and the THD_i is low. Due to the effects of difference inductance values and parasitic in input inductors, these three-individual inductor currents are not exactly equal. However, all inductor current has approximately same amplitude. Fig. 8 (e) shows the output voltage at -48 V and load current at -15.625A when output capacitor is 470 μF. Fig. 8 (f) shows the dynamic response of the output voltage and load current of the proposed system due to step load changes at the load current from 750 to 75 W and vice versa. The settling time of the output transient without power balance control technique is 30 ms, while the one with power balance control technique is 400 μs. The experimental results in Fig. 8 (g) and (h) indicate that such scheme is effective and fast transient response characteristic.

Therefore, according to the results obtained we have a modular three-phase rectifier with the following features :

- It has only one small dc bus capacitor.
- It can achieve a fast dynamic transient response and high power factor.
- It is easy to understand and to implement.
- It is simple and robust.
- It is naturally isolation.
- It operates either as step-up or step-down voltage.
- It can allow a regulated output voltage with only one power processing stage.

Conclusion

The modular three-phase rectifier with a small dc bus capacitor, using an average small-signal model, has been developed in this work. The system configuration can be obtained in terms of a system power supply performance requirement by using the power balance control concept. A simple method is presented to improve the dynamic response of the proposed system against load disturbance while maintaining low input current distortion. Design equations are presented to model the power circuit and to select the controller parameters. The paper has presented that, with reduce dc bus capacitor, high power factor, good inductor current sharing and fast dynamic transient response can be achieved for a three-phase ac to dc converter using isolated CUK rectifier modules. In this case, dc bus capacitor C_O = 470 μF according to ΔV_{droop}, $\Delta V_{overshoot}$, and delivered energy. Bus voltage is regulated by the designed PI controller with power balance control technique. Control circuit is simple and implemented by analog circuit. The experimental results prove that proposed system is meet harmonic distortion standards (IEC 61000-3-2 Class A limits).

References

[1] B. Singh, B.N. Singh, A. Chandra, K. Al-Haddad, A. Pandey, D.P. Kothari, "A review of single-phase improved power quality AC-DC converters," *IEEE Trans. Ind. Electron.,* vol. 50, Issue 5, pp. 962 – 981, Oct. 2003.

[2] B. Singh, B.N. Singh, A. Chandra, K. Al-Haddad, A. Pandey, D.P. Kothari, "A review of three-phase improved power quality AC-DC converters," *IEEE Trans. Ind. Electron.,* vol.51, Issue 3, pp. 641 – 660, June 2004.

[3] H.M. Suryawanshi, M.R. Ramteke, K.L. Thakre, V.B. Borghate, "Unity-Power-Factor Operation of Three-Phase AC–DC Soft Switched Converter Based On Boost Active Clamp Topology in Modular Approach," *IEEE Trans. Ind. Electron.* vol. 23 Issue: 1, pp. 229-236, Jan. 2008.

[4] P. Xiao, K.A. Corzine, G.K. Venayagamoorthy, "Multiple Reference Frame-Based Control of Three-Phase PWM Boost Rectifiers under Unbalanced and Distorted Input Conditions," *IEEE Trans. Power Electron.,* vol. 23, Issue: 4, pp. 2006-2017, July 2008.

[5] X.H. Wu, S.K. Panda, J.X. Xu, "Analysis of the Instantaneous Power Flow for Three-Phase PWM Boost Rectifier Under Unbalanced Supply Voltage Conditions," *IEEE Trans.Power Electron.* vol. 23 Issue : 4, pp. 1679-1691, July 2008.

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Analysis and Design of a Modular Three-Phase AC-to-DC Converter Using CUK Rectifier Module With Nearly Unity Power Factor and Fast Dynamic Response

Uthen Kamnarn and Viboon Chunkag

***Abstract*—In this paper, the analysis and design of a modular three-phase ac-to-dc converter using single-phase isolated CUK rectifier modules is discussed based on power balance control technique. This paper analyzes the operation of a modular converter as continuous-conduction-mode power factor correction (CCM-PFC). Design equations, as well as an average small-signal model of the proposed system to aid the control loop design are derived. It is used to obtain the inductor current compensator, thus the output impedance and audio susceptibility become zero, and therefore, the output voltage of the converter presented in this paper is independent of the variations of the dc load current and the utility voltage. The control strategy consists of a single output voltage loop and three-inductor current calculator. The main objective of the proposed system is to reduce the number of stages and improve dynamic response of dc bus voltage for distributed power system. The proposed scheme offers simple control strategy, flexibility in three-phase delta or star-connected, simpler design, fast transient response, good inductor current sharing, and power factor closed to unity. Both simulation and experimental results are presented.They are in agreement with the theoretical analysis and experimental work.**

***Index Terms*—Current sharing control, fast response, modular rectifier, power factor correction (PFC), three-phase converter.**

NOMENCLATURE

C_a, C_b	Intermediate capacitor.
C_o	Output capacitor.
d	Duty-cycle.
D	Diode.
F_1	Open-loop load current to input inductor current transfer function.
F_2	Open-loop output voltage to input inductor current transfer function.
F_3	Open-loop phase voltage to input inductor current transfer function.
G_1	Open-loop phase voltage to output current transfer function.
G_2	Open-loop inductor current to output current transfer function.
G_3	Open-loop output voltage to output current transfer function.
G_{VR}	Transfer function of PI controller.
$\bar{I}_{\rm load}, \tilde{i}_{\rm load}$	Load current.
$\bar{\hat{I}}_{L{\rm ref}_{1i}}, \tilde{\hat{i}}_{L{\rm ref}_{1i}}$	Reference for the peak value of inductor current.
$\bar{\hat{I}}_{L_{1i}}, \tilde{\hat{i}}_{L_{1i}}$	Peak inductor current.
$\bar{I}_{L_{1i}}, \tilde{i}_{L_{1i}}$	Inductor current.
$\bar{I}_o, i_o$	Average output current over a half-line cycle.
$\bar{I}_{VR}, \tilde{i}_{VR}$	Correcting signal of proportional-integral controller.
k_{fb}	Feedback gain.
$K_a(K_{a,\rm crit})$	Conduction parameter; critical conduction parameter.
K_1	RMS gain.
K_2	Conversion gain of inductor current.
$L_{11}; L_{12}; L_{13}$	Input side inductor.
$L_{21}; L_{22}; L_{23}$	Output side inductor.
$M, n_{\rm Tr}$	The voltage relation in CCM; the turn ratio between primary and secondary.
T_A	Audio susceptibility.
T_C	Control function.
$T_{\rm sw}$	Switching period.
$V_{S_{aN}}, V_{S_{bN}}, V_{S_{cN}}$	Input phase voltage.
$\bar{V}, \tilde{v}$	Caret $\bar{V}$ means steady state and $\tilde{v}$ means the introduced perturbation (small-signal value).
$\bar{V}_{gi}, \tilde{v}_{gi}$	Rectified input voltage.
$\bar{V}_o, \tilde{v}_o$	DC output voltage.
v,i	Instantaneous voltage and current.
$\tilde{v}_{\rm oref}$	Reference for the small-signal value of output voltage.
Z_L	Dynamic impedance.
Z_o	Output impedance.
ω_Z	Location of the zero.

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I. Introduction

IN RECENT years, high-quality rectifiers have been increasingly used in industrial, commercial, residential, aerospace, electronic equipment, telecommunication, and computer systems due to advantages of high quality, high power density, high efficiency, high reliablility, long lifetime, and low-cost power supplies. In order to comply with the international standards for electromagnetic compatibility and precise regulation, an approach to achieve almost unity power factor is to use an active power factor correction (PFC) circuit [1] followed by a dc-to-dc stage, which provides high-frequency insulation as well as tight output voltage regulation. As compared to boost [2]–[7], push–pull [8], buck–boost [9] or flyback [10], CUK, and single-ended primary inductor converter (SEPIC), PFC's are less popular due to their higher complexity. However, they overcome some basic limitations of other topologies. SEPIC [11] and CUK [12]–[15] converters can be attractive for PFC applications because they offer easy implementation of transformer isolation, inherent inrush current limitation during start-up and overload conditions, and ability to generate arbitrary output voltages. It has been shown that SEPIC and CUK converters have advantages over the boost converter in terms of the conducted noise or electromagnetic interference (EMI). In particular, in both configurations, all inductive components can be realized on the same core, and the magnetic components can be designed for very low inductor current ripples. To satisfy such requirements, the isolated CUK PFC converter is proposed.

An isolated dc–dc CUK converter is shown in Fig. 1. The input section resembles that of a boost converter, while the output section is similar to a buck stage. It offers either step-up or step-down output voltage with respect to the input, producing a negative output voltage from a positive input voltage. The magnetizing inductance of CUK converter does not carry a dc current component, so that the transformer can be fully utilized. It is interesting to note that, with a proper choice of the inductances, the line current of CUK converter remains continuous even if one or both of the inductors operate in the discontinuous conduction mode, and thus, input filter requirement can be reduced. Advantages can be gained by magnetically coupling the two inductors [16]–[18]. In the continuous conduction mode of operation, the voltage waveforms of the input inductor, output inductor, and transformer windings are proportional in magnitude, and have the same frequency and phase shift. Therefore, it is possible to integrate these three elements in one magnetic structure, with zero current ripples in both input and output inductors. Many additional benefits are achieved from the magnetic integration, such as high power density, low cost, lower operating frequency, low noise and EMI, high efficiency, and small-size filteringcomponent at the input and output side.

The active rectifier front end of a dc distributed power system (DPS) has been attracting increased attention due to incessantly growing power quality concerns. Modular design of each unit in the DPS is good for maintainability. Therefore, a single-phase parallel configuration using ac-to-dc boost, SEPIC, and CUK converters for dc DPS have been developed [19]–[21]. Due to its high efficiency, good current quality, and low EMI emissions,

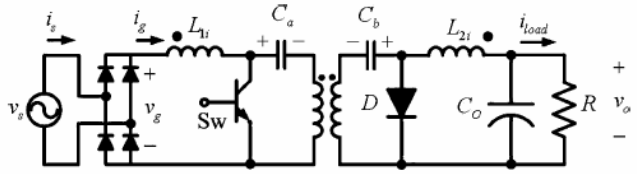

Fig. 1. Single-phase CUK rectifier.

a three-phase PWM rectifier is normally applied for high-power applications. However, this type of three-phase PFC converter has more component counts and a complicated controller design that causes poor reliability. A three-phase converter using single-phase single-switch modular rectifier topology has the merits of simple control and few components. They are becoming popular for low- voltage or medium-power applications [22], [23]. A great amount of work has already been done concerning the three-phase PWM boost [24]–[28], buck [29], [30], buck–boost [31], full-bridge [32], or CUK rectifiers [33]. They often require input or output transformer isolation for safety, and also offer a unity input power factor, limited input harmonic currents fed back to the ac power distribution system, high efficiency, and high power density.

A three-phase converter using three modified single-phase single-switch boost rectifier modules was proposed for high-power and high-voltage applications. Normally, a single-phase boost PFC converter converts an ac voltage to a dc voltage, which is higher than the ac peak value (for an ac three-phase 380 V supply, the dc output voltage may be higher than 588 V_{dc}). Compared to the conventional three-phase PWM rectifier, this type of three-phase PFC converter features a simple and robust configuration. The converter can achieve almost unity power factor, nearly sinusoidal input current, and adjustable output voltage. Some of the topologies are suitable only for step-up voltage conversion. When step-down voltage conversion is required, an additional power stage must be added, which will result in an increase in circuit components and cost. For telecommunications and computer system, usually a second-stage dc–dc converter is used to change the voltage from 380 to 48 V or −48 V. Existing high-power PFC approaches use a three-phase boost-type switched-mode rectifier as a first-stage converter to achieve ac–dc power conversion with a typical dc output voltage of 680 V. A second-stage dc–dc converter then converts the voltage from 680 to 48 V or −48 V. The major problems of existing boost-type schemes include the redundancy in the two-stage arrangement and the high intermediate dc voltage for a three-phase ac–dc converter. The two-stage operation would lead to reduced efficiency, and increased size and cost of magnetic, filtering components. To avoid the problem arising from the traditional two-stage conversion approach, a single-stage three-phase ac–dc converter, as shown in Fig. 2, is examined. It consists of three modules connected in parallel. Each module comprises a diode rectifier and a CUK converter with electrical isolation. The performance of the CUK converter suggests that this is the best topology. The CUK converter also offers greater flexibility in the configuration thatcan be implemented as isolation is easily incorporated.

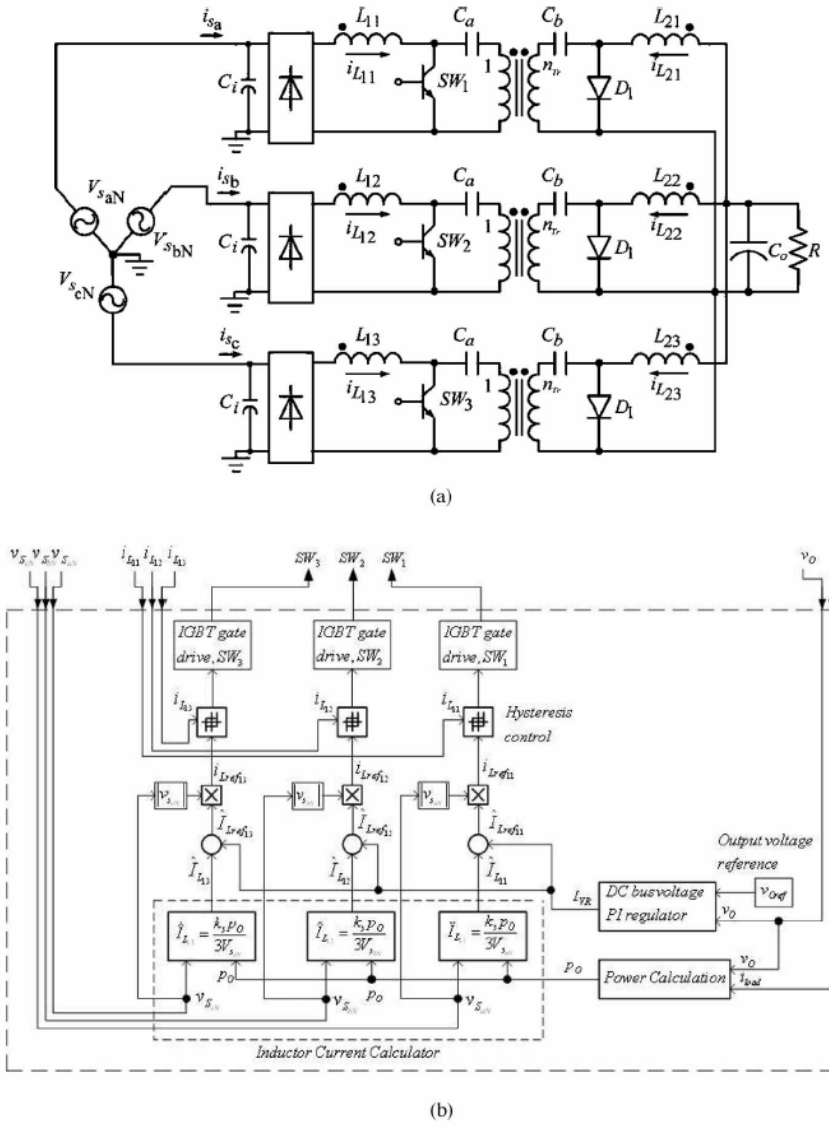

Fig. 2. Proposed system. (a) Power circuit of the modular three-phase ac-to-dc converter using CUK rectifier modules. (b) Control structure and detailed control block.

In this paper, the implementation and control of the modular three-phase ac-to-dc converter using three single-phase isolated CUK rectifier modules with nearly unity power factor and fast dynamic transient response for telecommunication systems is presented under the continuous-conduction-mode (CCM) of operation. The objective of the proposed scheme is to overcome the disadvantages of the three conversion stages in cascade (PFC stage, dc-to-ac stage, and ac-to-dc stage) to simplify the design procedure of the dc bus voltage regulator, PFC, and inductor current sharing, and to improve the dynamic response. The average small-signal model of the proposed system will be analyzed and designed. It is used to obtain the inductor current compensator, thus resulting in the output impedance and audio susceptibility becoming zero, i.e., the output voltage of the converter presented in this paper is independent of the variations of the dc load current and the utility voltage. This control strategy has high dynamic features, and can achieve a fast dynamic transient responseby action of the inductor current compensator.

The deduction of the proposed inductor current compensator is also quite easy, but the effect is sensible. Its main features include: the proposed system's modularity, simple control strategy, and design; the second-order harmonic current component in the output capacitor is cancelled, and this significantly reduces capacitor heating, improves its operating life, and could minimized a dc bus capacitor. The system behavior will be described for symmetric module conditions by simulation and experimental results. The experimental results demonstrate that the proposed system works well, has fast dynamic response, with simple control strategy, good PFC, and the inductor current sharing. In the following sections, a power stage topology and control scheme, dynamic modeling for controller design, results of circuit simulations,and hardware experiments are presented.

II. Single-Phase CUK Rectifier Module

A single-phase CUK PFC with input–output isolation is shown in Fig. 1, which consists of a diode full-bridge rectifier, a dc-to-dc isolated CUK converter, and an output filter. A CUK PFC was designed with the following characteristics: input voltage $V_s = 220$ V $\pm$ 10%, line frequency 50 Hz, power factor $\geq$0.95, maximum output power per module $P_o = 250$ W ($R = 9.216\,\Omega$), output dc voltage $V_o = -48$ V, the turn ratio between primary and secondary $n_{\rm Tr} = 0.5$, and efficiency $\eta \geq 85\%$. The input current is sinusoidal with unity power factor, and the interaction between modules is neglected.

The power factor circuit can also be optimized over a wide range of current ripple and efficiency. As the current ripple increases, the inductance decreases. The smallest inductance occurs at the discontinuous mode. Therefore, running the circuit in the discontinuous mode results in the smallest inductor size and power stage weight. The penalty is higher current stress and conduction loss. The input filter size also increases as the current ripple increases. Experiment has shown that a power factor circuit with smaller current ripple is suitable for high-power applications, when the noise generated by the inductor current and switch current stress are the primary concern. The discontinuous-mode operation, on the other hand, is better suited for low-power application when the objectives are small core size and low-cost control circuits. To operate at CCM, one can find the following.

1) The dc voltage conversion ratio $m(\theta) = V_o/(\hat{V}_g\,|\sin(\theta)|)$, the M ratio is

$$M = \frac{V_o}{\hat{V}_g} = 0.1543. \tag{1}$$

2) The conduction parameter of the CUK PFC circuit

$$K_a > \frac{1}{(2(M + n_{\rm Tr}\,|\sin(\theta)|)^2)} > 1.167. \tag{2}$$

Here, K_a is chosen to be equal to 2.

3) An equivalent inductance

$$L_{\rm eq} = \frac{RT_{\rm sw}K_a}{2} = 0.3072\ {\rm mH} \tag{3}$$

where, the diode voltage drops are neglected.

By choosing the input inductor current with 30% current ripple, $\Delta i_{L_{1i}} = 0.482$ A. The design of L_{1i} and L_{2i} is made using the desired ripple value of the input current. When the nominal duty cycle $d = 0.235$, the input-side inductor L_{1i} is chosen based on the specified maximum current ripple

$$L_{1i} = \frac{\hat{V}_g dT_{\rm sw}}{\Delta i_{L_{1i}}} = 5.068\ {\rm mH}. \tag{4}$$

Switching period $T_{\rm sw}$ is $1/f_{\rm sw}$. The measured inductance of the designed input inductor is 5 mH at 30 kHz. The output-side inductor L_{2i} is then selected using

$$L_{2i} = \frac{n_{\rm Tr}^2 L_{1i} L_{\rm eq}}{L_{1i} - L_{\rm eq}} = 81\ \mu{\rm H}. \tag{5}$$

TABLE I
Specification and Parameters of a Modular Three-Phase AC-to-DC Converter Using CUK Rectifier Modules

Characteristic	Power Modules
Input Phase Voltage	220 V
Input Frequency	50 Hz
Switching Frequency	Variable frequency, ≈ 25-30 kHz
Rated Module	250 W/module
Total Output Power	750 W
Output Voltage	-48 V
L_{11},L_{12},L_{13}	5.069 mH, 5.068mH, 5.066 mH
L_{21},L_{22},L_{23}	1.066 mH, 1.086 mH, 1.044 mH
C_a, C_b, C_o	0.68 μF, 13,600 μF
k_p, ω_z	1, 150
K_1,K_2	0.707, 1.414
n_{Tr}	0.5

The measured magnetizing inductance is 1 mH at 30 kHz. The design of the intermediate capacitor C_a, considering a resonant frequency of 2.5 kHz, which is a good initial approximation for C_a, is given by

$$C_a = \frac{1}{\omega_r^2\,(L_{1i} - L_{2i})} = 0.55\ \mu{\rm F}. \tag{6}$$

Let $C_a = 0.68\ \mu$F ($C_a = C_b$). The output dc capacitance C_O is determined according to the hold-up time $\Delta_{\rm th}$. By choosing $\Delta_{\rm th} \geq 2$ ms, one can find

$$C_{o,\min} = \frac{2P_o\Delta_{\rm th}}{V_o^2 - V_{o,\min}^2} = 10\,683\ \mu{\rm F}. \tag{7}$$

Minimum capacitor value ($C_{\rm o,min}$) must be derated for capacitor tolerance ($\Delta C_{\rm tol}$), 20% in this case, in order to guarantee that minimum capacitance requirement is satisfied, thus assuring minimum hold-up time

$$C_o = \frac{C_{o,\min}}{1 - \Delta C_{\rm tol}} = 13\,353\ \mu{\rm F}. \tag{8}$$

Let $C_o = 13\,600\ \mu$F. As can be seen from (7), for given V_o and $V_{o,\min}$, the larger the power P_o and/or the longer the hold-up time $\Delta_{\rm th}$, the larger the energy-storage capacitor C_o that needs to be used. As a result, in high-power applications, the size of the energy-storage capacitors often limits the maximum power density. Therefore, to maximize power density, the size of the energy-storage capacitors must be minimized. Table I shows the design results of a 750 W, −48 V, three-phase ac-to-dc using isolated CUK rectifier modules.

III. System Configuration

The schematic diagram of the proposed three-phase configuration is shown in Fig. 2. The three single-phase CUK-based PFC modules are connected in Y-connection with the neutral (Δ connection and Y-connection without the neutral are also possible) and in parallel at the output side. The Δ-connected switch-mode rectifier topology can be operated with a three-phase, three-wire supply system while Y-connected switch-mode rectifier topology needs neutral connection and is only good for three-phase, four-wire supply system. Therefore, contrary to Y-connected switch-mode rectifier, the Δ-connected switch-mode rectifier is good for a supply system where neutral connection is not available, such as telecommunication

equipment. However, to demonstrate the dynamic performance of Y-connected switch-mode rectifier topology, in this investigation, a three-phase four-wire supply system is considered.

All power devices of the PFC circuit, including the bridge rectifier, and the power circuit components of the CUK converter are modularized. A single-capacitor output C_o is connected at the output terminals for filtering the output voltage ripples. Block diagram of the proposed control scheme of a modular three-phase ac-to-dc converter based on power balance control technique, which is able to handle heavy step load change, is also shown. It consists of sinusoidal references, a PI controller, and inductor current calculators. The differential amplifier and precision full-wave rectifier circuit are used for generating an absolute sinusoidal waveform that synchronizes with the utility. The bandpass filter is used for reducing the effect of switching noises.

This paper proposes a control concept, denoted as the power balance control, to simplify the design procedure of the dc bus voltage regulator. This control strategy has high dynamic features, and can achieve a fast dynamic transient response by action of the inductor current compensator. The procedure of analysis presented here is less difficult than that of the conventional method. It is easy to understand and implement. The deduction of the proposed inductor current compensator is also quite easy, but the effect is sensible. The control block diagram, as shown in Fig. 2, can be easily implemented by analog circuits. It shows a good improvement in reducing manufacturing costs due to the use of analog control. The advantages of the proposed system are: high power factor, modularity, simple control strategy, and design; the line frequency harmonic current components in the output capacitor are cancelled. In addition, this significantly reduces capacitor heating, improves its operating life, and minimizes its value. The output voltage is regulated and fast dynamic response is obtained.

IV. Average Small-Signal Analysis

In this section, an analysis and design of the modular three-phase ac-to-dc converter using three single-phase isolated CUK rectifier modules with nearly unity power factor and fast dynamic transient response is presented under the CCM of operation. The small-signal analysis is performed on an average basis over a complete half-line cycle. There are two major concerns of the small-signal performance of the circuit. First, the control circuit has to force the input line current to track the input voltage waveform. The second consideration is that the analysis of the circuit is based on a cycle-to-cycle basis. The analytical model derivation is based on the power stage schematic shown in Fig. 1, where the ideal switches and zero equivalent series resistance (ESR) in the capacitors are assumed. The following equation can be derived from a set of different equations with the assumption of the balanced three-phase set of ac source and four-wire system.

The average small-signal model of the proposed system is

$$\sum_{i=a}^{c} V_{gi} I_{L_{1i}} = V_o I_o \tag{9}$$

where, $i = a, b,$ and c, V_{gi} is the rms value of rectified voltages, $I_{L_{1i}}$ is the rms value of input inductor currents, V_o is the average value of dc output voltage, and I_o is the average value of dc output current over a half-line cycle. The peak value of the inductor current is

$$\hat{I}_{L_{1i}} = \frac{K_2 V_o I_{\text{load}}}{3V_{gi}} \tag{10}$$

$$\hat{I}_{L\text{ref}_{1i}} = \hat{I}_{L_{1i}} + I_{VR} \tag{11}$$

where $\hat{I}_{L\text{ref}_{1i}}$ is the reference value for the peak value of input inductor currents, $\hat{I}_{L_{1i}}$ is the peak value of input inductor currents, I_{VR} is the correcting signal of PI controller, and K_2 is the conversion gain of inductor current. The inductor reference current is

$$i_{L\text{ref}_{11}} = \hat{I}_{L\text{ref}_{11}} \left|\sin(\omega t)\right| \tag{12}$$

$$i_{L\text{ref}_{12}} = \hat{I}_{L\text{ref}_{12}} \left|\sin(\omega t - 120^\circ)\right| \tag{13}$$

$$i_{L\text{ref}_{13}} = \hat{I}_{L\text{ref}_{13}} \left|\sin(\omega t - 240^\circ)\right|. \tag{14}$$

The dynamic equation of the output voltage is

$$\sum_{i=1}^{3} I_{oi} = I_o = C_o \frac{dV_o}{dt} + I_{\text{load}} \tag{15}$$

where I_{load} is the load current of the proposed system. For derivation of the small signal model, let

$$V_{gi} = \bar{V}_{gi} + \tilde{v}_{gi} \tag{16}$$

$$I_{L_{1i}} = \bar{I}_{L_{1i}} + \tilde{i}_{L_{1i}} \tag{17}$$

$$V_o = \bar{V}_o + \tilde{v}_o \tag{18}$$

$$I_o = \bar{I}_o + \tilde{i}_o \tag{19}$$

$$\hat{I}_{L\text{ref}_{1i}} = \bar{\hat{I}}_{L\text{ref}_{1i}} + \tilde{\hat{i}}_{L\text{ref}_{1i}} \tag{20}$$

$$I_{VR} = \bar{I}_{VR} + \tilde{i}_{VR} \tag{21}$$

$$\hat{I}_{L_{1i}} = \bar{\hat{I}}_{L_{1i}} + \tilde{\hat{i}}_{L_{1i}} \tag{22}$$

$$I_{\text{load}} = \bar{I}_{\text{load}} + \tilde{i}_{\text{load}} \tag{23}$$

where $\bar{V}$ means the steady-state value and $\tilde{v}$ means the introduced perturbation. Applying the perturbations in (9), (10), (11), and (15), and performing the small-signal approximation ($\tilde{v}.\tilde{v} = 0$) results in

$$K_1 \bar{V}_{gi} \bar{\hat{I}}_{L\text{ref}_{1i}} = \bar{V}_o \bar{I}_o \tag{24}$$

$$\bar{I}_o = \bar{I}_{\text{load}} \tag{25}$$

$$\tilde{i}_o = \frac{3K_1 \bar{\hat{I}}_{L\text{ref}_{1i}}}{\bar{V}_o} \tilde{v}_{gi} + \frac{3K_1 \bar{V}_{gi}}{\bar{V}_o} \tilde{\hat{i}}_{L\text{ref}_{1i}} - \frac{\bar{I}_o}{\bar{V}_o} \tilde{v}_o \tag{26}$$

$$\tilde{i}_o = C_o \frac{d\tilde{v}_o}{dt} + \tilde{i}_{\text{load}} \tag{27}$$

$$\tilde{i}_{L\text{ref}_{1i}} = \tilde{i}_{L_{1i}} + \tilde{i}_{VR} \tag{28}$$

$$\tilde{\hat{i}}_{L_{1i}} = \frac{K_2 \bar{V}_o}{3\bar{V}_{gi}} \tilde{i}_{\text{load}} + \frac{K_2 \bar{I}_{\text{load}}}{3\bar{V}_{gi}} \tilde{v}_o - \frac{K_2 \bar{V}_o \bar{I}_{\text{load}}}{3\left(\bar{V}_{gi}\right)^2} \tilde{v}_{gi}. \tag{29}$$

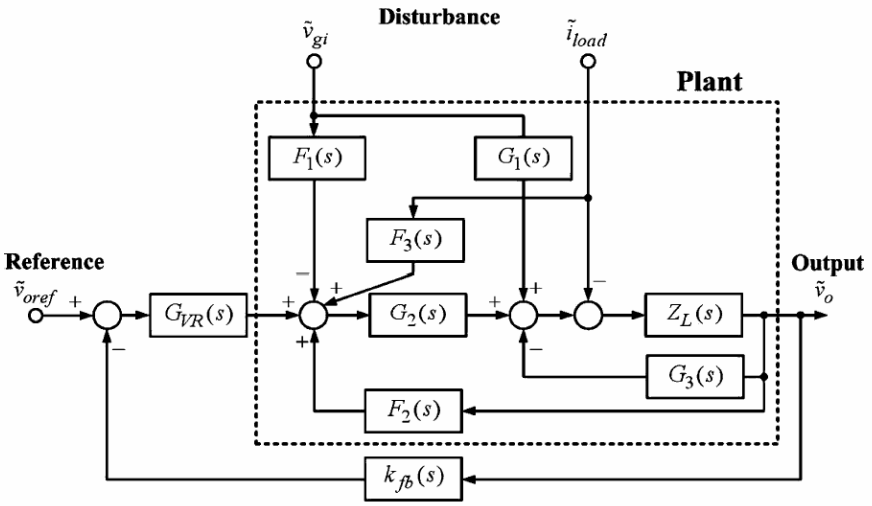

Fig. 3. Small-signal model of the modular three-phase ac-to-dc converter using isolated CUK rectifier module based on power balance control technique.

The parameters are given by

$$G_1 = \frac{3K_1 I_{L\mathrm{ref}_{1i}}}{\bar{V}_o} \tag{30}$$

$$G_2 = \frac{3K_1 \bar{V}_{gi}}{\bar{V}_o} \tag{31}$$

$$G_3 = \frac{\bar{I}_o}{\bar{V}_o} \tag{32}$$

$$F_1 = \frac{K_2 \bar{V}_o \bar{I}_{\mathrm{load}}}{3\left(\bar{V}_{gi}\right)^2} \tag{33}$$

$$F_2 = \frac{K_2 \bar{I}_{\mathrm{load}}}{3\bar{V}_{gi}} \tag{34}$$

$$F_3 = \frac{K_2 \bar{V}_o}{3\bar{V}_{gi}} \tag{35}$$

$$Z_L(s) = \frac{1}{C_o S}. \tag{36}$$

According to (24)–(36) and combining with the voltage regulator, Fig. 3 shows the small-signal control block diagram of the proposed system. Therefore, the output voltage can be expressed as

$$\tilde{v}_o = T_C \tilde{v}_{o_{\mathrm{ref}}} + T_A \tilde{v}_{gi} - Z_o \tilde{i}_{\mathrm{load}}. \tag{37}$$

From the small-signal model of Fig. 3, the following three criteria for the closed-loop performance of the converter can be identified, applying Mason gain formula. Here, T_C, T_A, and Z_o denote the control function, the audio susceptibility, and the output impedance, respectively.

The control function T_C, which carries the information about the absolute and relative stability of the converter, is

$$\frac{\tilde{v}_o}{\tilde{v}_{o_{\mathrm{ref}}}} = \frac{G_2 Z_L G_{VR}}{1 + k_{fb} G_2 Z_L G_{VR} + G_3 Z_L - G_2 Z_L F_2}. \tag{38}$$

The audio susceptibility: T_A, which presents the input-to-output noise transmission characteristics, is

$$\frac{\tilde{v}_o}{\tilde{v}_{gi}} = \frac{Z_L\left(G_1 - F_1 G_2\right)}{1 + k_{fb} G_2 Z_L G_{VR} + G_3 Z_L - G_2 Z_L F_2}. \tag{39}$$

The output impedance: Z_O, which characterizes the output voltage perturbation produced by a varying load

$$\frac{\tilde{v}_o}{\tilde{i}_{\mathrm{load}}} = \frac{Z_L\left(1 - F_3 G_2\right)}{1 + k_{fb} G_2 Z_L G_{VR} + G_3 Z_L - G_2 Z_L F_2}. \tag{40}$$

A converter is with fast dynamic regulation if the output impedance and audio susceptibility are zero, i.e., the output voltage of the converter is independent of variations of the load current and the input line voltage. It is easy to prove, from (24), (25), (39), and (40), that the proposed system is with fast dynamic regulation if $\tilde{v}_o/\tilde{v}_{gi} = 0$

$$0 = \frac{Z_L\left(G_1 - F_1 G_2\right)}{1 + k_{fb} G_2 Z_L G_{VR} + G_3 Z_L - G_2 Z_L F_2} \tag{41}$$

where

$$G_1 = G_2 F_1 \tag{42}$$

when $\tilde{v}_o/\tilde{i}_{\mathrm{load}} = 0$

$$0 = \frac{Z_L\left(1 - F_3 G_2\right)}{1 + k_{fb} G_2 Z_L G_{VR} + G_3 Z_L - G_2 Z_L F_2} \tag{43}$$

where

$$F_3 G_2 = 1. \tag{44}$$

Therefore, the gain K_2 can be expressed as

$$K_2 = K_1^{-1} = \sqrt{2}. \tag{45}$$

Then, the control function can be expressed as

$$\frac{\tilde{v}_o}{\tilde{v}_{o_{\mathrm{ref}}}} = \frac{3G_{VR}\bar{V}_{gi}K_1}{\bar{V}_o C_o S + 3G_{VR}\bar{V}_{gi}K_1 k_{fb}}. \tag{46}$$

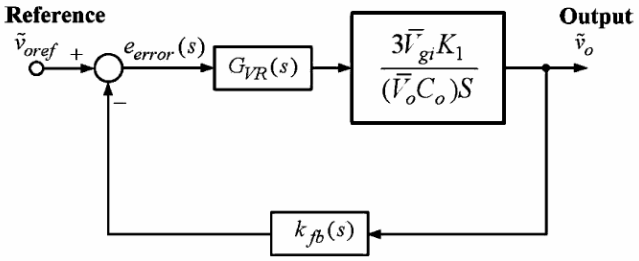

Fig. 4. Implementation of a power balance control technique.

Here, a PI controller is chosen for voltage regulation

$$G_{VR}(s) = \frac{k_p\,(S+\omega_Z)}{S}. \tag{47}$$

Plant transfer function is

$$\text{PTF} = \frac{3\bar{V}_{gi}K_1}{(\bar{V}_oC_o)S}. \tag{48}$$

Open-loop transfer function is

$$\text{OLTF} = \frac{3G_{VR}(s)\bar{V}_{gi}K_1k_{fb}}{(\bar{V}_oC_o)S}. \tag{49}$$

Power balance control technique is specially designed to remove the periodic errors generated due to the external disturbances. The idea of power balance control technique, which is based on the input voltage and load current feedforward principle, is to improve the control performance. The proposed control technique can be designed in the closed loop, as shown in Fig. 4.

The frequency response analysis is used to describe the stability of the proposed system. The design of the output voltage control loop must guarantee the stability and provide enough bandwidth in all the possible operation conditions of the system. A suitable network is based on integral action (zero and high frequency). With balance three-phase operation, there is no low-frequency ripple in the output voltage. Hence, the output voltage control loop can be designed for higher or lower bandwidth, resulting in dynamic response. The Bode diagram of (47), (48), and (49) is presented in Fig. 5. Since this is a linear system, superposition technique can be applied to drive the overall system transfer function. By superimposing the gains and phases of the stage around the loop, a Bode plot of the overall system is generated. The high- and zero frequency gain of the compensation network can then be used to optimize the system performance. Fig. 5 combines the Bode plots of the stages, and 180° phase shift is also added to account for the negative feedback of the system. The voltage loop is designed to have a crossover frequency of 50 Hz.It also gives a 65° phase margin.

V. Circuit Simulations

In this section, a modular three-phase ac-to-dc converter using CUK rectifier modules based on power balance control technique with nearly unity power factor and fast dynamic transient response are discussed. The configuration of the proposed system is simulated using SIMULINK program. The purpose of this simulation is to verify the control algorithms, design the controller parameters, and study the static and dynamic performances of the system. The converter under focus is capable of: 1) three-phase power balance condition; 2) two-module loss (in phase a and b); 3) one-module loss (in phase c); and 4) step load change from 100% to 10% and *vice versa* with three-phase power balance condition. A rated operation of 750 W output power and −48 V of dc output voltage with 220 V of ac line-to-neutral voltage in rms are assumed.

The control block diagram is shown in Fig. 2, where three inductor currents and dc voltage are sensed for the feedback control proposes. In addition, in order to improve dynamic response in the dc voltage control, load current i_{load} is also sensed and added to the inductor current amplitude reference as load feedforward. Fig. 6 shows steady-state and transient simulation results of four difference operating conditions. The simulation does analyze the following modules and load conditions: 0–100 ms: three-phase power balance condition, 100–200 ms: two-module loss (in phase a and b), 200–300 ms: return of loss modules in phase a and b, 300–400 ms: one-module loss (in phase c), 400–500 ms: return to three-phase balance condition, 500–550 ms: step load change from 100% to 10% with power three-phase balance condition, and 550–600 ms: step load change from 10% to 100% with power three-phase balance condition. The simulation results of the proposed system are shown in Fig. 7(a)–(d). Fig. 7(a) shows simulated input phase voltage and current waveform of the proposed system based on power balance control technique. It can be seen from these figures that almost unity power factor and nearly sinusoidal ac current operation are achieved. The simulation results of transient response of the input phase current waveforms, phase inductor current waveforms at step load change from 750 to 75 W and *vice versa* are shown in Fig. 7(b) and (c), respectively. It may be noted that the ac currents waveform quality under the lightly loaded condition in Fig. 7(b) is degraded. The simulation result of transient response of the output voltage and load current waveforms at step load 750 to 75 W and *vice versa* are shown in Fig. 7(d). The output voltage is recovered to its steady state within 100 μs. By utilizing load feedforward, high bandwidth of the voltage control loopis well-compensated and dc bus voltage is hardly disturbed.

VI. Hardware Experiments

A prototype of the modular three-phase ac-to-dc converter has been built and tested with the component values, as shown in Table I. The main objectives are to improve the dynamic transient response of dc bus output voltage, module load current sharing, and power factor correction. The analog circuit is used in the control circuitry of the prototype. The experimental results of the proposed system are shown in Figs. 8–10. A 1-μF capacitor C_i is placed before the bridge rectifier to filter the high-frequency switching current ripple. Fig. 8 shows the line voltage and current after filtering. Fig. 8(a) shows steady-state response of input voltage and current waveforms. It can be seen that the input currents are not significantly distorted while phase input voltage is distorted due to the normal condition of utility

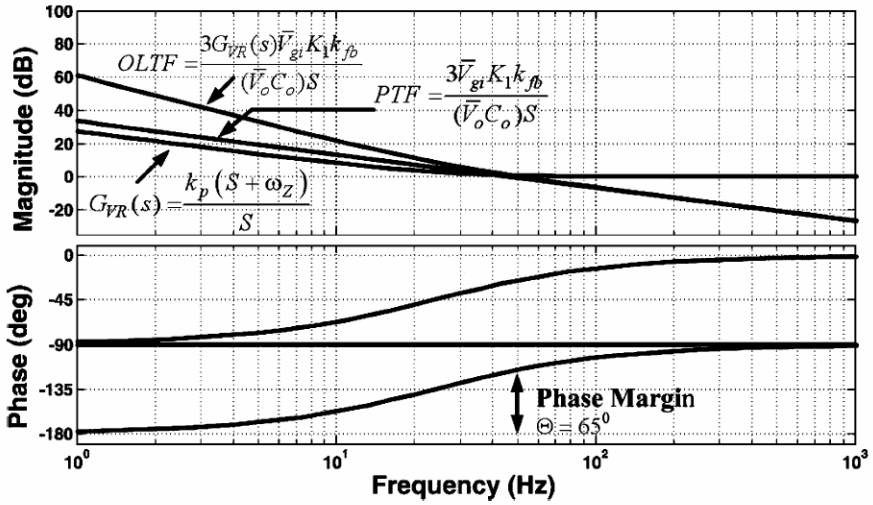

Fig. 5. Representative Bode plots of the proposed system.

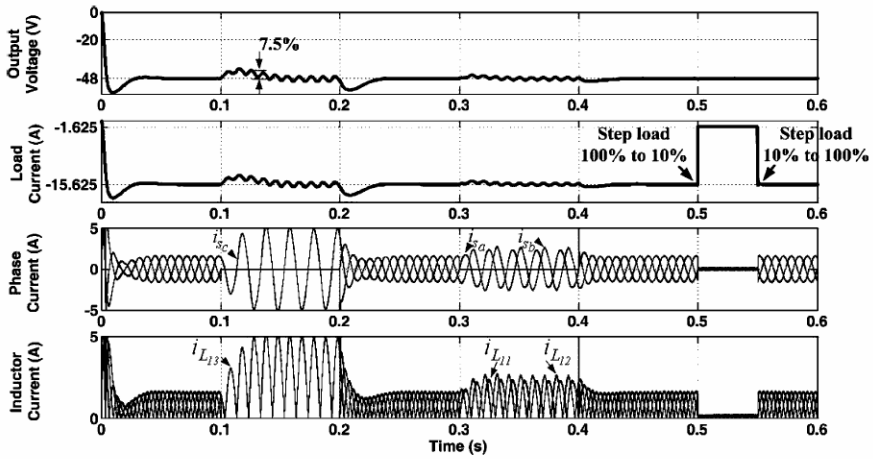

Fig. 6. Simulation results for the output voltage v_O and load current $i_{\rm load}$, the individual input phase currents ($i_{s_a}, i_{s_b}, i_{s_c}$), the inductor currents ($i_{L_{11}}, i_{L_{12}}, i_{L_{13}}$) for symmetric mains condition, module loss in phase a and b, module loss in phase c, and steps load change from 100% to 10% and back to 100%.

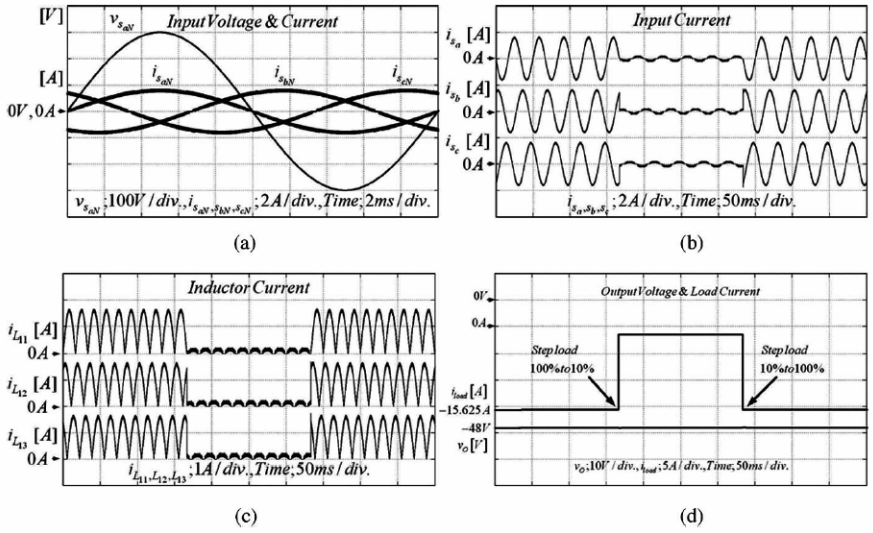

Fig. 7. Simulated steady-state and dynamic response of the proposed system.

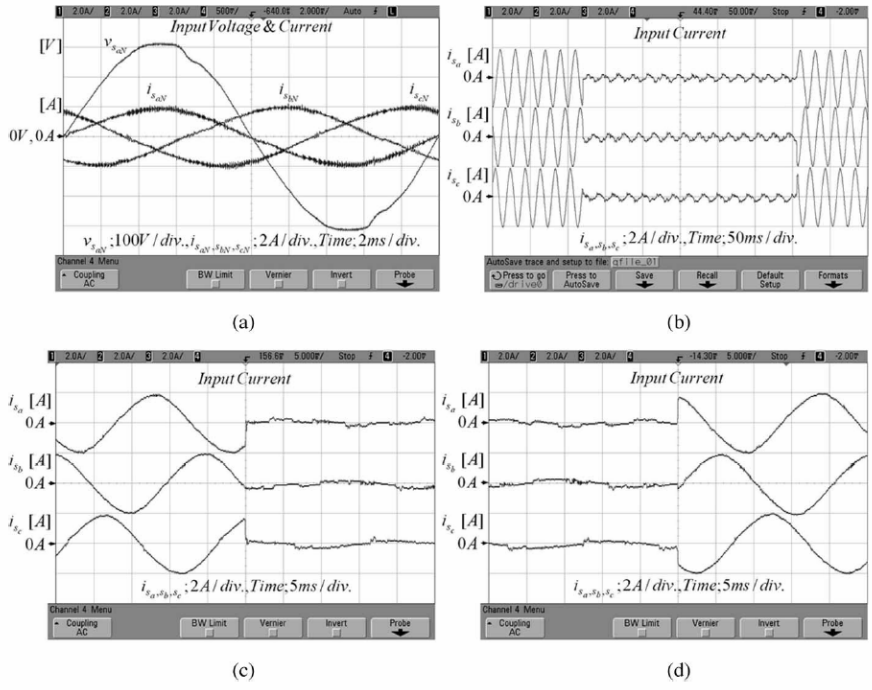

Fig. 8. Hardware experimental results of the input voltage v_{saN} and phase current i_{sa}, i_{sb}, and i_{sc}.

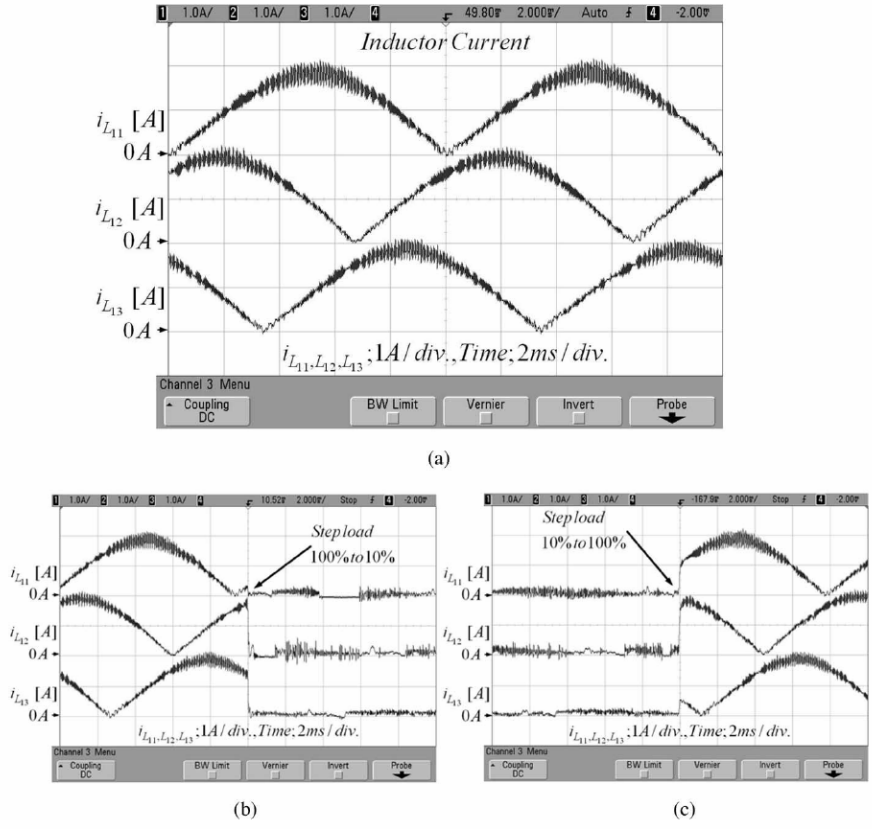

Fig. 9. Hardware experimental results of the inductor current.

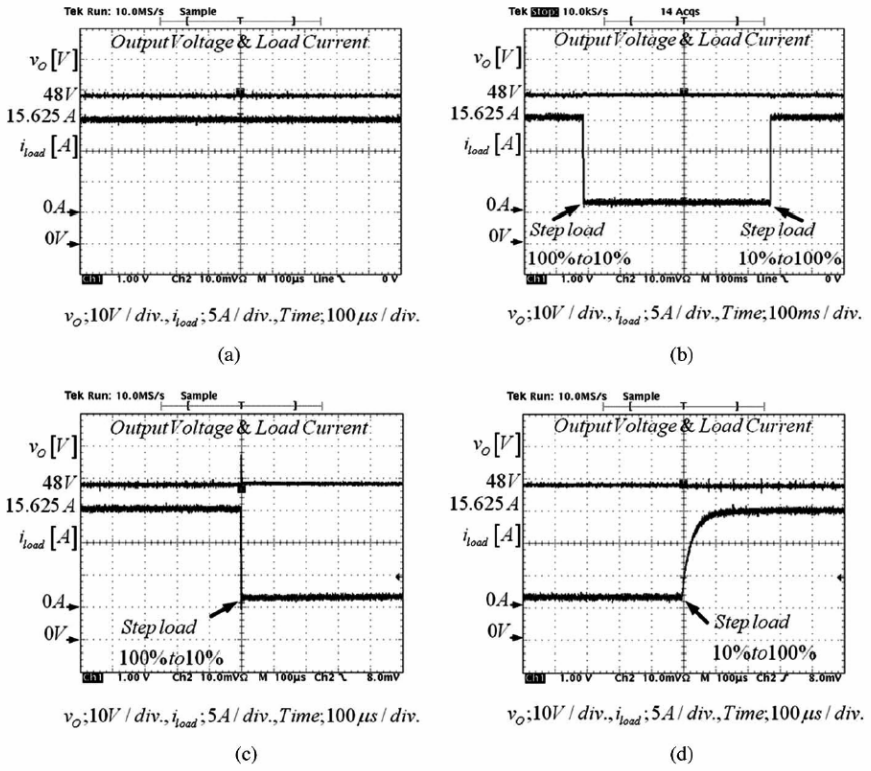

Fig. 10. Hardware experimental results of the output voltage v_O and load current $i_{\rm load}$.

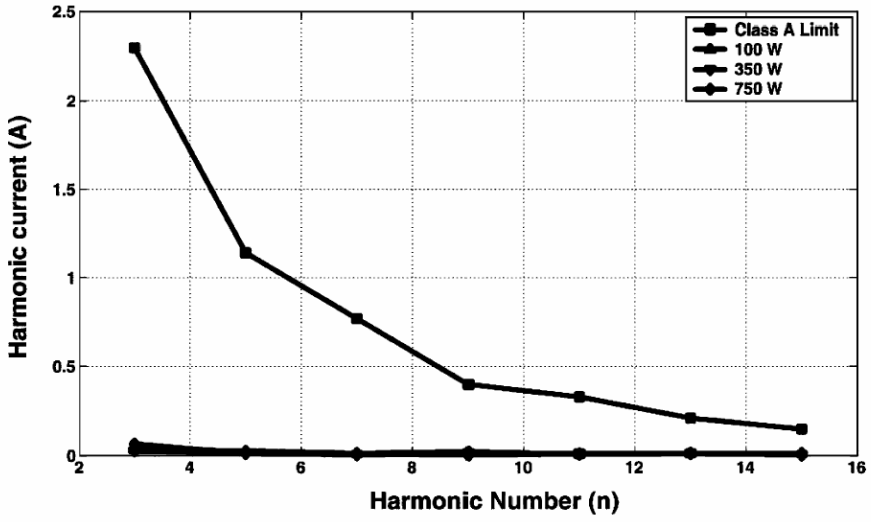

Fig. 11. Harmonics current as a function of harmonic order and output power versus IEC 61000-3-2 Class A limits ($V_s = 220$ V and $V_o = -48$ V).

voltage quality in the laboratory. Input currents are in phase with their relative phase voltages, almost sinusoidal and balanced. A power factor of 0.99 and a total harmonic distortion (THD) of 4% have been measured at input port of this high-power-factor ac-to-dc converter. However, the input current is distorted simply because the inner inductor current control loops do employ current reference values, which are generated by multiplying a reference peak value for input inductor currents with the actual absolute values of the line-to-neutral voltage. Therefore, up to a certain point, in the future research, the reference line-to-neutral voltages may be generated by mean of using a three-phase phase-locked loop (PLL) system.

The transient response of the three-input current at load step from 750 to 75 W and *vice versa* are shown in Fig. 8(b). The close-up of three-phase input currents while load has been changed from 750 to 75 W and from 75 to 750 W are shown in Fig. 8(c) and (d), respectively. One problem associated with the variable hysteresis control is the very high switching

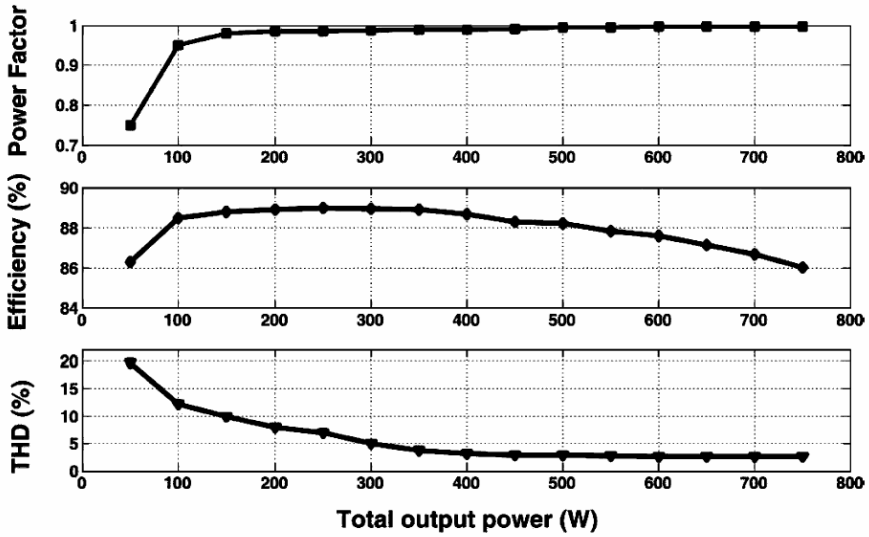

Fig. 12. Power factor, efficiency, and THD_i as a function of output power ($V_s = 220$ V and $V_o = -48$ V with resistive load).

frequency at the end of a rectified line cycle, where the voltage approaches zero. As predicated from the preceding sections, the ac currents waveform is relatively degraded in lightly loaded operation. Since the operation mode of CUK rectifier modules are changed from CCM to critical mode. Equation (2) can be satisfied only in a limited load range. In fact, increasing R (load resistance) produces a consequent decrease of the value of coefficient K_a unit; it becomes lower than the second term of (2). Moreover, for a given load resistance, converter operation can change from CCM to DCM. Designing the converter to always operate in CCM for a given load calls for an oversize of L_{eq}. An alternative approach could be to design the converter to operate in CCM for $\theta_{\mathrm{crit}} < \theta < \pi - \theta_{\mathrm{crit}}$ even at minimum load resistance. The critical angle θ_{crit} changes as the load R changes, and is derived from (2). The choice of θ_{crit} at full load is, therefore, a tradeoff between size of power stage components and input distortion in different load condition. Therefore, up to a certain point, selecting a bigger inductor reduces the large distortion and improves the performance of the power stage.

Fig. 9(a) shows the steady state of three-individual inductor current waveforms. The close-up of three-individual inductor currents at step load from 750 to 75 W and from 75 to 750 W are shown in Fig. 9(b) and (c). Due to the effects of difference inductance values and parasitic in input inductors, these three-individual inductor currents are not exactly equal. However, all inductor currents have approximately same amplitude.

Fig. 10(a) shows the output voltage at -48 V and load current at -15.625 A when dc bus capacitor is 13 600 μF. Fig. 10(b) and (c) shows the experimental transient response for step load variation with the inductor current compensator. Fig. 10(b) shows the transient response of the output voltage and load current at load change from 100% to 10% and *vice versa*. It can be observed from Fig. 10(c) that the output voltage recovered to its steady state within 100 μs and input current can still maintain a high-quality sinusoidal waveform. In particular, dc output voltage v_o is hardly disturbed in spite of the low bandwidth of the dc voltage control loop due to the load feedforward. It is indicated that good dynamic performance can be achieved.

The performance measurements of the proposed system are reported, in terms of power factor, THD_i, efficiency, and harmonic current comparing with the standard EN 61000-3-2 class A limits. Fig. 11 shows the current harmonics of the proposed system versus load variations. It shows the magnitude of the measured input current harmonics for the three-phase system operating under different power levels. It meets the regulation of EN 61000-3-2 Class A limits. Fig. 12 shows the key performance of the proposed system at different output power. The upper curve in Fig. 12 presents the measured power factor for different output power. For the rated load condition, the input power factor is high, greater than 0.99; the overall efficiency remains high, nearly 90%, and THD_i less than 4% at maximum load. In this case, dc bus capacitor $C_o = 13\,600$ μF, the dc output voltage is regulated to have good transient responses by the designed PI controller with power balance control technique. It should be noted that this dynamic response is fast enough for many conventional industrial applications, and hence, no second stage is needed. Thus, the proposed regulator is relatively feasible in medium-power applications, which has been verified by the measured results.

The characteristics of the two converters are compared for the conventional three-phase PWM rectifier (boost topology) and dc–dc case (modified PFC boost and isolated CUK rectifier module) in Table II. The boost and CUK converters are good choices for cases where the input current is subject to power quality constraints. The performance of the CUK converter suggests that this is the best topology. The CUK converter also offers greater flexibility in the configuration that can be implemented as isolation is easily incorporated.

TABLE II
PROPOSED CONVERTER SYSTEM COMPARED WITH A THREE-PHASE BOOST CONVERTER

Characteristic	**Three-phase rectifier using three isolated CCM CUK rectifier modules (Proposed system)**	**Three-phase rectifier using three modified single-phase single-switch boost PFC converter (CCM)**	**Three-phase full-bridge boost rectifier (CCM)**
No. of main switches	3	3	6
Converter Efficiency	Good	Fair	Good
Input Current Quality (PFC)	Excellent (DC+Ripple, coupling the inductors by using the same core can reduce the ripple), small high-frequency ripple on the input.	Good (DC+Ripple)	Good
Conducted EMI	Low	Low	Low
Output Voltage Range	$\hat{V}_s > V_o > \hat{V}_s$ (any output voltage). Full-range output regulation.	$V_o > 1.5\hat{V}_s$ (A second dc-dc converter is required to step down the output to its required level.)	$V_o > \hat{V}_s$ (A second dc-dc converter is required to step down the output to its required level.)
Output Current	DC+Ripple. Small high-frequency ripple on the output currents.	Pulsed	DC+Ripple
Power Application	Low or high voltage and medium power application	High voltage and medium power application	High voltage and high power application
Control Complexity	Very Simple (Analog or Digital), while ensuring high control robustness and good static and dynamic performance (based on power balance control technique).	Vary Simple (Analog or Digital)	Very Complex
Isolation	Easy to add isolating transformer	Difficult, second dc-dc stage required	Difficult, second dc-dc stage required
Magnetic Volume	Large number of magnetic components required. But, full utilization of the flux swing in the transformer core.	Fewer magnetic component required	Fewer magnetic component required

VII. CONCLUSION

A three-phase ac-to-dc converter using CUK rectifier modules with nearly unity power factor and fast dynamic transient response based on power balance control technique has been investigated in this paper. The circuit simulation of interest are capable of: 1) three-phase balance condition; 2) module loss condition; and 3) step load change from 100% to 10% and *vice versa*. An average small-signal model derivation has been presented. The main advantages of the proposed system are to reduce the number of the conversion stages and improve dynamic response. The simulation and experimental results of the proposed system have confirmed that at heavy step load change, excellent power factor correction under dc-regulated output voltage are obtained by the power balance control technique. Steady-state and dynamic analyses have been discussed. The proposed approach offers the following advantages: simple control and fast dynamic response. The results obtained are: a power factor of 0.99 and THD_i of 4% have been measured. It meets the harmonic regulations of EN 61000-3-2 class A limits. The system offers 88% efficiency.

REFERENCES

[1] B. Singh, B. N. Singh, A. Chandra, K. Al-Haddad, A. Pandey, and D. P. Kothari, "A review of single-phase improved power quality AC–DC converters," *IEEE Trans. Ind. Electron.*, vol. 50, no. 5, pp. 962–981, Oct. 2003.

[2] W. Stefanutti, P. Mattavelli, G. Spiazzi, and P. Tenti, "Digital control of single-phase power factor preregulators based on current and voltage sensing at switch terminals," *IEEE Trans. Power Electron.*, vol. 21, no. 5, pp. 1356–1363, Sep. 2006.

[3] Y. Jang, M. M. Jovanovic, K.-H. Fang, and Y.-M. Chang, "High-power-factor soft-switched boost converter," *IEEE Trans. Power Electron.*, vol. 21, no. 1, pp. 98–104, Jan. 2006.

[4] M. Chen and J. Sun, "Feedforward current control of boost single-phase PFC converters," *IEEE Trans. Power Electron.*, vol. 21, no. 2, pp. 338–345, Mar. 2006.

[5] M. Chen and J. Sun, "Low-frequency input impedance modeling of boost single-phase PFC converters," *IEEE Trans. Power Electron.*, vol. 22, no. 4, pp. 1402–1409, Jul. 2007.

[6] J.-R. Tsai, T.-F. Wu, C.-Y. Wu, Y.-M. Chen, and M.-C. Lee, "Interleaving phase shifters for critical-mode boost PFC," *IEEE Trans. Power Electron.*, vol. 23, no. 3, pp. 1348–1357, May 2008.

[7] L. Huber, B. T. Irving, and M. M. Jovanovic, "Open-loop control methods for interleaved DCM/CCM boundary boost PFC converters," *IEEE Trans. Power Electron.*, vol. 23, no. 4, pp. 1649–1657, Jul. 2008.

[8] R. T. Chen and Y. Y. Chen, "A single-stage push–pull boost converter with integrated magnetics and input current shaping technique," *IEEE Trans. Power Electron.*, vol. 21, no. 5, pp. 1193–1203, Sep. 2006.

[9] J. Chen, D. Maksimovic, and R. W. Erickson, "Analysis and design of a low-stress buck–boost converter in universal-input PFC applications," *IEEE Trans. Power Electron.*, vol. 21, no. 2, pp. 320–329, Mar. 2006.

[10] D. D.-C. Lu, H. H.-C. Iu, and V. Pjevalica, "A single-stage AC/DC converter with high power factor, regulated bus voltage, and output voltage," *IEEE Trans. Power Electron.*, vol. 23, no. 1, pp. 218–228, Jan. 2008.

[11] R. Zane and D. Maksimovic, "Nonlinear-carrier control for high-power-factor rectifiers based on up–down switching converters," *IEEE Trans. Power Electron.*, vol. 13, no. 2, pp. 213–221, Mar. 1998.

[12] L. Rossetto, G. Spiazzi, P. Tenti, B. Fabiano, and C. Licitra, "Fast-response high-quality rectifier with sliding mode control," *IEEE Trans. Power Electron.*, vol. 9, no. 2, pp. 146–152, Mar. 1994.

[13] R. Itoh and K. Ishizaka, "Single-phase step-up/down current-source rectifier with suppressed resonance," *Inst. Electr. Eng. Electr. Power Appl.*, vol. 141, no. 1, pp. 19–25, Jan. 1994.

[14] C.-J. Tseng and C.-L. Chen, "A novel ZVT PWM CUK power-factor corrector," *IEEE Ind. Electron.*, vol. 46, no. 4, pp. 780–787, Aug. 1999.

[15] S. Buso, G. Spiazzi, and D. Tagliavia, "Simplified control technique for high-power-factor flyback CUK and Sepic rectifiers operating in CCM," *IEEE Trans. Ind. Appl.*, vol. 36, no. 5, pp. 1413–1418, Sep./Oct. 2000.

[16] M. Brkovic and S. Cuk, "Input current shaper using CUK converter," in *Proc. IEEE INTELEC Conf.*, 1992, pp. 532–539.

[17] G. Ranganathan and L. Umanand, "Power factor improvement using DCM CUK converter with coupled inductor," in *Proc. Inst. Electr. Eng. Electr. Power Appl. Conf.*, 1999, pp. 231–236.

[18] D. S. L. Simonetti, J. Sebastian, F. S. dos Reis, and J. Uceda, "Design criteria for SEPIC and CUK converters as power factor preregulators in discontinuous conduction mode," in *Proc. IEEE PEMC Conf.*, 1992, pp. 283–288.

[19] A. Newton, T. C. Green, and D. Andrew, "AC/DC power factor correction using interleaved boost and CUK converters," in *Proc. Inst. Electr. Eng. PEVSD Conf.*, 2000, pp. 293–298.

[20] S. Kim and P. N. Enjeti, "Control of multiple single-phase PFC modules with a single low-cost DSP," *IEEE Trans. Ind. Appl.*, vol. 39, no. 5, pp. 1379–1385, Sep./Oct. 2003.

[21] S. Kim and P. N. Enjeti, "A parallel-connected single phase power factor correction approach with improved efficiency," *IEEE Trans. Power Electron.*, vol. 19, no. 1, pp. 87–93, Jan. 2004.

[22] J. Hahn, P. N. Enjeti, and I. J. Pitel, "A new three-phase power-factor correction scheme using two single-phase PFC modules," *IEEE Trans. Ind. Appl.*, vol. 38, no. 1, pp. 123–130, Jan./Feb. 2000.

[23] B. Singh, S. Gairola, B. N. Singh, A. Chandra, and K. Al-Haddad, "Multipulse AC–DC converters for improving power quality: A review," *IEEE Trans. Power Electron.*, vol. 23, no. 1, pp. 260–281, Jan. 2008.

[24] B. Singh, B. N. Singh, A. Chandra, K. Al-Haddad, A. Pandey, and D. P. Kothari, "A review of three-phase improved power quality AC–DC converters," *IEEE Trans. Ind. Electron.*, vol. 51, no. 3, pp. 641–660, Jun. 2004.

[25] G. Spiazzi and F. C. Lee, "Implementation of single-phase boost power-factor-correction circuits in three-phase applications," *IEEE Trans. Ind. Electron.*, vol. 44, no. 3, pp. 365–371, Jun. 1997.

[26] L. C. Gomes de Freitas, M. G. Simoes, C. A. Canesin, and L.C. de Freitas, "Programmable PFC based hybrid multipulse power rectifier for ultra clean power application," *IEEE Trans. Power Electron.*, vol. 21, no. 4, pp. 959–966, Jul. 2006.

[27] H. M. Suryawanshi, M. R. Ramteke, K. L. Thakre, and V. B. Borghate, "Unity-power-factor operation of three-phase AC–DC soft switched converter based on boost active clamp topology in modular approach," *IEEE Trans. Ind. Electron.*, vol. 23, no. 1, pp. 229–236, Jan. 2008.

[28] X. H. Wu, S. K. Panda, and J. X. Xu, "Analysis of the instantaneous power flow for three-phase PWM boost rectifier under unbalanced supply voltage conditions," *IEEE Trans. Power Electron.*, vol. 23, no. 4, pp. 1679–1691, Jul. 2008.

[29] P. Xiao, K. A. Corzine, and G. K. Venayagamoorthy, "Multiple reference frame-based control of three-phase PWM boost rectifiers under unbalanced and distorted input conditions," *IEEE Trans. Power Electron.*, vol. 23, no. 4, pp. 2006–2017, Jul. 2008.

[30] T. Nussbaumer and J. W. Kolar, "Improving mains current quality for three-phase three-switch buck-type PWM rectifiers," *IEEE Trans. Power Electron.*, vol. 21, no. 4, pp. 967–973, Jul. 2006.

[31] T. Nussbaumer, M. Baumann, and J. W. Kolar, "Comprehensive design of a three-phase three-switch buck-type PWM rectifier," *IEEE Trans. Power Electron.*, vol. 22, no. 2, pp. 551–562, Mar. 2007.

[32] L.-S. Yang, T.-J. Liang, and J.-F. Chen, "Analysis and design of a novel three-phase AC–DC buck-boost converter," *IEEE Trans. Power Electron.*, vol. 23, no. 2, pp. 707–714, Mar. 2008.

[33] Y. K. E. Ho, S. Y. R. Hui, and Y.-S. Lee, "Characterization of single-stage three-phase power-factor-correction circuit using modular single-phase PWM DC-to-DC converters," *IEEE Trans. Power Electron.*, vol. 15, no. 1, pp. 62–71, Jan. 2000.

[34] J. A. Pomilio and G. Spiazzi, "High-precision current source using low-loss, single-switch, three-phase AC/DC converter," *IEEE Trans. Power Electron.*, vol. 11, no. 4, pp. 561–566, Jul. 1996.

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