รายงานวิจัยฉบับสมบูรณ์

โครงการ
วงจรกรองความถี่ต่ำผ่านที่กินกำลังระดับนาโนวัตต์โดยใช้วงจรตาม แรงดันแบบพลิกกลับสำหรับการตรวจรับคลื่นไฟฟ้าหัวใจ

โดย นายชูธรรม สาวิกันย์และคณะ

มิถุนายน 2562

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สนับสนุนโดยสำนักงานคณะกรรมการการอุดมศึกษา และสำนักงานกองทุนสนับสนุนการวิจัย

บทสรุปผู้บริหาร

ชื่อโครงการ วงจรกรองความถี่ต่ำผ่านที่กินกำลังระดับนาโนวัตต์โดยใช้วงจรตามแรงดันแบบพลิกกลับสำหรับการตรวจรับคลื่นไฟฟ้าหัวใจ

Project title: A Nanopower Flipped Voltage follower Lowpass Filter for ECG Acquisition

บทคัดย่อ โครงการวิจัยนี้ได้เสนอการนำวงจรที่สร้างจากทรานซิสเตอร์สนามไฟฟ้าที่เรียกว่า “วงจรตามแรงดันแบบพลิกกลับ” มาสร้างเป็นวงจรกรองความถี่ต่ำผ่านอันดับสี่แบบ “ทรานส์คอนดักแตนซ์ตัว-เก็บประจุ” วงจรกรองดังกล่าวนี้ถือว่ามีความกะทัดรัดที่สุดและกินกำลังงานต่ำสุดในปัจจุบัน โดยได้ทำการออกแบบและผลิตขึ้นจากเทคโนโลยีวงจรรวมขนาด 0.35 ไมโครเมตรให้ทำงานจากไฟเลี้ยง 0.6 โวลท์และกินกำลังงานในภาวะสงบเพียง 0.9 นาโนวัตต์ โดยมีคุณสมบัติที่เหมาะสมต่อการกรองสัญญาณไฟฟ้าจากร่างกาย โครงการนี้ครอบคลุมถึงการคิดค้นระเบียบวิธีในการออกแบบวงจรเพื่อให้ได้ความถี่ตัดที่ปรับได้ในย่านความถี่ 100 เฮิรตซ์ ถึง 250 เฮิรตซ์ และได้พิสัยพลวัตของสัญญาณสูงกว่า 45 เดซิเบล การทดสอบวงจรเพื่อพิสูจน์สมรรถนะของการกรองสัญญาณในระบบตวจจับคลื่นไฟฟ้าหัวใจที่กินกำลังงานต่ำยิ่ง ผลการวิจัยจากโครงการนี้ถูกสรุปและนำเสนอเป็นบทความตีพิมพ์ใน IEEE Transaction on Very Large Scale Integration System

Abstract: This project proposes the concept of using a compact CMOS circuit cell called “flipped voltage follower” to design a fourth-order *gm-C* lowpass filter. The filter is the most compact and power-efficient to date. The circuit has been designed and fabricated using subthreshold MOS devices to function from a supply voltage of 0.6 V and to consume 0.9 nW static power with suitable characteristics for bio-potential filtering. This project involves the development of the filter design methodology to obtain a fully integrated lowpass filter with an adjustable cutoff frequency within 100-250 Hz and dynamic range greater than 45 dB. Experiments have been done confirming the suitability of using this filter for an ultra-low-power Electrocardiography acquisition system. The findings of this project have been concluded in an article published in “IEEE Transaction on Very Large Scale Integration Systems”.

Keywords: Analog filter, Bio-potential acquisition, CMOS, Flipped voltage follower, Nanopower

Research area / Sub area of this project: “Electronics”/ “Biomedical Integrated Circuits”

1. Introduction

Designing an analog filter in CMOS technology to be functional from a low-voltage supply and to consume extremely low power, MOSFETs are usually biased in weak inversion region as they must conduct currents in the range of a few nanoamps [1]. The filter's circuit structure also needs to be suitable for a supply voltage that is minimized [2]. The aforementioned requirements call for innovative design strategies that exploit a single MOSFET to its full potential. Recently, a MOSFET that operates fundamentally as a nonlinear transconductor has been placed into several g_m-C topologies in order to design compact and power-efficient analog filters. This design concept can be categorized as a 'transistorized filter' [3] and it has been implemented successfully for cutoff frequencies from hundred-hertz [4] up to megahertz ranges [3], [5], [6].

Developed further from the concept of source-follower filter (SFF) [5], the design of 100 Hz biopotential LPFs has been proposed in [4] by biasing the SFFs in the subthreshold region. Fabricated in a 0.35 μm CMOS technology, the LPFs consume only 15 nW from a supply voltage of 3 V and attains a dynamic range (DR) of 56 dB. Although the application of the LPFs to electrocardiography (ECG) filtering has been demonstrated, it is still possible to enhance the power consumption further by employing a new transistor-level architecture that requires a supply voltage less than that of [4] while maintaining suitable circuit performance for ECG recording applications. Figure 1 illustrates the ECG detection system. The ECG voltage that varies between 0.05 - 4 mV [7] is first enlarged by a low-noise instrumentation amplifier (IA) with a voltage gain in the range of 10 to 20 [8]-[9]. After this IA stage, the LPF enhances the frequency selectivity of the system before amplifying further by a variable-gain amplifier (VGA). Finally, the signal will be converted by an analog-to-digital converter (ADC).

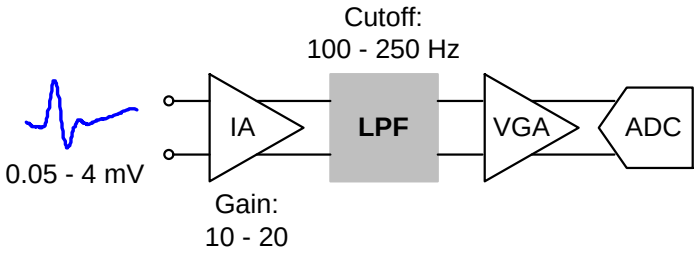

Fig. 1. ECG recording system.

Considering the amplitude variation of an ECG, the dynamic range (DR) of all the circuit blocks must be more than 44 dB [7]. Focusing on the LPF, as the ECG spectrum locates between 100 to 250 Hz [7]-[8], [10]-[11] a wide tuning capability of the LPF is not needed. Besides, the LPF needs not to handle large signal amplitudes (i.e., maximum 80 mV, for the IA's gain of 20). Moreover, it was indicated in [12] that total harmonic distortion (THD) of 3.5% can maintain significant features of an ECG. As a consequence of the moderate signal swing and generously accepted non-linearity mentioned above, the LPF should be made more power-efficient than the latest design.

Recently, the author proposed to incorporate the subthreshold pMOS flipped voltage follower (FVF) [13] and a couple of capacitors into a second-order LPFs called "pFVF biquad (pFVFB)" [14]. The pFVFB is then considered a potential candidate for the realization of a low-voltage and power-efficient second-order section and it is thus chosen to be developed further here. We should also note here that the very similar idea to [14] that employs strong inversion MOSFETs can also be found in [15] and [16]. However, the filters of [15] and [16] are dedicated for different frequency ranges and different applications.

This project proposes a power-efficient 4^{th}-order ECG LPF that fits well with the low-power ECG acquisition environment. The nMOS version of the FVFB (nFVFB) is introduced here as a complementary counterpart for the realization of a higher-order LPF. The proposed LPF circuit has been designed and fabricated in a 0.35 μm CMOS technology. It operates properly from a 0.6 V supply and consumes only 0.9 nW quiescent power. The chip measurement results and the experiment demonstrating the potential use of the LPF in ECG recording are also reported.

2. Flipped-Voltage-Follower Biquadratic Cells

Since we focus on the power and area minimization of filters, this section thus describes relevant aspects of the nano-current subthreshold FVFBs only. Strong inversion features of the FVF filter are beyond our scope.

2.1 Transistor-Level Topologies and Transfer Functions

Figures 2(a) and 2(b) show the transistor-level circuits of the n and p FVFBs, respectively. Each of them comprises transistors M_1 and M_2, and a constant current source I_B. Capacitors C_1 and C_2 are connected across the drain and source terminals of M_1 and M_2, respectively. The difference is that C_1 are connected between signal nodes but one terminal of C_2 is connected to the ac ground node. The superior aspect of FVFBs is at the stacking current-reuse structure that M_1 and M_2 are sharing the same I_B. Figure 2(c) shows the bias setup to accommodate the signal swing for the nFVFB (Fig. 2(a)) in comparison with the nMOS version of the most recent subthreshod biquad [4]. The signal inversion was made by cross-coupling connection embedded in the differential circuit of [4]. Thus there is no common-mode difference between input and output terminals of the inverting block. Note that only the nMOS versions of the biquads are illustrated here for the sake of conciseness. The pMOS versions can be also arranged in a similar manner. With these arrangements, we can see that $V_{DDA} = V_{inpp}+V_{GS1}+V_{dsat2}$ and $V_{DDB} = V_{inpp}+V_{GS1}+V_{GS2}+V_{effB}$, where V_{effB} and V_{dsat2} are the minimum voltage that the current source requires and the saturation voltage of M_2, respectively.

The current source (I_B) is made from an ordinary current mirror circuit operating in weak inversion saturation [1], we have $V_{effB} = V_{dsat2} \approx 4U_T \approx 0.1$ V. It can be seen that V_{DDA} is lower than V_{DDB} for one V_{GS1}. For the 0.35 μm n-well process employed here, threshold voltages are $V_{tn} \approx 0.46$ V and $V_{tp} \approx -0.68$ V, for n- and p-channel devices, respectively. In the subthreshold operation where n and p MOS devices conduct currents less than 1 nA, V_{GS1} and V_{SG2} can be managed (by proper sizing the transistor) to be as low as ≈ 0.45 V. Therefore, without process

and temperature variations, the FVFBs can be fit into V_{DD} of 0.6 V to accommodate V_{inpp} of 25 mV (this amplitude will approximately be doubled for differential operation presented in Sec. IID).

Consider the small-signal operation of MOSFETs by neglecting the channel length modulation (CLM), the widely-used models are shown in Figs. 3(a) and 3(b) for nMOS and pMOS, respectively. Note that CLM can be neglected here since all transistors used in this design conduct very low drain currents and having channel lengths more than ten times greater than the minimum allowable size (see Table III). Since we deal with g_m-C filters, a convenient equivalent model shown in Fig. 3(c) is proposed here to represent small-signal operations of both M_1 and M_2.

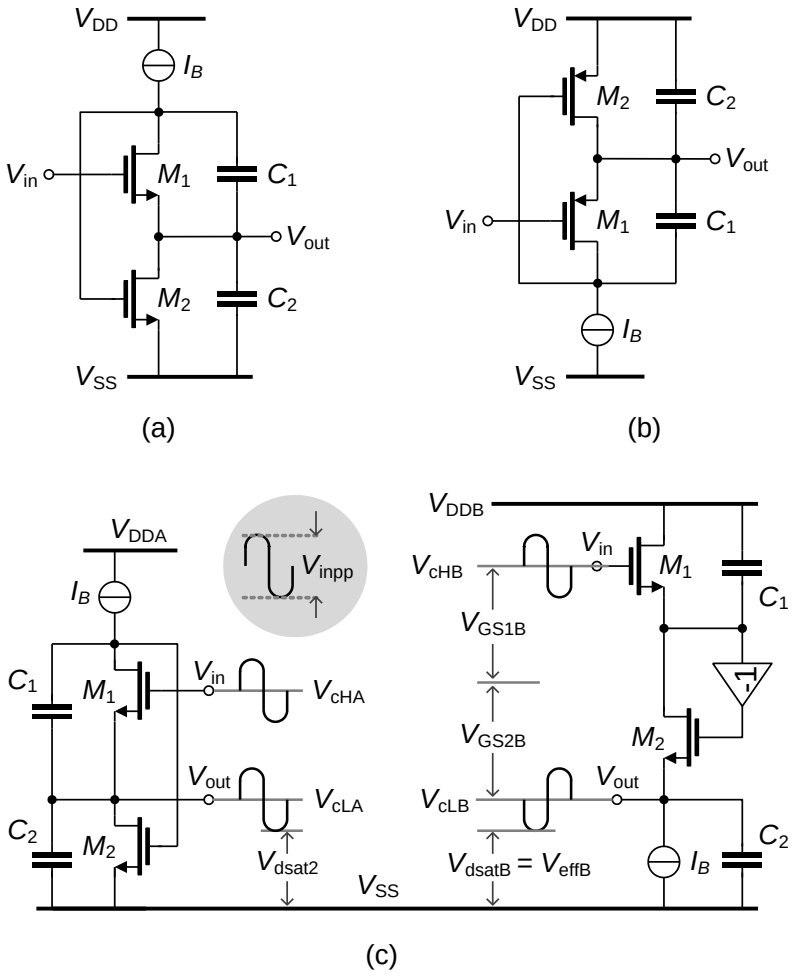

Fig. 2. FVFB circuits: (a) nFVFB, (b) pFVFB [12] and (c) bias points arrangement.

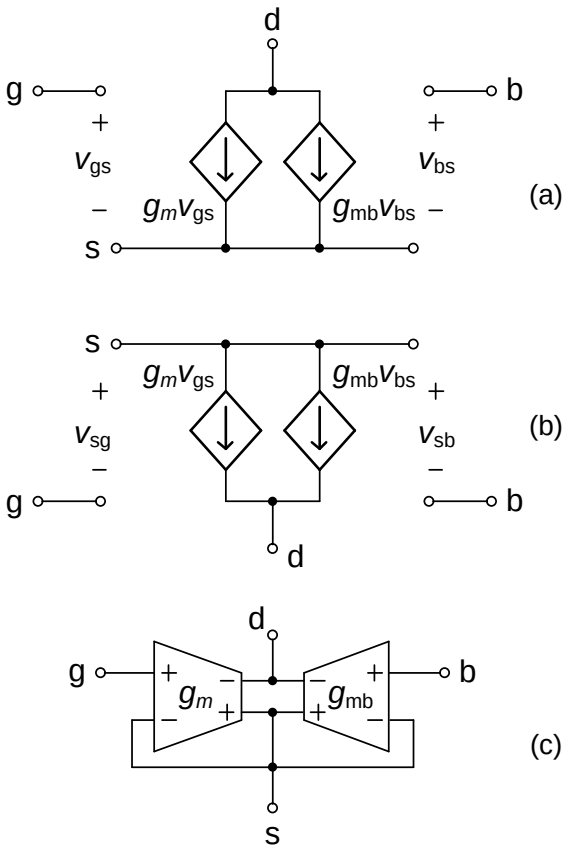

Fig. 3. Small-signal equivalent circuits: (a) nMOS, (b) pMOS, and (c) unified model available for both nMOS and pMOS.

Applying the model in Fig. 3(c) to the circuits in Fig. 2, we achieve two second order g_m-C filters represented by the macro-model shown in Fig. 4. Assuming that our filter is realized in a standard n-well CMOS process, the body terminal of nMOS M_1 in Fig. 2(a) needs to be connected to its substrate potential (V_{SS}). As a result, the body effect introduces transconductor g_{mb1} to the nFVFB as shown in the shaded area of Fig. 4. This will attenuate the passband gain of the biquad. For the pFVFB, both M_1 and M_2 can be made free from the body effect by connecting their body and source terminals together and the g_{mb1} in Fig. 4 will be omitted.

Straightforward analysis of the circuit in Fig. 4 leads to the transfer function of nFVFB as shown in (1). The transfer function of pFVFB can also be obtained from (1) by setting g_{mb1} to zero.

$$H_n(s) = \frac{V_{\text{out}}(s)}{V_{\text{in}}(s)} = \frac{\dfrac{g_{m1}g_{m2}}{C_1C_2}}{s^2 + s\left(\dfrac{g_{m2}}{C_2}\right) + \dfrac{\left(g_{m1}+g_{\text{mb1}}\right)g_{m2}}{C_1C_2}}. \quad (1)$$

Due to the current-reuse structure of FVFBs that all transistors conduct the same current I_B, we obtain small-signal transconductances $g_{m1} \cong g_{m2} \cong g_m = I_B / n_i V_T$, where V_T is the thermal voltage and n_i is the slope factor associated to each transistor [1]. Thus, passband gain K_0, natural frequency ω_n, and quality factor Q of n and p FVFBs can be extracted as shown in Table I. It can be seen that each filter's cutoff frequency can be adjusted linearly by varying the bias current. The quality factors of the filters can be set via the ratio of C_1 and C_2.

TABLE I. Biquad Parameters

Parameter	nFVFB	pFVFB
K_0	$\dfrac{1}{1+\left(g_{\text{mb1}}/g_m\right)} = \dfrac{1}{n_n}$	1
ω_n	$\dfrac{g_m}{\sqrt{KC_1C_2}} = \dfrac{I_B}{V_T\sqrt{n_nC_1C_2}}$	$\dfrac{g_m}{\sqrt{C_1C_2}} = \dfrac{I_B}{n_pV_T\sqrt{C_1C_2}}$
Quality factor	$Q_N = \sqrt{\dfrac{C_2}{KC_1}} = \sqrt{\dfrac{n_nC_2}{C_1}}$	$Q_P = \sqrt{\dfrac{C_2}{C_1}}$

TABLE II. Percentage of Noise Contribution in FVFBs

Circuit element	nFVFB	pFVFB
M_1	16.07%	16.66%
M_2	18.57%	16.36%
I_B	65.37%	66.98%
*Simulated op noise	38.86 μV_{rms}	42.32 μV_{rms}
Calculated op noise	41.8 μV_{rms}	47.47 μV_{rms}

* Integrated from 1 Hz-10f_n

2.2 Noise

Operated as a filter, the output impedances of the FVFBs (Z_{out}) are frequency-dependent and can be estimated, albeit neglecting CLM from the model in Fig. 3. It can be found for nFVFB that

$$z_{\mathrm{outN}}(s) = \frac{\dfrac{s}{C_2}}{s^2 + s\left(\dfrac{g_{m2}}{C_2}\right) + \dfrac{\left(g_{m1} + g_{\mathrm{mb1}}\right) g_{m2}}{C_1 C_2}} \quad , \tag{2}$$

and we can set g_{mb1} in (2) to zero to obtain the output impedance of pFVFB ($Z_{\mathrm{outP}}(s)$).

Fig. 5 shows the FVFBs with equivalent noise sources. Consider the noise current from M_2 (i_{n2}), it experiences the low impedances of the output nodes and then turn into the output noise voltages (v_{on2}) by the impedances or noise transfer functions defined by (2).

For nFVFB, the noise currents (i_{nB}) from current sources I_B can be converted into the output noise voltage (v_{onB}) by

$$H_{\mathrm{BN}}(s) = \frac{v_{\mathrm{onN}}(s)}{i_{\mathrm{nB}}(s)} = \frac{\dfrac{s}{C_2} - \dfrac{g_{m2}}{C_1 C_2}}{s^2 + s\left(\dfrac{g_{m2}}{C_2}\right) + \dfrac{\left(g_{m1} + g_{\mathrm{mb1}}\right) g_{m2}}{C_1 C_2}} . \tag{3}$$

Setting g_{mb1} in (3) to zero, the noise transfer function from the current source for pFVFB ($H_{\mathrm{BP}}(s)$) will be obtained.

The noise currents of M_1 (i_{n1}) can be split into two correlated noise sources located in parallel with i_{nB} and i_{n2}, respectively. The noise transfer functions for i_{n1} can thus be obtained by subtracting (2) from (3), resulting in

$$H_{1N}(s)=\frac{v_{onN}(s)}{i_{n1}(s)}=\frac{\dfrac{g_{m2}}{C_1C_2}}{s^2+s\left(\dfrac{g_{m2}}{C_2}\right)+\dfrac{(g_{m1}+g_{mb1})g_{m2}}{C_1C_2}}, \tag{4}$$

for nFVFB.

Similarly, for the case of pFVFB, g_{mb1} in (4) can be set to zero to obtain the noise transfer function for i_{n1}.

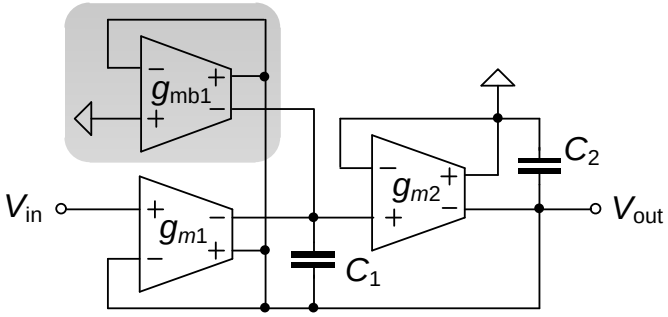

Fig. 4. g_m-C-equivalent FVFB.

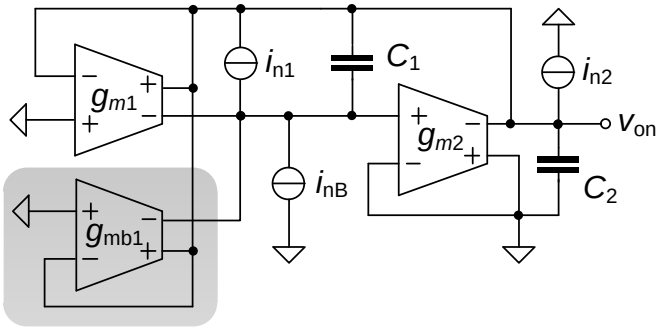

Fig. 5. FVFBs with noise sources.

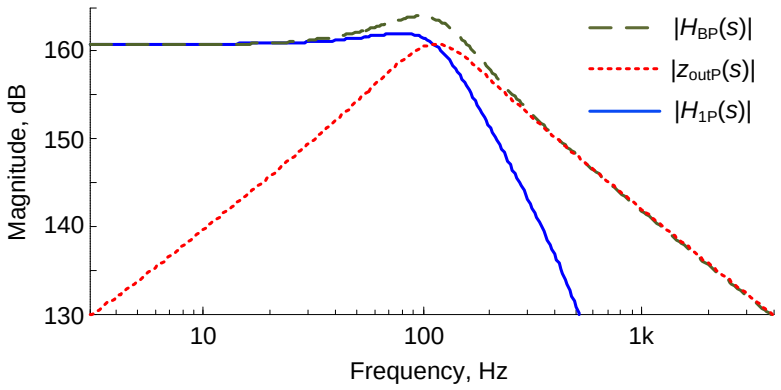

Fig. 6. Simulated noise transfer functions for pFVFB in Fig. 1(b) for $C_1 = C_2 = 12.24$ pF: $f_n \cong 100$ Hz and $Q = 1$.

Fig. 6 shows the simulated magnitude responses of the noise transfer functions of pFVFB in Fig. 2(b) for $I_B = 0.3$ nA (made by an nMOS current mirror circuit), $V_{DD} = 0.6$ V, and $C_1 = C_2 = 12.24$ pF. It can be seen that the area under the green dashed line is largest compared with the other lines. This reveals that the average output noise power contributed by I_B is greater than those by M_1 and M_2. In the case that I_B is made by a simple unity-gain current mirror that contains two identical transistors (M_B), when the weak inversion short noise is concerned, the noise current spectral densities of the transistors are defined by $S_1 = S_2 = 0.5S_B = 2qI_D$, where q and I_D stand for the electronic charge and drain current of the transistors [17], respectively ($I_D = I_B$ for all transistors in this case). Shaped by (2), (3), and (4), the average output noise power of nFVFB can be found as

$$\overline{v_{\text{on,N}}^2} \cong \underbrace{\frac{kT}{2C_1}}_{M_1} + \underbrace{\frac{n_n kT}{2C_2}}_{M_2} + \underbrace{\left(\frac{kT}{C_1} + \frac{n_n kT}{C_2} + \frac{2kT}{\sqrt{C_1 C_2}} F_N \right)}_{\text{current source transistors}} \tag{5}$$

$$\cong kT \left(\frac{1.5}{C_1} + \frac{1.5 n_n}{C_2} + \frac{2F_N}{\sqrt{C_1 C_2}} \right)$$

Also, the average output noise power of pFVFB is

$$\overline{v_{\text{on, P}}^{\,2}} \cong n_p kT\left(\frac{1.5}{C_1}+\frac{1.5}{C_2}+\frac{2F_P}{\sqrt{C_1C_2}}\right), \tag{6}$$

where the multiplication factors F_N and F_P are defined by

$$F_P=\frac{F_N}{\sqrt{n_n}}=\frac{1}{\sqrt{4Q^2-1}}\left(1-\frac{2}{\pi}\arctan\left(\frac{1-2Q^2}{\sqrt{4Q^2-1}}\right)\right). \tag{7}$$

For the same value of quality factor i.e., $Q_N = Q_P$, the multiplication factor F_N will equal F_P. Besides, (7) are valid in the range of $0.5 < Q_{N,P} \le \infty$. We verify our noise analysis by simulating the circuits in Fig. 2 and summarizing the noise contribution in each circuit compared with (5) and (6) using Boltzmann constant k = 1.38 × 10^{-23} JK^{-1}, simplified condition of $n_n \cong n_p \cong 1.5$, and V_T = 26 mV. The results are obtained in Table II showing that the calculated values differ from the simulated values by approximately 8% and 11% for n and p FVFBs, respectively.

As the filter contains only three MOSFETs and the filter is dedicated for low-frequency ECG signals, all transistors should be sufficiently large and I_B should be lower than 1 nA to suppress the flicker noise's corner frequency below 1 Hz. This can be done successfully while the chip area is still dominated by capacitors (see Fig. 11 in section V).

2.3 Feedback and Stability

Figure 7(a) represents the feedback block diagram valid for both n and p FVFB circuits in Fig. 2. The gray block (g_{mb1}) is omitted for pFVFB as the bulk effect is absent and the full diagram is applied for nFVFB. Blocks Z_1 and Z_2 represent impedances across drain and source terminals of M_1 and M_2, respectively. For realistic approximation in the extremely low-current subthreshold regime that drain-source conductances of M_1 and M_2 are sufficiently small, the loop gain (LG) of the nFVFB can be calculated as

$$\mathrm{LG_N}(s)=\frac{g_{m1}g_{m2}Z_1Z_2}{1+g_{m2}Z_2\left(1+g_{\mathrm{mb1}}Z_1\right)}$$

$$\cong\frac{\dfrac{g_{m1}}{g_{\mathrm{mb1}}}}{1+s\left(\dfrac{C_1}{g_{\mathrm{mb1}}}\right)+s^2\left(\dfrac{C_1C_2}{g_{\mathrm{mb1}}g_{m2}}\right)}\quad . \tag{8}$$

Setting g_{mb1} in (8) to zero, LG of the pFVFB circuit ($\mathrm{LG_P}$) can be obtained. In our case, $g_{m2} > g_{\mathrm{mb1}}$ and $g_{m1} = g_{m2}$. The phase margin (ϕ_M) of pFVFB is worse than nFVFB and it can be approximated as $\phi_M \cong 90^\circ - \arctan\left(C_2/C_1\right)$.

Figure 7(b) shows the magnitude and phase responses of $\mathrm{LG_N}$ and $\mathrm{LG_P}$ for $g_{m1} = g_{m2} = 2g_{\mathrm{mb1}} = 8$ nS (approximated that $n_n = n_p = 1.5$), $C_1 = 0.25C_2 = 6$ pF. These values of capacitors result in $Q_P = 2$ and $Q_N \approx 2.45$. The quality factor of each biquad used in our design is lower than those values guaranteeing the filter's stability.

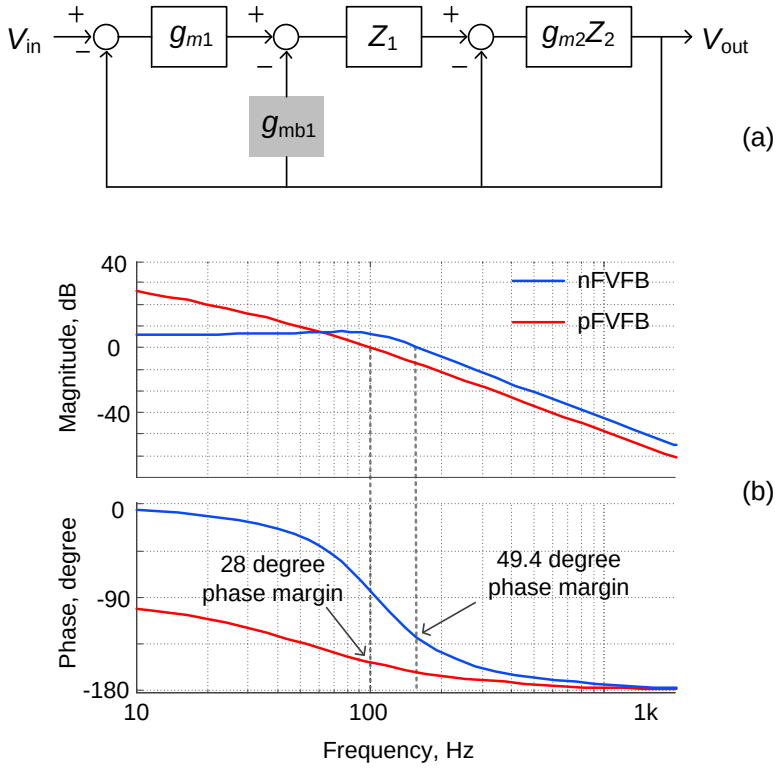

Fig. 7. Feedback block diagram of the FVFBs (a) and frequency responses of their loop gains (b).

2.4 Pseudo-Differential FVFBs

To maximize the linear input range thereby cancelling out even-order harmonic components, FVFBs are coupled to be in a pseudo differential form as shown in Fig. 8. Compared with the single-ended versions in Fig. 2 for the same value of f_C, C_1, power, and number of transistors will be double, but C_2 will be reduced for 50%. Also, approximately 50% of the noise contributed by the current source can be correlated and cancelled out. Thus the output noise in this differential version will be less than 200% compared with the single-ended versions defined by (5) and (6).

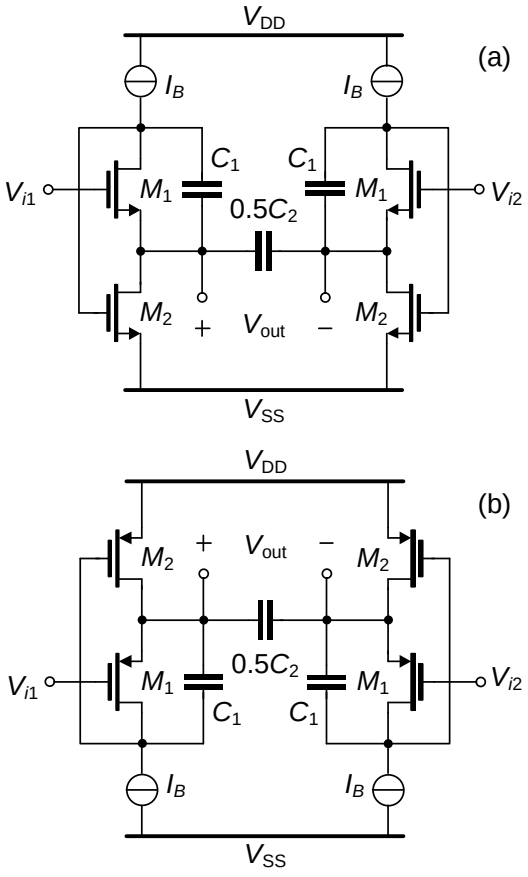

Fig. 8. Pseudo-differential FVFBs: (a) nMOS and (b) pMOS versions.

2.5 Common-Mode and Power Supply Rejections

The pseudo differential circuits in Fig. 8 do not attain any common-mode rejection as they are based on a unity-gain voltage buffer that the output voltage (source terminal of M_1) follows the

input voltage (gate terminal of M_1). To understand this mechanism, let's considered the common-mode components of input and output voltages of the pMOS version in Fig. 8(b): V_{icm}= 0.5(V_{i1}+V_{i2}) and V_{ocm}= 0.5(V_{out+}+V_{out-}), respectively. It can be seen that V_{o+} = V_{i1}+V_{SG1} and V_{o-} = V_{i2}+V_{SG1} (supposed that M_1 and I_B pairs are matched). In this case, we will have V_{icm}= V_{ocm}. There is indeed none common-mode rejection. The similar mechanism as explained above also occurs in nMOS version.

On the other hand, the nFVFBs can tolerate V_{DD} variation depending on the value of output resistance of the current source used. It can usually be made negligible compared with the more severe case happening on another supply rail. As the source terminal of M_2 is connected to V_{SS}, the variation of V_{SS} can be leaked through drain-source resistance of M_2 (r_{ds2}) and appears as a voltage variation at the output node. This voltage can be estimated by the voltage division between r_{ds2} and Z_{outN}(s). Hence, according to (2), we can expect the worst power supply rejection ratio (PSRR) at frequencies near f_C. For pFVFB circuit in Fig. 8(b), the circuit behaves vice versa.

3. FVF Electrocardiogram Lowpass Filter

We realize an ECG LPF by cascading the proposed FVFBs as shown in Fig. 9. The values of capacitors are set in order to achieve a 4th-order Butterworth transfer function. To minimize the input-referred noise (IRN) of the filter, the first stage chosen to be the pMOS version as it has higher passband gain than the nMOS one. This is because pFVFB's passband gain is not attenuated by the bulk effect (see Table I). All biasing current sources are made by unity-gain current mirror circuits (M_{Bp1}-M_{Bp3} and M_{Bn1}-M_{Bn3}). Focusing at each FVFB, the two current sources (M_{Bp2}-M_{Bp3} for nFVFB or M_{Bn2}-M_{Bn3} for pFVFB) are coupled to the same diode-connected transistor (M_{Bp1} for nFVFB or M_{Bn1} for pFVFB). As a consequence, M_{Bn1} and M_{Bp1} contribute common-mode noise voltages at the output nodes and they will be cancelled out almost completely. The filter parameters are shown in Table III. The values of g_m and f_C are obtained using approximations of $n_n = n_p = 1.5$ and $I_{D1} = I_{D2} = I_B$. The quality factor of the first stage is made lower than the second stage to keep voltage signal swing within internal nodes low to obtain minimal distortion [18].

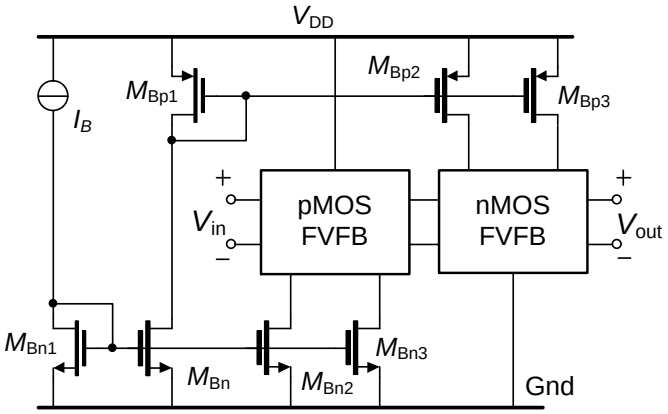

Fig. 9. 4th-order ECG lowpass filter based on FVFBs with bias circuits.

TABLE III. Approximated Filter Design Parameters

Parameter	nFVFB	pFVFB
I_B	0.3 nA	0.3 nA
$^*g_m$, g_{mb1}	8 nA/V, 4 nA/V	8 nA/V, 0
C_1, C_2	13.63 pF, 16.58 pF	23.5 pF, 6.876 pF
f_C	100 Hz	100 Hz
K_0, Q	0.67, 1.306	1, 0.541
W_1, W_2	36 μm, 36 μm	12 μm, 4 μm
L_1, L_2	6 μm, 6 μm	6 μm, 16 μm

*Assuming that $n_p \approx n_n \approx 1.5$, then we have $g_{m1} \approx g_{m2} \approx g_m$

TABLE IV. Effect of PVT Variations on The Cutoff Frequency

T	0° C			30° C			60° C		
V_{DD} [V]	f_C [Hz]			f_C [Hz]			f_C [Hz]		
	S	*T*	*F*	*S*	*T*	*F*	*S*	*T*	*F*
0.55	88	95	94	81	98	69	88	91	52
0.60	73	103	66	88	99	56	90	92	57
0.65	27	108	60	96	100	54	90	91	79

**S, T, F* stand for slow, typical, and fast models, respectively.

4. Simulation and Measurements Results

The ECG LPF in Fig. 9 has been simulated concerning the effects of mismatch and process-voltage-temperature (PVT) variations. From a 100-run Monte-Carlo simulation and setting I_B = 0.3 nA. The frequency response variation is shown in Fig. 10(a). The mean value of the bandwidth is 99.16 Hz with 4.3 Hz standard deviation (std.) as shown in Fig. 10(b). The mean of THD as shown in Fig. 10(c), when the 25 mV_P and 60 Hz sinusoidal input voltage was applied to the proposed filter, is −53.8 dB with 2.37 dB std.

The PVT that affects the filter's bandwidth is revealed in Table IV. With V_{DD} varied from 0.55 to 0.65 V and temperature changed from 0 to 60 C, the f_C varies within ±20% of the targeted value (100 Hz) for both slow and typical models. Except at 0.65 V and $0^{\circ}\mathrm{C}$, the filter fails to operate for the case of slow model. Additionally, using fast model, the filter cannot perform properly for all conditions.

The ECG LPF chip has also been fabricated in 0.35 μm CMOS technology. Capacitors C_1 - C_4 are made by poly capacitors. On-chip source follower circuits are inserted to drive parasitic capacitances of the output pads and instrument probes. The filter occupies a silicon area of 0.168 mm^2 (including the buffer circuits) which is dominated by capacitors as shown in Fig. 11. The measurement has been done using a SR780 dynamic signal analyzer. Bias currents and bias voltages were supplied to the chip by a precision source measurement unit (Keysight B2912A). The chip was put inside a test fixture (Agilent 16442A), to obtain reliably repeatable results.

The magnitude responses of the filter for different values of I_B adjusted to cover all recommended cutoff frequencies for ECG are shown in Fig. 12. The solid lines represent the measured results and the dotted lines are obtained from simulations. The simulation targets the filter's bandwidth of 100, 200 and 300 Hz for I_B of 0.3, 0.6 and 0.9 nA, respectively while the measurements show that the bandwidth of 101, 197, and 272 Hz are obtained for I_B of 0.3, 0.6 and 0.9 nA, respectively. The maximum error of almost 10% is found for the highest bias current. In terms of passband gain, we can see that measured results deviate maximally from

the simulated results at the cutoff frequencies approximately 1.8 dB for all three cases. Note that the ~ 70 dB nearly constant attenuation of the measured magnitude response is noticeable beyond 600 Hz whilst the simulation result keeps falling. This is due to the parasitic mutual capacitance of ~0.5 pF that creates an extra feed-forward path allowing the input signal to travel to the output terminal directly [19]. Fortunately, this effect is not harmful significantly to our filter's functionality.

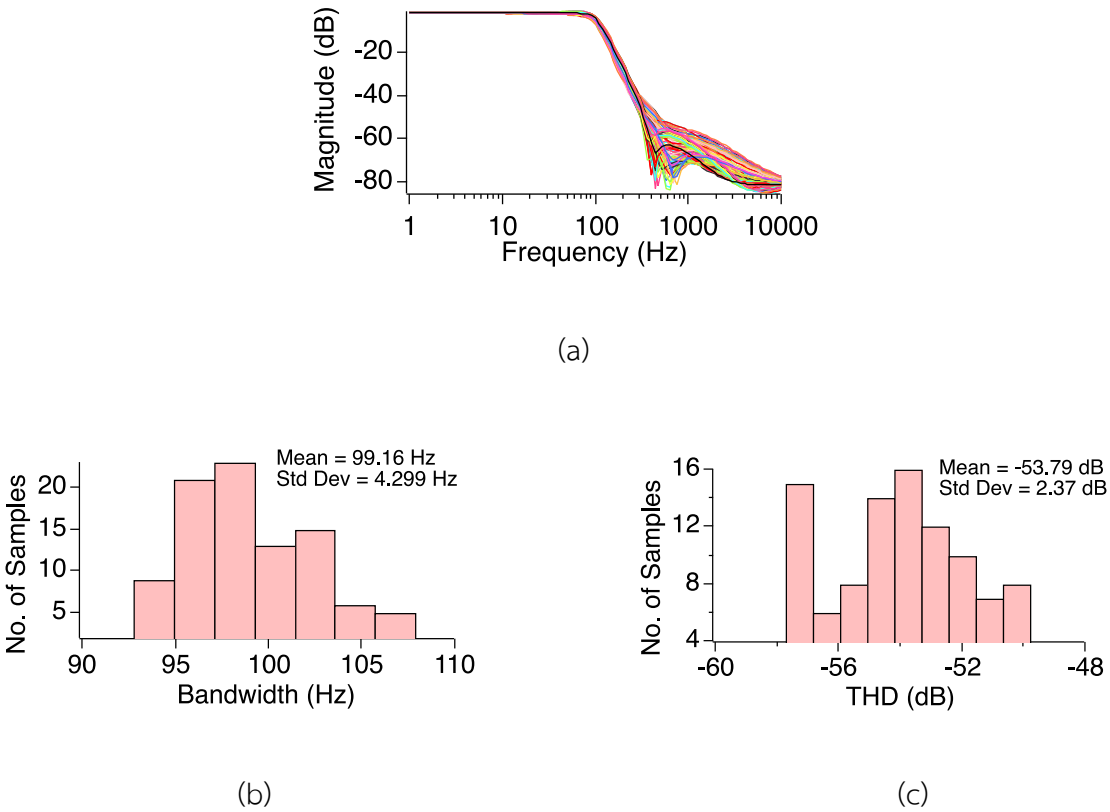

Fig. 10. 100 runs Monte-Carlo simulation on: (a) magnitude response, (b) bandwidth and (c) THD.

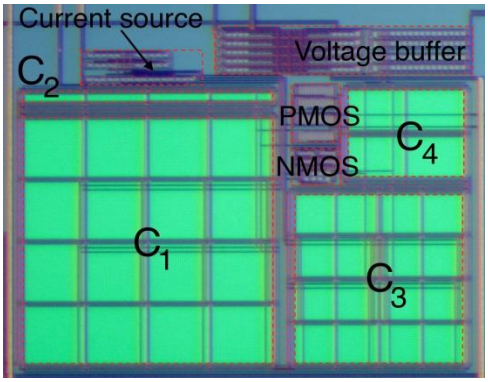

Fig. 11. ECG filter photograph with 362 μm × 466 μm die size including the on-chip buffer

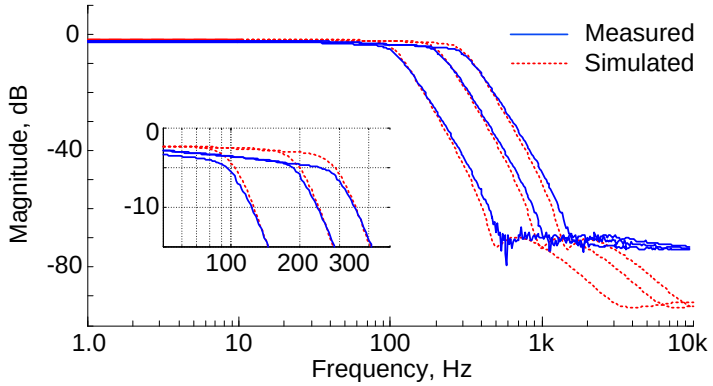

Fig. 12. Magnitude responses of the proposed ECG filter.

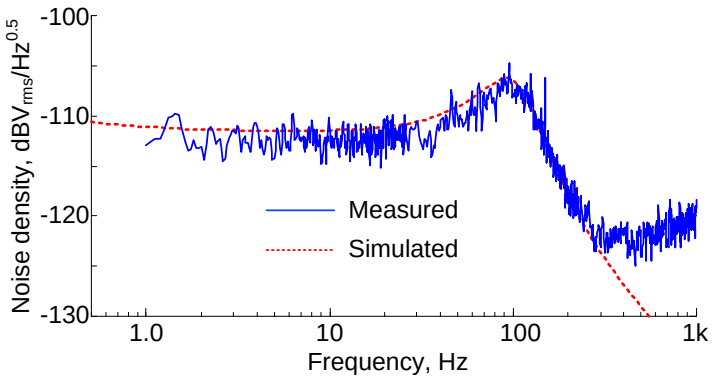

Fig. 13. Noise voltage spectral density of the proposed ECG filter.

Figure 13 shows output noise voltage spectral density of the ECG filter for the case of I_B = 0.3 nA targeting f_C (f_{Ctar}) of 100 Hz. From both simulation (dotted line) and measurement (solid line), we can see that the flicker noise's corner frequency appears below 1 Hz as expected. Integrated over the range of 1 to 200 Hz, the output noise of 46.6 μV_{rms} and 43.9 μV_{rms} are obtained from measurement and simulation, respectively. This gives rise to the measured IRN of 64 μV_{rms}.

The linearity of the filter was estimated by measuring harmonic distortion for the case of I_B = 0.3 nA (f_{Ctar} = 100 Hz) as well. Fig. 14(a) shows the harmonic distortion obtained from applying a sinusoid differential input voltage (V_{id}) with 25 mV amplitude and varying the input signal frequency (f_{in}) from 20 to 120 Hz. The third harmonic distortion (HD_3) is worse than the second harmonic distortion (HD_2) for more than 15 dB for all input frequencies except at 40 Hz. At this frequency, HD_2 jumps as high as −70.5 dB whilst HD_3 appears at −62.5 dB. Nevertheless, the trend of total harmonic distortion (THD) follows closely with HD_3. As expected, the values of THD appear low for low values of f_{in} and rises gradually when f_{in} approaches 100 Hz. Eventually the THD drops again for f_{in} higher than f_C (120 Hz). The harmonic distortions were also tested versus amplitude of the input signal for f_{in} = 100 Hz (this frequency is where Fig. 14(a) shows the worst THD). The results are obtained in Fig. 14(b). It shows the THD of −40.2 dB is associated with V_{id} = 65 mV_p. Concerning the amplitude at this point and the IRN obtained from Fig. 13, the filter's DR of 57.1 dB is achieved.

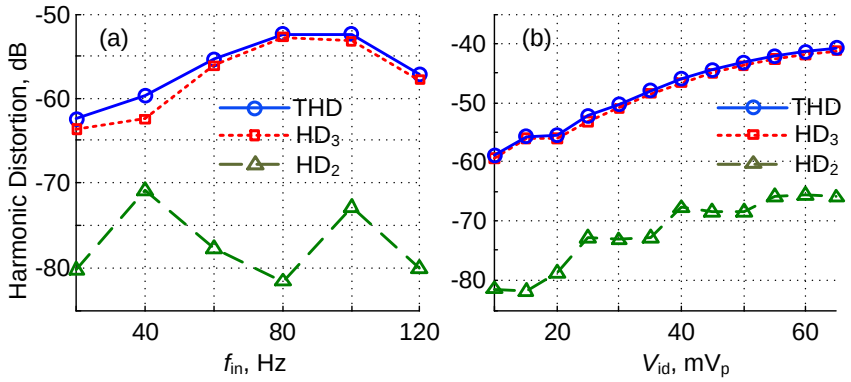

Fig. 14. Harmonic distortions of the ECG filter for I_B = 0.3 nA targeting f_C of 100 Hz. Measured versus: (a) f_{in} and (b) amplitude for f_{in} = 100 Hz.

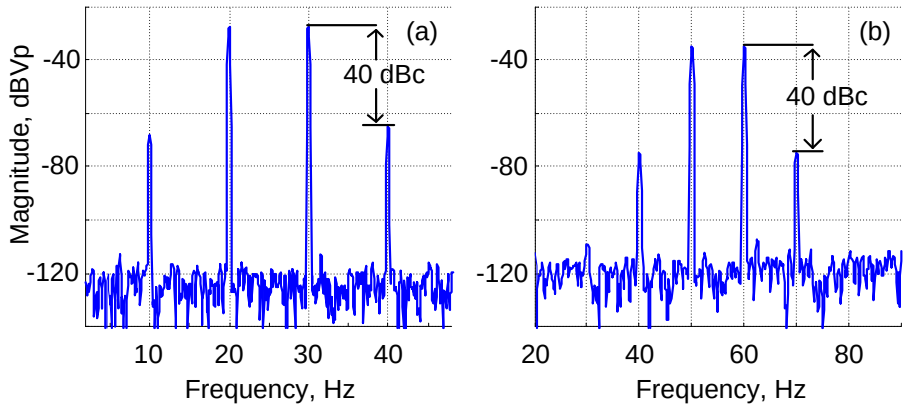

Fig. 15. Intermodulation distortions for the case of I_B = 0.3 nA with two situations: (a) f_{in1} = 20 Hz and f_{in2} = 30 Hz, and (b) f_{in1} = 50 Hz and f_{in2} = 60 Hz.

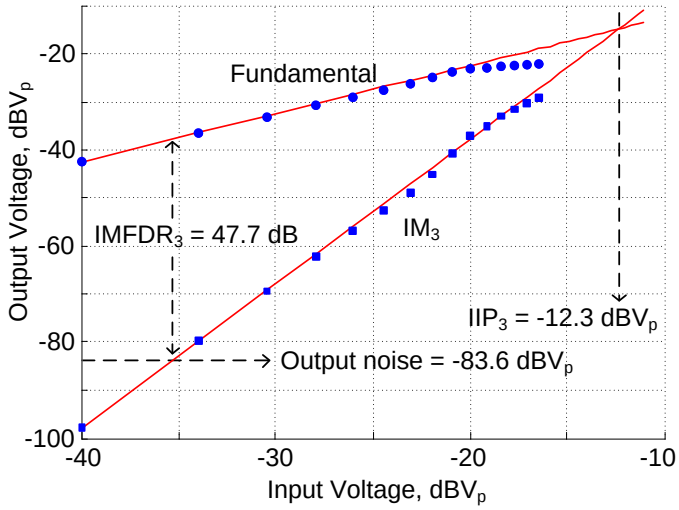

Fig. 16. Fundamental and third-order intermodulation components for I_B = 0.3 nA, f_{in1} = 50 Hz and f_{in2}= 60 Hz.

Two-tone test was also performed to assess the intermodulation behavior of the filter for I_B = 0.3 nA. We applied input signals with two different frequencies (f_{in1} and f_{in2}) seeking identical input amplitudes that lead to the third order intermodulation distortion (IMD_3) of −40 dBc for two cases: f_{in1} and f_{in2} of 20 Hz and 30 Hz, and 50 Hz and 60 Hz, respectively. The measurement reveals that the input amplitude of 56 mV and 24 mV are obtained for the former and latter case, respectively. These results are shown in Fig. 15. We also investigated the

latter case further to obtain the third-order input-referred intercept point (IIP_3) by increasing the amplitudes. The fundamental and third-order intermodulation components are plotted in Fig. 16. Here the IIP_3 equals −12.3 dBV_p. With the output noise level of −83 dBV_p, we obtain 47.7 dB for intermodulation free dynamic range (IMFDR) of the proposed filter.

Relevant filter parameters are collected and summarized for different values of I_B in Table V. Table VI compares our filter parameters (for the case that I_B = 0.3 nA was set) to other existing designs. To make a relevant comparison we divide the literature into two categories, namely nanopower (including [4], [7], [20], [21]) and high-frequency (including [5], [6], [15], [16], [22], [23]) LPFs. This comparison with high-frequency filters is not relevant directly to biomedical fields but provided optionally for a broad perspective. In terms of power consumption, it can be seen that our design operates from the least supply voltage and consumes the lowest power. When DR is concern, the proposed filter is comparable to other LPFs in the nanopower category but less than those in the group of high-frequency LPFs.

In terms of figure of merit (FoM) we adopt two different definitions suitable for different categories to make the most reasonable comparison. FoM_1 defined by (9) is widely used for nanopower filter design comparison as the filters are mostly designed for biomedical applications so they can rarely face intermodulation between two adjacent frequencies [4]. FoM_2 is defined by (10) recently used in [6] and [16] suitable to comparison of filter design for high-frequency communication systems. For both FoM_1 and FoM_2, parameters N and f_C represent the number of poles and bandwidth of the filter, respectively. DR_1 is where HD_3 of −60 dB is produced. Frequency f_{IM3L} is obtained from the two-tone test defined by $2f_{in1}-f_{in2}$ [6].

$$\mathrm{FoM}_1 = \frac{P}{N \times f_C \times \mathrm{DR}} \quad . \tag{9}$$

$$\mathrm{FoM}_2 = 10 \times \log\left(\frac{N \times f_{\mathrm{IM3L}} \times \mathrm{IMFDR}_3}{P} \right). \tag{10}$$

It can be seen from the bottom row of Table VI (high-frequency category) that FoM_2 of the proposed filter falls in the middle of the group (160 dBJ^{-1}). Note that the design of [15] and

[16] that provide better FoM_2 than the proposed filter are also based on a FVF circuit but biased in strong inversion. Hence the LPFs of [15] and [16] can handle larger input signal swing than this work and it should be the reason to obtain better FoM_2.

Fig. 17 shows the graphs of FoM_1 plotted against the V_{DD} compared with other designs in the nanopower category. The proposed filter attains the lowest FoM_1 of 46.5 aJ. Compared with the latest design of [4], the number obtained is approximately two times better. This is mainly due to the power consumption of the proposed design is a lot lower. However, as we have analyzed in Sec. IIA, the LPF of [4] should be operational from V_{DD} lower than 3 V and the power consumption can be lower. Moreover, when the silicon area is concerned, the proposed LPF is slightly more than two times larger than the LPF of [4]. If we take this issue into account for FoM_1, the design of [4] and this work should be very comparable.

Figure 18 demonstrates the capability of the proposed filter for out-of-band signal filtering. The ECG with 65 mV peak value superimposed with artificial noise (a 20 mV, 300 Hz sinusoidal signal) generated by a waveform generator (Keysight 33522B) shown in Fig. 18(a) were applied. The LPF was configured for 100 Hz f_C by setting I_B = 300 pA. After filtering, the interference signal is suppressed while the integrity of ECG signal is maintained as shown in Fig. 18 (b). It is noticeable that the third peak of the input signal that was corrupted by the noise can be recovered at the output terminal of the LPF.

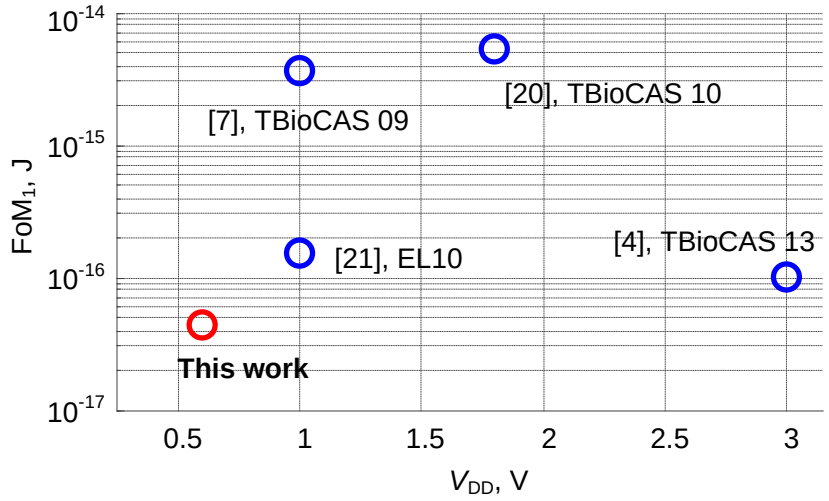

Fig. 17. FoM$_1$ versus V_{DD}.

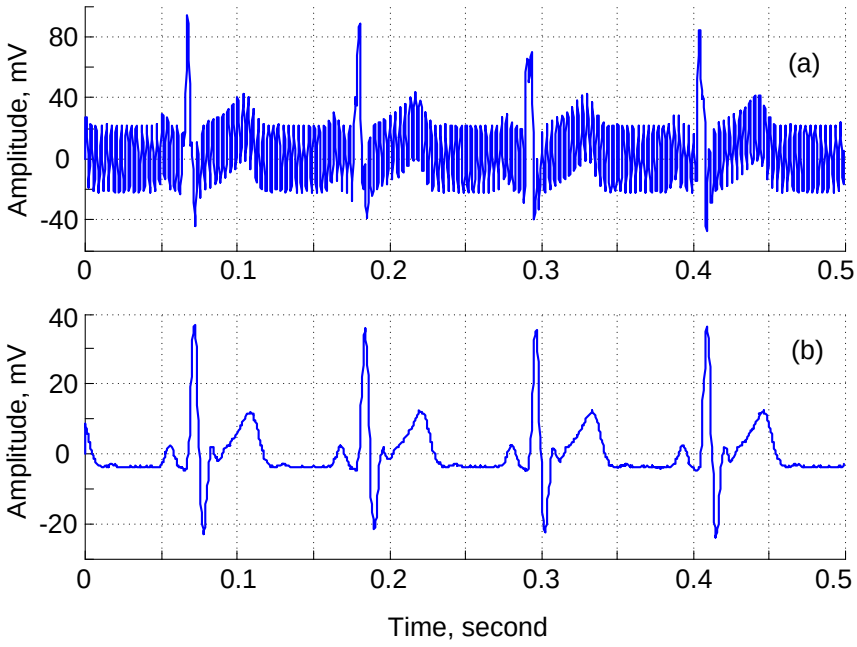

Fig. 18. ECG signal testing: (a) Noisy ECG and (b) Filtered ECG.

TABLE V

Measured Performance Summary for V_{DD} = 0.6 V

Bias current I_B [nA]	0.3	0.6	0.9
Power consumption [nW]*	0.9	1.8	2.7
f_{Ctar}; f_{Cmea} [Hz]	100; 101	200;197	300;272
dc gain [dB]	−2.77	−2.57	−2.53
Measured op. noise [μV_{rms}]**	46.6	46.4	46.8
Simulated op. noise [μV_{rms}]**	43.9	42	44.9
IRN [μV_{rms}]	64	62	63
THD@f_{Ctar} [dB] (V_{in} = 65 mV_p)	−40.5	−41	−42.5
V_{in}@ −50 dB HD3 [mV_p] (f_{in} = 0.3f_{Ctar}, f_{in} = 0.6f_{Ctar})	63, 40	65, 39	60, 38
IMD_{3A}@V_{in} = 56 mV_p [dBc] (f_1 = 0.2f_{Ctar}, f_2 = 0.3f_{Ctar})	−40.44	−40.29	−40.23
IMD_{3B}@V_{in} = 24 mV_p [dBc] (f_1 = 0.5f_{Ctar}, f_2 = 0.6f_{Ctar})	−40.02	−40.11	−40.22
DR@−50 dB HD_3 [dB] (f_{in}= 0.6f_{Ctar})	52.89	52.91	52.66
PSRR@f_{Ctar} [dB]	37.2	37.8	39.5
FoM_1 [aJ]	11.5	11.7	13.4

* 5 branches of I_B (4 for the filter core and 1 for the bias circuit)

** integrated from 1 Hz to 2f_{Ctar}

5. Conclusion

The implementation of a pseudo differential 4^{th}-order ECG filter based on cascading the FVFBs has been done by this project. The filter has been fabricated in 0.35 μm CMOS process. The measured results reveal the superiority of the proposed filter over the previously published nanopower LPFs in terms of circuit complexity, supply voltage, power consumption. With the DR obtained this proposed filter can be useful for acquisition of ECG and other types of bio-potential signals.

Appendix: Publication

C. Sawigun and S. Thanapitak, "A 0.9-nW, 101-Hz, and 46.3 uVrms-IRN Low-Pass Filter for ECG Acquisition Using FVF Biquads," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 26, no. 11, pp. 2290-2298, Nov. 2018.

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A 0.9-nW, 101-Hz, and 46.3-μV_{rms} IRN Low-Pass Filter for ECG Acquisition Using FVF Biquads

Chutham Sawigun, *Member, IEEE*, and Surachoke Thanapitak, *Member, IEEE*

***Abstract*— This paper presents a differential fourth-order low-pass filter suitable for electrocardiography (ECG) acquisition. It is formed by cascading two compact and power-efficient biquads operating in the subthreshold region. Each biquad combines two capacitors and a flipped voltage follower circuit. The filter attains a cutoff frequency adjustable to cover the entire range of ECG (150–250 Hz). The filter prototype has been fabricated in a 0.35-μm CMOS technology. It occupies an area of 362 μm × 466 μm and operates from a 0.6-V supply. Measurements confirm that the filter consumes 0.9-nW static power for a 101-Hz cutoff frequency and contributes the input-referred noise of 46.27 μV_{rms}. For a 60-Hz input frequency, the filter achieves a dynamic range of 47 dB where the third-harmonic distortion of −60 dB is produced. This leads to the figure of merit of 46.5 × 10^{-18} J. When the chip area is also concerned, the proposed filter performs comparably to the recent state-of-the-art nanowatt-class low-pass filter.**

***Index Terms*— Analog filter, biomedical filter, biopotential acquisition, CMOS, electrocardiography (ECG) detection, g_m–C, health monitoring, low voltage, nanopower, transistorized filter, voltage follower.**

I. Introduction

DESIGNING an analog filter in CMOS technology to be functional from a low-voltage supply and to consume extremely low power, MOSFETs are usually biased in the weak inversion region as they must conduct currents in the range of a few nanoamperes [1]. Filter's circuit structure also needs to be suitable for a supply voltage that is minimized [2]. The aforementioned requirements call for innovative design strategies that exploit a single MOSFET to its full potential. Recently, an MOSFET that operates fundamentally as a nonlinear transconductor has been placed into several g_m–C topologies in order to design compact and power-efficient analog filters. This design concept can be categorized as a "transistorized filter" [3], and it has been implemented successfully for cutoff frequencies from hundreds of hertz [4] up to megahertz ranges [3], [5], [6].

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Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

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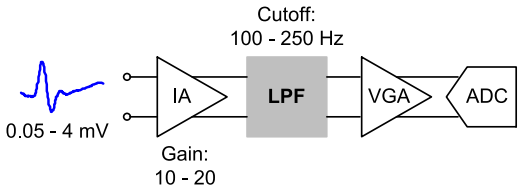

Fig. 1. ECG recording system.

Developed further from the concept of the source-follower filter (SFF) [5], the design of 100-Hz biopotential low-pass filters (LPFs) has been proposed in [4] by biasing the SFFs in the subthreshold region. Fabricated in a 0.35-μm CMOS technology, the LPFs consume only 15 nW from a supply voltage of 3 V and attain a dynamic range (DR) of 56 dB. Although the application of the LPFs to electrocardiography (ECG) filtering has been demonstrated, it is still possible to enhance the power consumption further by employing a new transistor-level architecture that requires a supply voltage less than that of [4] while maintaining suitable circuit performance for ECG recording applications.

Fig. 1 shows the ECG detection system. The ECG voltage that varies between 0.05 and 4 mV [7] is first enlarged by a low-noise instrumentation amplifier (IA) with a voltage gain in the range of 10–20 [8], [9]. After this IA stage, the LPF enhances the frequency selectivity of the system before amplifying further by a variable-gain amplifier. Finally, the signal will be converted by an analog-to-digital converter. Considering the amplitude variation of an ECG, the DR of all the circuit blocks must be more than 44 dB [7]. Focusing on the LPF, as the ECG spectrum locates between 100 and 250 Hz [7], [8], [10], [11], a wide tuning capability of the LPF is not needed. Besides, the LPF needs not to handle large-signal amplitudes (i.e., maximum 80 mV, for IA's gain of 20). Moreover, it was indicated in [12] that total harmonic distortion (THD) of 3.5% can maintain significant features of an ECG. As a consequence of the moderate signal swing and generously accepted non-linearity mentioned above, the LPF should be made more power efficient than the latest design.

Recently, the subthreshold pMOS flipped voltage follower (FVF) [13] was employed to incorporate with a couple of capacitors into a second-order LPF called 'pFVF biquad (pFVFB)' [14]. The pFVFB is then considered a potential candidate for the realization of a low-voltage and power-efficient second-order section, and it is thus chosen to be developed further here. We should also note here that the very

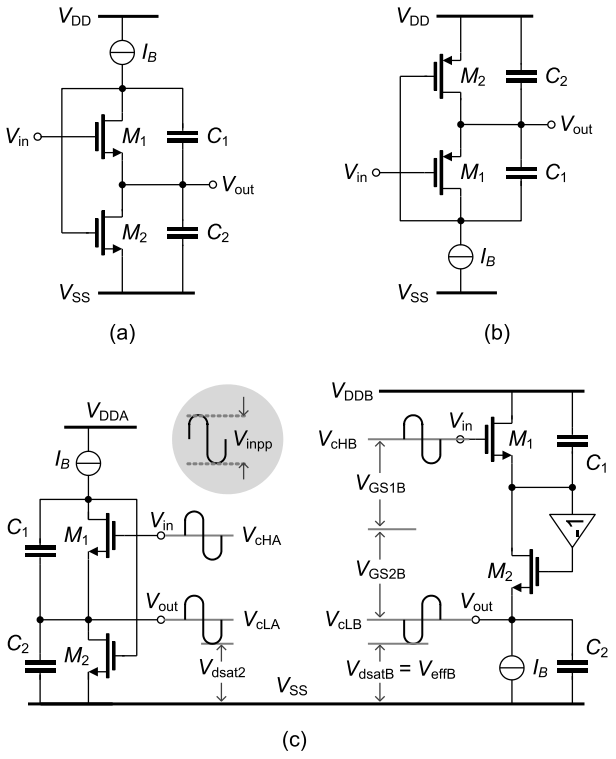

Fig. 2. FVFB circuits. (a) nFVFB. (b) pFVFB [12]. (c) Bias points' arrangement.

similar idea to [14] that employs strong inversion MOSFETs can also be founded in [15] and [16]. However, the filters of [15] and [16] are dedicated to different frequency ranges and different applications.

This paper presents a power-efficient fourth-order ECG LPF that fits well with the low-power ECG acquisition environment. The nMOS version of the FVFB (nFVFB) is introduced here as a complementary counterpart for the realization of a higher order LPF. The proposed LPF circuit has been designed and fabricated in a 0.35-μm CMOS technology. It operates properly from a 0.6-V supply and consumes only 0.9-nW quiescent power. The chip measurement results and the experiment demonstrating the potential use of the LPF in ECG recording are also reported.

In Section II, we will present descriptions of the FVFB circuits as well as their relevant performance analysis. Section III presents the proposed ECG filter using the FVFBs. The prototype chip measurements are presented in Section IV with comparisons with the state-of-the-art designs. Section V provides the conclusion.

II. Flipped Voltage Follower Biquadratic Cells

Since we focus on the power and area minimization of filters, this section thus describes the relevant aspects of the nanocurrent subthreshold FVFBs only. Strong inversion features of the FVF filter are beyond our scope.

A. Transistor-Level Topologies and Transfer Functions

Fig. 2(a) and (b) shows the transistor-level circuits of the nFVFB and pFVFB, respectively. Each of them comprises transistors M_1 and M_2 and a constant current source I_B. Capacitors C_1 and C_2 are connected across the drain and source terminals of M_1 and M_2, respectively. The difference is that C_1 is connected between signal nodes but one terminal of C_2 is connected to the ac ground node. The superior aspect of FVFBs is at the stacking current-reuse structure that M_1 and M_2 are sharing the same I_B.

Fig. 2(c) shows the bias setup to accommodate the signal swing for the nFVFB [Fig. 2(a)] in comparison with the nMOS version of the most recent subthreshod biquad [4]. The signal inversion was made by cross-coupling connection embedded in the differential circuit of [4]. Thus, there is no common-mode difference between the input and output terminals of the inverting block. Note that only the nMOS versions of the biquads are illustrated here for the sake of conciseness. The pMOS versions can also be arranged in a similar manner. With these arrangements, we can see that $V_{DDA} = V_{inpp} + V_{GS1} + V_{dsat2}$ and $V_{DDB} = V_{inpp} + V_{GS1} + V_{GS2} + V_{eff\,B}$, where $V_{eff\,B}$ and V_{dsat2} are the minimum voltage that the current source requires and the saturation voltage of M_2, respectively.

The current source (I_B) is made from an ordinary current mirror circuit operating in weak inversion saturation [1]; we have $V_{eff\,B} = V_{dsat2} \approx 4U_T \approx 0.1$ V. It can be seen that V_{DDA} is lower than V_{DDB} for one V_{GS1}. For the 0.35-μm n-well process employed here, threshold voltages are $V_{tn} \approx 0.46$ V and $V_{tp} \approx -0.68$ V, for n-channel and p-channel devices, respectively. In the subthreshold operation where nMOS and pMOS devices conduct currents less than 1 nA, V_{GS1} and V_{SG2} can be managed (by proper sizing the transistor) to be as low as $\approx$0.45 V. Therefore, without process and temperature variations, the FVFBs can be fit into V_{DD} of 0.6 V to accommodate V_{inpp} of 25 mV. (This amplitude will approximately be doubled for differential operation presented in Section II-D.)

Considering the small-signal operation of MOSFETs by neglecting the channel-length modulation (CLM), the widely used models are shown in Fig. 3(a) and (b) for nMOS and pMOS, respectively. Note that CLM can be neglected here since all transistors used in this design conduct very low drain currents and have channel lengths more than 10$\times$ greater than the minimum allowable size (see Table III). Since we deal with g_m–C filters, a convenient equivalent model shown in Fig. 3(c) is proposed here to represent the small-signal operations of both M_1 and M_2.

Applying the model in Fig. 3(c) to the circuits in Fig. 2, we achieve two second-order g_m–C filters represented by the macromodel shown in Fig. 4. Assuming that our filter is realized in a standard n-well CMOS process, the body terminal of nMOS M_1 in Fig. 2(a) needs to be connected to its substrate potential (V_{SS}). As a result, the body effect introduces transconductor g_{mb1} to the nFVFB as shown in the shaded area of Fig. 4. This will attenuate the passband gain of the biquad. For the pFVFB, both M_1 and M_2 can be made free from the body effect by connecting their body and source terminals together, and g_{mb1} in Fig. 4 will be omitted.

A straightforward analysis of the circuit in Fig. 4 leads to the transfer function of nFVFB as shown in (1). The transfer function of pFVFB can also be obtained from the following

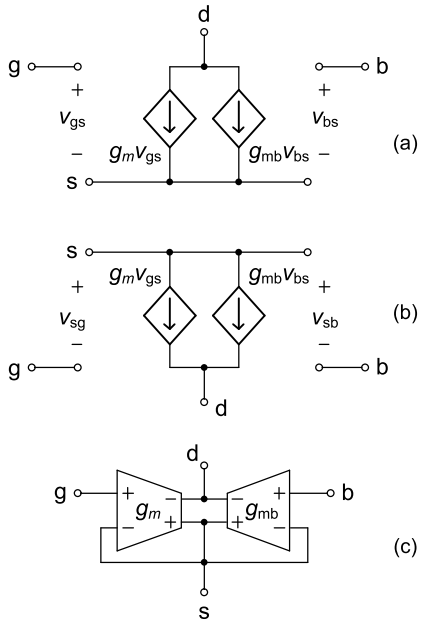

Fig. 3. Small-signal equivalent circuits. (a) nMOS. (b) pMOS. (c) Unified model available for both nMOS and pMOS.

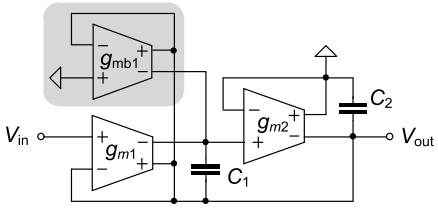

Fig. 4. g_m–C equivalent FVFB.

equation by setting g_{mb1} to 0:

$$H_n(s) = \frac{V_{\text{out}}(s)}{V_{\text{in}}(s)} = \frac{\frac{g_{m1}g_{m2}}{C_1C_2}}{s^2 + s\left(\frac{g_{m2}}{C_2}\right) + \frac{(g_{m1}+g_{mb1})g_{m2}}{C_1C_2}}. \quad (1)$$

Due to the current-reuse structure of FVFBs that all transistors conduct the same current I_B, we obtain small-signal transconductances $g_{m1} \cong g_{m2} \cong g_m = I_B/n_i V_T$, where V_T is the thermal voltage and n_i is the slope factor associated with each transistor [1]. Thus, passband gain K_0, natural frequency ω_n, and quality factor Q of nFVFB and pFVFB can be extracted as shown in Table I. It can be seen that each filter's cutoff frequency can be adjusted linearly by varying the bias current. The quality factors of the filters can be set via the ratio of C_1 and C_2.

B. Noise

Operated as a filter, the output impedances of the FVFBs (Z_{out}) are frequency-dependent and can be estimated, albeit neglecting CLM from the model in Fig. 3. It can be found for nFVFB that

$$z_{\text{out}N}(s) = \frac{\frac{s}{C_2}}{s^2 + s\left(\frac{g_{m2}}{C_2}\right) + \frac{(g_{m1}+g_{mb1})g_{m2}}{C_1C_2}} \quad (2)$$

and we can set g_{mb1} in (2) to 0 to obtain the output impedance of pFVFB [$Z_{\text{out}P}(s)$].

TABLE I
BIQUAD PARAMETERS

Parameter	nFVFB	pFVFB
K_0	$\frac{1}{1+(g_{\text{mb1}}/g_m)} = \frac{1}{n_n}$	1
ω_n	$\frac{g_m}{\sqrt{KC_1C_2}} = \frac{I_B}{V_T\sqrt{n_nC_1C_2}}$	$\frac{g_m}{\sqrt{C_1C_2}} = \frac{I_B}{n_pV_T\sqrt{C_1C_2}}$
Quality factor	$Q_N = \sqrt{\frac{C_2}{KC_1}} = \sqrt{\frac{n_nC_2}{C_1}}$	$Q_P = \sqrt{\frac{C_2}{C_1}}$

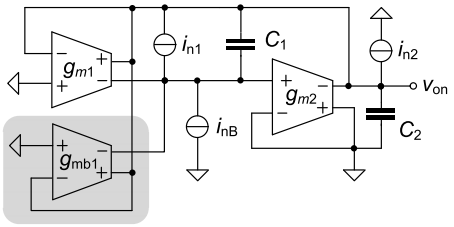

Fig. 5. FVFBs with noise sources.

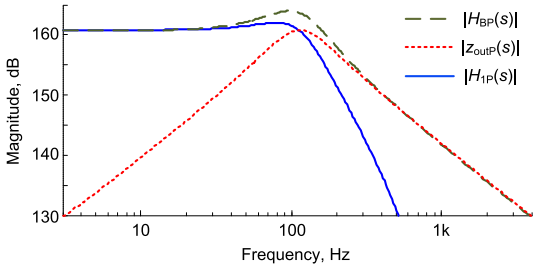

Fig. 6. Simulated noise transfer functions for pFVFB in Fig. 1(b) for $C_1 = C_2 = 12.24$ pF: $f_n \cong 100$ Hz and $Q = 1$.

Fig. 5 shows the FVFBs with equivalent noise sources. Considering the noise current from M_2 (i_{n2}), it experiences the low impedances of the output nodes and then turns into the output noise voltages ($v_{\text{ON}2}$) by the impedances or noise transfer functions defined by (2).

For nFVFB, the noise currents (i_{nB}) from current sources I_B can be converted into the output noise voltage ($v_{\text{ON}B}$) by

$$H_{\text{BN}}(s) = \frac{v_{\text{ON}N}(s)}{i_{nB}(s)} = \frac{\frac{s}{C_2} - \frac{g_{m2}}{C_1C_2}}{s^2 + s\left(\frac{g_{m2}}{C_2}\right) + \frac{(g_{m1}+g_{mb1})g_{m2}}{C_1C_2}}. \quad (3)$$

Setting g_{mb1} in (3) to 0, the noise transfer function from the current source for pFVFB [$H_{\text{BP}}(s)$] will be obtained.

The noise currents of M_1 (i_{n1}) can be split into two correlated noise sources located in parallel with i_{nB} and i_{n2}, respectively. The noise transfer functions for i_{n1} can thus be obtained by subtracting (2) from (3), resulting in

$$H_{1N}(s) = \frac{v_{\text{ON}N}(s)}{i_{n1}(s)} = \frac{\frac{g_{m2}}{C_1C_2}}{s^2 + s\left(\frac{g_{m2}}{C_2}\right) + \frac{(g_{m1}+g_{mb1})g_{m2}}{C_1C_2}} \quad (4)$$

for nFVFB. Similarly, for the case of pFVFB, g_{mb1} in (4) can be set to 0 to obtain the noise transfer function for i_{n1}.

Fig. 6 shows the simulated magnitude responses of the noise transfer functions of pFVFB in Fig. 2(b) for $I_B = 0.3$ nA

TABLE II
PERCENTAGE OF NOISE CONTRIBUTION IN FVFBS

Circuit element	nFVFB	pFVFB
M_1	16.07%	16.66%
M_2	18.57%	16.36%
I_B	65.37%	66.98%
*Simulated op noise	38.86 μV_{rms}	42.32 μV_{rms}
Calculated op noise	41.8 μV_{rms}	47.47 μV_{rms}

* Integrated from 1 Hz-10f_n

(made by an nMOS current mirror circuit), $V_{DD} = 0.6$ V, and $C_1 = C_2 = 12.24$ pF. It can be seen that the area under the green dashed line is the largest compared with the other lines. This reveals that the average output noise power contributed by I_B is greater than those by M_1 and M_2. In the case that I_B is made by a simple unity-gain current mirror that contains two identical transistors (M_B), when the weak inversion short noise is concerned, the noise current spectral densities of the transistors are defined by $S_1 = S_2 = 0.5S_B = 2qI_D$, where q and I_D stand for the electronic charge and drain current of the transistors [17], respectively ($I_D = I_B$ for all transistors in this case). Shaped by (2), (3), and (4), the average output noise power of nFVFB can be found as

$$\overline{v_{\mathrm{ON},N}^2} \cong \underbrace{\frac{kT}{2C_1}}_{M_1} + \underbrace{\frac{n_n kT}{2C_2}}_{M_2} + \underbrace{\left(\frac{kT}{C_1} + \frac{n_n kT}{C_2} + \frac{2kT}{\sqrt{C_1C_2}}F_N\right)}_{\text{current source transistors}}$$
$$\cong kT\left(\frac{1.5}{C_1} + \frac{1.5n_n}{C_2} + \frac{2F_N}{\sqrt{C_1C_2}}\right). \quad (5)$$

Also, the average output noise power of pFVFB is

$$\overline{v_{\mathrm{ON},P}^2} \cong n_p kT\left(\frac{1.5}{C_1} + \frac{1.5}{C_2} + \frac{2F_P}{\sqrt{C_1C_2}}\right) \quad (6)$$

where the multiplication factors F_N and F_P are defined by

$$F_P = \frac{F_N}{\sqrt{n_n}} = \frac{1}{\sqrt{4Q^2-1}}\left(1 - \frac{2}{\pi}\arctan\left(\frac{1-2Q^2}{\sqrt{4Q^2-1}}\right)\right). \quad (7)$$

For the same value of quality factor, i.e., $Q_N = Q_P$, the multiplication factor F_N will equal F_P. Besides, (7) is valid in the range of $0.5 < Q_{N,P} \leq \infty$. We verify our noise analysis by simulating the circuits in Fig. 2 and summarizing the noise contribution in each circuit compared with (5) and (6) using Boltzmann's constant $k = 1.38 \times 10^{-23}$ J $\cdot$ K^{-1}, simplified condition of $n_n \cong n_p \cong 1.5$, and $V_T = 26$ mV. The results are obtained in Table II, showing that the calculated values differ from the simulated values by approximately 8% and 11% for nFVFB and pFVFB, respectively.

As the filter contains only three MOSFETs and the filter is dedicated for low-frequency ECG signals, all transistors should be sufficiently large and I_B should be lower than 1 nA to suppress flicker noise's corner frequency below 1 Hz. This can be done successfully while the chip area is still dominated by capacitors (see Fig. 11).

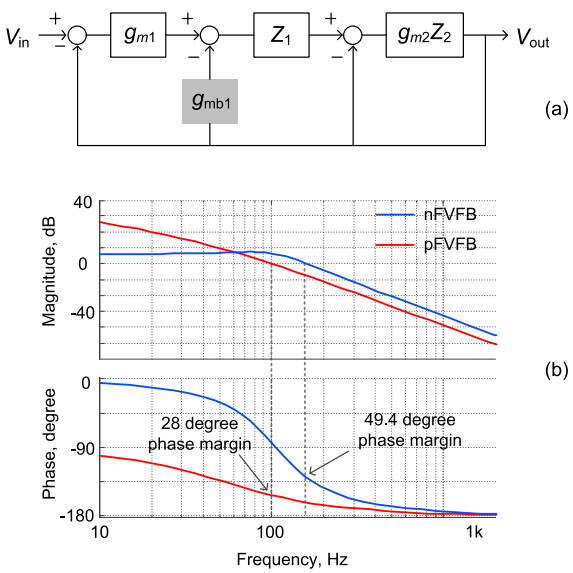

Fig. 7. (a) Feedback block diagram of the FVFBs. (b) Frequency responses of their LGs.

C. Feedback and Stability

Fig. 7(a) shows the feedback block diagram valid for both nFVFB and pFVFB circuits in Fig. 2. The gray block (g_{mb1}) is omitted for pFVFB as the bulk effect is absent and the full diagram is applied for nFVFB. Blocks Z_1 and Z_2 represent impedances across drain and source terminals of M_1 and M_2, respectively. For realistic approximation in the extremely low-current subthreshold regime that drain–source conductances of M_1 and M_2 are sufficiently small, the loop gain (LG) of the nFVFB can be calculated as

$$\mathrm{LG}_N(s) = \frac{g_{m1}g_{m2}Z_1Z_2}{1 + g_{m2}Z_2(1 + g_{mb1}Z_1)} \cong \frac{\frac{g_{m1}}{g_{mb1}}}{1 + s\left(\frac{C_1}{g_{mb1}}\right) + s^2\left(\frac{C_1C_2}{g_{mb1}g_{m2}}\right)}. \quad (8)$$

Setting g_{mb1} in (8) to 0, LG of the pFVFB circuit (LG_P) can be obtained. In our case, $g_{m2} > g_{mb1}$ and $g_{m1} = g_{m2}$. The phase margin (ϕ_M) of pFVFB is worse than nFVFB, and it can be approximated as $\phi_M \cong 90° - \arctan(C_2/C_1)$.

Fig. 7(b) shows the magnitude and phase responses of LG_N and LG_P for $g_{m1} = g_{m2} = 2g_{mb1} = 8$ nS (approximated that $n_n = n_p = 1.5$), $C_1 = 0.25$ pF, and $C_2 = 6$ pF. These values of capacitors result in $Q_P = 2$ and $Q_N \approx 2.45$. The quality factor of each biquad used in our design is lower than those values guaranteeing filter's stability.

D. Pseudodifferential FVFBs

To maximize the linear input range thereby canceling out even-order harmonic components, FVFBs are coupled to be in a pseudodifferential form as shown in Fig. 8. Compared with the single-ended versions in Fig. 2 for the same value of f_C, C_1, power, and number of transistors will be doubled, but C_2 will be reduced by 50%. Also, approximately 50% of the noise contributed by the current source can be correlated and canceled out. Thus, the output noise in this differential

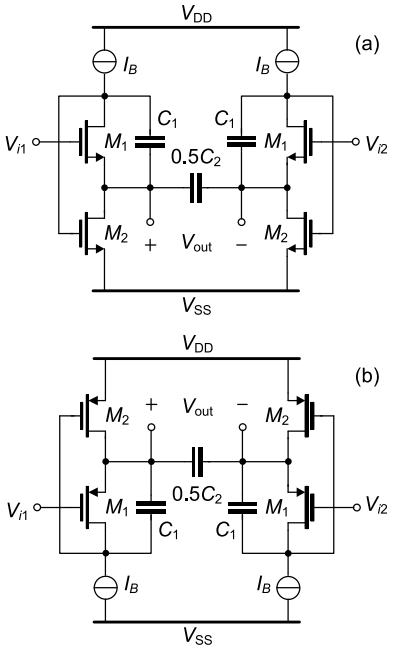

Fig. 8. Pseudodifferential FVFBs. (a) nMOS and (b) pMOS versions.

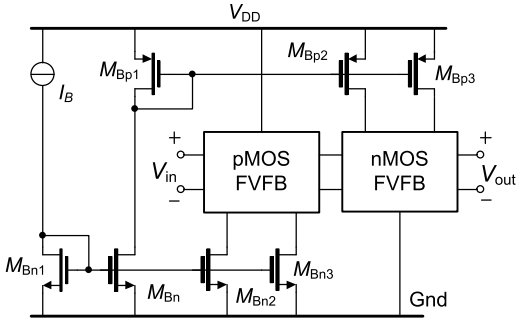

Fig. 9. Fourth-order ECG low-pass filter based on FVFBs with bias circuits.

TABLE III
APPROXIMATED FILTER DESIGN PARAMETERS

Parameter	nFVFB	pFVFB
I_B	0.3 nA	0.3 nA
$^*g_m$, g_{mb1}	8 nA/V, 4 nA/V	8 nA/V, 0
C_1, C_2	13.63 pF, 16.58 pF	23.5 pF, 6.876 pF
f_C	100 Hz	100 Hz
K_0, Q	0.67, 1.306	1, 0.541
W_1, W_2	36 μm, 36 μm	12 μm, 4 μm
L_1, L_2	6 μm, 6 μm	6 μm, 16 μm

*Assuming that $n_p \approx n_n \approx 1.5$, then we have $g_{m1} \approx g_{m2} \approx g_m$

version will be less than 200% compared with the single-ended versions defined by (5) and (6).

E. Common-Mode and Power Supply Rejections

The pseudodifferential circuits in Fig. 8 do not attain any common-mode rejection as they are based on a unity-gain voltage buffer that the output voltage (source terminal of M_1) follows the input voltage (gate terminal of M_1). To understand this mechanism, let us considered the common-mode components of the input and output voltages of the pMOS version in Fig. 8(b): $V_{\rm icm} = 0.5(V_{i1} + V_{i2})$ and $V_{\rm ocm} = 0.5(V_{\rm out+} + V_{\rm out-})$, respectively. It can be seen that $V_{o+} = V_{i1} + V_{\rm SG1}$ and $V_{o-} = V_{i2} + V_{\rm SG1}$ (supposed that M_1 and I_B pairs are matched). In this case, we will have $V_{\rm icm} = V_{\rm ocm}$. There is indeed none common-mode rejection. The similar mechanism as explained above also occurs in the nMOS version.

On the other hand, the nFVFBs can tolerate $V_{\rm DD}$ variation depending on the value of output resistance of the current source used. It can usually be made negligible compared with the more severe case happening on another supply rail. As the source terminal of M_2 is connected to $V_{\rm SS}$, the variation of $V_{\rm SS}$ can be leaked through drain–source resistance of M_2 ($r_{\rm ds2}$) and appears as a voltage variation at the output node. This voltage can be estimated by the voltage division between $r_{\rm ds2}$ and $Z_{{\rm out}N}(s)$. Hence, according to (2), we can expect the worst power supply rejection ratio at frequencies near f_C. For the pFVFB circuit in Fig. 8(b), the circuit behaves vice versa.

III. PROPOSED FVF ECG LOW-PASS FILTER

We realize an ECG LPF by cascading the proposed FVFBs as shown in Fig. 9. The values of capacitors are set in order to achieve a fourth-order Butterworth transfer function. To minimize the input-referred noise (IRN) of the filter, the first stage is chosen to be the pMOS version as it has higher passband gain than the nMOS one. This is because pFVFB's passband gain is not attenuated by the bulk effect (see Table I). All biasing current sources are made by unity-gain current mirror circuits ($M_{\rm Bp1}$–$M_{\rm Bp3}$ and $M_{\rm Bn1}$–$M_{\rm Bn3}$). Focusing at each FVFB, the two current sources ($M_{\rm Bp2}$ and $M_{\rm Bp3}$ for nFVFB or $M_{\rm Bn2}$ and $M_{\rm Bn3}$ for pFVFB) are coupled to the same diode-connected transistor ($M_{\rm Bp1}$ for nFVFB or $M_{\rm Bn1}$ for pFVFB). As a consequence, $M_{\rm Bn1}$ and $M_{\rm Bp1}$ contribute common-mode noise voltages at the output nodes, and they will be canceled out almost completely. The filter parameters are shown in Table III. The values of g_m and f_C are obtained using approximations of $n_n = n_p = 1.5$ and $I_{D1} = I_{D2} = I_B$. The quality factor of the first stage is made lower than the second stage to keep voltage signal swing within internal nodes low to obtain minimal distortion [18].

IV. SIMULATION AND MEASUREMENT RESULTS

The ECG LPF in Fig. 9 has been simulated concerning the effects of mismatch and process–voltage–temperature (PVT) variations. From a 100-run Monte Carlo simulation and setting $I_B = 0.3$ nA, the frequency response variation is shown in Fig. 10(a). The mean value of the bandwidth is 99.16 Hz with 4.3-Hz standard deviation (std.) as shown in Fig. 10(b). The mean of THD as shown in Fig. 10(c), when the 25 mV_P and 60-Hz sinusoidal input voltage was applied to the proposed filter, is −53.8 dB with 2.37-dB std.

The PVT that affects filter's bandwidth is revealed in Table IV. With $V_{\rm DD}$ varied from 0.55 to 0.65 V and temperature changed from 0 °C to 60 °C, the f_C varies within ±20% of the targeted value (100 Hz) for both the

TABLE IV
EFFECT OF PVT VARIATIONS ON THE CUTOFF FREQUENCY

T	0°C			30°C			60°C		
V_{DD} [V]	f_C [Hz]			f_C [Hz]			f_C [Hz]		
	S	*T*	*F*	*S*	*T*	*F*	*S*	*T*	*F*
0.55	88	95	94	81	98	69	88	91	52
0.60	73	103	66	88	99	56	90	92	57
0.65	27	108	60	96	100	54	90	91	79

* *S, T, F* stand for slow, typical, and fast models, respectively.

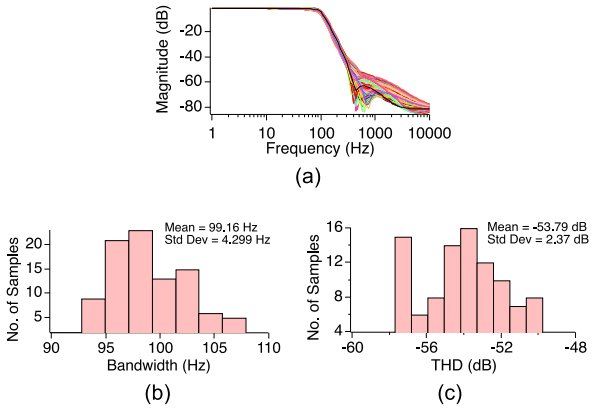

Fig. 10. 100-runs Monte Carlo simulation on (a) magnitude response, (b) bandwidth, and (c) THD.

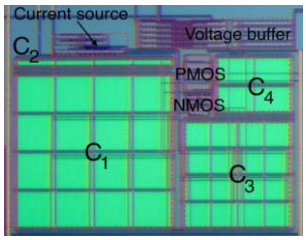

Fig. 11. ECG filter photograph with 362 μm × 466 μm die size including the on-chip buffer.

slow and typical models. Except at 0.65 V and 0 °C, the filter fails to operate for the case of the slow model. In addition, using the fast model, the filter cannot perform properly for all conditions.

The ECG LPF chip has also been fabricated in 0.35-μm CMOS technology. Capacitors C_1–C_4 are made by poly-capacitors. On-chip source-follower circuits are inserted to drive parasitic capacitances of the output pads and instrument probes. The filter occupies a silicon area of 0.168 mm^2 (including the buffer circuits) which is dominated by capacitors as shown in Fig. 11. The measurement has been done using an SR780 dynamic signal analyzer. Bias currents and bias voltages were supplied to the chip by a precision source measurement unit (Keysight B2912A). The chip was put inside a test fixture (Agilent 16442A) to obtain reliably repeatable results.

The magnitude responses of the filter for different values of I_B adjusted to cover all recommended cutoff frequencies for ECG are shown in Fig. 12. The solid lines represent the measured results, and the dotted lines are obtained

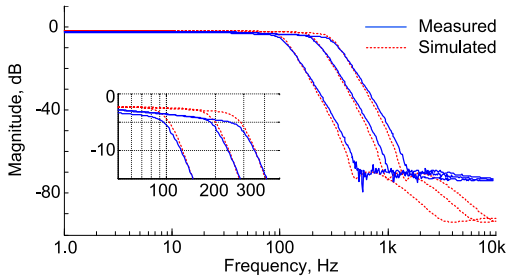

Fig. 12. Magnitude responses of the proposed ECG filter.

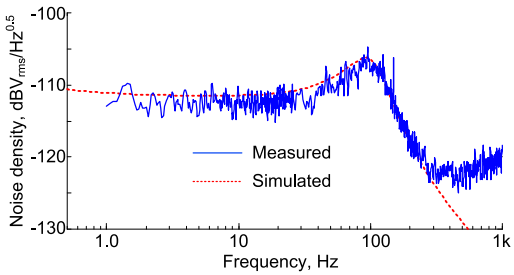

Fig. 13. Noise voltage spectral density of the proposed ECG filter.

from simulations. The simulation targets filter's bandwidth of 100, 200, and 300 Hz for I_B of 0.3, 0.6, and 0.9 nA, respectively, while the measurements show that the bandwidths of 101, 197, and 272 Hz are obtained for I_B of 0.3, 0.6, and 0.9 nA, respectively. The maximum error of almost 10% is found for the highest bias current. In terms of passband gain, we can see that measured results deviate maximally from the simulated results at the cutoff frequencies approximately 1.8 dB for all three cases. Note that the ~70 dB nearly constant attenuation of the measured magnitude response is noticeable beyond 600 Hz while the simulation result keeps falling. This is due to the parasitic mutual capacitance of ~0.5 pF that creates an extra feed-forward path allowing the input signal to travel to the output terminal directly [19]. Fortunately, this effect is not harmful significantly to our filter's functionality.

Fig. 13 shows the output noise voltage spectral density of the ECG filter for the case of I_B = 0.3 nA targeting f_C ($f_{C\text{tar}}$) of 100 Hz. From both the simulation (dotted line) and measurement (solid line), we can see that flicker noise's corner frequency appears below 1 Hz as expected. Integrated over the range of 1–200 Hz, the output noise of 46.6 and 43.9 μV_{rms} are obtained from measurement and simulation, respectively. This gives rise to the measured IRN of 64 μV_{rms}.

The linearity of the filter was estimated by measuring harmonic distortion for the case of I_B = 0.3 nA ($f_{C\text{tar}}$ = 100 Hz) as well. Fig. 14(a) shows the harmonic distortion obtained from applying a sinusoid differential input voltage (V_{id}) with 25-mV amplitude and varying the input signal frequency (f_{in}) from 20 to 120 Hz. The third-harmonic distortion (HD_3) is worse than the second-harmonic distortion (HD_2) for more than 15 dB for all input frequencies except at 40 Hz. At this frequency, HD_2 jumps as high as −70.5 dB while HD_3 appears at −62.5 dB. Nevertheless, the trend of THD follows closely with HD_3. As expected, the values of THD appear low for low values of f_{in} and rise gradually

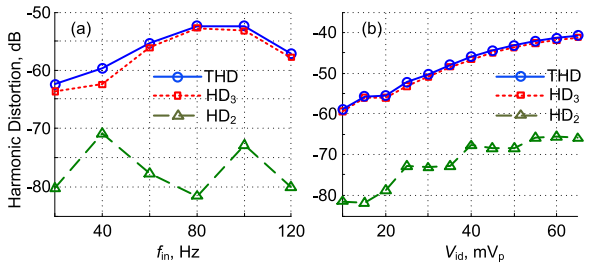

Fig. 14. Harmonic distortions of the ECG filter for $I_B = 0.3$ nA targeting f_C of 100 Hz. Measured versus (a) f_{in} and (b) amplitude for $f_{\text{in}} = 100$ Hz.

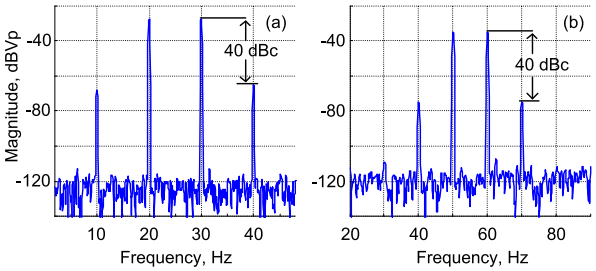

Fig. 15. Intermodulation distortions for the case of $I_B = 0.3$ nA with two situations. (a) $f_{\text{in1}} = 20$ Hz and $f_{\text{in2}} = 30$ Hz. (b) $f_{\text{in1}} = 50$ Hz and $f_{\text{in2}} = 60$ Hz.

when f_{in} approaches 100 Hz. Eventually, the THD drops again for f_{in} higher than f_C (120 Hz). The harmonic distortions were also tested versus amplitude of the input signal for $f_{\text{in}} = 100$ Hz. [This frequency is where Fig. 14(a) shows the worst THD.] The results are obtained in Fig. 14(b). It shows that the THD of -40.2 dB is associated with $V_{\text{id}} = 65$ mV$_p$. Concerning the amplitude at this point and the IRN obtained from Fig. 13, filter's DR of 57.1 dB is achieved.

A two-tone test was also performed to assess the intermodulation behavior of the filter for $I_B = 0.3$ nA. We applied input signals with two different frequencies (f_{in1} and f_{in2}) seeking identical input amplitudes that lead to the third-order intermodulation distortion (IMD$_3$) of -40 dBc for two cases: f_{in1} and f_{in2} of 20 and 30 Hz, and 50 and 60 Hz, respectively. The measurement reveals that the input amplitudes of 56 and 24 mV are obtained for the former and latter case, respectively. These results are shown in Fig. 15. We also investigated the latter case further to obtain the third-order input-referred intercept point (IIP$_3$) by increasing the amplitudes. The fundamental and third-order intermodulation components are plotted in Fig. 16. Here, the IIP$_3$ equals -12.3 dB $\cdot$ V$_p$. With the output noise level of -83 dB $\cdot$ V$_p$, we obtain 47.7 dB for intermodulation free DR of the proposed filter.

The relevant filter parameters are collected and summarized for different values of I_B in Table V. Table VI shows the comparison of our filter parameters (for the case that $I_B = 0.3$ nA was set) to other existing designs. To make a relevant comparison we divide the literature into two categories, namely, nanopower (including [4], [7], [20], and [21]) and high-frequency (including [5], [6], [15], [16], [22], and [23]) LPFs. This comparison with high-frequency filters is not relevant directly to biomedical fields but

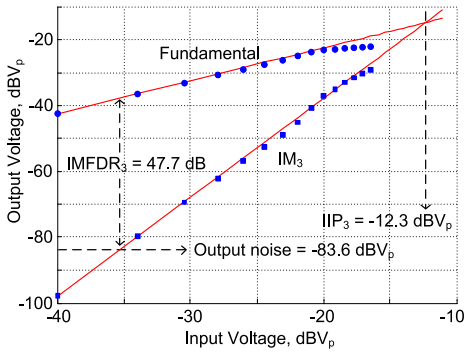

Fig. 16. Fundamental and third-order intermodulation components for $I_B = 0.3$ nA, $f_{\text{in1}} = 50$ Hz, and $f_{\text{in2}} = 60$ Hz.

TABLE V
MEASURED PERFORMANCE SUMMARY FOR $V_{\text{DD}} = 0.6$ V

Bias current I_B [nA]	0.3	0.6	0.9
Power consumption [nW]*	0.9	1.8	2.7
$f_{C\text{tar}}$; $f_{C\text{mea}}$ [Hz]	100; 101	200; 197	300; 272
dc gain [dB]	−2.77	−2.57	−2.53
Measured op. noise [μV$_{\text{rms}}$]**	46.6	46.4	46.8
Simulated op. noise [μV$_{\text{rms}}$]**	43.9	42	44.9
IRN [μV$_{\text{rms}}$]	64	62	63
THD@$f_{C\text{tar}}$ [dB] ($V_{\text{in}} = 65$ mV$_p$)	−40.5	−41	−42.5
V_{in}@−50 dB HD3 [mV$_p$] ($f_{\text{in}} = 0.3f_{C\text{tar}}, f_{\text{in}} = 0.6f_{C\text{tar}}$)	63, 40	65, 39	60, 38
IMD$_{3A}$@$V_{\text{in}} = 56$ mV$_p$ [dBc] ($f_1 = 0.2f_{C\text{tar}}$, $f_2 = 0.3f_{C\text{tar}}$)	−40.44	−40.29	−40.23
IMD$_{3B}$@$V_{\text{in}} = 24$ mV$_p$ [dBc] ($f_1 = 0.5f_{C\text{tar}}$, $f_2 = 0.6f_{C\text{tar}}$)	−40.02	−40.11	−40.22
DR@−50 dB HD$_3$ [dB] ($f_{\text{in}} = 0.6f_{C\text{tar}}$)	52.89	52.91	52.66
PSRR@$f_{C\text{tar}}$ [dB]	37.2	37.8	39.5
FoM$_1$ [aJ]	11.5	11.7	13.4

* 5 branches of I_B (4 for the filter core and 1 for the bias circuit)
** integrated from 1 Hz to $2f_{C\text{tar}}$

provided optionally for a broad perspective. In terms of power consumption, it can be seen that our design operates from the least supply voltage and consumes the lowest power. When DR is concerned, the proposed filter is comparable to other LPFs in the nanopower category but less than those in the group of high-frequency LPFs.

In terms of figure of merit (FoM), we adopt two different definitions suitable for different categories to make the most reasonable comparison. FoM$_1$ defined by (9) is widely used for nanopower filter design comparison as the filters are mostly designed for biomedical applications so that they can rarely face intermodulation between two adjacent frequencies [4]. FoM$_2$ defined by (10) is recently used in [6] and [16] suitable to the comparison of filter design for high-frequency communication systems. For both FoM$_1$ and FoM$_2$, N and f_C represent the number of poles and bandwidth of the filter, respectively. DR$_1$ is where HD$_3$ of -60 dB is produced. Frequency f_{IM3L} is obtained from the two-tone test defined

TABLE VI
PERFORMANCE SUMMARY AND COMPARISON

References	This work	[7]	[20]	[21]	[4]	[22]	[5]	[23]	[6]	[15]	*[16]
V_{DD} [V]	0.6	1	1.8	1	3	1.8	1.8	1.2	1.8	1.35	1.8
Tech. [μm]	0.35	0.18	0.18	0.18	0.35	0.18	0.18	0.13	0.18	0.18	0.18
Order	4	5	9	4	4	5	4	6	4	4	3
f_C [Hz]	101	250	3k	732	100	1.17M	10M	280M	33M	30.8M	1G
IRN [μV_{rms}]	46.27**	340	564	50	29**	50.4	24	368	45	126	213
HD_3 [dB]	−60	−49	−38.4	−40	−60	NA	−40	−31	−50	NA	−40
DR [dB]	47	50	34	55	55.70	60	78.93	53.80	70.97	71	62.4
Power [W]	0.9n	453n	360n	14.4n	15n	1m	4.1m	120μ	138m	620μ	2.3m
DC gain [dB]	−2.77	−10.5	0	−6	0	18.4	−3.5	0	< 0	−0.15	−2.9
IIP3	−12.3 dBV	NA	NA	NA	NA	24 dBV	17.5 dBm	11 dBm	1 dBm	29 dBm	25 dBm
$IMFDR_3$ [dB]	47.7	NA	NA	NA	NA	73.3	64.59	44.4	49.9	62.7	56.9
f_{IM3L}/f_C	0.396	NA	NA	NA	NA	1	0.2	0.004	0.003	0.0552	0.1
Area [mm^2]	0.168	0.13	0.03	0.13	0.08	0.15	0.43	0.018	0.14	0.1	NA
FoM_1 [aJ]	46.5	3624	5308	156	101	109.2	1.31	0.29	0.84	0.4	0.44
FoM_2 [dB(J^{-1})]	160	NA	NA	NA	NA	172.94	157.49	151	144.57	163	168

*Simulation, ** integrated over f_C

by $2f_{in1} - f_{in2}$ [6]

$$\text{FoM}_1 = \frac{P}{N \times f_C \times \text{DR}} \tag{9}$$

$$\text{FoM}_2 = 10 \times \log\left(\frac{N \times f_{\text{IM3L}} \times \text{IMFDR}_3}{P}\right). \tag{10}$$

It can be seen from the bottom row of Table VI (high-frequency category) that FoM_2 of the proposed filter falls in the middle of the group (160 dB $\cdot$ J^{-1}). Note that the designs of [15] and [16] that provide better FoM_2 than the proposed filter are also based on an FVF circuit but biased in strong inversion. Hence, the LPFs of [15] and [16] can handle the larger input signal swing than this paper, and it should be the reason to obtain better FoM_2.

Fig. 17 shows the graphs of FoM_1 plotted against the V_{DD} compared with other designs in the nanopower category. The proposed filter attains the lowest FoM_1 of 46.5 aJ. Compared with the latest design of [4], the number obtained is approximately two times better. This is mainly due to the power consumption of the proposed design is a lot lower. However, as we have analyzed in Section II-A, the LPF of [4] should be operational from V_{DD} lower than 3 V and the power consumption can be lower. Moreover, when the silicon area is concerned, the proposed LPF is slightly more than two times larger than the LPF of [4]. If we take this issue into account for FoM_1, the designs of [4] and this paper should be very comparable.

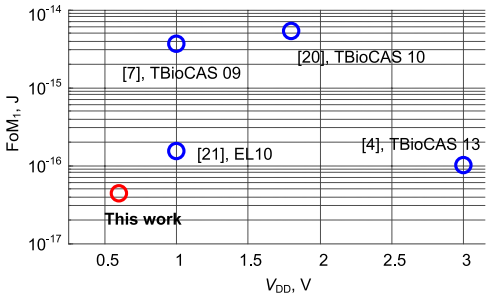

Fig. 17. FoM_1 versus V_{DD}.

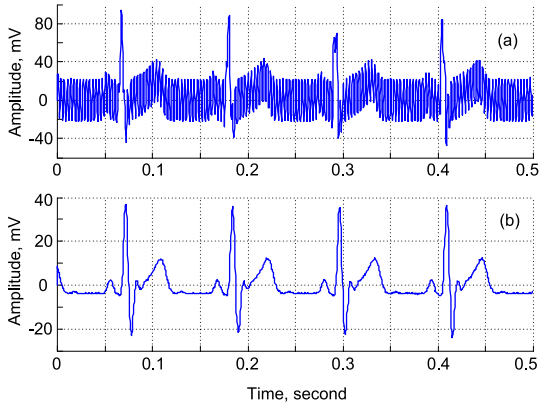

Fig. 18. ECG signal testing. (a) Noisy ECG. (b) Filtered ECG.

Fig. 18 shows the capability of the proposed filter for out-of-band signal filtering. The ECG with 65-mV peak value superimposed with artificial noise (a 20-mV, 300-Hz sinusoidal signal) generated by a waveform generator (Keysight 33522B) shown in Fig. 18(a) was applied. The LPF was configured for 100-Hz f_C by setting I_B = 300 pA. After filtering, the interference signal is suppressed while the integrity of the ECG signal is maintained as shown in Fig. 18(b). It is

noticeable that the third peak of the input signal that was corrupted by the noise can be recovered at the output terminal of the LPF.

V. Conclusion

We have described n-type and p-type FVFBs and the implementation of a pseudodifferential fourth-order ECG filter based on cascading the FVFBs. The filter has been fabricated in 0.35-μm CMOS process. The measured results reveal the superiority of the proposed filter over the previously published nanopower LPFs in terms of circuit complexity, supply voltage, and power consumption. With the DR obtained, this proposed filter can be useful for the acquisition of ECG and other types of biopotential signals.

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