PDF4280042 ผศ.ดร. จิตรเกษม งามนิล

รายงานวิจัยฉบับสมบูรณ์

# โครงการการออกแบบวงจรที่ใช้พลังงานต่ำมากโดยใช้ซีมอสในย่านต่ำกว่าแรงดันขีดเริ่มและมอสเฟทแบบเกทลอยสำหรับอุปกรณ์ชีวการแพทย์

# Micropower circuit designs for Biomedical Applications using Subthreshold CMOS and Floating-gate MOSFET

โดย

ผศ.ดร.จิตรเกษม งามนิล มหาวิทยาลัยเทคโนโลยีมหานคร

กฤษณพงศ์ นันทศรี มหาวิทยาลัยเทคโนโลยีมหานคร

กรณิการ์ มูลโพธิ์ มหาวิทยาลัยเทคโนโลยีมหานคร

ธันวาคม 2546


รายงานวิจัยฉบับสมบูรณ์

# โครงการการออกแบบวงจรที่ใช้พลังงานต่ำมากโดยใช้ซีมอสในย่านต่ำกว่าแรงดันขีดเริ่มและมอสเฟทแบบเกทลอยสำหรับอุปกรณ์ชีวการแพทย์

# Micropower circuit designs for Biomedical Applications using Subthreshold CMOS and Floating-gate MOSFET

โดย

ผศ.ดร.จิตรเกษม งามนิล มหาวิทยาลัยเทคโนโลยีมหานคร

กฤษณพงศ์ นันทศรี มหาวิทยาลัยเทคโนโลยีมหานคร

กรณิการ์ มูลโพธิ์ มหาวิทยาลัยเทคโนโลยีมหานคร

ธันวาคม 2546

สัญญาเลขที่ PDF/42/2542

รายงานวิจัยฉบับสมบูรณ์

# โครงการการออกแบบวงจรที่ใช้พลังงานต่ำมากโดยใช้ซีมอสในย่านต่ำกว่าแรงดันขีดเริ่มและมอสเฟทแบบเกทลอยสำหรับอุปกรณ์ชีวการแพทย์

# Micropower circuit designs for Biomedical Applications using Subthreshold CMOS and Floating-gate MOSFET

โดย

ผศ.ดร.จิตรเกษม งามนิล มหาวิทยาลัยเทคโนโลยีมหานคร

กฤษณพงศ์ นันทศรี มหาวิทยาลัยเทคโนโลยีมหานคร

กรณิการ์ มูลโพธิ์ มหาวิทยาลัยเทคโนโลยีมหานคร

สนับสนุนโดยสำนักงานกองทุนสนับสนุนการวิจัย

# กิตติกรรมประกาศ

โครงการวิจัยการออกแบบวงจรอิเล็กทรอนิกส์ที่ใช้พลังงานต่ำมากโดยใช้ซีมอสในย่านต่ำกว่าแรงดันขีดเริ่มและมอสเฟทแบบเกทลอยสำหรับอุปกรณ์ชีวการแพทย์นี้ ได้รับทุนสนับสนุนการวิจัยจากสำนักงานกองทุนสนับสนุนการวิจัย สัญญาเลขที่ PDF/42/2542 และได้รับการสนับสนุนอุปกรณ์และเครื่องมือการทดลองจากมหาวิทยาลัยเทคโนโลยีมหานคร คณะผู้วิจัยขอบพระคุณเป็นอย่างสูงมา ณ โอกาสนี้

# บทคัดย่อ

รหัสโครงการ PDF/42/2542

ชื่อโครงการ การออกแบบวงจรที่ใช้พลังงานต่ำมากโดยใช้ซีมอสในย่านต่ำกว่าแรงดันขีดเริ่มและมอสเฟทแบบเกทลอยสำหรับอุปกรณ์ชีวการแพทย์

ชื่อนักวิจัยและสถาบัน ผศ.ดร.จิตรเกษม งามนิล มหาวิทยาลัยเทคโนโลยีมหานคร
กฤษณพงศ์ นันทศรี มหาวิทยาลัยเทคโนโลยีมหานคร
กรณิภาร์ มูลโพธิ์ มหาวิทยาลัยเทคโนโลยีมหานคร

อีเมล์ jitkasam@mut.ac.th

ระยะเวลาโครงการ 4 ปี

วงจรอิเล็กทรอนิกส์ที่ใช้พลังงานต่ำมากหมายถึงวงจรที่มีอัตราการใช้พลังงานในระดับไมโครวัตต์ ซึ่งเป็นการกำหนดว่าวงจรใดๆ ที่ใช้แหล่งจ่ายไฟมากกว่าหนึ่งโวลต์จะสามารถใช้กระแสไบอัสให้แก่อุปกรณ์ทรานซิสเตอร์ได้ในระดับพิโคหรือนาโนแอมแปร์เท่านั้น หรือสามารถใช้กระแสไบอัสได้ในระดับไมโครแอมแปร์ถ้าวงจรนั้นๆ ใช้แหล่งจ่ายไฟประมาณหนึ่งโวลต์ หรือในอีกทางหนึ่งคือการออกแบบวงจรให้มีจำนวนกิ่งที่ต่ออยู่ระหว่างแหล่งจ่ายไฟเป็นจำนวนน้อยที่สุดเท่าที่จะทำได้ เพื่อให้สามารถบรรลุเป้าประสงค์นี้ เราสามารถออกแบบวงจรโดยใช้อุปกรณ์ซีมอสในย่านต่ำกว่าแรงดันขีดเริ่มและมอสเฟทแบบเกตลอยจากเทคโนโลยีแบบซีมอสในปัจจุบัน โดยเฉพาะอุปกรณ์มอสเฟตแบบเกตลอยบนเทคโนโลยีซีมอสมาตรฐานที่มีชั้นสารโพลีสองชั้นนั้น สามารถอำนวยให้นักออกแบบสร้างสรรค์วงจรใหม่ๆ เพื่อการประยุกต์ใช้งานในด้านวงจรแรงดันต่ำและใช้พลังงานต่ำมาก วงจรประมวลผลข้อมูลแบบอนาลอกและอื่นๆ งานวิจัยนี้ได้ทำการรวบรวมความรู้พื้นฐานเกี่ยวกับอุปกรณ์มอสเฟตแบบเกตลอยได้แก่ คุณสมบัติหลัก คุณลักษณะในการทำงานและแบบจำลองทั้งทางคณิตศาสตร์และทางการจำลองการทำงานโดยโปรแกรมจำลองการทำงานวงจรอิเล็กทรอนิกส์ นอกจากนี้ ยังได้นำเสนอการออกแบบวงจรประมวลผลสัญญาณเชิงอนาลอกพื้นฐานอีกหลายวงจรเพื่อการนำไปประยุกต์ใช้งานทางด้านระบบชีวการแพทย์ อาทิ วงจรเลียนแบบการทำงานของเซลและอวัยวะ การปรับปรุงสัญญาณและการเชื่อมต่อกับอุปกรณ์ตรวจจับต่างๆ

คำหลัก แรงดันต่ำ พลังงานต่ำ พลังงานต่ำมาก มอสเฟตแบบเกตลอย การประมวลผลสัญญาณเชิงอนาลอก วงจรในโหมดกระแส

# Abstract

Project Code: PDF/42/2542

Project Title: Micropower circuit designs for Biomedical Applications using Subthreshold CMOS and Floating-gate MOSFET

Investigator: Jitkasame Ngarmnil, Mahanakorn University of Technology

Krissanapong Nundhasri, Mahanakorn University of Technology

Komika Moolpho, Mahanakorn University of Technology

Email Address: jitkasam@mut.ac.th

Project Period: 4 years

The term 'Micropower' defines a class of circuits with power consumption in micro watts level. It implies that the bias current level must be between the level of pico and nano Amp for circuit operation above 1V power supply or the bias current level can also be in the range of micro Amp for circuit operation around 1V power supply. The other mean is to design circuits with as less as possible the branches drawing current from the supply rails. In state of the art CMOS technologies, weak inverted MOSFET and Floating-gate MOSFET allow circuit designers to achieve the goals. The Floating-gate MOSFET or FGMOS on a standard double-poly CMOS offers various new useful functions which can be used to create many novel circuits such as low voltage low power circuits, analogue computational circuits and etc. This research gives a review of the FGMOS such as the principle properties, characteristics and modeling for simulations. Several analog signal processing building blocks have been proposed. They are very useful to applications in biomedical systems such as biologically inspired circuits, signal conditioning and sensor interfacing.

Keywords: Low voltage, Low power, Micropower, Floating-gate MOSFET, Analog signal processing, Current-mode circuit

## Contents

# 1. INTRODUCTION

Nowadays, Low power and Low voltage circuits are significantly demanded by the market of portable devices and applications. Together with the further device shrinking of new coming commercial CMOS technologies, the continuously down scaling of supply voltage is obviously inevitably in modern microelectronic environments. In the contrary, performances and capabilities of electronic systems have never been scaled down. System complexities are increasing significantly every year. Design caution has then been seriously given to the management of power consumption. Currently, most computational systems are performed digitally and based on applications of microcomputers where high speed and high complexity functions have little been considered to optimize power consumption and complexity. Excessive resources and devices have been provided to achieve the required speed and complexity functions. Hence the higher the component counts the higher the power consumption. In biomedical applications where electronic circuits are operated by battery cells and sometimes used intact with or inner human body, power consumption must be limited in order to prolong the battery life and to require very less battery changing, while the speed and system functionalities are still the main requirement. In this case, analog circuits and systems are a good candidate, having a high potential to achieve a high complexity and high computational capability with less power consumption than in digital systems. In this case, Floating-gate MOSFET devices (FGMOS) will play an important role in performing low power analog signal processing because the FGMOS devices have multiple gate terminals which enable the MOSFET to theoretically compute multiple signals at a time. However, this goal can only be achieved in conjunction with a support of new circuit techniques and structures.

In early days, FGMOS devices have been used in digital circuits as storage devices. Currently, FGMOS devices receive a widespread use as a data storage element in commercial EPROM and EEPROM circuits that are typical examples where data are stored in a form of charge on the floating-gates. The devices have been proven to be very efficient in binary information storage because of ease in programming as well as the long-term charge retention. In the present binary data processing, information storing is achieved by effectively depositing on or removing off the charges on the floating-gate. Today, the device has been proved to be very reliable and very compact integration as indicated by the commercial manufacturing of megabit

flash memory. In the last decade while FGMOS devices played very important roles in Memories, FGMOS transistors had received little attention as analog circuit elements. However, during the transition of the new decade, there have been many applications of these devices in analog circuits based on their unique characteristics of the variable threshold voltage. In other words, the threshold voltage is programmable. As the trend of integrated circuits moves toward low voltage applications, the floating-gate MOSFET is now very useful in analog integrated circuits and signal processing applications. In reduced power supply voltage, FGMOS transistor with programmable threshold voltage can then be used with reduced effective threshold voltage and hence the smaller required gate-source voltage. The floating-gate transistors can also be used in analog circuit trimming of which the advantage over traditional fuse trimming technologies is that the trimming is reversible if drift in the circuit occurs. There are also other applications, such as input offset trimming of differential pairs, low voltage op-amp with floating-gate input stages, D/A [1], electronic programming [2,3], multiple input Op-Amp [4], low-voltage operation [5], circuit trimming [6], neural network [7] and four-quadrant analog multiplier [8,9].

At the beginning of this report, reviews and basic principle of the FGMOS devices are introduced in Section 2, where the fundamental and literature reviews from previous reported works are summarized to give an overview of Floating-gate devices, circuits and systems.

In Section 3, Floating-gate devices and modeling are addressed including a physical structure of floating-gate device, capacitive models, mathematical and macro models for SPICE simulations including some simulation results.

In Section 4, a novel Hysteresis Tunable Voltage Comparator is presented. The circuit is basically a simple voltage comparator embedded with a positive feedback scheme to create the hysteresis. In this work, two FGMOS devices are employed to perform the feedback where one of the control gate voltages is used to tune an amount of the feedback current to the input devices. As a result, the trip voltages; $V_{TRP+}$ and $V_{TRP-}$ of the comparator can be tuned electronically. The proposed idea is demonstrated on a standard double-poly CMOS processes. Since the design normally incorporates with layout of the FGMOS in order to get the value of the gate capacitances effectively, Magic Program is used to create the layouts on AMI 1.2μm CMOS process available

through MOSIS. Simulation results from HSPICE are given to demonstrate the functionality.

In section 5, Digital comparators using FGMOS devices are proposed here as another version of comparator for digital domain. The comparators use FGMOS devices as an input stage to create a 4-bit digital comparator based on classical analog voltage comparator. Two types of the 4-bit digital comparator are explained in this section, a normal 4-bit comparator and a regenerative 4-bit comparator. Based on the two type comparators, an 8-bit digital comparator is also presented. Simulation results verifying the functionality of the proposed comparators are demonstrated.

In section 6, an application of the multiple-input FGMOS comparator is also proposed in this section as a design of Class-D amplifier. Based on the used of the proposed comparators, the amplifiers have a simple architecture and are easy to be integrated with other circuit blocks on a chip scale system level. This amplifier exploits the proposed multiple-inputs FGMOS voltage comparators.

In Section 7, a new low voltage current amplifier is proposed. The circuit is totally formed in the class AB structure, utilizing CMOS inverters and the recently proposed additive analog inverter using floating-gate MOSFETs. Operating in a negative feedback topology, the amplifier can deal with wide signal swings up to $\pm 200\mu A$, with 1% of the THD and 10pF of $C_L$. Designs and HSPICE simulation results are demonstrated on 0.5μm double poly CMOS processes with 1.5V and 1V power supplies to indicate high frequency and low power capabilities respectively.

In Section 8, a low voltage inverting second generation current conveyor is proposed. The circuit can be operated up to a 100MHz with $\pm 0.75V$ power supply. The circuit is formed in class AB structure using CMOS inverters and a pseudo floating-gate MOSFETs additive analog inverter facilitating a negative feedback loop to regulate accurate signal tracking of the terminal voltage X to Y and the terminal current Z to X. Simulation results on 0.5μm double poly CMOS processes confirm high precision conveying features, wide signal swing and low voltage capabilities of the current conveyor.

In section 9, a new high speed low input current comparator is proposed in this section. Based on a simple negative feedback scheme around the transimpedance stage with an emphasis on a very large loop-gain, the transformed voltage signal is

maintained at the lowest swing that results in a speed improvement. On a 0.25um TSMC CMOS process, simulation results demonstrate propagation delays of 3.6ns with ±100nA input current and 1.5Volts power supply, while the smallest input current is ±50pA. Performances are also shown with other $V_{DD}$ such as 1.0, 1.8 Volts.

Finally, conclusions and suggestions for future improvements are discussed in Section 10.

## 2. FLOATING GATE MOSFET

Floating-gate MOSFET abbreviated as FGMOS is a device on standard double-poly CMOS processes. It offers various new useful functions which can be used to create many novel circuits such as low voltage low power circuits, analogue computational circuits etc. This section gives a review of FGMOS and also includes some of examples from earlier reported works as a background understanding for this device

### 2.1 LITERATURE REVIEWS: INITIAL WORKS ON FLOATING-GATE CIRCUITS

Floating-gate MOSFET (FGMOS) structure has been invented for a long time since 1967 by Kahng and Sze [10]. Until now FGMOS is widely use for many famous nonvolatile digital storage device such as EPROMs, EEPROMs and flash $E^2$PROMs. The floating-gate structure has a unique structure different from a conventional MOSFET. The gate of FGMOS is composed of two layers; poly1 and poly2, as shown in Fig.2.1. The gate on poly1 is basically a conventional gate of MOSFETs but it is completely encased in an insulator made of Silicon Dioxide ($SiO_2$). Since $SiO_2$ is a very good isolator, so this electrode has no direct electrical connection to any other electrical conductor, then it is often referred to as "floating-gate". The other adjacent gate conductor plate made of poly2 is an input gate which is a capacitive coupling terminal to the floating-gate. Potential at the input gate can be coupled to modulate the potential on the floating-gate which then controls the current flow in the channel of the MOSFET. If electrons are trapped inside the floating-gate, they cannot leak out due to the property of the oxide. Changing the number of electrons on the floating-gate means alter this potential. In memory applications, altering the logic output by changing the number of charge on the floating-gate is referred to as "writing" to the memory device and the state can be maintained for more than 10 years without an effect during read cycle. After the invention of FGMOS device in 1967, there are many researchers working to develop the device as shown in growth vs. year of developments in Fig.2.2

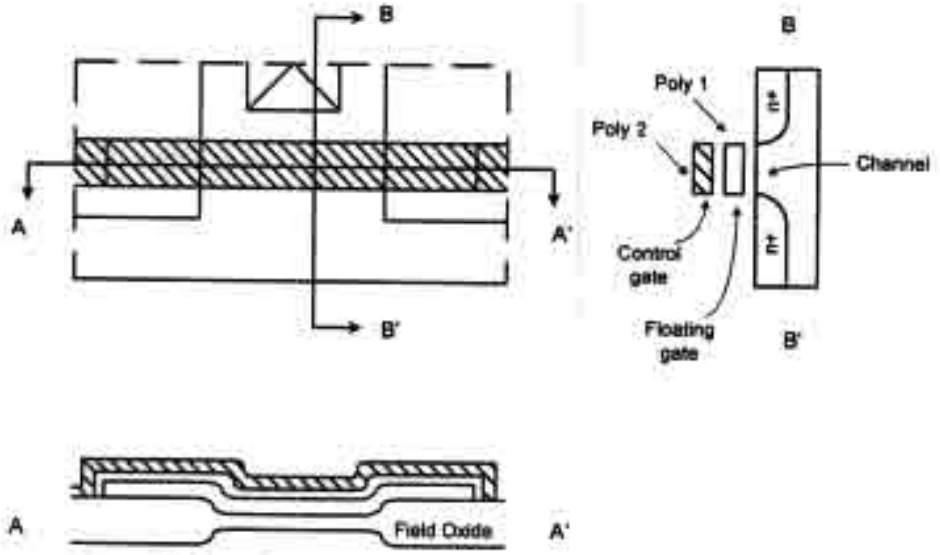



Figure 2.1 Top view and cross-section views through a typical EPROM

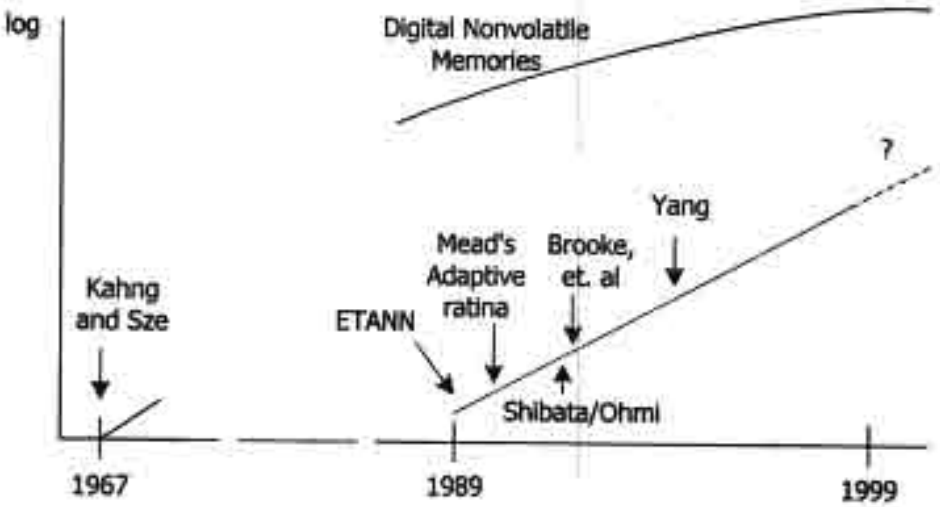



Figure 2.2 Development of floating-gate [11]

The current interest in floating-gate circuits started from developing large-scale computations in neuromorphic systems [11]. The introduction of the ETANN chip by Intel in 1989 showed the potential of using floating-gate devices for applications other than digital memory elements [12]. The core of the chip's function was an analog vector-matrix calculation employing a floating-gate array of 10240 analog matrix elements. This floating-gate device developed in a specialized EEPROM fabrication process, were used as an analog floating-gate memory. The chip has an impressive computational ability but the production cost of this chip cause it receiving less interests.

After Intel's invention chip, a new functional transistor had been proposed in 1992, which worked more intelligently than a mere switching device by Shibata and Ohmi [14]. This transistor can calculate the weighted sum of all input signals at the gate level, and controls the "on" and "off" of the transistor based on the result of such a

weighted sum calculation of all input gate potentials. Since the function is quite analogous to that of a biological neuron, the new transistor is called "a neuron MOSFET" or "neuMOS" (abbreviated as VMOS) in short. The device as shown in Fig.2.3 is composed of a floating-gate and multiples of input gates that introduce the capacitive coupling effect for the weight sum calculation. There is essentially no power dissipation occurs in the calculation mechanism, making the device ideal for ULSI implementation that need less power consumption as possible.

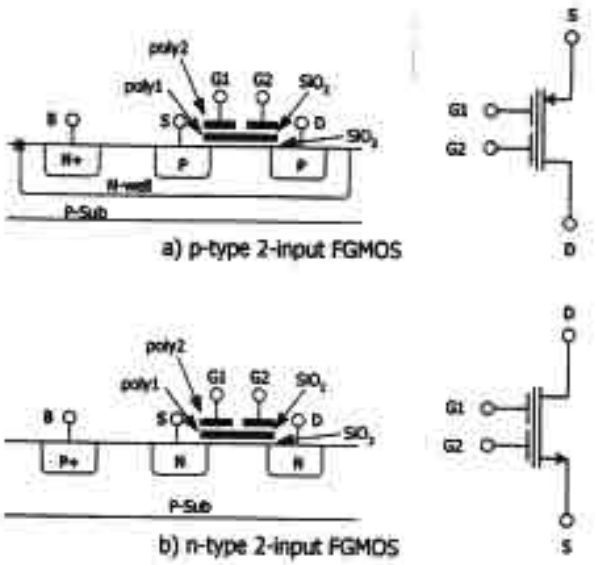



Figure 2.3 Simplified 2-input FGMOS structure and symbol (a) p-type (b) n-type MOS

Three research group accomplishments laid the groundwork for most of the current floating-gate circuit developments. The earlier accomplishments could be defined into three approaches of using the FGMOS devices as follows.

1) Thomsen and Brook [13] demonstration and use of electron tunneling in a standard CMOS double-poly process allowed many researchers to investigate and to exploit floating-gate circuit concepts without requiring accessing to specialized fabrication process. This research works laid a new approach to accurately control the amount of charge on the floating gate. As a result, it led to later developments and researches in analog memory [2, 3].

2) The VMOS approached by Shibata and Ohmi [14] provided the initial inspiration and framework to use capacitors for linear computations that using multiple input FGMOS to compute analog information. These researchers concentrated on the floating-gate circuit properties instead of the device properties, and used either ultra-

violet (UV) light to equalize charge, or simulated floating-gate elements by opening and closing MOSFET switches. Today many researchers work on computational systems with the floating-gate devices that were firstly established by Shibata and Ohmi. The way of thinking about FGMOS transistors introduced by Shibata and Ohmi has resulted in a number of interesting analog and digital information-processing circuits [1, 4, 8, 9, 16, 17, 18, 21-27], including a multiple-input floating-gate differential amplifier, a four-quadrant floating-gate multiplier, simple D/A converters, Translinear circuits and etc.

3) Carver Mead's adaptive retina [15] gave the first example of using continuously operating floating-gate programming/erasing techniques, as the backbone of an adaptive circuit technology. The works led to the later developments and implementations of adaptive circuits in neuron network [19, 20].

## 2.2 OUTSTANDING PROPERTIES OF FGMOS DEVICE

FGMOS device is basically a multiple-input device of which the main properties can be very useful for analog and digital computational circuits. It has unique and attractive characteristics of which the most important properties to be applied in this research and report are as follows:

1) As a multiple-input gate device, the voltage appears at the floating gate is a linear summation of its input voltage at all input terminals. This characteristic makes the device suitable for analog computation.

2) The effective threshold voltage ($V_{th}$) seen at the input gate is tunable.

These two phenomena are very attractive to analog designers. The first feature of the multiple-input gates allows analog designers to design a novel or to adapt many existing circuits to work with more complexity function without adding power consumption, while the second feature allows FGMOS devices to be operated at a very low the supply voltage as a result of the threshold voltage tunability. Both low voltage and low power operations are the most important requirement for biomedical applications.

## 3. FGMOS DEVICE AND MODELING

Floating gate MOSFET has many impressive characteristics that can be used to design a novel circuit or to enhance exist analog circuits for additional special features such as very low power, low voltage. With the available FGMOS device, one can put a new function into the present circuits. However, one problem that can cause trouble to designers is how to design and simulate an FGMOS circuit in the conventional simulation programs. This section describes a basis of floating gate structure, modeling and simulate macro models that are essential to design and simulation of FGMOS circuits. Threshold voltage shifting and weight summation characteristics of FGMOS are demonstrated by simulation results.

### 3.1 DEVICE STRUCTURES AND THEORY

Many applications using multiple-input floating-gate transistors in analog circuits have been reported over the last few years, based on the main properties that make these devices attractive for analog applications as follows.

1) The long-term retention characteristic of the charge injected into the floating-gate features analog memory, which are very useful applications for DC offset trimming, neural networks for weight storage and etc.

2) The simple implementation of linear weighted voltage addition is performed by only one FGMOS device.

Normally, these operations require relatively complex circuitry when using conventional MOS or bipolar devices but they are performed by only one FGMOS device. However, a practical problem with a multiple-input floating-gate device is that all circuit simulators consider capacitor as an open circuit for DC analysis and for this reason there is obviously a DC convergence problem with the floating-gate nodes, if the conventional MOSFET model and capacitors are used straightforwardly. Consider the floating-gate transistor represented Fig.3.1, of which the practical layout is given in Fig.3.2. The equivalent circuit of this device including capacitors between each of the inputs and the floating gate (denoted as poly1-poly2 capacitors) has shown in Fig.3.3. These capacitors are labeled $C_1$, $C_2$, ..., $C_n$. The conventional gate-source and gate-drain capacitances are labeled $C_{fg\text{-}s}$ and $C_{fg\text{-}d}$ respectively. For example, if we assume a FGMOS device with only two input gates, the extract netlist of the layout will be derived as shown in Fig.3.4, in which we can see that there is only one conventional MOSFET

and five capacitors denoted as $C_0$ to $C_4$. $C_2$ and $C_4$ are input coupling capacitors between the input gate g1 and g2 to the floating-gate node respectively. It is noted that floating-gate node is floating for the time being and can not be used for simulation directly although the netlist has been extracted from the correct layout. It is concluded that the conventional equivalent circuit and netlist always lead to DC convergence problems in DC analysis of the simulator as a result of the floating node. There is a need to modify the extracted netlist in order to provide a DC path to the floating node with affecting the circuit behavior. This will allow a successful simulation of the extracted netlist.

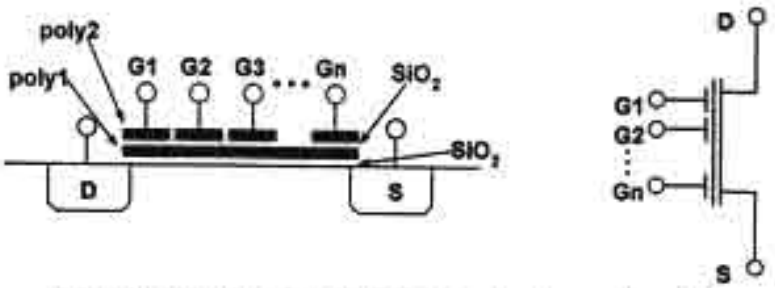



Figure 3.1 Multiple-input floating-gate structure and symbol

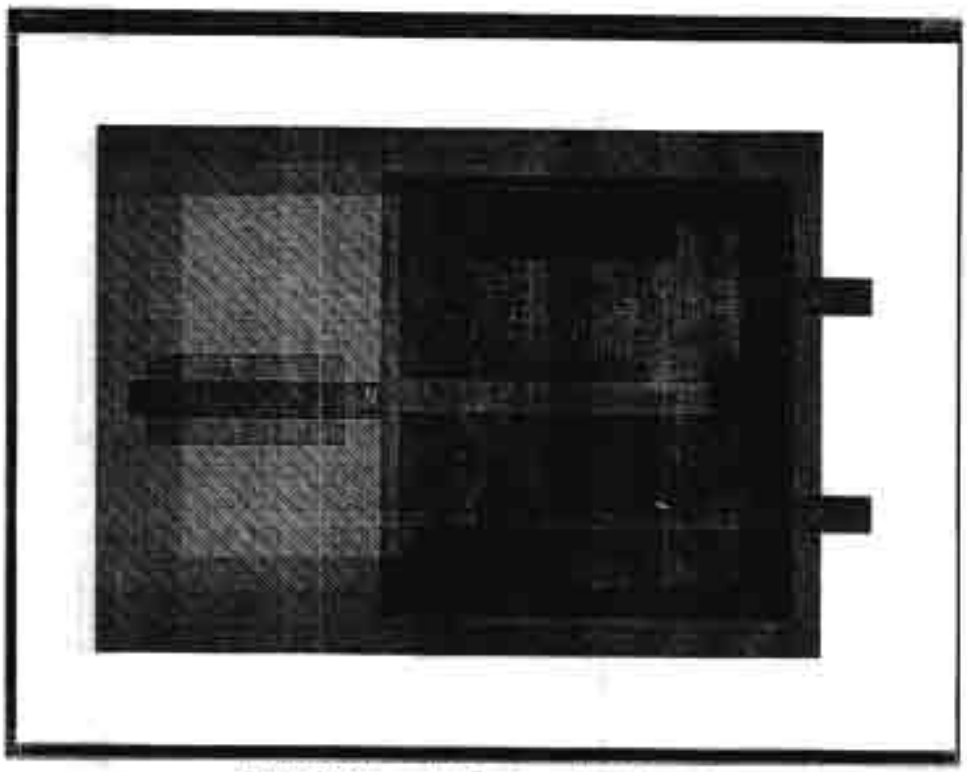


Figure 3.2 Layout of two-input floating-gate

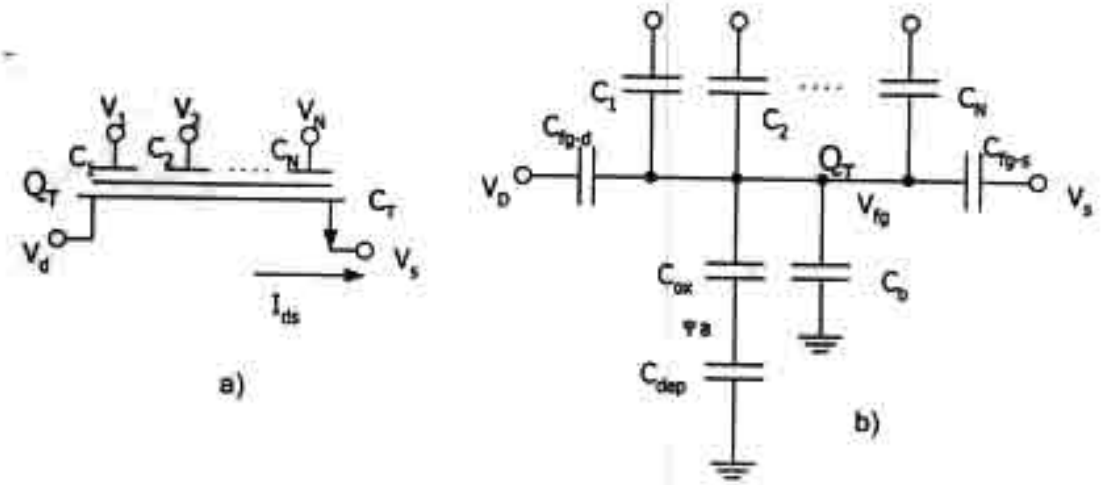



Figure 3.3 Multiple-input FGMOS a) symbol, b) capacitive model

```
* HSPICE file created from fgmosp.ext - technology: scm

.option scale=0.6u

m0 D Fg S B pfet w=22 l=4
+ ad=66 pd=50 as=66 ps=50
C0 B B 7.0fF
C1 B Fg 24.1fF
C2 g1 Fg 161.8fF
C3 B S 7.0fF
C4 g2 Fg 161.8fF

** hspice subcircuit dictionary
ic2:" $ []
```

Figure 3.4 Extraction of layout of two-input floating-gate in Fig.3.2

## 3.2 MODELING OF MULTIPLE INPUT FLOATING-GATE MOSFET

The basic structure of the FGMOS transistor is shown in Fig.3.2. It consists of a MOS transistor with a floating-gate (1st polysilicon layer) over the channel and in some cases extending over to the field oxide area. Array of control gates (multiple input gates) are formed by the 2nd polysilicon layer over the 1st polysilicon which is the same layer with the floating-gate. The capacitive couplings between the multiple input gates and floating-gate and the channel are shown in Fig.3.3(b) while Fig.3.3(a) is a symbolic representation of such the device. At the floating-gate node, total charge must be conserved [28-30] and the stored charge in the floating-gate, $Q_T$, is

$$Q_T = \left(\sum_{i=1}^{n} -C_i(V_i - V_{FG})\right) - C_{FD}(V_D - V_{FG}) - C_{FS}(V_S - V_{FG}) - C_{FB}(V_B - V_{FG}) - Q_{ch} \quad (3.1)$$

where $C_i$ is the capacitance between the floating-gate and each of the $i^{th}$ input gate. $V_i$ is the $i^{th}$ input voltage. $V_{FG}$, $V_D$, $V_S$ and $V_B$ are the floating-gate, drain, and

substrate voltages, respectively. $C_{FD}$, $C_{FS}$, and $C_{FB}$ are the overlap capacitances between the floating-gate and drain, source, and bulk, respectively.

Now $Q_{ch}$ is the total channel charge obtained by integration of the channel charge per unit area, $Q_n(y)$, along the channel and can be given as (3.2) [30, 31].

$$Q_n(y) = -\frac{C_{OX}}{WL}\left(V_{FG} - V_T^* - V_{ch}(y) + V_S\right) \tag{3.2}$$

where $y$ is the distance along the channel, $V_{ch}(y)$ is the voltage along the channel, $C_{OX}$ is the floating-gate gate oxide capacitance, and $V_T^*$ is the threshold voltage seen from the floating-gate. The variation of depletion charge along the channel is neglected by using only its value at the source. Hence, by taking the integral of (3.2) and substituting $Q_{ch}$ into (3.1), the equation for the drain current of the FGMOS transistor in saturation is obtained.

$$I_d = \frac{1}{2}K\left[\frac{Q_T}{C_T} + \frac{\sum_{i=1}^{n} C_i V_i}{C_T} + \frac{C_{FD}V_D}{C_T} + \frac{C_{FB}}{C_T}V_B - V_S \times \left[1 - \left(\frac{C_{FS}}{C_T} + \frac{2C_{OX}}{3C_T}\right)\right] - \left(1 - \frac{2C_{OX}}{3C_T}\right)V_T^*\right]^2 \tag{3.3}$$

where $K = \mu_n\left(C_{OX}/L^2\right)$ is the transconductance parameter, $\mu_n$ is the electron mobility, and $L$ is the channel length. $C_T$ is the total capacitance associated with the floating-gate, which is given by

$$C_T = \frac{2}{3}C_{OX} + C_{FD} + C_{FS} + C_{FB} + \sum_{i=1}^{n} C_i \tag{3.4}$$

With UV illumination after fabrication, zero initial stored charge on the floating-gate can be assumed, neglecting charge injection during device operation, and assuming $C_{FD}$ is much less than $C_T$, (3.3) can be simplified to the following form.

$$I_d = \frac{1}{2}K\left(\sum_{i=1}^{n} w_i V_i + w_B V_B - w_S V_S - w_T V_T^*\right)^2 \tag{3.5}$$

where the capacitive coupling ratios are defined as $w_i = \left(\frac{C_i}{C_T}\right)$, $w_B = \left(\frac{C_{FB}}{C_T}\right)$, $w_S = \left[1 - \left(\frac{C_{FS}}{C_T}\right) - \frac{2C_{OX}}{3C_T}\right]$, $w_T = 1 - \frac{2C_{OX}}{3C_T}$. Equation (3.5) shows that the FGMOS transistor drain current in saturation is proportional to the square of the weighted sum of the input voltage signals, where the weight of each input signal is determined by the capacitive coupling ratio of the input to the total capacitance around the floating-gate area. Hence, the squaring operation on the two signals is inherently performed in the

FGMOS transistor. From (3.5), the drain current of a multiple input floating gate MOSFET, can be rearranged as (3.6) and (3.7).

$$I_d = \frac{1}{2}\mu C_{ox}\frac{W}{L}[(w_1 V_{G1} - V_S) - (V_{TH} - w_2 V_{G2})]^2 \quad (3.6)$$

$$I_d = \frac{1}{2}\mu C_{ox}\frac{W}{L}[(w_1 V_{G1} + \ldots + w_n V_{Gn}) - V_S - V_{TH}]^2 \quad (3.7)$$

The drain current is essentially a linear sum voltage of all inputs weighted by the capacitive coupling ratios. Equation (3.6) is arranged to show the threshold tuning operation with only two input gates are assumed. It is seen that $V_{G1}$ can be utilized as a signal port while $V_{G2}$ is used to tune the effective threshold voltage seen from the input G1. Equation (3.7) is written to show a linear sum of the weighted multiple-input voltages. The two characteristics will be exploited in this work.

Equation (3.5) can be used to derive an equivalent circuit that allows calculation of a DC operating point at the floating-gate node and also satisfies the charge conservation shown in (3.1). This circuit is shown in Fig.3.5. It includes the necessary additional branch with an arbitrarily large resistor $R_G$ (1000GΩ) and n+2 voltage sources controlled by the voltages $V_1$, $V_2$,...,$V_n$, $V_S$ and $V_D$. These elements are connected in series between the floating-gate and ground. The gain control factor for each voltage source corresponds to the ratio of the input voltage source corresponds to the ratio of the input capacitance associated to each control voltage over the total capacitance $C_T$. This branch is included in order to allow DC convergence during DC analysis of the simulation and is neglected on the AC and/or transient performance of the circuit. The equation given above assumes that the gate-source and gate-drain capacitances, $C_{FS}$ and $C_{FD}$, are approximation constant. This, in practice is a good approximation if the transistor remains in triode or saturated mode, which is the case for most analog circuit applications. For the case that $C_{FS}$, $C_{FD} << C_1$, $C_2$,...,$C_n$ then $C_T \approx C_1 + C_2 + \mathrm{K} + C_n$, and variations in $C_{FS}$ and $C_{FD}$ when the transistor changes from saturations to triode mode (or to cutoff) do not cause a significant change in the gain coefficients of voltage control voltage source (VCVS:E) a1, a2,...,an. The listing of a SPICE sub-circuit for a two-input floating-gate N-channel transistor with width over length ratio W/L=25/3 and input capacitance C2=2C1=288fF is given in Table 3.1. $C_1$ and $C_2$ correspond to poly1-poly2 capacitors with area of $300u^2$ and $600u^2$ respectively. $C_{FS}$ and $C_{FD}$ have values of 44.5fF. They were calculated using 2um CMOS N-well technology parameters according to $C_0=C_{ox}WL+C_{GSO}W$, $C'_0=C_{GDO}W$,

where $C_{ox}$, $C_{GSO}$ and $C_{GDO}$ are the oxide capacitance density and the gate-source overlap capacitance per unit length respectively.

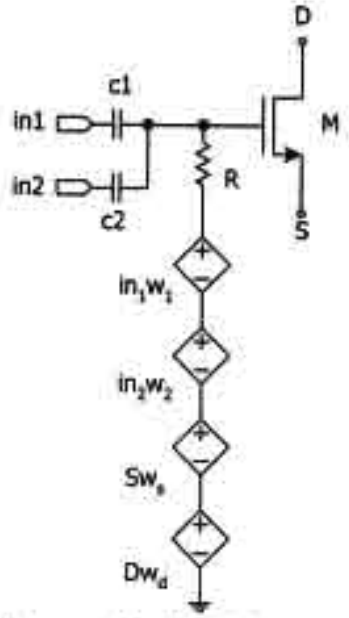



Figure 3.5 Macro model of multiple-input FGMOS [26]

Table 3.1 Multiple FGMOS sub-circuit

```
.SUBCKT input3 B D g1 g2 g3 S
C1 fg g1 50fF
C2 fg g2 50fF
C3 fg g3 50fF
M4 D fg S B NMOS L=1u W=20u AD=66p PD=24u AS=66p PS=24u
R5 fg N9 5g
e6 N9 N5 g1 S 0.5
e7 N5 N2 g2 S 0.5
e8 S N2 S g3 0
.ENDS input3
```

Based on the FGMOS model in (3.6), a tested circuit for the threshold voltage tuning can be shown in Fig.3.6 of which the drain current versus voltage at control gates curve of the drawn p-type 2-input FGMOS in Fig.3.2 can be demonstrated in Fig.3.7. In order to show $V_{gf}$ tuning capability, the circuit has been tested under the condition that $V_{CG2}$

is used as the threshold tuning voltage and set to 0V, 1V, 2V, ..., 5V while $V_{G1}$ is used as an input terminal

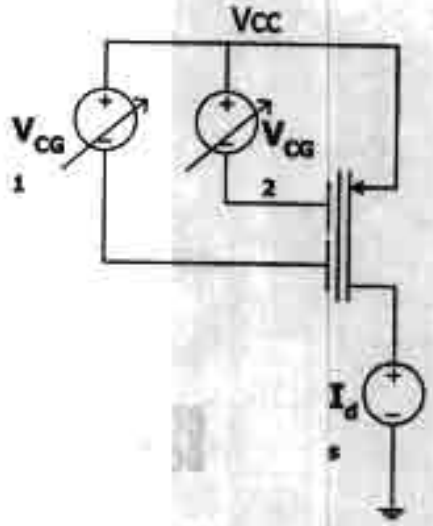



Figure 3.6 Test circuit for DC sweep of p-type 2-input FGMOS

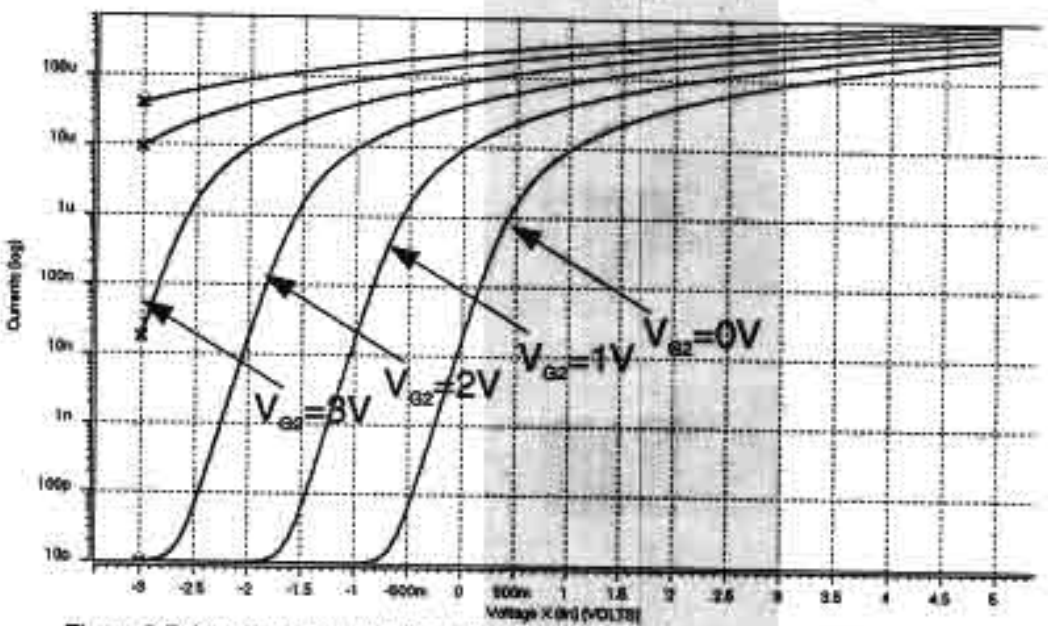



Figure 3.7 Simulation result of test circuit in Fig.3.6 using macro model in Fig.3.5

Regarding the drain current equation in (3.6) and (3.7), the initial stored charge on the floating-gate is assumed to be zero. The drain current equations are quite trivial. However, the stored charge is normally unpredictable. Thus before any operations in analog applications, the stored charge should be removed completely. The means in controlling the charge relating to two physical phenomena such as: hot carrier injection [31] and Fowler-Nordheim tunneling (F-N tunneling) [32]. These are the phenomena used for writing process in commercial UV-EPROMs [33], byte-alterable $E^2$PROMs and flash EEPROMs.

# 4. HYSTERESIS ANALOG FGMOS COMPARATOR

A voltage comparator is a circuit that compares the instantaneous value of an input signal $v_{in}(t)$ with a reference voltage $V_{ref}$ and produces a logic output level depending on whether the input is larger or smaller than the reference level. The most important application for a high-speed voltage comparator occurs in and analog-to-digital converter system and etc. In this section, a design of analog voltage comparator that capable to tune window size of its hysteresis loop is presented. This comparator based on conventional analog comparator but there is a tuning capability on the ratio of positive feedback performed by multiple-input FGMOS devices. Some fundamental of the comparator are reviewed and then design and simulation results are shown in this section.

## 4.1 FUNDAMENTAL COMPARATOR

One very important and widely used comparator configuration is a high-gain differential input, single-ended output amplifier [34]. Fig.4.1 (a) shows the symbol of a differential comparator which is very similar to that of an operational amplifier. Usually, the comparator stage is followed by a latch, which is essentially a bi-stable multivibrator. The latch provides a large and fast output signal of which amplitude and waveform are independent of those of the input signal and is hence well suited for the logic circuits following the latch. If no latch is used, the output $V_{out}$ should have a large swing, say, 0 to +5, as the input changes from −1mV to +1mV. Thus the required gain is around 5V/2m = 2500, or 68dB. If a latch is used, $V_{out}$ is only needed to be higher than the combined offset and threshold voltages of the latch; this value is around 0.2V or less. Hence a gain of 200 is adequate. A comparator is therefore essentially a high-gain op-amp designed for open-loop operation but it does not require frequency compensation.

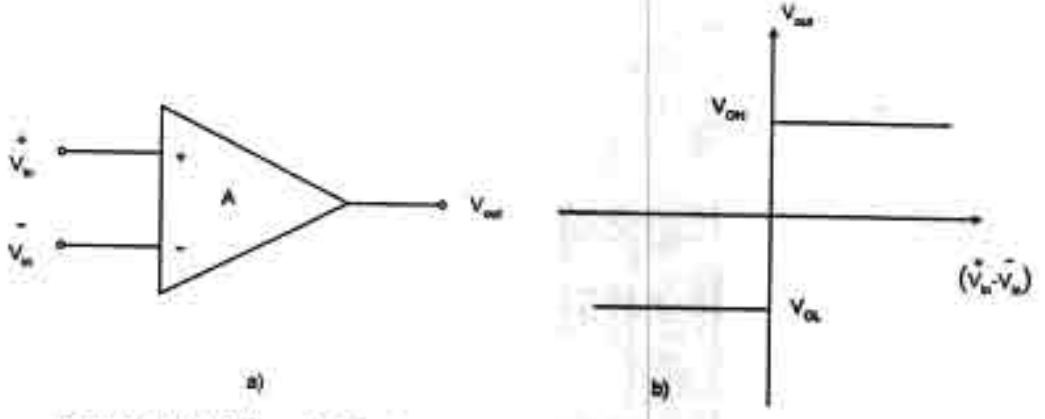



Figure 4.1 (a) Differential-input comparator (b) Transfer curve of ideal comparator

The transfer curve of the ideal differential comparator is shown in Fig.4.1(b). In this figure the negative input of the comparator in Fig4.1(a) is tied to a reference voltage $V_{ref}$. When the positive input is greater than $V_{ref}$ the output is logic high ($V_{OH}$), and when it is less than $V_{ref}$, the output is logic low ($V_{OL}$). The ideal transfer curve of Fig.4.1(b) corresponds to a differential gain of infinity. In actuality the differential gain has a finite value equal to Av. Another non-ideal effect of the differential comparator is the input-referred dc transfer curve will begin changing only after the input difference exceeds $V_{off}$. The dc transfer curve of a practical differential comparator with finite gain of Av and a dc-offset voltage of $V_{off}$ are shown in Fig.4.2 where $V_{IL}$ and $V_{IH}$ are the input excess of that required to cause the output to switch state. Finally, the speed or response time is another important parameter of a comparator. In most applications it is required that following an appropriate input level change, the comparator must switch between two output levels with fast rise and fall times in the shortest amount of time.

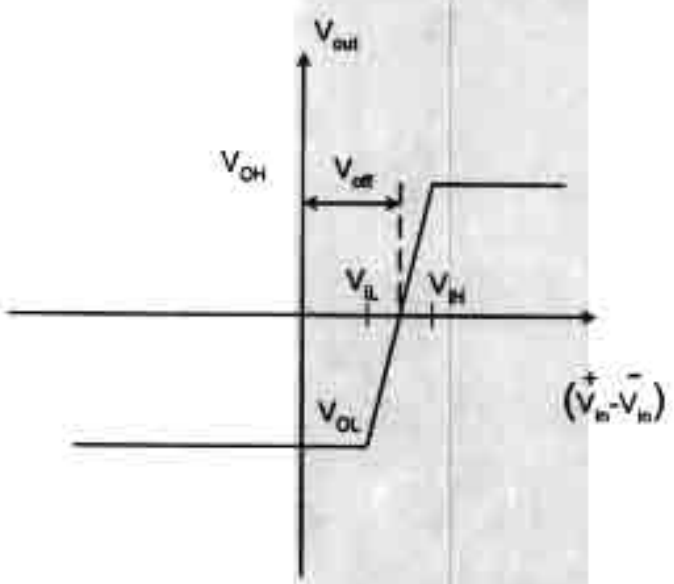



Figure 4.2 Transfer curve of comparator with finite gain and dc offset voltage

## 4.2 COMPARATOR WITH HYSTERESIS

Hysteresis is the quality of the comparator in which the input threshold or the trip voltages change as a function of the input (or output) level. In particular, when the input passes the threshold, the output changes and the input threshold is subsequently reduced so that the input must return beyond the previous threshold before the comparator output changes its state again. This can be illustrated much clearer with the diagram shown in Fig.4.3. Notice that as the input starts negative and goes positive, the output dose not change until it reaches the positive trip point, $V_{TRP+}$. Once the output

goes high, the effective trip point is changed. When the input returns in the negative direction, the output dose not switch until it reaches the negative trip point, $V_{TRP-}$.

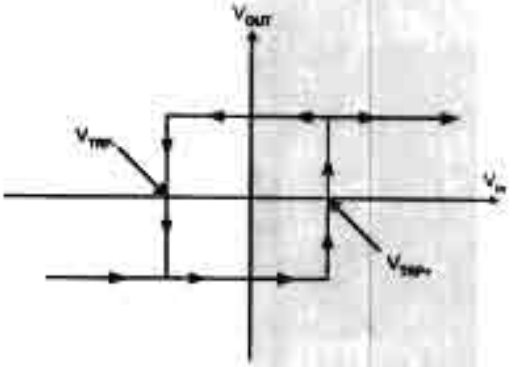



Figure 4.3 Comparator Hysteresis curve

The advantage of hysteresis in a noisy environment can be clearly seen from the illustration given in Fig.4.4. In this figure, a noise signal is shown as the input to a comparator without hysteresis. The intention is to have the comparator output follow the low-frequency signal. Because of noise variations near the threshold points, the comparator output is too noisy the response of the comparator can be improved by adding hysteresis equal to or greater than the amount of the largest expected noise amplitude. The response of such a comparator is shown in Fig.4.5.

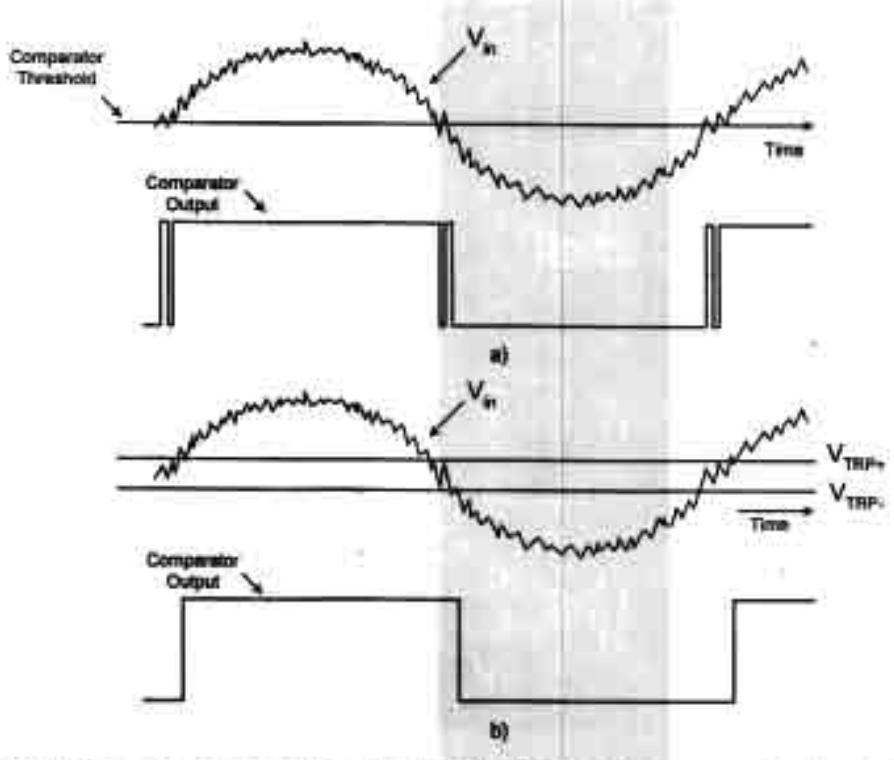



Figure.4.4 (a) Comparator response to noisy input (b) Comparator response to noisy input when hysteresis is added

### 4.2.1 CMOS HYSTERESIS COMPARATOR

There are many ways to accomplish hysteresis in a comparator. All of them involve some from of positive feedback. Referring to the differential input stage given in Fig.4.5, it is seen that there are two paths of feedback. The first is current-series feedback through the common-source node of transistors M1 and M2. This feedback path is negative. The second path is the voltage-shunt feedback through the gate-drain connections of transistors M10 and M11. This path of feedback is positive. If the positive feedback factor is less than the negative feedback factor, then the overall feedback will be negative and there is no hysteresis. If the positive feedback factor becomes greater than the negative feedback, the overall feedback will be positive, which will give rise to hysteresis in the voltage transfer curve. As long as the ratio $\beta_{10} / \beta_3$ is less than one, there is no hysteresis in the transfer function. When this ratio is greater than one, hysteresis will result. The following analysis will develop the equations for the trip points when there is hysteresis.

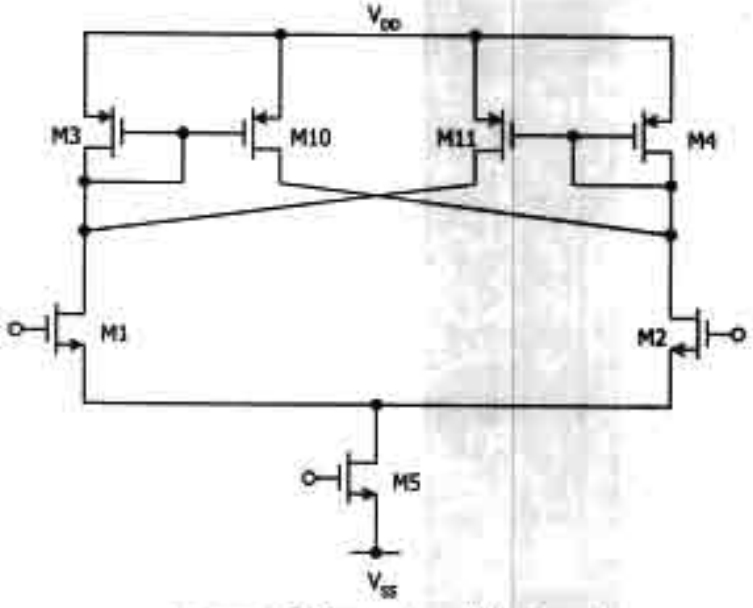
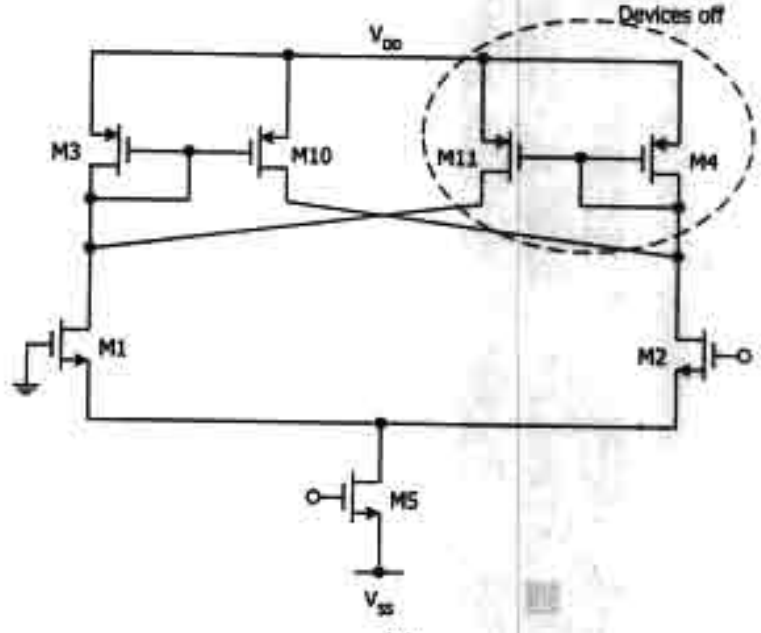


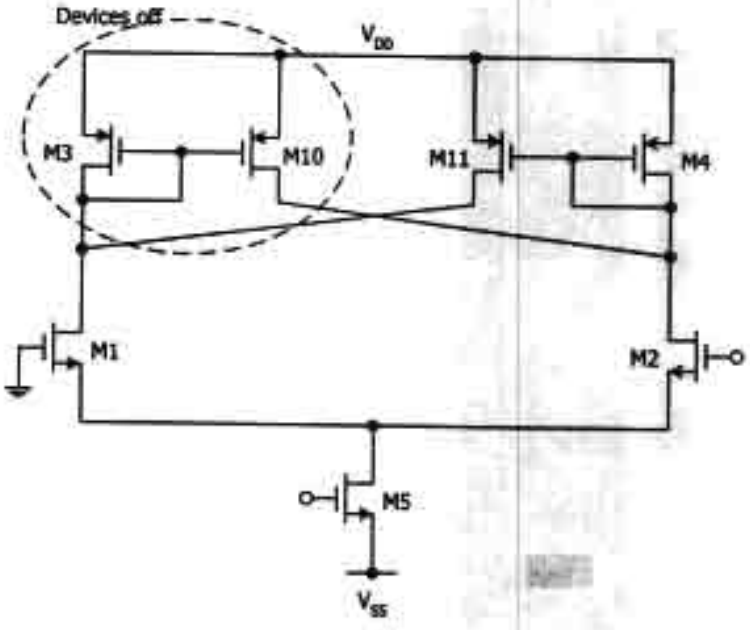

Figure 4.5 Comparator with hysteresis

It is assumed that the plus and minus supply voltages are used and the gate of M1 is tied to ground while an input voltage signal is applied to the gate of M2. With the input of M2 of much less than zero, M1 is on and M2 off, thus turning on M3 and M10 and turning off M4 and M11. All drain current of M5 flows through M1 and M3, so the voltage at the drain of M1 is logic high. The resulting circuit is shown in Fig.4.6 (a). (Notice that, M2 is shown even though it is off.) At this point, M10 is attempting to source the following amount of current.

$$i_{10} = \frac{(W/L)_{10}}{(W/L)_3} i_5 \tag{4.1}$$




(a)




(b)

Figure 4.6 (a) Comparator in a state where $V_{in}$ is vary negative and increasing toward $V_{TRP+}$ (b) Comparator in a state where $V_{in}$ is vary positive and decreasing toward $V_{TRP-}$

As $V_{in}$ increases toward the threshold point, some of the tail current beginning to flow through M2 is supplied by the current of M10. As long as M10 still can supplied current to M2, there is no state switching. Just beyond this point the comparator switches state.

To approximately calculate one of the trip points, the circuit must be analyzed right at the point where the current of M2 equals to those of M10. Mathematically this is

$$i_{10} = \frac{(W/L)_{10}}{(W/L)_3} i_3 \tag{4.2}$$

$$i_2 = i_{10} \tag{4.3}$$

$$i_5 = i_2 + i_1 \quad (i_1 = i_3) \tag{4.4}$$

$$i_3 = \frac{i_5}{1 + \left[(W/L)_{10}/(W/L)_3\right]} = i_1 \tag{4.5}$$

$$i_2 = i_5 - i_1 \tag{4.6}$$

Knowing the currents in both M1 and M2, it is easy to calculate their respective $V_{gs}$ voltage. Since the gate of M1 is at ground, the difference in their gate-source voltages will yield the positive trip point as given below

$$v_{GS1} = \left(\frac{2i_1}{\beta_1}\right)^{1/2} + V_{T1} \tag{4.7}$$

$$v_{GS2} = \left(\frac{2i_2}{\beta_2}\right)^{1/2} + V_{T2} \tag{4.8}$$

$$V_{TRP+} = v_{GS2} - v_{GS1} \tag{4.9}$$

Once the threshold is reached, the comparator changes state so that the majority of the tail current now flows through M2 and M4. As a result, M11 is also turned on thus turning off M3 and M10 and M1. As in the previous case, as the input returns negative the circuit reaches a point at which the current in M1 increases until it equals the current in M11. The input voltage at this point is the negative trip point $V_{TRP-}$. The equivalent circuit in this state is shown in Fig.4.7 (b). To calculate the trip point, the following equations will be applied.

$$i_{11} = \frac{(W/L)_{11}}{(W/L)_4} i_4 \tag{4.10}$$

$$i_1 = i_{11} \tag{4.11}$$

$$i_5 = i_2 + i_1 \tag{4.12}$$

Therefore,

$$i_4 = \frac{i_5}{1 + \left[(W/L)_{11}/(W/L)_4\right]} = i_2 \tag{4.13}$$

using (4.7) and (4.8) to calculate $V_{GS}$, the trip point is

$$V_{TRP-} = v_{GS2} - v_{GS1} \tag{4.15}$$

while these equations do not take into account the effect of channel length modulation.

The differential stage described so far is generally not useful alone, and thus requires an output stage to achieve reasonable voltage swings and output resistance. There are a number of ways to implement an output for this type of input stage. One of these is given in Fig.4.7. Differential-to-single-ended conversion is accomplished at the output and thus provides a class-AB type of driving capability.

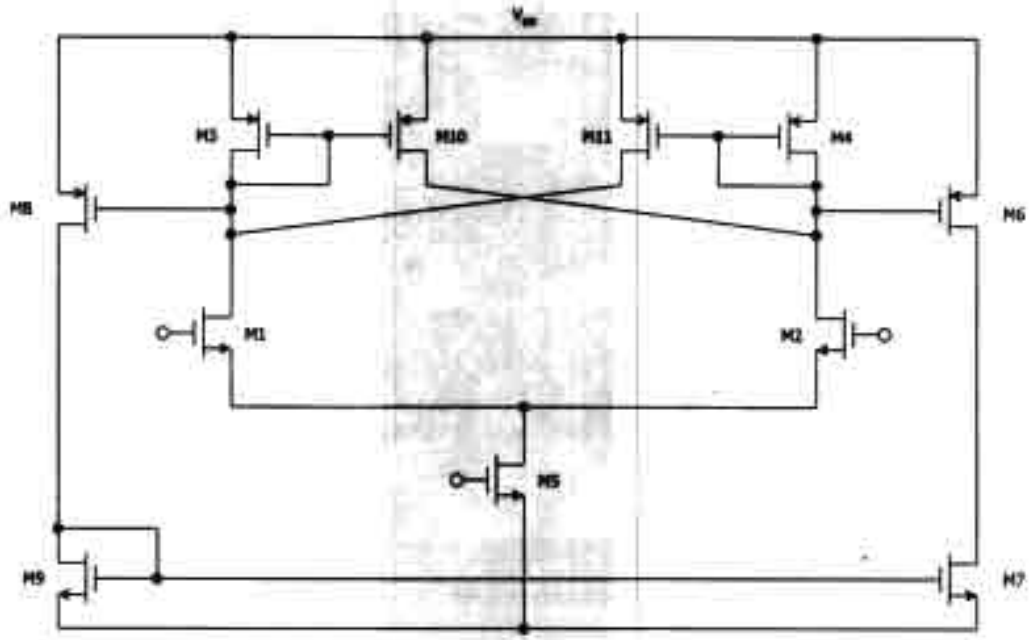



Figure 4.7 Complete schematic of a CMOS comparator with hysteresis

## 4.3 DESIGN OF HYSTERESIS TUNABLE VOLTAGE COMPARATOR

Regarding to the mentioned hysteresis mechanism, a simple hysteresis tunable analog comparator can be designed and shown in Fig.4.8 where M3 and M4 are replaced by the FGMOSs. The hysteresis involves a positive feedback produced by M10 and M11. The positive feedback occurs only when the current ratio of $I_{10}/I_3$ is greater than one. If the ratio is higher, the amount of the feedback current will also increase and result in a wider of the positive and negative trip point voltage, $V_{TRP+}$ and $V_{TRP-}$. Hence the hysteresis can be controlled. However, the $V_{TRP+}$ and $V_{TRP-}$ can be developed from the condition that $I_2$ equals to $I_{10}$ and $I_1$ equals to $I_{11}$, correspondingly.

$$V_{TRP+} = \sqrt{\frac{2I_3}{\beta_1}}\left(\frac{\sqrt{I_{10}/I_3}-1}{\sqrt{1+I_{10}/I_3}}\right)$$
$$V_{TRP-} = \sqrt{\frac{2I_3}{\beta_1}}\left(\frac{\sqrt{I_{11}/I_4}-1}{\sqrt{1+I_{11}/I_4}}\right) \qquad (4.16)$$

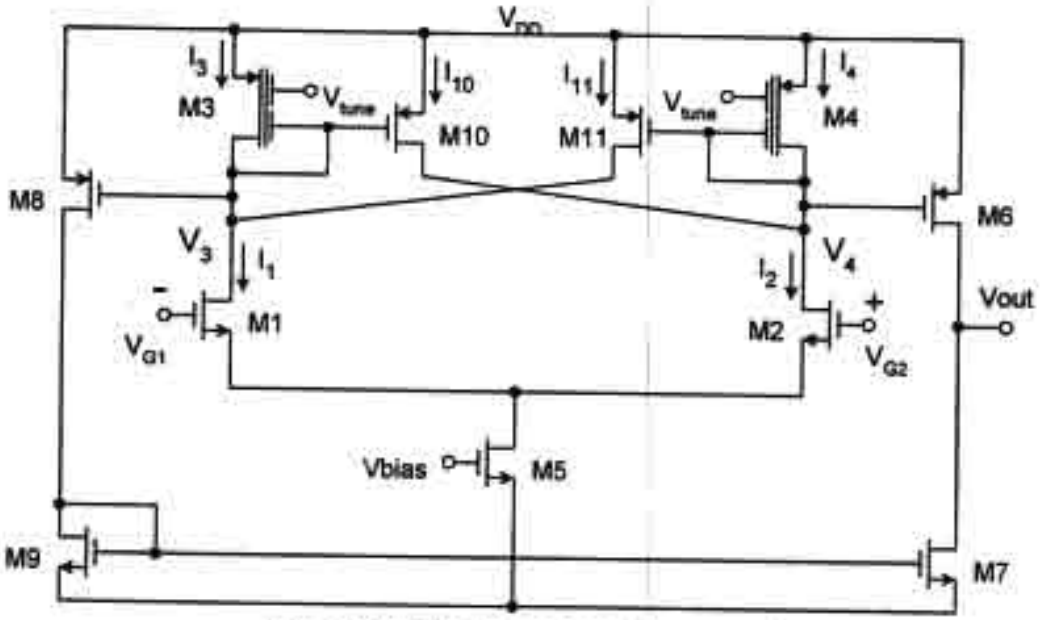



Figure 4.8 Hysteresis tunable analog comparator

Thus, by the virtue of the FGMOS, the ratio of $I_{D10}/I_{D3}$ and $I_{D11}/I_{D4}$ can be tuned electronically by $V_{tune}$ at the input gate of M3 and M4. Hence $V_{TRP+}$ and $V_{TRP-}$ can be tuned orthogonally. If the tuning voltage at the input gates of M3 and M4 are different. M3 and M4 are designed with an equal area of $G_1$ and $G_2$ as $10.8\times22.8\mu m^2$ while the floating-gate area is set to $13.2\text{x}2.4\ \mu m^2$, which also equal to those of M10 and M11.

## 4.4 SIMULATION RESULTS OF HYSTERESIS TUNABLE ANALOG VOLTAGE COMPARATOR

The circuit has been simulated on Hspice with an assistance of the FGMOS macro model in [22] and supply voltage is set to 5.0V. Fig.4.9 shows $V_{TRP+}$ and $V_{TRP-}$ vs. $V_{tune}$ varied in the range of 2.5-5.0V.

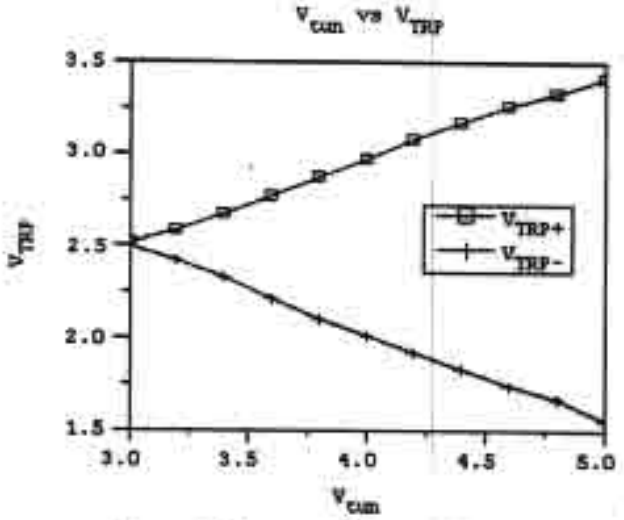



Figure 4.9 $V_{TRP+}$ and $V_{TRP-}$ vs. $V_{tune}$

A DC transfer curve of the hysteresis tunable comparator is also shown in Fig.4.10 where the input gates G1 and G2 are tied together and connected to the tuning voltages, $V_{tun}$. Fig.4.10 shows the input-output DC transfer curve with the hysteresis. $V_{tun}$ are varied in the range of 2.5-5.0V which correspond to $V_{TRP+}$ in the range of 2.5~3.4V and $V_{TRP-}$ in the range of 2.5V down to 1.6V.

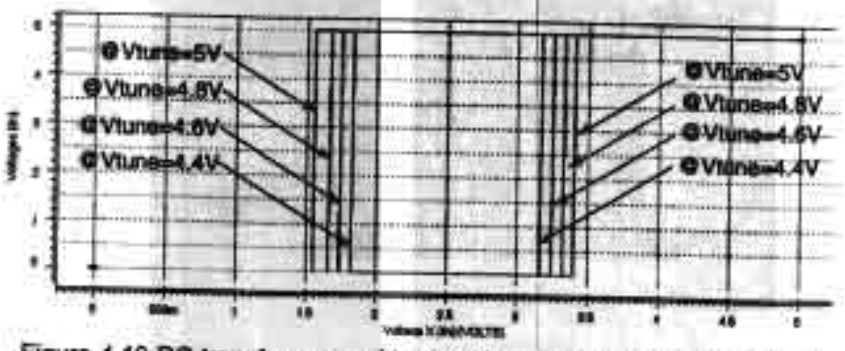



Figure 4.10 DC transfer curve of hysteresis tunable voltage comparator

Time-domain simulation is also performed to express the performance of the comparator in a noisy environment. The circuit is tested with a noise-modulated signal with the noise amplitude set to $0.4V_{peak}$ while $V_{tune}$ is set to 3.8V. Simulation results are shown in comparison with those from a non-hysteresis comparator in Fig.4.11.

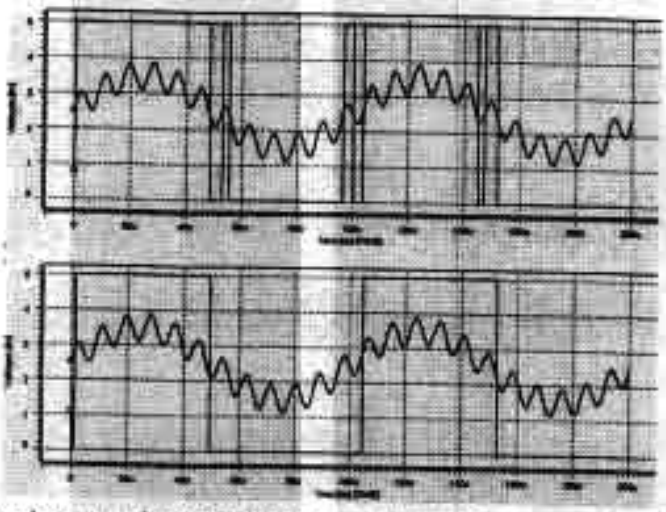


Figure 4.11 Time-domain comparisons between a non-hysteresis comparator and hysteresis tunable voltage comparator

From Fig.4.8, it could also be noted that the terminal G1 of both M3 and M4 are not necessarily connected to the same voltage, $V_{tun}$. With the different voltages at both inputs, $V_{TRP+}$ and $V_{TRP-}$ are asymmetrically tuned. Hence, $V_{TRP+}$ and $V_{TRP-}$ can be tuned orthogonally. If G1 of M3 and M4 are connected to $V_{tun1}$ and $V_{tun2}$ respectively, the simulation results are shown in Fig.4.12 and Fig.4.13 where $V_{TRP+}$=3.3V and $V_{TRP-}$=2.2V are set by $V_{tun1}$=4.6V and $V_{tun2}$=3.6V.

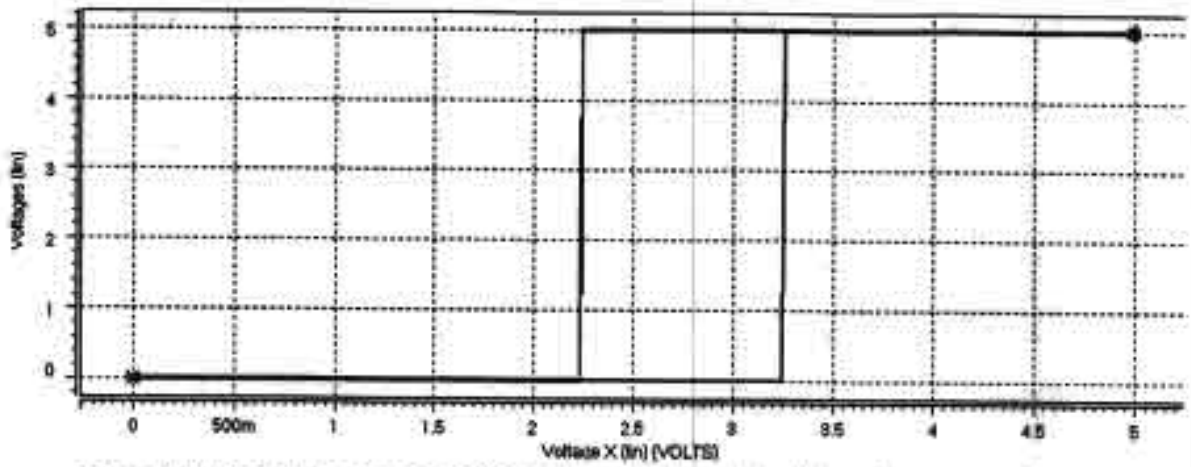



Figure 4.12 DC transfer curve of orthogonal tune hysteresis tunable voltage comparator

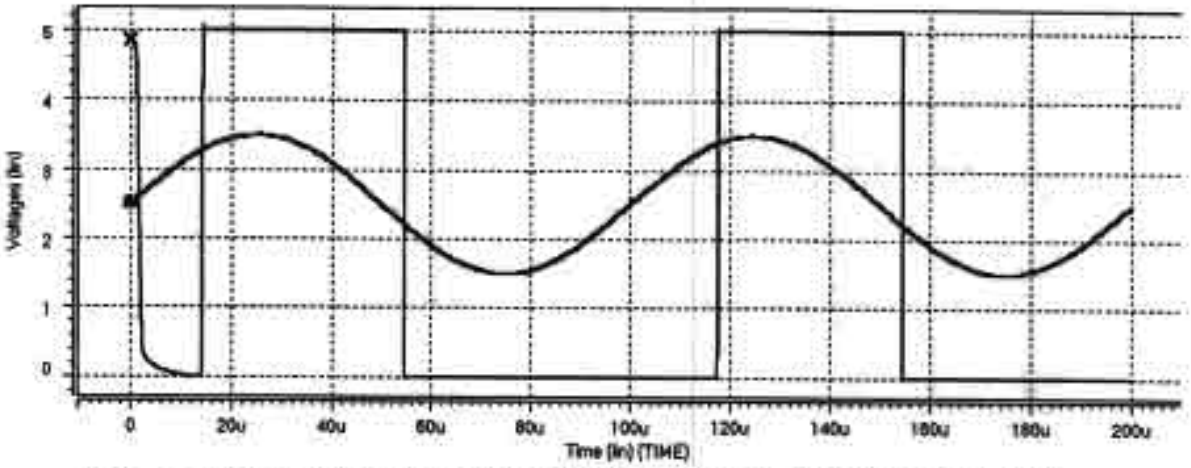



Figure 4.13 Transient analysis of orthogonal tune hysteresis tunable voltage comparator

An experiment of the back-gate tuning of M3 and M4 has also been investigated with a result in Fig.4.14 showing that the range of $V_{TRP+}$ and $V_{TRP-}$ are not as wide as those offered by the circuit employing FGMOS. Also, the back-gate biasing always experiences an amount of leakage current because the bulk terminal is not fully isolated as in the case of poly1 and poly2 gates.

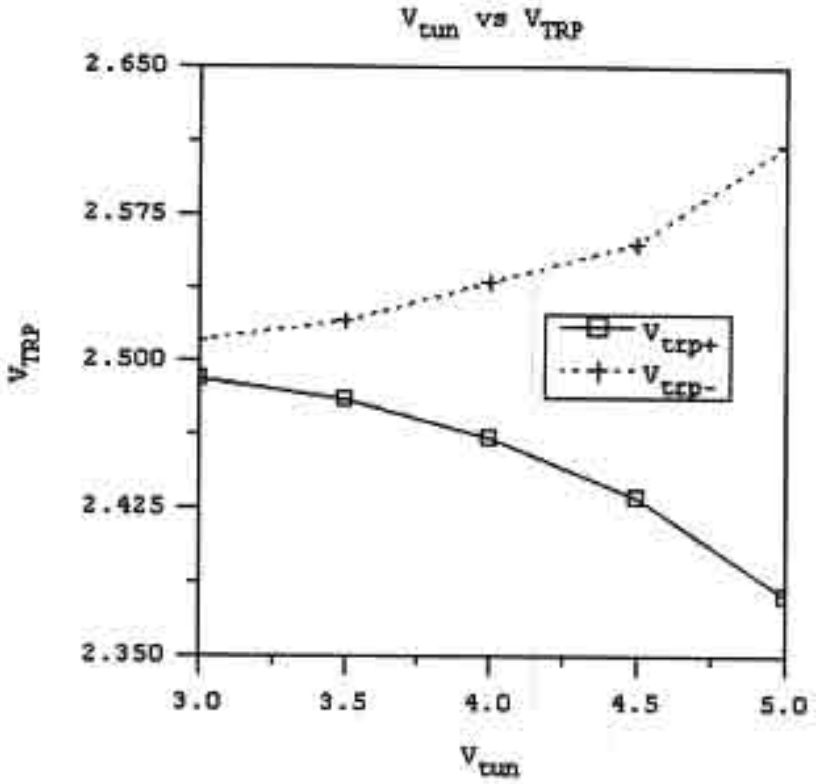



Figure 4.14 $V_{TRP+}$ and $V_{TRP-}$ vs. $V_{tune}$ at the back gate of M3 and M4

A Hysteresis Tunable Voltage Comparator using FGMOS is already proposed. The circuit is essentially exploiting FGMOS devices in the positive feedback scheme to create the hysteresis. Based on the tunability of the FGMOS, the current ratio of $I_{D10}/I_{D3}$ and $I_{D11}/I_{D4}$ corresponding to the amount of feedback current is used to tune the hysteresis effectively. An experiment of the back-gate tuning of M3 and M4 has also been investigated with a result showing that the range of $V_{TRP+}$ and $V_{TRP-}$ are not as wide as those offered by the circuit employing FGMOS. Also, the back-gate biasing always experiences an amount of leakage current because the bulk terminal is not fully isolated as in the case of poly1 and poly2 gates. The proposed idea is implementable on any standard double-poly CMOS processes. The work has been performed on AMI 1.2μm CMOS process available through MOSIS. All the simulation results confirm well the functionality. Performance optimizing will be placed as future works.

# 5. DIGITAL FGMOS COMPARATOR

Designs of digital comparators are presented in this section. The main idea is to exploit the well-known characteristics of the floating-gate MOSFET onto an opamp based voltage comparator. The threshold voltage operation of the floating-gate MOSFET is exploited to achieve a hysteresis tunable analog voltage comparator of which the positive feedback factor is tunable. Based on the analog comparator circuit, a digital comparator is realized with replacement of the floating-gate MOSFETs for the input devices of which the drain currents as a linear sum of the weighted multiple-input voltages is exploited. Basically the internal mechanisms of both proposed comparators are analog functions. Designs and simulation results on Hspice on 1.2μm AMI CMOS are given to demonstrate the functionalities.

## 5.1 4-BIT DIGITAL COMPARATOR

A 4 bits digital comparators are presented in this section. Based on the same opamp based comparator as in the analog case, the new comparator can also be realized by employing the floating-gate MOSFETs as the input devices. The 4-bits digital comparators are proposed separately as non-hysteresis and hysteresis types. Both circuits are utilized further for designing an 8-bits digital comparator that will be discussed in the next section. Input of 4-bits comparators are using 5-inputs FGMOS, 4 input gates are used for 4-bits digital input and another for biasing. From (3.5) and (3.6), drain current equations of multiple input floating gate MOSFET, can be rearranged to (5.1) and (5.2) for 5-inputs FGMOS as shown below.

$$I_d = \frac{1}{2}\mu C_{ox}\frac{W}{L}\left[\sum_{i=1}^{4}\left(w_i V_{Gi} - V_S\right) - \left(V_{TH} - w_5 V_{G5}\right)\right]^2 \qquad (5.1)$$

$$I_d = \frac{1}{2}\mu C_{ox}\frac{W}{L}\left[\left(w_1 V_{G1} + \ldots + w_5 V_{G5}\right) - V_S - V_{TH}\right]^2 \qquad (5.2)$$

The drain current is essentially a linear sum of all inputs weighted by the capacitive coupling ratios. Equation (5.2) is written to show a linear sum of the weighted multiple-input voltages. This equation is used to design all comparators in this section.

### 5.1.1 NON-HYSTERESIS 4-BITS DIGITAL COMPARATOR

The non-hysteresis digital comparator is shown in Fig.5.1. It is seen that FGMOSs are employed as the input devices in order to exploit the drain current, which is written in (5.2) as a linear sum of the weighted multiple-input voltages of the binary

bits. Then the circuit is digital at the input and output but it internally works as an analog circuit.

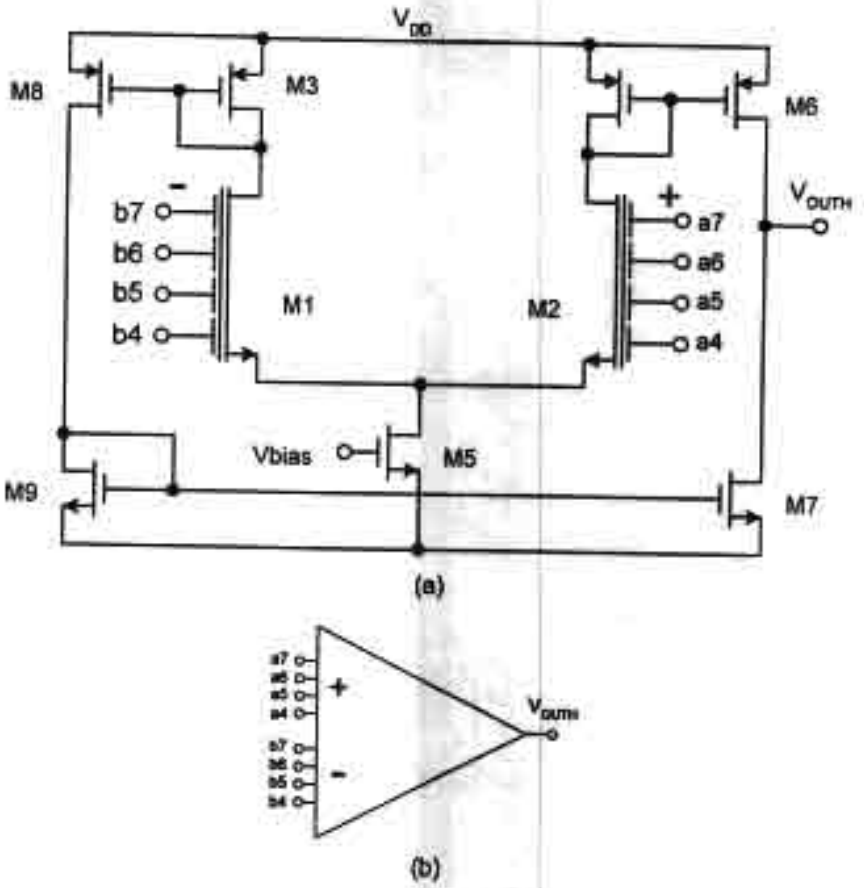



Figure 5.1 Non-hysteresis 4-bits Digital Comparator (a) schematic (b) symbol

From Fig.5.1 (a), the FGMOS $M_1$ and $M_2$ are designed with the floating-gate area of $12\times3\mu m^2$. Let $k_4,...,k_7$ are the weights of the input gates denoted as a4,..,a7 and b4,...,b7 respectively, where a4 and b4 are the least significant bit of this comparator. The inputs gates have the sizes set by the binary weights as in Table 5.1.

Table 5.1 Design parameters of the FGMOS

| | k4 | k5 | k6 | k7 |
|---|---|---|---|---|
| Binary weights | 1/16 | 1/8 | ¼ | 1/2 |
| Sizes($\mu m^2$) | 10.8×22.8 | 21.6×22.8 | 43.2×22.8 | 86.4×22.8 |
| Capacitance(fF) | 159.7 | 319.5 | 638.9 | 1277.8 |

This non-hysteresis 4-bits comparator can be represented as a symbol in Fig.5.1(b). The circuit delivers three levels of the output signal such as logic High or $V_{dd}$ when the total weighted sum of the binary inputs at the positive terminal is higher than that of the negative terminal. The output signal is logic Low or GND when the total weighted sum of the binary inputs at the positive terminal is lower than that of the negative terminal. The output is $V_{dd}/2$ when the total weighted sums of the binary inputs of both terminals are equal. This particular function implies an ability to detect the equality of the binary inputs. The functionalities are confirmed by the simulation results in Fig.5.2.

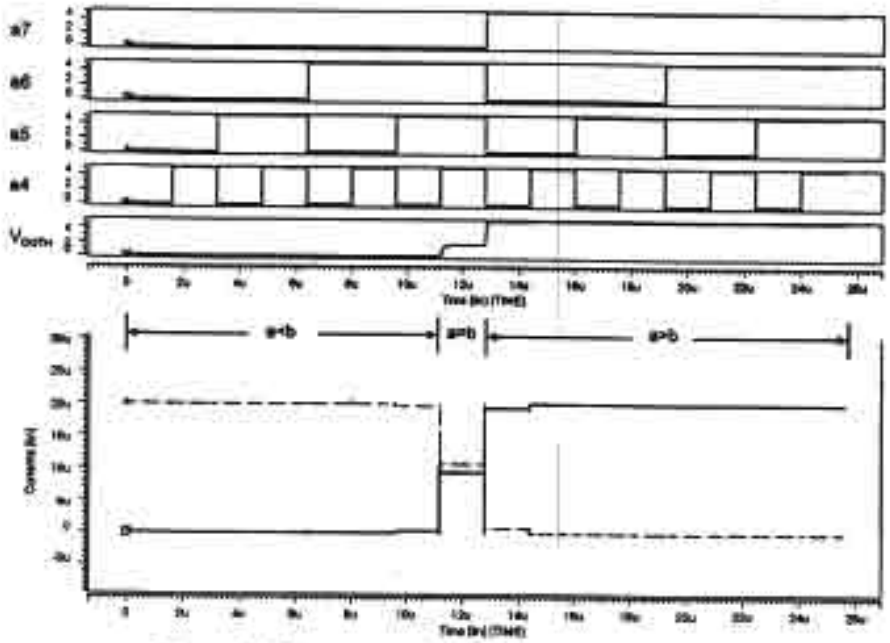



Figure 5.2 Simulation results of the non-hysteresis

Fig.5.2 shows output signal as $V_{OUTH}$ and drain currents of the input devices where the binary a7-a4 are swept digitally and the binary b7-b4 are set to #b0111. It is seen that the output voltage is at $V_{dd}/2$ and the input drain currents are equal when the binary a7-a4 equals to b7-b4. This property will also be utilized further in the design of the 8-bits comparator.

### 5.1.2 4-BIT HYSTERESIS COMPARATOR

The hysteresis comparator is shown in Fig.5.3 (a), which is similar to Fig.5.1(a) except that the hysteresis tuning part used in the analog comparator is employed. Because of the hysteresis operation, this circuit delivers only two levels of the output signal at high or low. As a result of the hysteresis tuning, the output signal is delivered according to the arithmetic functions of A>B or A≥B that are selected by $V_{tune}$. Based on the same dimensions of all MOSFETs in Fig.5.1(a) and M3, M4 are set to

$15\times2.4\mu m^2$ and the two input gates are set to $77\times31\mu m^2$ for the signal input gate and $11\times31\mu m^2$ for $V_{tune}$. The simulation results are shown in Fig.5.4.

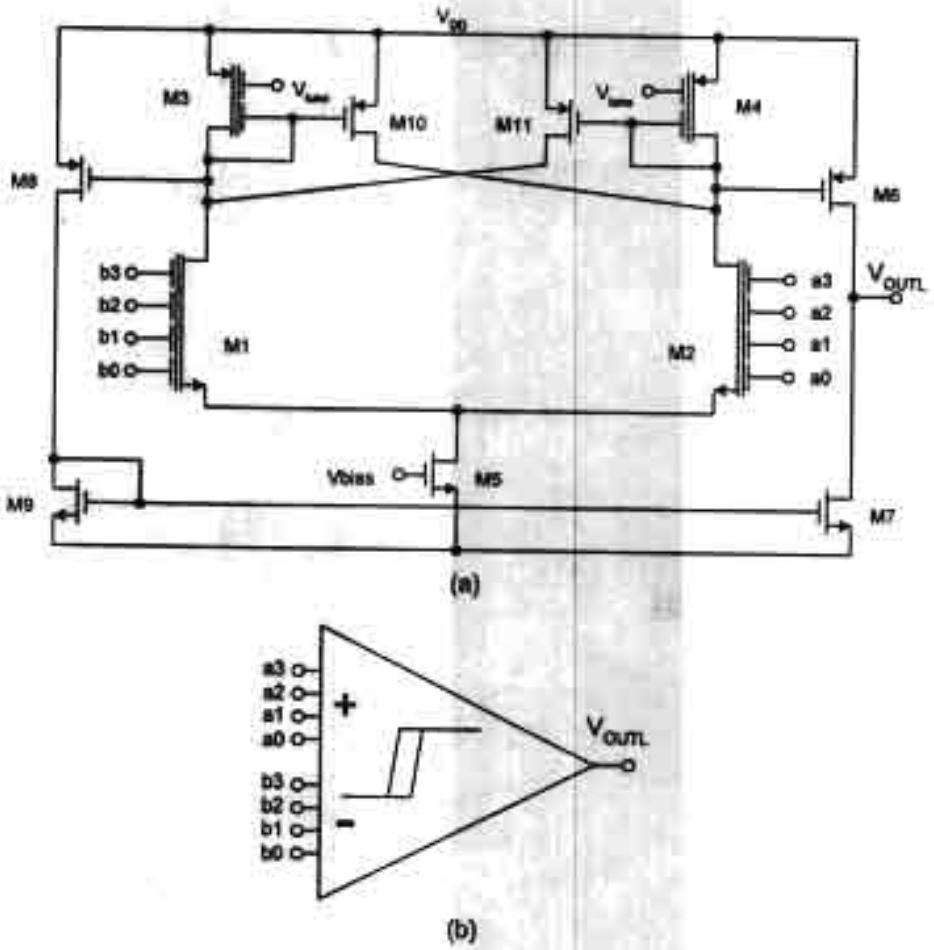



Figure 5.3 Hysteresis 4-bits Digital Comparator a) schematic b) symbol

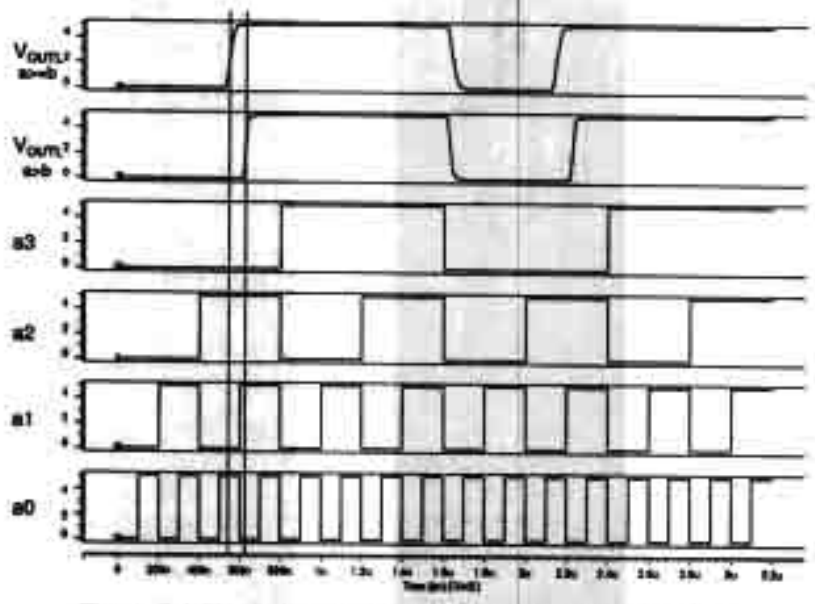



Figure 5.4 Simulation results of the hysteresis comparator

From Fig.5.4, the binary b3-b0 are set to #b0101 while the binary a3-a0 are swept digitally. It is seen that if $V_{tune}$ is set to High, the output signal changes its stage when both binary sets are equal. The circuit performs the function A≥B. If $V_{tune}$ is set to Low, the comparator will perform the function A>B. In the next section, both hysteresis and non-hysteresis digital comparator will be utilized for the design of 8 bits digital comparator.

## 5.2 8-BITS DIGITAL COMPARATOR

An 8-bits digital comparator is realized by using those two 4-bits comparators described in section 5.1 and another two input voltage comparator as shown in Fig.5.5.

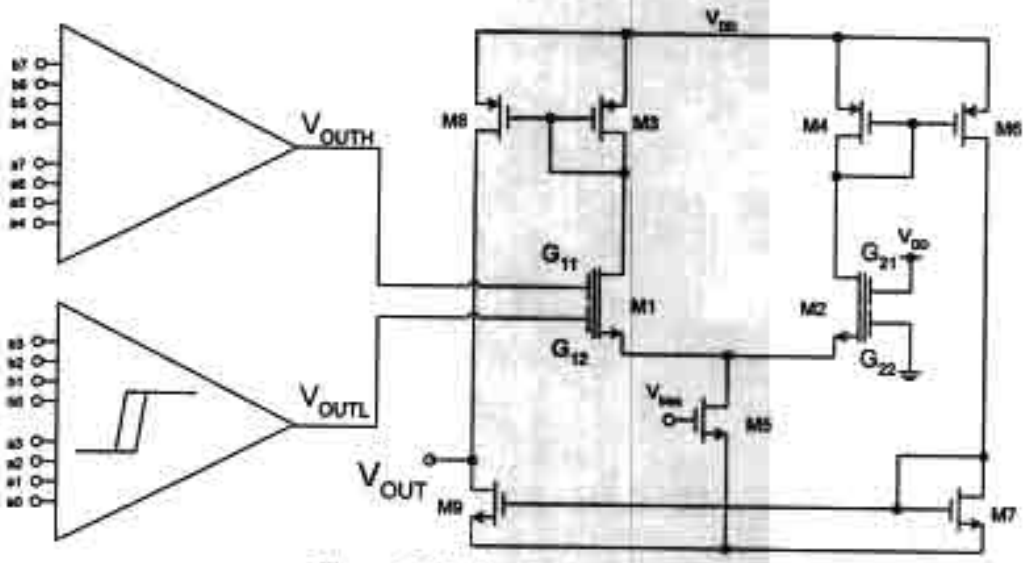



Figure 5.5 8-bits digital comparator

From Fig.5.5, it is seen that the 4-bits non-hysteresis comparators is used to compare the upper 4-bits where the three levels of output voltage at $V_{OUTH}$ are delivered out when A>B, A<B and A=B. The 4-bits hysteresis comparator is used for the comparison of the lower 4-bits where only two levels of output voltage at $V_{OUTL}$ are delivered. The third comparator is used as the main comparator, of which the referenced input is connected to $V_{dd}$ and GND. The functions of the main comparator are concluded in Table 5.2.

Table 5.2 Functions of the main comparator

| Upper 4 bits output | Lower 4 bits output | Output |
|---|---|---|
| High / $V_{dd}$ | X | High / $V_{dd}$ |
| Equal / $V_{dd}/2$ | High / $V_{dd}$ | High / $V_{dd}$ |
| Equal / $V_{dd}/2$ | Low / GND | Low / GND |
| Low / GND | X | Low / GND |

where X denotes don't care condition. It is seen that when the upper 4-bits inputs of A are higher or lower than those of B, the output is High or Low right away. If the upper 4-bits inputs of A are equal to those of B, the output will correspond to the comparison of the lower 4-bits of A and B. However, in order to have the functions correspond to Table 5.2, the main comparator must have the four input gates such as $G_{11}$, $G_{12}$, $G_{21}$, $G_{22}$ be designed with proper sizes. The weights of each input are denoted as $k_{11}$, $k_{12}$, $k_{21}$, $k_{22}$, correspondingly, which are considered as in Table 5.3.

Table 5.3 Sizing criteria for the main comparator

| Inputs | | Output | Weight sum operations |
|---|---|---|---|
| $V_{OUTH}$ | $V_{OUTL}$ | $V_{OUT}$ | |
| 5V | X | 5V | $k_{11}\times5+ k_{12}\times0 > k_{21}\times5+ k_{22}\times0$<br>$\therefore k_{11} > k_{21}$ |
| 0 | X | 0 | $k_{11}\times0+ k_{12}\times5 < k_{21}\times5+ k_{22}\times0$<br>$\therefore k_{12} < k_{21}$ |
| 2.5V | 0 | 0 | $k_{11}\times2.5+ k_{12}\times0 < k_{21}\times5+ k_{22}\times0$<br>$\therefore k_{11} < 2\cdot k_{21}$ |
| 2.5V | 5V | 5V | $k_{11}\times2.5+ k_{12}\times5 > k_{21}\times5+ k_{22}\times0$<br>$\therefore k_{11}+ 2\cdot k_{12} > k_{21}$ |

where 5V and 0 stands for the logic High and Low and X denotes the don't care condition. Examining the weight sum operations, we can conclude that all weights must conform to the condition that $k_{21} < k_{11} < 2k_{21} < k_{11}+2k_{12}$. So, the weights and sizes of the input gate capacitances are designed and calculated as in Table 5.4.

Table 5.4 Design parameters of $G_{11}$, $G_{12}$, $G_{21}$, $G_{22}$

| | $G_{11}$ | $G_{12}$ | $G_{21}$ | $G_{22}$ |
|---|---|---|---|---|
| Binary weights | 12/16 | 4/16 | 7/16 | 9/16 |
| Sizes($\mu m^2$) | 129.6×22.8 | 43.2×22.8 | 75.6×22.8 | 97.2×22.8 |
| Capacitance (fF) | 1916.4 | 638.8 | 1117.9 | 1437.3 |

Then the functionalities can be demonstrated by the simulation results in Fig.5.6.

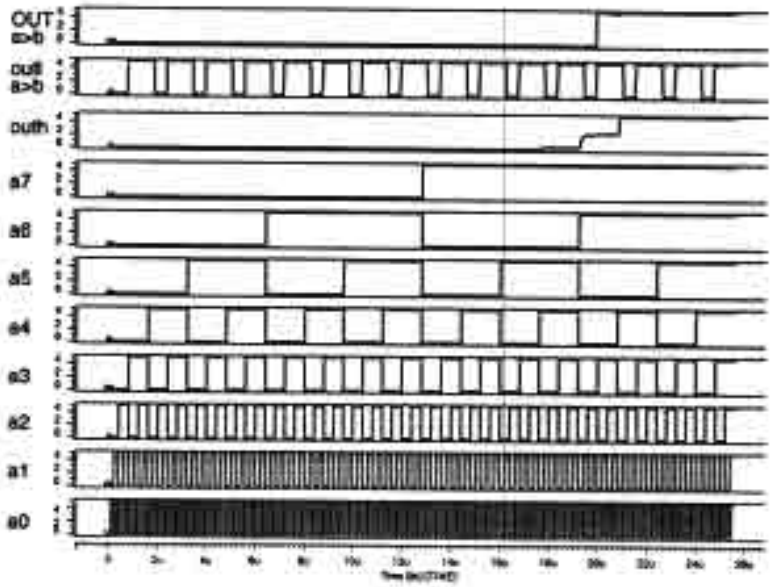



Figure 5.6 Simulation results of the 8-bits comparator

In Fig.5.6, the binary B is set to #b11000110 while the binary A is swept digitally from 0. It is seen that the $V_{OUTH}$ of the upper comparator contributes $V_{dd}/2$ when the binary A=B, and then the output corresponds to the $V_{OUTL}$ of the lower comparator.

This section presents a design of a non-clocked 8-bits digital comparator that essentially manipulates the proposed analog voltage comparator to realize the new digital circuit in which the signal is internally processed in an analogue fashion. The proposed idea can be implemented on any standard double-poly CMOS and be useful to mixed signal and computational applications. All the simulation results confirm well the functionality.

# 6. FGMOS COMPARATOR ON CLASS-D POWER AMPLIFIER

Most audio power amplifiers are designed in Class-A or class-AB, which normally delivers a limited efficiency because their power transistors operate in the linear area that consumes a huge biasing current, and then result in power dissipation or heat. In order to improve the efficiency, switching converters such as the Pulse Width Modulation (PWM) can be applied to an audio amplifier, which is then referred as switching amplifiers or class-D amplifiers [35, 36]. This type of amplifiers presents several advantages over the conventional class-A or AB amplifiers in their high efficiency and low internal power dissipation. However, this section presents the development of another type of the class-D amplifier based on the RWDM technique [37]. The circuit is designed for applications of battery-operated-devices such as output drives in mobile speakerphones, hearing-aid devices and implantable medical devices. The design also incorporates with a multiple input hysteresis comparator using floating-gate MOSFETs, which gave more computational ability than any other comparators that will discussed in detail.

## 6.1 CLASS-D AMPLIFIER

Conventionally, most class-D amplifiers are based on the Pulse Width Modulation (PWM) technique where the pulse width of the output PWM signal is made proportional to the amplitude of the modulating signal between the audio input signal and the triangular signal. The signal at the output is recovered from PWM signal by passing it through a low pass filter, which could be formed by a resistor and inductor circuit inherently obtained from earphones or speakers. Fig.6.1 shows basic building blocks of a conventional class D amplifier such as 1) triangular waveform generator 2) comparator and 3) output stage.

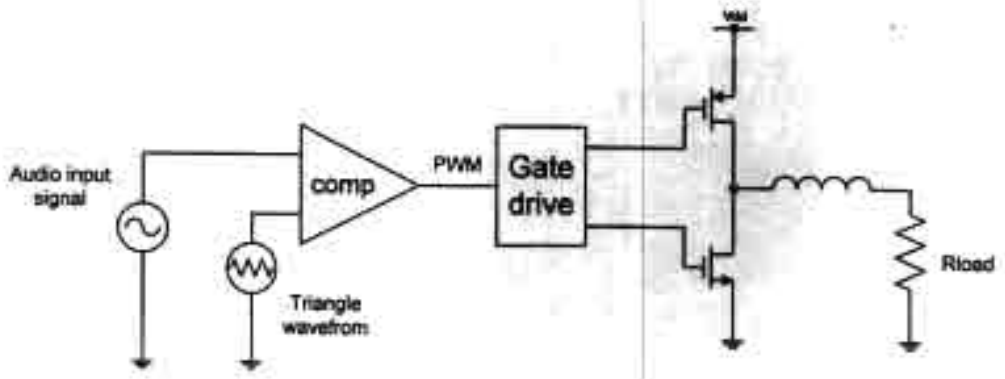



Figure 6.1 Conventional PWM class-D amplifier

From Fig.6.1, the comparator compares the audio signal input with the triangular waveform from the waveform generator to produce a PWM signal, which is then used to control the switching timing of the output stage transistors to drive a low impedance load. The output power is delivered to the load by mean of the average output current controlled by the duty cycle of the PWM signal. The duty cycle is 50% when there is no signal at the input, thus the average output voltage is zero. The PWM class-D amplifiers can dissipate less power by properly arranging the switching timing of the output power MOSFETs between two lowest-dissipation modes such as fully on and fully off. In an actual amplifier, the efficiency of 98% could be obtained [38].

RWDM principle is also another technique used in class-D amplifier and shown in Fig.6.2. The concept of RWDM is mostly like PWM, except that the input signal $V_R(t)$ is compared with the feedback signal $V_e(t)$ in the negative feedback loop. The feedback signal $V_e(t)$ is essentially the integration signal of RWDM by a low-pass filter. Since there is a hysteresis in the comparator, $V_e(t)$ can track the amplitude of $V_R(t)$ within the $\pm\Delta V$ boundary as can be shown in Fig.6.2.

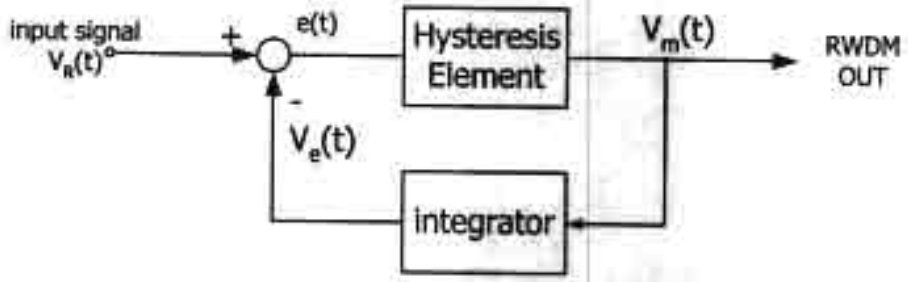



Figure 6.2 Block diagram of RWDM technique

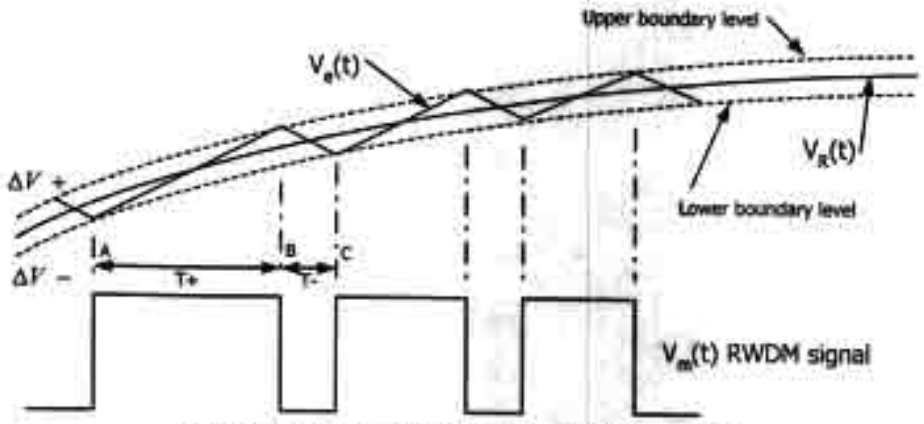



Figure 6.3 Signaling of RWDM technique in Fig.6.2

Based on the RWDM mechanism in Fig.6.2, the switching frequency of the RWDM output signal can be calculated as in (6.1).

$$f = \frac{1}{T} = \frac{S_C}{4\Delta V}\left[1 - \left(\frac{S_R(t)}{S_C}\right)^2\right] \tag{6.1}$$

where $S_R$ and $S_C$ denote the slope of the input signal $V_R(t)$ and the feedback signal $V_e(t)$ correspondingly and $\Delta V$ is the magnitude of the hysteresis loop which is controlled directly by the trip voltage of the hysteresis comparator. $S_C$ is also controlled by the time constant of the integrator in the feedback path. An example of a simulated RWDM signal of a sinusoid signal can be shown in Fig.6.3.

## 6.2 THE PROPOSED RWDM CLASS-D AMPLIFIER

A new proposed class-D amplifier based on RWDM technique is presented as a block diagram in Fig.6.4, which is seen that the amplifier comprises only a hysteresis comparator, driving circuits and an integrator formed by an RL low-pass network. The circuit can be integrated onto a monolithic chip except the inductor and the load resistor.

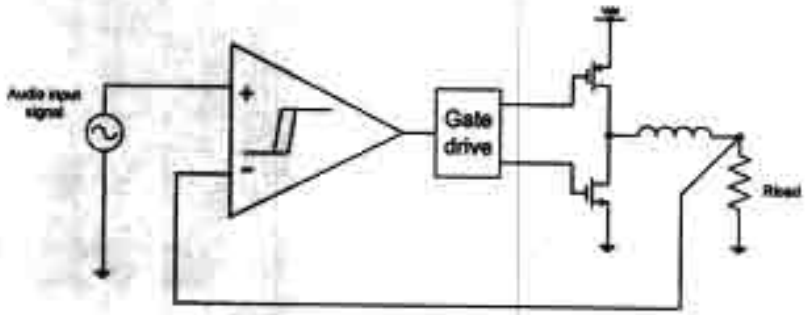



Figure 6.4 Proposed Class-D audio amplifier

From Fig.6.4 the audio input signal is directly connected to the input gate of the comparator, which is basically a high impedance node. The comparator then compares the input signal with the feedback signal from the output, which is initially zero. With the hysteresis loop, the comparator can delivers an RWDM signal comprising only logic low or high that is then integrated by the inductor resistor network. The feedback signal is a saw-tooth-like signal used to compare with input signal in the next cycle. All circuit blocks of the proposed amplifier such as comparator, driving circuit and the low-pass filter will be described in the detail in the following sections.

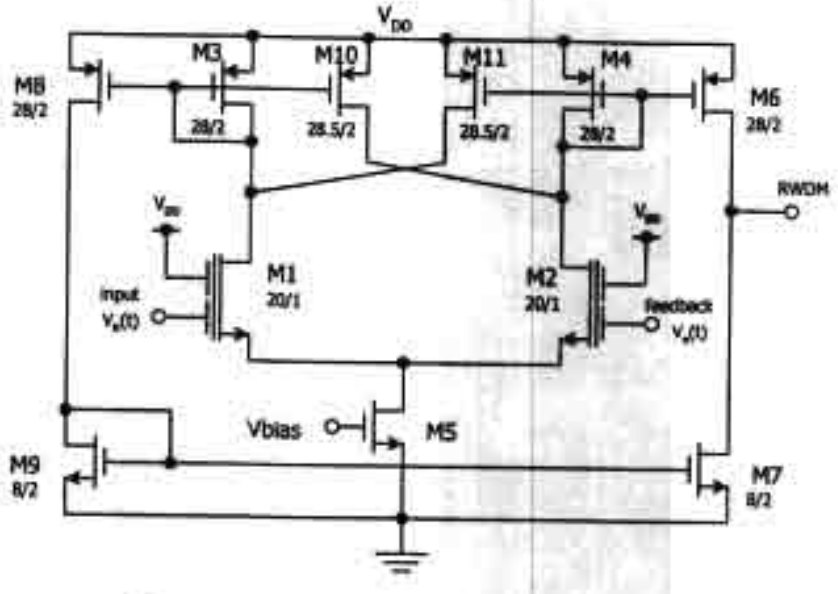



Figure 6.5 Rail to rail input Hysteresis comparator

The hysteresis comparator shown in Fig.6.5 is a schematic of the comparator in Fig.6.4. This circuit is capable to receive a wide-range input signal. The particular capability is achieved by the employment of two-inputs FGMOS as the input transistor M1 and M2. This characteristic allows the feedback signal at the gate of M2 to track the amplitude of the input signal at the gate of M1 effectively between the supply voltage and ground. Both two-inputs n-type FGMOSs are identical and also have equal size of the input gates. With one of the input gates connected to Vdd, the FGMOSs are ensured to be turned on at all level of the input signal. In other words, the comparator possesses the rail-to-rail characteristic.

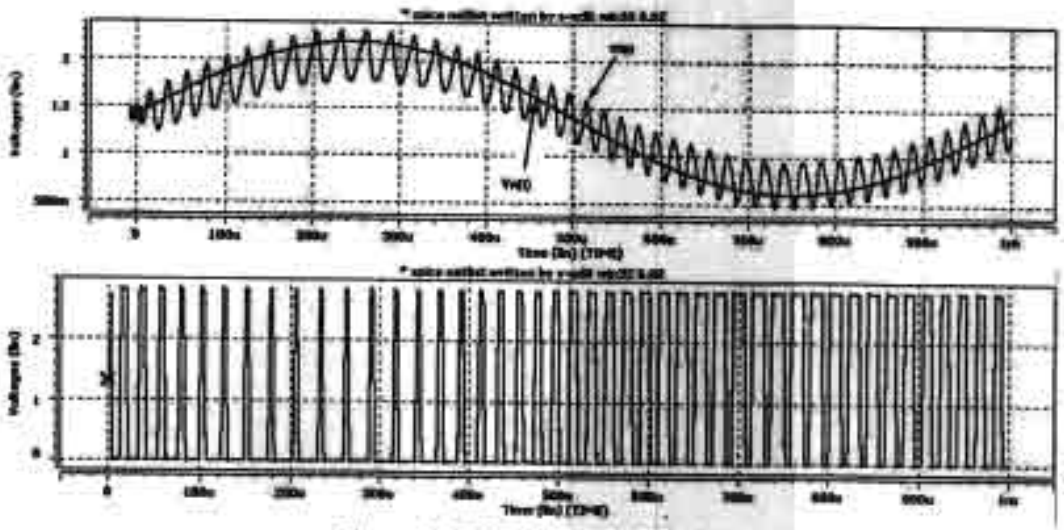


Figure 6.6 RWDM signal of Fig.6.4

All the signal of the proposed circuit are shown in Fig.6.6 that the pure sinusoid is the input that compares with the "saw-tooth-like" signal from the output to generate the PWM signal shown in the lower of the figure.

## 6.3 THE PROPOSED RWDM BTL CLASS-D

A Bridge Tied Load (BTL) class-D amplifier based on the RWDM technique is presented in Fig.6.7. It is basically a fully differential version of the proposed RWDM concept shown in Fig.6.4. With the BTL configuration the output voltage swing can be double those of the half-bridge configuration in Fig.6.4. The audio input signal is directly connected to the input of the comparator, which is normally in the range of 0~$V_{DD}$ so we use 3-inputs floating-gate MOSFETs as the input differential pairs of the hysteresis comparator.

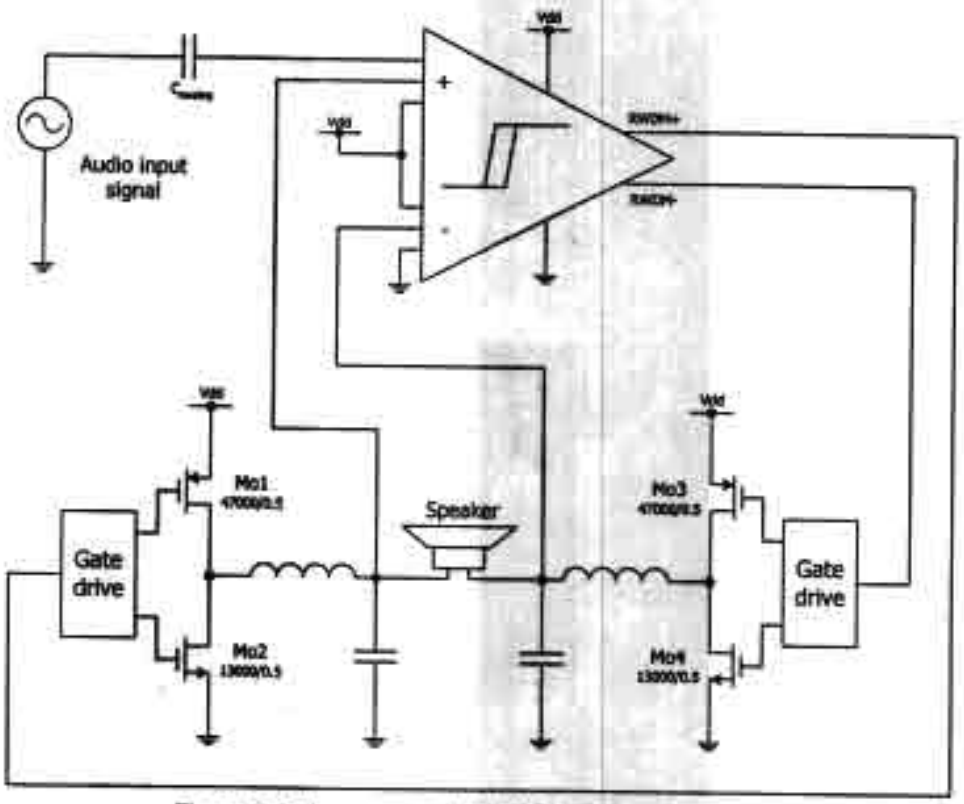



Figure 6.7 The proposed RWDM BTL class-D amplifier

In Fig.6.8, the 6-inputs fully differential hysteresis comparator comprises three-input gates FGMOS devices as the differential pairs of which the coupling capacitors are designed as $C_1$=200fF, $C_2$=128fF and $C_3$=64fF which correspond to the capacitive coupling ratios of k1, k2 and k3 to 0.5, 0.32 and 0.16 respectively. The first inputs of both plus and minus terminals having the weight factor of 0.5 are connected to $V_{DD}$ to bias the differential pairs. This results in a DC potential of 0.5$V_{DD}$ at the floating-gate on Poly1 of the differential pairs. The 2$^{nd}$ input gates having weight of 0.32 are used as the

inputs of the comparator while the 2nd gate of M1 is connected to the AC-coupled audio input signal and the 2nd gate of M2 is connected to Gnd. The weights of the 2nd inputs allow a wide input swing for the comparator. The 3rd input gates with the weight of 0.16 are connected to output nodes of the amplifier respectively. They are designed with half of the weight factor of the 2nd gates in order to make the close loop gain of the amplifier equal to 2, which is the requirement to have an output signal swing of +/- 2.8V while the input signal swing is only in the range 0~2.8V. The other advantage of this fully differential comparator is that the RWDM output signals from the comparator are exactly out of phase without any delay. The control of the power MOSFETs of both sides of the loads will be very precise. Dimensions of all MOSFETs are also shown in the figure.

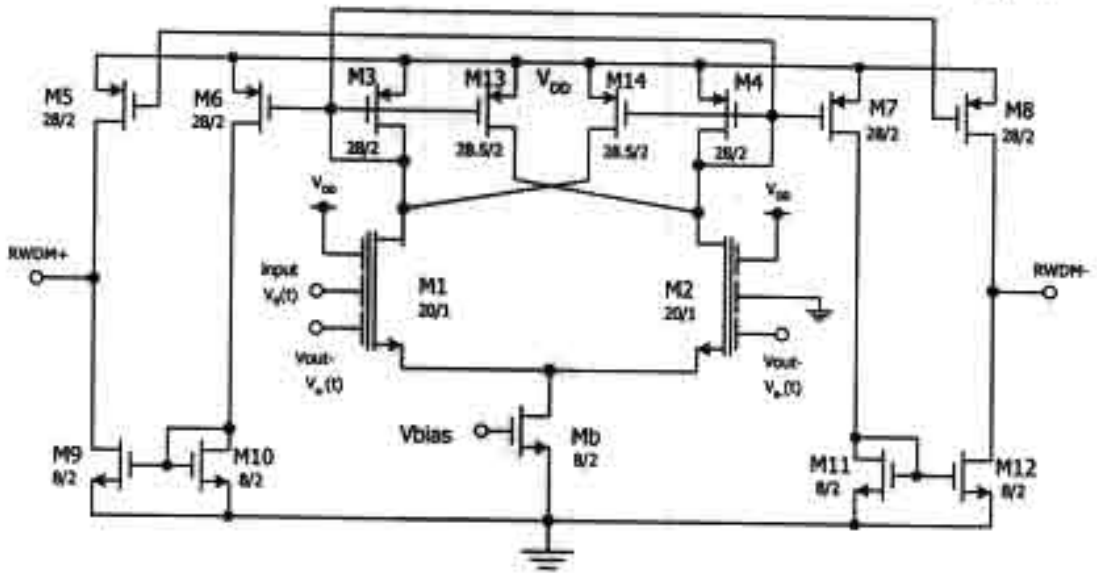



Figure 6.8 Fully differential comparator

## 6.4 SIMULATION RESULTS

Based on the proposed amplifier circuit in Fig.6.7 with the comparator shown in Fig.6.8, the amplifier can deliver current to the 8Ω resistive loads and correspond to the output signal of $5.2V_{p-p}$. Time domain simulation is show in Fig.6.9 and THD vs Signal frequency and input amplitude is show in Fig.6.10. Other performances based on simulation results on HSPICE are summarized in Table 6.1.

Table 6.1 Summary of the proposed amplifier

| | |
|---|---|
| Process technology | Alcatel 0.5μm CMOS |
| Supply voltage | 2.8V |
| Static Power dissipation | 79.51μW |

| | |
|---|---|
| Maximum output swing | $5.2V_{p-p}$ |
| Output load | 8Ω |
| Maximum power | 0.88W |
| Efficiency | 95% |

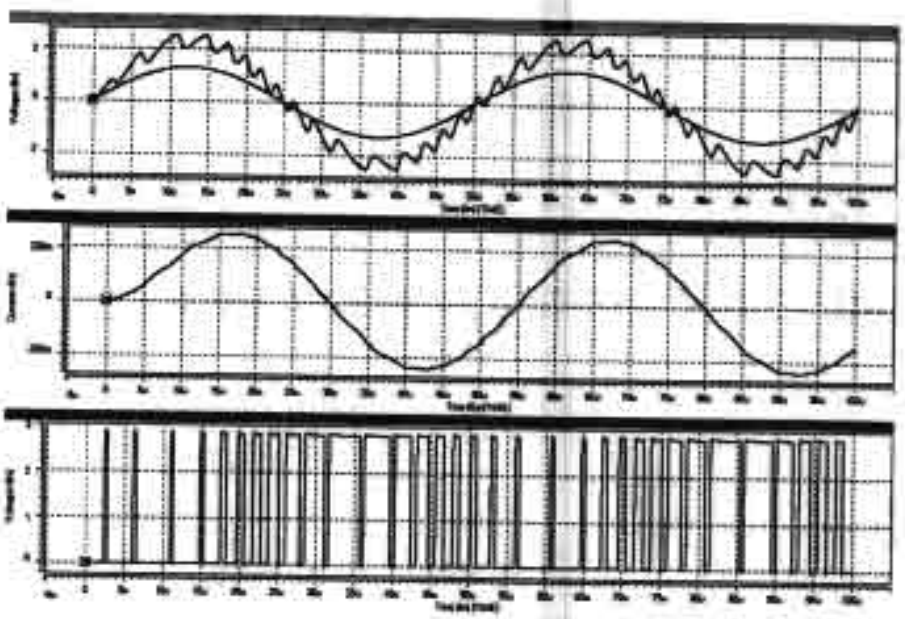


Figure 6.9 Voltage output signal, current output signal and the RWDM output signal at input $1.3V_p$, 20kHz

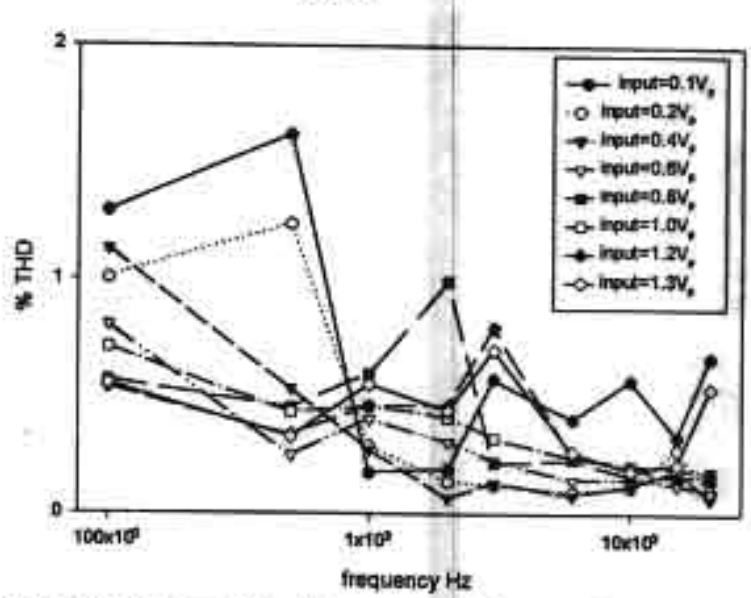



Figure 6.10 THD vs. Signal frequency and input amplitude

A single-chip low-voltage high-efficiency Class-D Power Amplifier for portable devices has been proposed. The amplifier has a very simple architecture that makes it easier to be integrated with other circuit blocks on a system level. By virtue of the high

efficiency of Class-D architecture coupled with the low voltage operation provided by the use of floating-gate MOSFET hysteresis comparator, this amplifier is suitable for portable devices with battery operations. It exhibits high distortion at low input signal due to the small changing of the input signal compared to the ripple at the output. The efficiency of this circuit is 95% at 0.88Watt with a 2.8V power supply.

## 7. A LOW-VOLTAGE WIDE-SWING FGMOS CURRENT AMPLIFIER

In the last decade, current-mode circuits [39] have drawn lots of interest due to their attractive features such as wide bandwidths, wide dynamic ranges and low voltage operations, all of which are very important for modern integrated circuits. Several elegant techniques for current-mode signal processing have been demonstrated successfully. These have mostly utilized current mirror cells, Gilbert gain cells and log-domain, square-root domain or translinear cells to perform filtering, multiplications, modulations, etc. For amplification purposes, current-mode amplifiers [40] based on a high open-loop current gain used for an accurate closed-loop configuration is also a very promising technique since use of a high gain device in a negative feedback loop allows large collection of transfer functions, performances of which are independent of the large but sensitive open-loop gain. So far, several high performance current amplifiers and opamps [41-47] have been proposed on CMOS technologies with various structures and topologies such as Differential Input Differential Output (DIDO), Differential Input Single-ended Output (DISO) or Single Input Differential Output (SIDO), etc. In general, the current opamp principle can be shown as a block diagram as in Fig.7.1, where the input current signal is firstly converted to a voltage quantity by the transimpedance amplifier (Rm) and then amplified again by the transconductance amplifiers (Gm) to produce the output current and hence the open-loop current gain. There is usually at least one high impedance node in the circuit that should be connected by a compensation capacitor for stability.

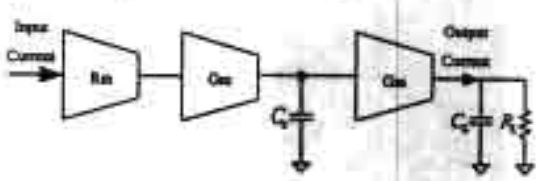


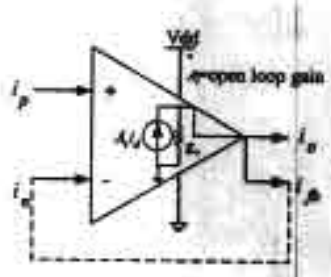
Figure 7.1 Current opamp principle

So far, most design efforts have been directed at the development of fully differential structures and enhancement of the open-loop gain and CMRR. In this work, we aim for a high signal swing by trying to avoid a class A circuit for which the limitation of current signal swing and slew rate is a result of the existing current sources, which also limit the charging current for the compensation capacitor at the high impedance node. Thus this section proposes a new current amplifier circuit totally formed in the class AB structure utilizing CMOS inverters and the recently proposed additive analog inverter [27] using floating-gate MOSFETs. Since there is no biasing current source to

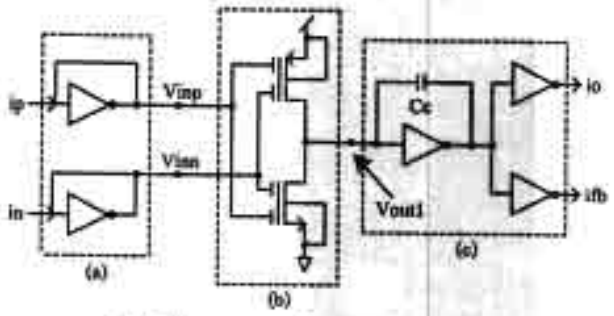
limit the signal swing, our amplifier possesses a wide swing and high slew rate. The design is applied on a 0.5μm CMOS with 1.5 Volts power supply to demonstrate high frequency operation and with 1 Volt power supply to show the feasibility of low power operations at a lower frequency range where all MOSFETs are biased in the weak inversion region.

## 7.1. THE PROPOSED CURRENT AMPLIFIER

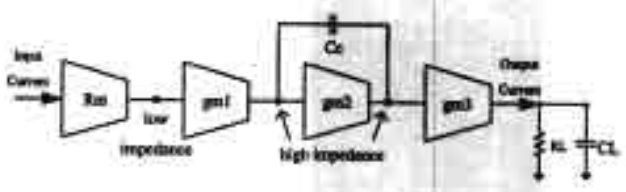
The proposed current amplifier, as symbolically shown in Fig.7.2(a), has two identical input terminals denoted as $i_p$ and $i_n$, and two output terminals delivering the same phase of the signal denoted as $i_o$ and $i_{fb}$, which are used as the output and the feedback port respectively. At the input terminals, it is noted that the input $i_n$ can only be symbolized as an inverting terminal when the amplifier is connected in the negative feedback configuration as shown by the dashed line. This will be discussed later in this section.




(a) Symbol




(b) The proposed current amplifier




(c) Block diagram

Figure 7.2 The proposed current amplifier

In Fig.7.2(b), the amplifier comprises three circuit blocks as shown in the dashed boxes. The transimpedance amplifier is shown in box (a) and written as

$$Rm = \frac{1}{(gm_n + gm_p)} \tag{7.1}$$

where $gm_n$ and $gm_p$ are respectively the transconductance of NMOS and PMOS of the inverter . The additive analog inverter in box (b) is basically a two-input CMOS inverter elegantly built from the floating-gate MOSFETs and proposed in [41]. It is employed in this circuit together with the other Rm and gm blocks to work as a differential amplifier because the polarity of $i_{fb}$ is inversed to those of $i_p$ causing the voltage at node $V_{inn}$ to be inversed to those at node $V_{inp}$. Considering only the NMOS, a large signal current equation can be written as in (7.2) where the coefficient of $V_{inn}$ is now negative.

$$I_D = \frac{1}{2}\mu C_{ox}\frac{W}{L}\left[\left(k_1 V_{inp} - k_2 |V_{inn}|\right) - V_S - V_{TH}\right]^2 \tag{7.2}$$

Here k1 and k2 are the capacitive division factors [27, 48] $C_1/C_T$ and $C_2/C_T$, where $C_1$ and $C_2$ are the effective coupling capacitances between the input gates and the floating gate and $C_T$ is the total capacitance seen from the floating gate. All capacitances correspond directly to the sizes of the input gates and the floating gate areas obtained from the layout of the circuit. In this case, the equal input gate areas of $i_p$ and $i_n$ are set and result in equal values of $C_1$ and $C_2$ of 50fF and k1 and k2 of 0.5. The two-inputs CMOS inverter works as if a differential amplifier for which the small signal voltage gain between the output $V_{out1}$ and the differential inputs can be derived as

$$\frac{V_{out1}}{\left(V_{inp} - V_{inn}\right)} = -(gm_{1n} + gm_{1p})\left(r_{o1n} // r_{o1p}\right) \tag{7.3}$$

Here $r_{o1n}$ and $r_{o1p}$ are the respective output resistances to the floating-gate NMOS and PMOS in the dashed box (b). With further analysis using the diagram in Fig.7.2(c), the open-loop current gain of the whole circuit can be derived as

$$A_i = Rm \cdot gm_1 r_{o1} gm_2 r_{o2} gm_3 \tag{7.4}$$

and the dominant pole frequency($\omega_d$) is

$$\omega_d = \frac{1}{r_{o1} gm_2 r_{o2} C_C} \tag{7.5}$$

while the GBW is

$$GBW = \frac{Rm \cdot gm_1 gm_3}{C_C} \tag{7.6}$$

## 7.2. DESIGN AND SIMULATION RESULTS

Based on the proposed concept, the design schematic can be simplified as shown in Fig.7.3, where it is seen that the circuit can be designed in a modular fashion

where all inverters including the additive analog inverter have the same dimensions of NMOS and PMOS correspondingly. If a higher gain of the $gm_2$ and $gm_3$ blocks is required, we simply add more cells of the identical inverters in parallel. $R_C$ and $C_C$ are employed for the frequency compensation.

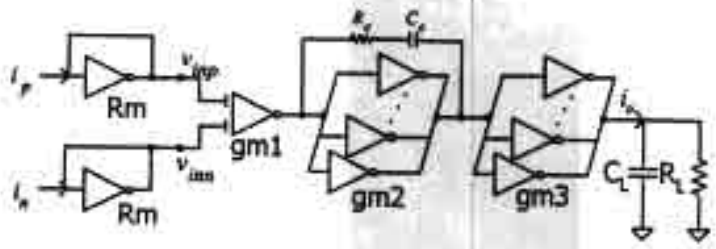
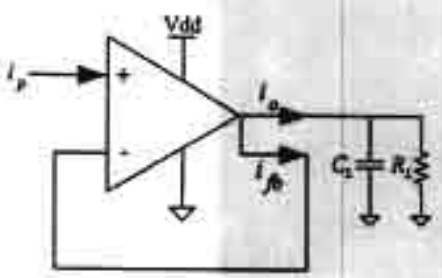
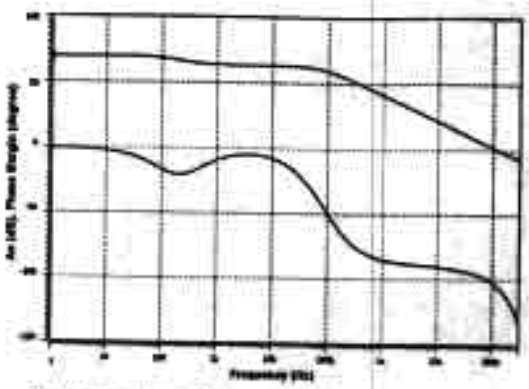



Figure 7.3 The design Schematic

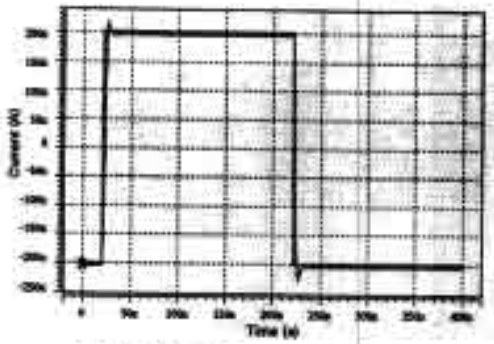
On the Alcatel 0.5μm CMOS process, two amplifiers have been designed for $V_{DD}$ of 1.5V and 1V to demonstrate high frequency operations and low power respectively. With $V_{DD}$ of 1.5V, all NMOS and PMOS are designed with the dimensions of 6.9/0.5 and 23.6/0.5 respectively resulting in the idle currents of 30μA for each inverter. As seen in Fig.7.3, only one CMOS inverter is employed for each Rm and gm1 block but extra input gates on Poly2 are connected to the inverter of the gm1 block. Then four and three inverters connected in parallel are employed for the $gm_2$ block and the $gm_3$ block respectively. The amplifier is loaded with $C_L$ of 10pF and $R_L$ of 1.69k $\Omega$ that is the same value as Rm or its input resistance. To improve the phase margin, $R_C$ of 1k Ohms and $C_C$ of 0.8pF are also included in the compensation scheme. The circuit was simulated on HSPICE with the performances shown in Fig.7.4 where 69.6dB Open-loop gain, 127MHz GBW and 74° Phase margin were achieved with a supply voltage of 1.5Volts and 635μW of power consumption. As a unity gain buffer, step response and linearity were measured at the maximum signal amplitude of ±200μA and are shown in Fig.7.4(d) and (e) where the 1% settling times are measured as 9.4 and 34.5 ns with and without $C_L$ respectively.



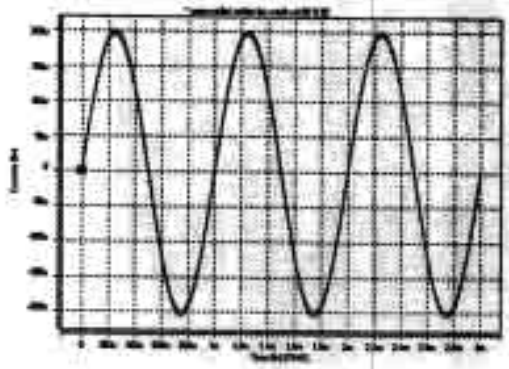

(a) Unity gain amplifier



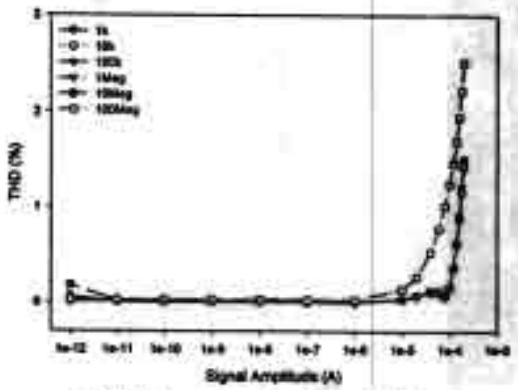
(b) Open loop Gain and Phase responses



(c) ±200μA Step Responses



(d) ±200μA Signal Swings of O/P vs. I/P




(e) THD vs. O/P signal amplitude

Figure 7.4 Simulation results

Another amplifier with a 1V power supply was designed including all NMOS and PMOS with the dimensions of 8/0.5 and 19.9/0.5 respectively operated in the weak

inversion region. As in Fig.7.3, only one CMOS inverter is employed for each Rm and gm1 block. Then five and two inverters connected in parallel are employed for the $gm_2$ block and the $gm_3$ block respectively. The amplifier is loaded with $C_L$ of 10pF and $R_L$ of 47.86k$\Omega$. From simulations, an open-loop gain of 68.3dB, with 2.68MHz GBW and 68° phase margin is achieved with 6$\mu$W power consumption. Due to space restrictions, not all performance graphs could be included here. However, in Table 7.1 all performances are compared with those of some earlier designs. The 1.5V $V_{DD}$ version amplifier is also tested in negative feedback structure with passive networks to set the closed loop gains higher than 1 as shown in Fig.7.5.

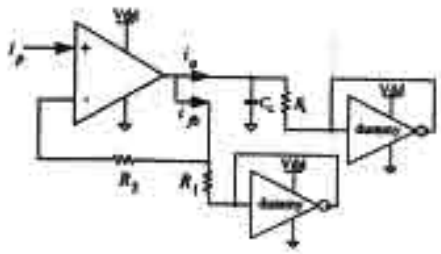


Figure 7.5 The amplifier in negative feedback

Fig.7.5 displays a non-inverting amplifier with a resistive negative feedback network. We arbitrarily put the dummy shorted input-output inverters to work as resistive loads and also to set the DC offset voltage to half of the $V_{DD}$ which is the same DC voltage at all input and output nodes. Then the closed loop gain can be derived as

$$A_{CL} = 1 + \frac{R_2 + Rm}{R_1 + Rm} \qquad (7.7)$$

where $R_1$ and $R_2$ are the resistances in the range of 0~10k$\Omega$ which are integrable value on a chip. The dummy inverter load is used to settle a proper dc level in order to avoid DC offset of the feedback current. From (7.7), Rm with $R_1$ is the transimpedance of the dummy inverter while Rm with $R_2$ is the input resistance of the $i_n$ terminal. Hence all Rms are the same value. With $V_{DD}$ of 1.5V, by setting $R_1$ at 10$\Omega$ and adjusting $R_2$ for various close-loop gains, the THD of the O/P signal were measured and shown in Fig.7.6 where the labels in the plot show details of the input signals.

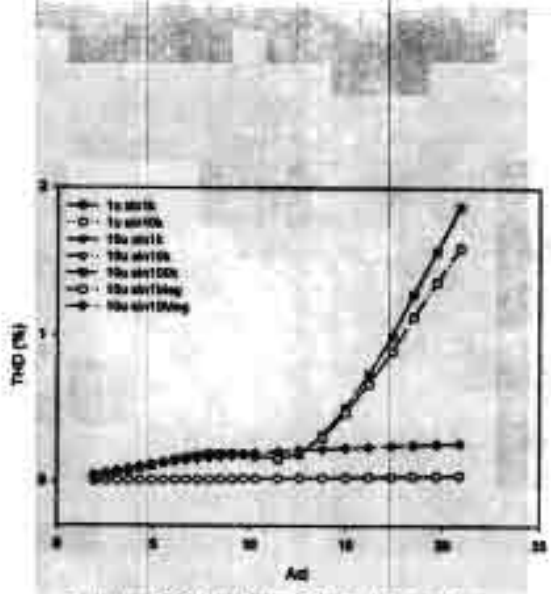



Figure 7.6 THD vs. Close-loop gain

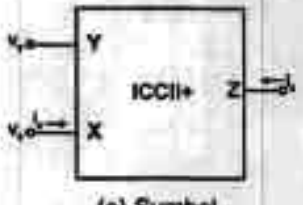
This section has presented a new low voltage wide swing current amplifier that can receive a signal swing as large as ±200μA amplitude while a THD of about 1% is still maintained. The circuits can totally be realized in the class AB thanks to the use of CMOS inverters and the available additive analog inverter cells using floating-gate MOSFETs. An effect of complex poles and zeros around the 100Hz of the open loop gain in Fig.7.4 (a) can be noticed as a result from the coupling capacitors of the FGMOS devices. A deep analysis will be placed as future works. The circuit is called a current amplifier instead of opamp due to the lack of CMRR capability, which will be part of our future works.

## 8. A LOW-VOLTAGE WIDE-SWING HIGH PRECISION CURRENT CONVEYOR

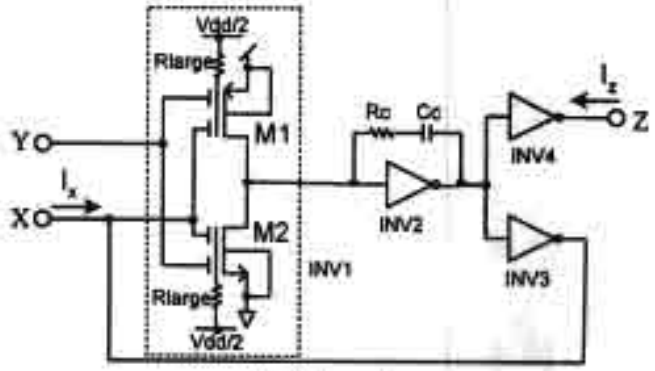
Recently, several signal processing techniques [49-50] based on second generation current conveyors (CCII) have been demonstrated successfully such as filtering, log-domain translinear, squarer and rectifier and multiplier circuits. Most reported CCII structures are based on a translinear cell which is stacked on current mirror circuits. A high precision CMOS CCII [51] was also realized with voltage follower and current mirrors with an emphasis on local negative feedback loop around $v_y$ and $v_x$ terminals. All these circuits have encountered with limitation on low voltage applications since the circuits are based on stacking topology of transistors. For low voltage applications, a CMOS CCII [52] was proposed nicely using CMOS inverters allowing only two stacked devices between the supply rails. The circuit is in a class-AB form of which the current signal swing can be very high because there is any fixed bias current source to limit the signal swing. However, the circuit is restricted to applications where the Y input is only referenced to signal ground. A flipped voltage follower based CCII was also proposed recently in [53] exhibiting performances on low voltage and compactness. However, the current signal swing of terminal X and Z are limited to the fix bias current source.

In this section, we proposes a new inverting second generation current conveyor 'positive' (ICCII+) totally formed in the class AB structure utilizing CMOS inverters and the recently proposed additive analog inverter [27, 54] using Pseudo or Quasi floating-gate MOSFETs, of which the offset voltage of the floating gate terminal can be weakly controlled effectively via a large valued resistor thanks to the inventions proposed in [55-58]. The design is emphasized on negative feedback with a high loop gain to enhance the conveying precisions relating to $v_y$ to $v_x$ and $i_x$ to $i_z$. Thanks to the class AB topology, the circuit is also capable with wide swing signals. The design is applied on a 0.5μm double poly CMOS with ±0.75V power supply demonstrating low voltage capability and high frequency operation up to 100MHz.

### 8.1. THE PROPOSED ICCII+




(a) Symbol




(b) Schematic

Figure 8.1 The proposed ICCII+

The proposed ICCII+ is shown in Fig.8.1 of which the port relations [59] among voltage and current terminals are described as.

$$\begin{bmatrix} i_y \\ v_x \\ i_z \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ -1 & 0 & 0 \\ 0 & 1 & 0 \end{bmatrix} \begin{bmatrix} v_y \\ i_x \\ v_z \end{bmatrix} \tag{8.1}$$

where terminal Y is a high impedance node and does not draw any input current. Terminal X is a low impedance node with voltage value $v_x$ equal to $-v_y$. Terminal Z is a high impedance node with the terminal current $I_z$ equal to $i_x$. These properties are transformed to the proposed ICCII+ shown in Fig.8.1. It is seen that Y is connected to the input gate of floating-gate MOSFETs and is perfectly a high impedance node. Z is connected to the output node of an inverter which is obviously a high impedance node with current driving capability. It will be shown later on that there is an internal negative feedback loop from Y terminal to X terminal. By virtue of the negative feedback loop, X can be derived as a low impedance node with a current driving capability by inverter INV3 which is shown in Fig.8.1 (b).

In Fig.8.1(b), the ICCII+ comprises four circuit blocks designated as INV1, INV2, INV3 and INV4. The INV1 is an additive analog inverter or basically a two-input CMOS inverter built from floating-gate MOSFETs M1 and M2 and was proposed in [27, 54]. Based on the idea of Pseudo or Quasi floating-gate MOSFET in [56-58], large value resistors (Rlarge) are shown to connect the floating-gate terminals of M1 and M2 to Vdd/2 thus the DC offset of the floating-gate MOSFETs can be effectively controlled and the complicated initial charge programming scheme such as UV removal can be avoided. The resistors are built from reverse-biased diode connected PMOSs. The INV1 is employed in this circuit together with INV2 and INV3 blocks to mimic the function of differential amplifier which allows the output of INV3 to negatively feedback to the node

X. Since voltage polarity of INV3 output is inversed to those of $v_y$ causing the voltage at node $v_x$ to be inversed to those at node $v_y$ hence the function of inverting CCII to copy the voltage $-v_y$ to $v_x$ can be fulfilled. Moreover, the diode connected PMOSs are always in reverse bias because voltage at the floating-gate is small as a result of the negative feedback. A modulated AC voltage at the floating-gate can be written in (8.2) where the coefficient of $v_x$ is negative as a result of the negative feedback via INV2 and INV3.

$$v_{FG} = k_1 v_y - k_2 |v_x| \tag{8.2}$$

Here k1 and k2 are the capacitive division factors $C_1/C_T$ and $C_2/C_T$, where $C_1$ and $C_2$ are the input coupling capacitances of M1 and M2. $C_T$ is the total capacitance seen from the floating gate. All capacitances correspond directly to the sizes of the input coupled gates. In this case, the equal input coupling $C_1$ and $C_2$ of M1 and M2 are set to 60fF and 100fF respectively and result in approximated equal values $k_1$ and $k_2$ of 0.5. A small signal voltage gain between the output $V_{out,INV1}$ and the differential inputs can be derived as

$$\frac{\partial V_{out\_INV1}}{\partial (V_y - V_x)} = -(gm_{1n} + gm_{1p})(r_{o1n} // r_{o1p}) \tag{8.3}$$

where $gm_{1n}$, $gm_{1p}$ and $r_{o1n}$, $r_{o1p}$ are the respective transconductance and output resistances of M1 and M2 respectively. The voltage transfer of $v_y$ to $v_x$ is derived as

$$\frac{v_x}{v_y} = \frac{-gm_1 r_{o1} gm_2 r_{o2} gm_3 r_{o3}}{1 + gm_1 r_{o1} gm_2 r_{o2} gm_3 r_{o3}} \approx -1 \tag{8.4}$$

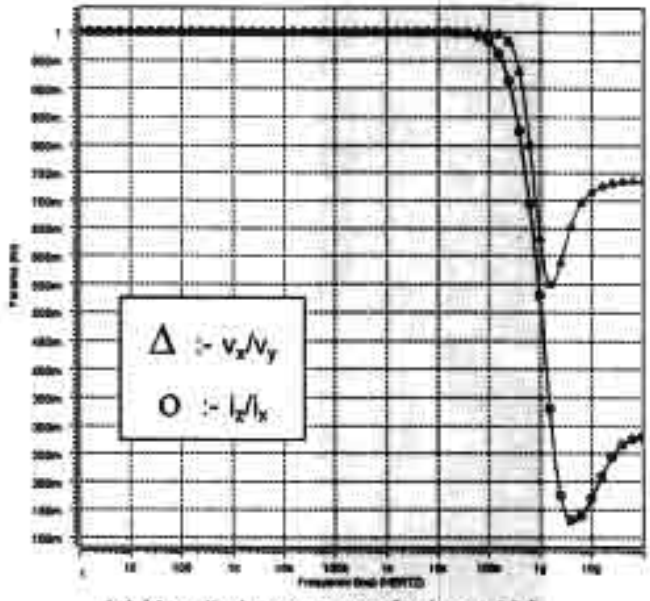
where $gm_1 r_{o1}$, $gm_2 r_{o2}$, $gm_3 r_{o3}$ are the intrinsic voltage gain of the INV1, INV2 and INV3 respectively. We can also derive the output resistance of terminal X as $r_x$ in (8.5) which is low as a result of the negative feedback.

$$r_x = \frac{r_{o2}}{1 + gm_1 r_{o1} gm_2 r_{o2} gm_3 r_{o3}} \tag{8.5}$$

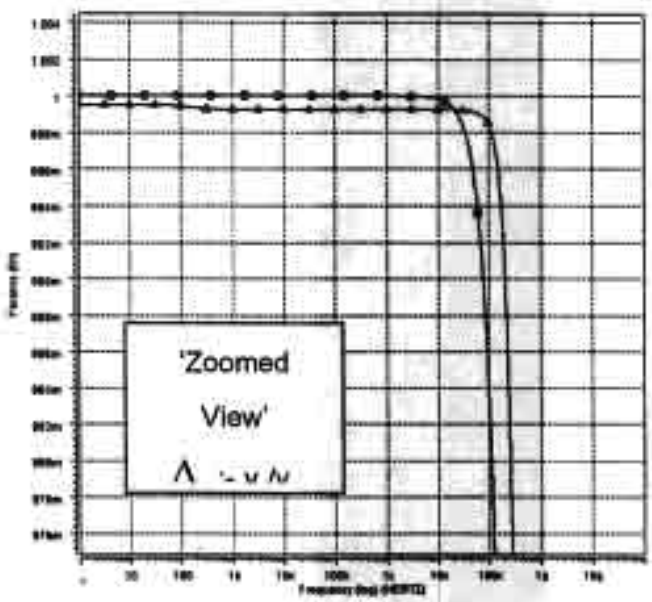
## 8.2. DESIGN AND SIMULATION RESULTS

Based on the proposed schematic in Fig.8.1(b), the circuit can be designed in a modular fashion where all inverters including the additive analog inverter have the same dimensions of NMOS and PMOS correspondingly. If a higher gain of any inverter blocks is required, we simply add more cells of the identical inverters in parallel. The circuit has been designed on the Alcatel 0.5μm double poly CMOS process with ±0.75V power supply. For each inverter module, NMOS and PMOS are designed with the dimensions of 8.4/0.5 and 24/0.5 respectively corresponding to $gm_n$ of 344uA/V and

$gm_p$ of 314uA/V and resulting in the idle currents of 34μA for each inverter. The compensation network with $R_C$ of 500 Ohms and $C_C$ of 0.35pF are employed for stability since there are two high impedance nodes across INV2. In this circuit, we employ only one CMOS inverter for the additive inverter INV1 block. There are nine inverters connected in parallel for INV2 and three parallel inverters for INV3 and INV4 blocks hence making $i_z$ equals to $i_x$. Both X and Z terminals are loaded with external resistors of 1kΩ. Fig.8.2 shows frequency responses of the ratio $v_x/v_y$ and $i_z/i_x$ which are seen that the circuit contributes very low tracking errors of $v_x/v_y$ to less than 1% and those of $i_z/i_x$ to 1.6% at the frequency of 100MHz.




(a) Magnitude response of $v_x/v_y$ and $i_z/i_x$




(b) Zoomed view of (a)

Figure 8.2 Magnitude responses of $v_x/v_y$ and $i_z/i_x$

The magnitude responses of the X terminal output resistance $r_x$ was derived in (8.5) and is shown in Fig.8.3. The value is less than 1 Ohms at DC rising to 500 Ohms at 100MHz. It is increasing dependent to the frequency in the high frequency range because the loop gain of the negative feedback is decreasing at high frequency. However, the operating frequency of the circuit is bound to 100MHz.

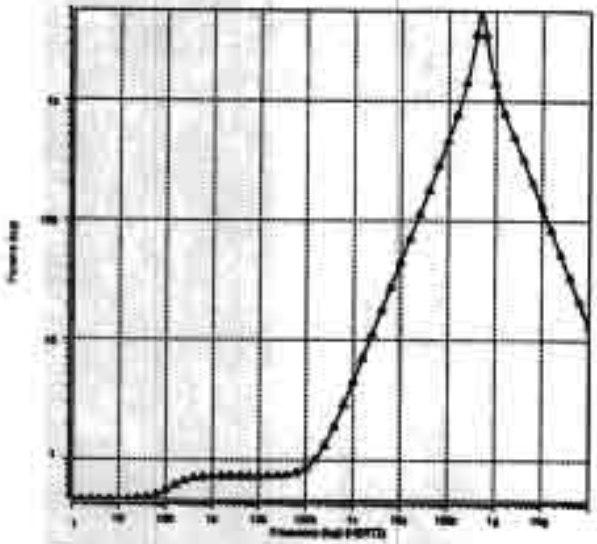
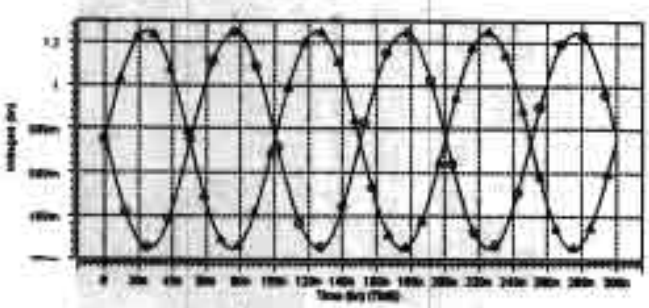
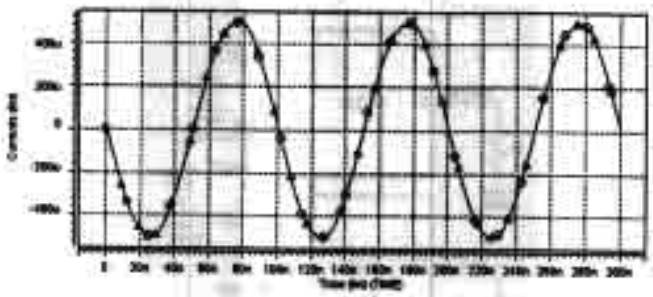


Figure 8.3 Magnitude response of $r_x$ (Ohms)

Fig.8.4 shows the transient responses at 10MHz of $v_y$ vs. $v_x$ and $i_x$ vs. $i_z$. In Fig.8.4 (a) the responses of $v_y$ vs. $v_x$ confirm well with (8.4). It is seen that the signal swing is as large as $\pm$500mV. Fig.8.4 (b) shows a perfect matching of $i_x$ vs. $i_z$ with the current swing as large as $\pm$500uA. For high frequency capability, Fig.8.5 shows the transient responses at 100MHz. In Fig.8.5 (a) shows the responses of $v_y$ vs. $v_x$ with signal swing of $\pm$200mV. Fig.8.5 (b) shows the responses of $i_x$ vs. $i_z$ with the current swing of $\pm$200uA. It is seen that the corresponding signals $v_y$ vs. $v_x$ and $i_x$ vs. $i_z$ are still matched but with a small phase shift. All signal amplitudes are set to confine the THD to less than 1%. Total power consumption is 816$\mu$W which can be lowered with a reduced bandwidth.

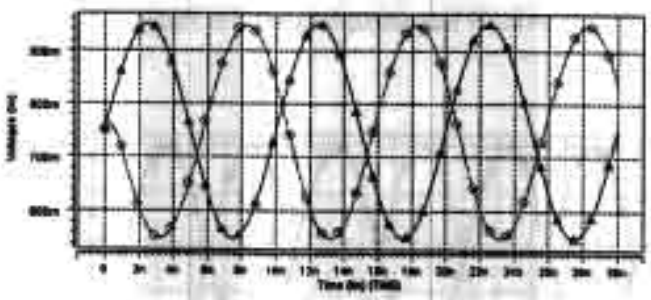


(a) $\Delta$ for $v_y$ and O for $v_x$

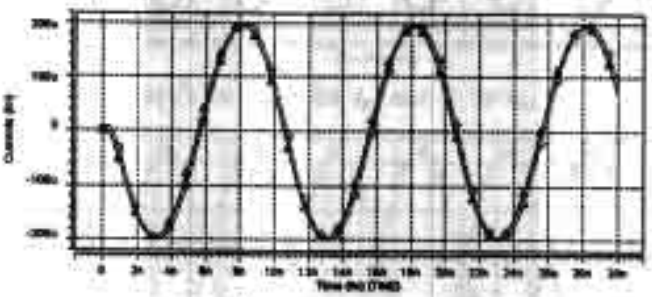


(b) Δ for $i_x$ and O for $i_z$

Figure 8.4 Transient responses at 10MHz with THD<1%



(a) Δ for $v_y$ and O for $v_x$



(b) Δ for $i_x$ and O for $i_z$

Figure 8.5 Transient responses at 100MHz with THD<1%

In many current conveyor applications, there is a need to have both polarities of output current $i_Z$ or multiple outputs $i_{Z+}$ and $i_{Z-}$. In some conventional CCII, this facility is usually performed using additional current mirrors to copy and invert polarity of the output current $i_Z$. However non-ideal characteristics of current mirror always introduce some tracking error between the current $i_{Z+}$ and $i_{Z-}$. In the similar way on this topology, we can not straightforwardly cascade additional inverters at the output Z terminal in order to make an inverted-direction current $i_{Z-}$ since there is usually an excess phase shift that causing an unperfected tracking between the currents $i_{Z+}$ and $i_{Z-}$. In this case, we demonstrate a parallel connected ICCII+s as shown Fig.8.6. Fig.8.7 (a) shows a perfected tracking of the voltage signal at terminals $v_{y1}$, $v_{x1}$ and $v_{x2}$. The perfected tracking in both magnitude and out of phase of $i_{Z+}$ and $i_{Z-}$ are shown in Fig.8.7 (b) confirming a high precision property of this ICCII+.

connected PMOSs producing the large resistors are always in reverse bias because the voltage at the floating-gate is small as a result of the negative feedback. With ±0.75V supply, the circuit can handle signal swing as large as ±500μA amplitude through X and Z terminals and ±500mV at Y and X terminals while the THD is maintained to less then 1%. The circuit is designed to operate up to 100MHz signal frequency.

## 9. A HIGH SPEED LOW INPUT CURRENT LOW VOLTAGE CMOS CURRENT COMPARATOR

In the last decade, current-mode circuits [39, 43, 54] have drawn lots of interest for modern integrated circuits and sensory systems. This is due to their attractive features such as high speed, wide dynamic ranges and low voltage operation, all of which are mainly due to the fact that all node voltages swing are very low. In analogue and mixed signal processing, the current comparator is also one of the key elements. The circuit is not purely in a current-mode operation since although the input signal is current the output signal is digital logics or rail to rail voltage signal. Obviously there is a requirement to transform the input current to a large voltage signal. Thus to design a high speed current comparator, one has to take care of the voltage swing carefully since it directly determines the propagation delay. Conventionally, most reported current comparators [60-63] are based on the concept shown as a block diagram in Fig.9.1 (a), where the input current signal is converted to the voltage $V_{in}$ and $V_1$ by the transimpedance stage comprising inverter amplifier $A_1$ and voltage buffer $A_2$. The resulting voltage $V_1$ is then amplified by the latter high gain inverter amplifiers $A_3$ to produce output logic voltage. There exist parasitic capacitors at all nodes. Ideally for high speed comparators, the signal swing at $V_1$ should be maintained as small as possible and situated exactly around the inverter threshold voltage of the inverter $A_3$. However, the reported works were relating to improve the lowest input current acquiring ability by arranging a proper biasing to turn on the MOSFETs of the buffer $A_2$ all the time. Most of them utilized diode connected MOSFETs as a level shifter to create $V_{GS}$ of the buffer MOSFETs. It is seen that although the transimpedance stage is formed in a negative feedback loop a much larger loop gain has not been exploited to keep the signal $V_{in}$ and $V_1$ as low as possible. Moreover with a larger loop gain, the input impedance at node $V_{in}$ could be much lower and receive a much smaller input current in the pico Amps range. The so called dead zone which is the smallest input current range to which comparators are insensitive is then minimized. However, a drawback of having the small voltage swing at $V_1$ is that the gain of the latter inverter amplifier must be necessarily high with hence a higher power consumption. Obviously, there is a conflict that if a speed as a result of a small voltage swing of the tranresistance stage is desired, a very high gain of the latter inverter amplifier will be necessary to provide the rail to rail output swing. In this paper, we propose an idea based on Fig.9.1 (b), where a much higher loop gain is emphasized to gain speed and then trade power to the latter

high gain inverter amplifier. The circuit utilizes only CMOS inverters and is suitable for a low $V_{DD}$ operation.

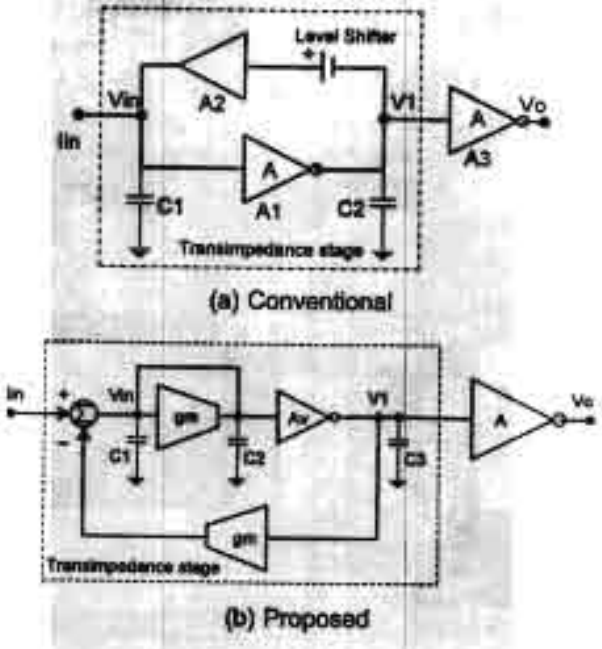



Figure 9.1 Current comparator concepts

## 9.1 THE PROPOSED CIRCUIT

As discussed above, we concentrate on a high speed or smallest average propagation delays and low input current acquiring capability or smallest dead zone. In this work, we trade off power for the required speed by maintaining the lowest voltage swing of the transimpedance stage and then providing high power to build up the latter high gain stage using inverter amplifiers. We then focus on the two separated circuit blocks as follows.

### 9.1.1 TRANSIMPEDANCE STAGE

The transimpedance stage, shown as the dashed block in Fig.9.2, plays the most important role in determining the speed of the comparator. It is seen that the whole stage is formed in a negative feedback loop by observing the polarities of output voltages and currents of each inverter. $A_1$ as a shorted input-output transconductance amplifier or inverter is basically an equivalent grounded resistor with the value of 1/gm. $A_2$ and $A_3$ are two high voltage gain amplifiers constructed from two cascaded inverters. Since there are two high impedance nodes in the loop RC frequency compensation is necessary to make the circuit stable. Capacitor C is set to 0.1pF while the resistor R is set to 1.6k Ohms. Note that the C and R could be made from a parasitic capacitor and a triode MOSFET respectively. The transconductance amplifier $A_4$ is used to provide

negative feedback current to the input node. All amplifiers $A_1$ to $A_4$ are CMOS inverters designed with the same dimensions which are 2.1um/0.25um and 7um/0.25um for W/L of NMOS and PMOS respectively.

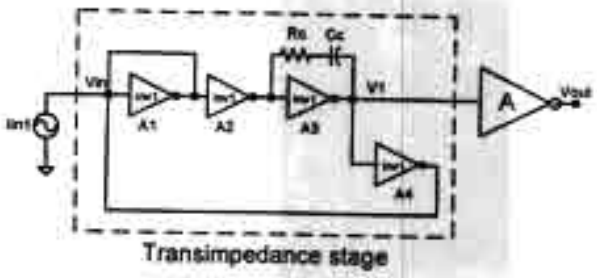



Figure 9.2 Transimpedance stage

Constructed in the feedback loop, the input resistance at node $V_{in}$ can be derived as.

$$R_{in} = \frac{1}{gm_T} \frac{1}{\left(1 + A_{vo}^2\right)} \tag{9.1}$$

where $gm_T$ is an equivalent transconductance of $A_1$ and and $A_{vo}$ is a voltage gain of the amplifier $A_2$ and $A_3$. Note that all inverters have the same transconductance and voltage gain because they have the same dimensions. It is seen that the input resistance $R_{in}$ is very small which results in a minimum voltage swing at node $V_{in}$ and also the same value of $V_1$ at the output of $A_3$. Fig.9.3 shows an open loop gain and phase of the feedback current to the input current. It is seen that dc gain of 56dB, GBW of 906MHz and PM of $45^{\circ}$ are achieved in the open loop transconductance stage. With this specification, we have enough loop gain to suppress signals for the lowest voltage swings at $V_{in}$ and $V_1$ as shown in Fig.9.4. The negative feedback also stabilizes the common-mode voltage at all nodes to $V_{DD}/2$ which is set by the node $V_{in}$. This property is crucial for assuring that the signal swing is very small and also situated right at the center of the gate threshold voltage of the latter inverter of the gain stage.

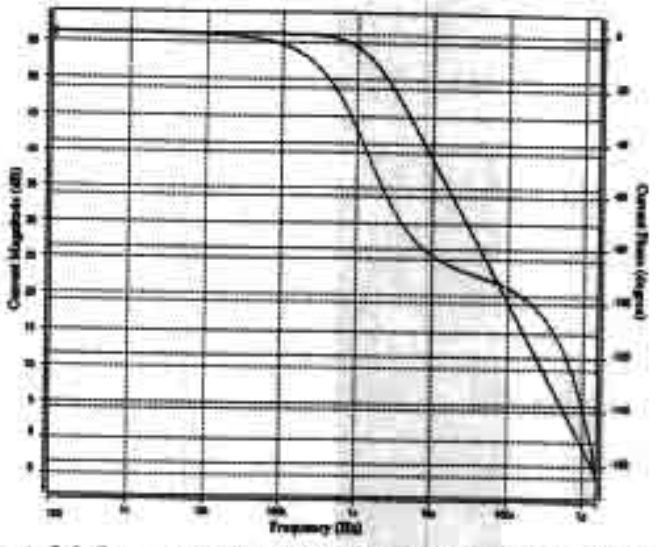


Figure 9.3 Open-loop responses of the transconductance stage

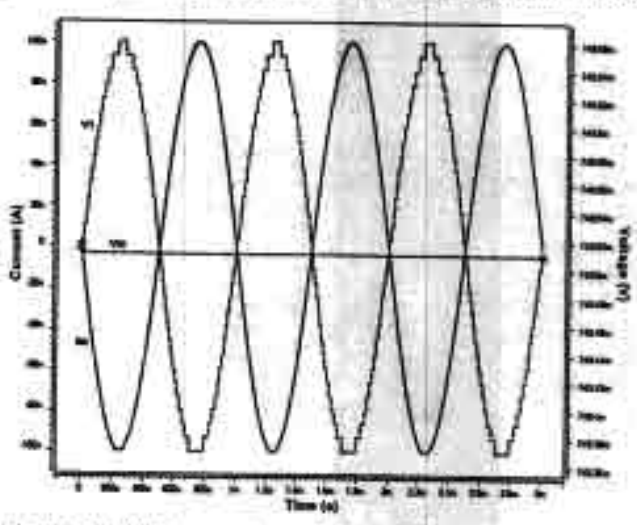


Figure 9.4 Voltage swings at $V_{in}$ and $V_1$ vs. input current

### 9.1.2 GAIN STAGES

We have now a very small voltage swing $V_1$ at the input of $A_5$ of the gain stage. The main aim in designing this part is to construct high voltage gain to produce rail to rail output logic. Based on the use of the same dimension inverters, the high gain stage can be constructed in a modular fashion as shown in Fig.9.5. INV1 has the same dimension as those in the transconductance stage. INV2 has smaller dimensions than those of INV1 by half, i.e. 1um/0.25um and 3.5um/0.25um for W/L of NMOS and PMOS respectively. The modules could be placed in parallel for higher gain. For $A_5$, there are six INV1s connected in parallel, where each INV1 possesses an output current equal to $I_{in}$. $A_9$ and $A_{10}$ are only needed when $I_{in}$ is lower than 10nA. Cascading many stages of the inverter does not deteriorate the speed much because each inverter has a very small propagation delay which is less than 1ns. So as discussed earlier the major contributor to the delay is the transimpedance stage.

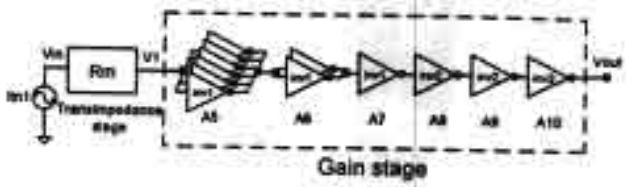
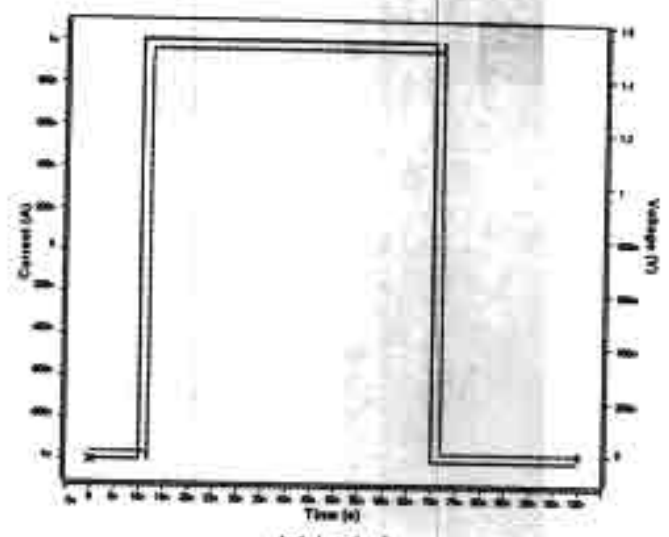


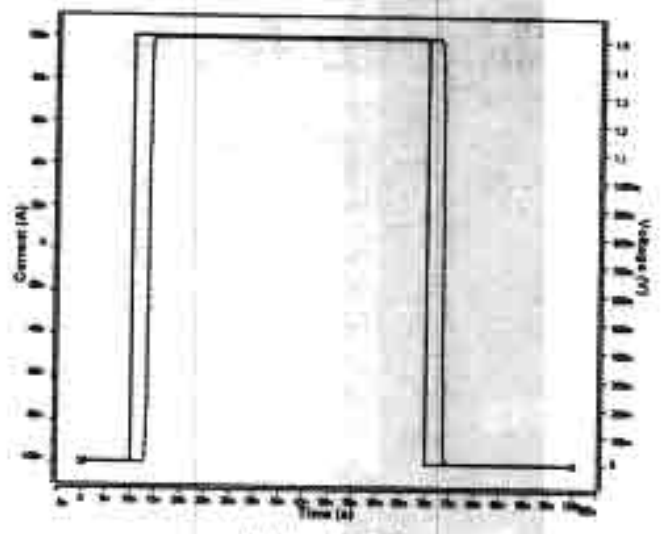

Figure 9.5 Gain stage

## 9.2 SIMULATION RESULTS

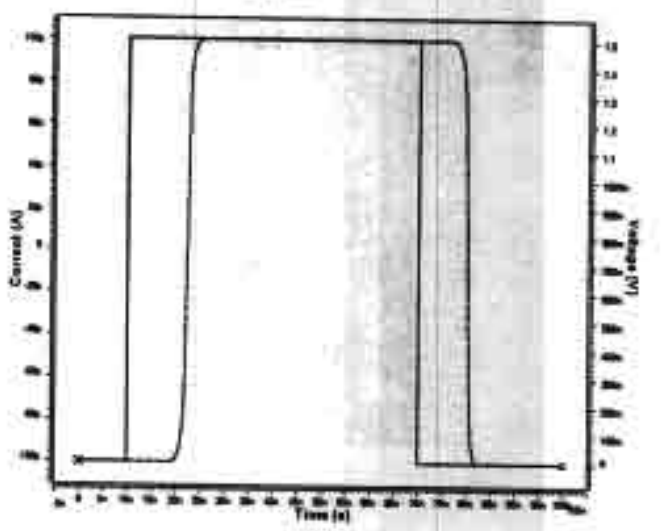
The proposed current comparator has been designed on a 0.25um TSMC CMOS process and tested with various power supplies and input current amplitudes. On HSPICE and with $V_{DD}$ set to 1.5V, the comparator responses of three input current amplitudes of 1uA, 100nA and 100pA are shown in Fig.9.6 where the average propagation delays are 1.95ns, 3.6ns and 10.7ns respectively. Performances vs the input current amplitudes at 1.5V $V_{DD}$ such as average propagation delay, static power and power delay product (PDP) are shown in Fig.9.7. It is seen that the lowest input current amplitude is at $\pm$50pA thanks to the small input resistance as a result of the negative feedback with high loop gain. The average propagation delay is inversely proportional to the input current amplitudes since the voltage swing at the output of the transconductance stage is small. With small input current amplitudes, the static power also increases because all node voltages are around the common-mode value or $V_{DD}/2$ where most MOSFETs of the inverters are fully turned on. Propagation delays at various $V_{DD}$ and input signal amplitudes are shown in Fig.9.8. Performance comparisons among many reported circuits are listed in Table 9.1. It is seen that the power is higher than those from some earlier designs because the scaling down of the $V_{DD}$ normally degrades some properties of the inverter such as average drain current, voltage gain and propagation delay. Thus more power has to be pumped into the circuits in order to achieve the required speed and rail to rail output voltage swing.



(a) $I_{in}$=1uA



(b) $I_{in}$=100nA



(c) $I_{in}$=100pA

Figure 9.6 Transient Response of $V_{OUT}$ vs. $I_{in}$ at 1.5V $V_{DD}$

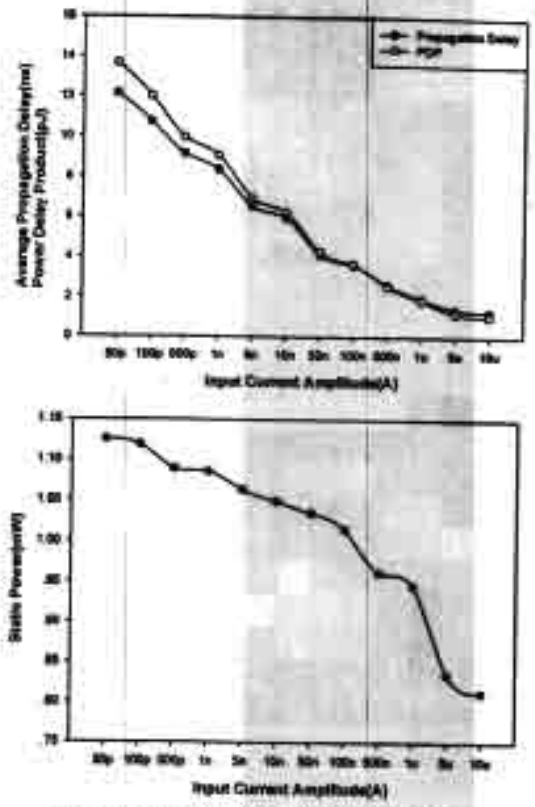


Figure 9.7 Performances at 1.5V $V_{DD}$

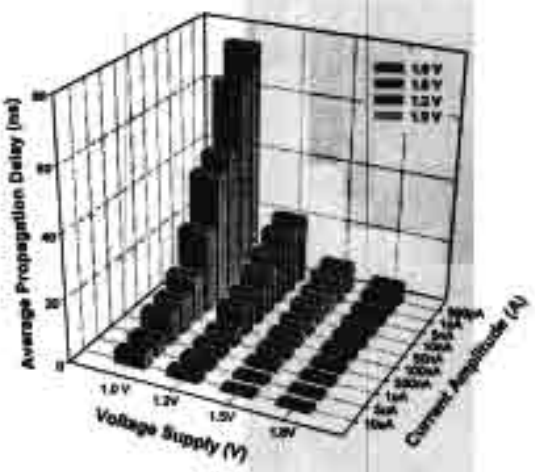


Figure 9.8 Propagation delays at $V_{DD}$ 1.0-1.8 Volts

A new high speed low input current low voltage current comparator has been demonstrated on a 0.25um TSMC CMOS process. Based on the concept of a high speed current-mode technique, we exploit a negative feedback scheme around the transimpedance stage with an emphasis on a very large loop-gain to produce a very small transformed voltage swing which is situated at the center of the gate threshold voltage of the latter stage. This will ensure the fastest response time. The same dimension inverters are used in all amplifier stages. They are fast and simple and suitable for low voltage operation. There is no extra biasing circuit and stacked

transistor, thus the same design can be applied with various $V_{DD}$ - ie there is no need to readjust the design.

Table 9.1 Performance comparisons

| | Traff [60] | Tang [61] | Ravezzi[62] | Min [64] | Lin [63] | Proposed circuit | | |
|---|---|---|---|---|---|---|---|---|
| Year | 1992 | 1994 | 1997 | 1998 | 2000 | 2002 | 2002 | 2002 |
| Power Supply (V) | 5 | 5 | 5 | 3 | 3 | 1.5 | 1.0 | 1.8 |
| Process (μm) | 2 | 1.6 | 2.5 | 0.35 | 0.35 | 0.25 | 0.25 | 0.25 |
| Minimum Input Current Amplitude (nA) | 10 | 10 | 100 | 10 | 1 | 0.05 | 0.05 | 0.5 |
| Propagation delay | ±1μA/ 10ns | ±0.1μA/ 11ns | ±0.1μA/ 19ns | ±0.1μA/ 7ns | ±0.1μA/ 2.8ns | ±0.1μA/ 3.5ns | ±0.1μA/ 14.65ns | ±0.1μA/ 2.6ns |
| Power consumption (mW) (at 0.1μA) | 0.390 | 1.4 | NA | 0.45 | 0.56 | 1.01 | 0.022 | 2.73 |
| PDP (pJ) | NA | NA | NA | 3.15 | 1.4 | 3.648 | 0.32 | 7.25 |

## 10. CONCLUSION

A floating-gate MOSFET or FGMOS on a standard double-poly CMOS offers various new useful functions which can be used to create many novel circuits such as low voltage low power circuits, analogue computational circuits and etc. This report gives a review of FGMOS such as the principle properties, functional characteristics and modeling for simulation tools. FGMOS device is basically a multiple-input device of which the main properties can be very useful for analog and digital computational circuits. It has unique and attractive characteristics of which the most important properties to be applied in this research and report are as follows: 1) As a multiple-input gate device, the voltage appears at the floating gate is a linear summation of its input voltage at all input terminals. This characteristic makes the device suitable for multiple signal computation. 2) The effective threshold voltage ($V_{th}$) seen at the input gate is tunable. These two phenomena are very attractive to analog designers. The first feature of the multiple-input gates allows analog designers to design a novel or to adapt many existing circuits to work with more complexity function without adding power consumption, while the second feature allows FGMOS devices to be operated at a very low the supply voltage as a result of the threshold voltage tunability. Both low voltage and low power operations are the most important requirement for biomedical applications. In this research, several analog signal processing building blocks have been proposed. They are very useful to various applications in biomedical systems such as biologically inspired circuits, electronic cochlea, silicon retina and analogue neural networks.

A Hysteresis Tunable Voltage Comparator using FGMOS is already proposed. The circuit is essentially exploiting FGMOS devices in the positive feedback scheme to create the hysteresis. Based on the tunability of the FGMOS, the current ratio of $I_{D10}/I_{D3}$ and $I_{D11}/I_{D4}$ corresponding to the amount of feedback current is used to tune the hysteresis effectively. An experiment of the back-gate tuning of M3 and M4 has also been investigated with a result showing that the range of $V_{TRP+}$ and $V_{TRP-}$ are not as wide as those offered by the circuit employing FGMOS. Also, the back-gate biasing always experiences an amount of leakage current because the bulk terminal is not fully isolated as in the case of poly1 and poly2 gates. The proposed idea can be implemented on any standard double-poly CMOS processes. The work has been performed on AMI 1.2μm CMOS process available through MOSIS. All the simulation

results confirm well the functionality. Performance optimizing will be placed as future works. Following the design of the Hysteresis Tunable Voltage Comparator, a non-clocked 8-bits digital comparator is also presented. It essentially manipulates the proposed analog voltage comparator to realize the new digital circuit in which the signal is internally processed in an analogue fashion. The proposed idea can be implemented on any standard double-poly CMOS and be useful to mixed signal and computational applications. All the simulation results confirm well the functionality.

As an application of a multiple input voltage comparator, designs of a single-chip low-voltage high-efficiency Class-D Power Amplifier for portable devices has been proposed. The amplifier has a very simple architecture that makes it easier to be integrated with other circuit blocks on a system level. By virtue of the high efficiency of Class-D architecture coupled with the low voltage operation provided by the use of floating-gate MOSFET hysteresis comparator, this amplifier is suitable for portable devices with battery operations. It exhibits high distortion at low input signal due to the small changing of the input signal compared to the ripple at the output. The efficiency of this circuit is 95% at 0.88Watt with a 2.8V power supply.

In this research, a novel approach in exploitation of CMOS inverter in a negative feedback form is presented. Normally, the CMOS inverter has only one input terminal which is not convenience to be used in a negative feedback form. However, the negative feedback can be performed successfully via an assistance of the floating-gate additive analog inverter. A new low voltage wide swing current amplifier is then proposed. It can receive a signal swing as large as $\pm 200\mu A$ amplitude while a THD of about 1% is still maintained. The circuits can totally be realized in the class AB thanks to the use of CMOS inverters and the available additive analog inverter cells using floating-gate MOSFETs. The circuit is called a current amplifier instead of opamp due to the lack of CMRR capability, which will be part of our future works. Based on the same concept of designing CMOS inverter circuits in a negative feedback form, a low voltage wide swing inverting second generation CMOS current conveyor of which the design focuses on the use of CMOS inverters and the negative feedback to enhance conveying precisions, signal linearity and low output resistance property at the terminal X. The circuit is totally realized in class AB thanks to the use of CMOS inverters and the available floating-gate MOSFET additive analog inverter cell which facilitates the negative feedback channel to the normal CMOS inverter. With the programming approach of pseudo or quasi floating-gate MOSFET, DC offset of the floating-gate

inverter can be effectively controlled to Vdd/2 and the complicated initial charge programming schemes could be avoided. The diode connected PMOSs producing the large resistors are always in reverse bias because the voltage at the floating-gate is small as a result of the negative feedback. With ±0.75V supply, the circuit can handle signal swing as large as ±500μA amplitude through X and Z terminals and ±500mV at Y and X terminals while the THD is maintained to less then 1%. The circuit is designed to operate up to 100MHz signal frequency.

A new high speed low input current low voltage current comparator has also been proposed and demonstrated on a 0.25um TSMC CMOS process. Based on the concept of a high speed current-mode technique, a negative feedback scheme has been exploited around the transimpedance stage with an emphasis on a very large loop-gain to produce a very small transformed voltage swing which is situated at the center of the gate threshold voltage of the latter stage. This will ensure the fastest response time. The same dimension inverters are used in all amplifier stages. They are fast and simple and suitable for low voltage operation. There is no extra biasing circuit and stacked transistor, thus the same design can be applied with various $V_{DD}$ - ie there is no need to readjust the design.

This research works have been leading the way to exploit the floating-gate MOSFET device in various low voltage low power applications based on the fundamental concepts of analog signal processing and current mode circuit designs. All proposed analog building blocks are useful for micro power system designs and integrations. The first attempt in using the CMOS inverter in negative feedback form has been pointed out and should be exploited further for future works.

## 11. REFERENCES


[1] Liming Yin, S.H.K. Embabi, E. Sanchez-Sinencio, "A floating-gate MOSFET D/A converter," in Proc. ISCAS '97, 1997, vol. 1, pp. 409-412.

[2] R. R. Harrison, J. A. Bragg, P. Hasler, B. A. Minch, S. P. Deweerth, "A CMOS programmable analog memory-cell array using floating-gate circuits," IEEE Trans Analog and Digital Signal Processing, vol. 48 Issue 1, pp. 4-11, Jan 2001.

[3] E. O. Rodriguez, A. Yufera, A. Rueda, "A gm-C floating-gate MOS integrator" in Proc. ISCAS 2000, 2000, vol. 4, pp.153 -156.

[4] K. Yang, A. G. Andreou, "Multiple input floating-gate MOS differential amplifiers and applications for analog computation," in Proc of the 36th Midwest Symposium on Circuits and Systems 1993, 1993, vol. 2, pp. 1212-1216.

[5] Y. Berg, S. Aunet, O. Ness, H. Gundersen, M. Hovin, "Extreme low-voltage floating-gate CMOS transconductance amplifier," in Proc. ISCAS 2001, 2001, vol. 1, pp. 37-40.

[6] R. R. Harrison, "Floating gate current mirror for gain correction in CMOS translinear circuits", in Proc. ISCAS '99,1999, vol. 2, pp. 404-407.

[7] T. Shibata, M. Konda, Y. Yamashita, T. Nakai, T. Ohmi, "Neuron-MOS-based association hardware for real-time event recognition," in Proc. Microelectronics for Neural Networks, 1996, pp. 94-101.

[8] H.R. Mehrvarz, C. Y. Kwok, "A novel multi-input floating-gate MOS four-quadrant analog multiplier," IEEE Journal of Solid-State Circuits, vol. 31, Issue: 8, Aug. 1996 pp. 1123-1131.

[9] Y. Berg, O. Naess, M. Hovin, "Ultralow-voltage floating-gate analog multiplier with tunable linearity," in Proc. ISCAS 2000, 2000, vol. 4, pp. 245-248.

[10] D. Kahng, S. M. Sze, "A Floating-Gate and Its Application to Memory Devices," The Bell System Technical Journal, vol. 46, no. 4, pp. 1288-1295, 1967.

[11] M. Holler, S. Tam, H. Castro, R. Benson, "An electrically trainable artificial neural network (ETANN) with 10240 'floating gate' synapses," International Joint Conference on Neural Networks, 1989, vol. 2, pp.191-196.

[12] P. Hasler, B. A. Minch, C. Diorio, "Floating-gate devices: they are not just for digital memories any more," in Proc. ISCAS '99, 1999, vol. 2, pp. 388-391.

[13] A. Thomsen, M. A. Brooke, "Low control voltage programming of floating gate MOSFETs and applications," IEEE Trans Circuit and systems, vol. 41, no. 6, pp. 443-452, June 1994

[14] T. Shibata, T. Ohmi, "A functional MOS transistor featuring gate-level weighted sum and threshold operations," IEEE Trans Electron Devices, vol. 39, Issue: 6, pp. 1444-1455, June 1992.

[15] C. Mead, Analog VLSI and Neural Systems, Reading, MA: Addison-Wesley, 1989.

[16] T. Inoue, H. Nakane, Y. Fukuju, "A low-voltage fully-differential current-mode analog CMOS integrator using floating-gate MOSFETs," in Proc. ISCAS 2000, 2000, vol. 4 , pp. 145-148 vol.4

[17] J. Ramirez-Angulo, R. G. Carvajal, J. Tombs, A. Torralba, "A.Low-voltage CMOS op-amp with rail-to-rail input and output signal swing for continuous-time signal processing using multiple-input floating-gate transistors," IEEE Trans Circuits and Systems II: Analog and Digital Signal Processing, vol. 48, Issue: 1, pp. 111-116, Jan 2001.

[18] B. A. Minch, P. Hasler, C. Diorio, "Multiple-input translinear element networks," in Proc. ISCAS '98, 1998, vol. 1, pp. 88 -91.

[19] F. Osamu, A. Yoshihito, "A Floating-Gate Analog Memory Device for Neural Networks," IEEE Trans. Electron Devices, vol. 40, no. 11, Nov. 1993.

[20] P. Hafliger, C. Rasche, "Floating gate analog memory for parameter and variable storage in a learning silicon neuron," in Proc. ISCAS '99, 1999, vol. 2, pp. 416-419.

[21] K. Yang, A. G. Andreou, "Subthreshold analysis of floating-gate MOSFET's," in Proc. The Tenth Biennial University/Government/Industry Microelectronics Symposium, 1993, pp. 141-144

[22] J. Ramirez-Angulo, G. Gonzalez-Altamirano, S. C. Choi, "Modeling Multiple-input Floating-gate transistors for analog signal processing," in Proc.ISCAS'97, 1997, vol. 3, pp. 2020-2023.

[23] K. Yang; A. G. Andreou, "The multiple input floating gate MOS differential amplifier: an analog computational building-block," in Proc. ISCAS '94, 1994, vol. 5, pp. 37-40.

[24] B. A. Minch, P. Hasler, C. Diorio, "Multiple-input translinear element networks," in Proc. ISCAS '98, 1998, vol. 1, pp. 88-91.]

[25] Y. Berg, D. T. Wisland, T. S. Lande, S. Mikkelsen, "Ultra low-voltage digital floating-gate UVMOS (FGUVMOS) circuits," in Proc. ISCAS '98,1998,vol. 2, pp. 37-40.

[26] J. Ramirez-Angulo, S. C. Choi, G. Gonzale-Altamimo, "Low-Voltage Circuit Building Blocks Using Multiple-Input Floating-Gate Transistors," IEEE Trans circuits and system: fundamental theory and applications, vol.42, no.11, Nov 1995

[27] Y. Berg, O. Naess, M. Hovin, "Ultra low-voltage floating-gate transconductance amplifier with tunable gain and linearity," in Proc. ISCAS 2000, 2000, vol. 3 pp. 343-346.

[28] P. Klein, K. Hoffmann, O. Kowarik, "An EEPROM compact circuit model," in Proc. Custom Integrated Circuits Conference 1996, 1996, pp. 325-328.

[29] G. V. Steenwijk, K. Hoen, H. Wallinga, "A nonvolatile analog programmable voltage source using the VIPMOS EEPROM structure," IEEE J. Solid-State Circuits, vol. 28, no. 7, pp. 784-788, July 1993.

[30] C. K. Sin, A. Ktamer, V. Hu, R. R.Chu, P. K. Ko, "EEPROM as an analog device, with particular application in neural," IEEE Trans. Electron devices, vol. 39 no. 6, pp. 1410-1419.

[31] C. Hu, "Lucky Electron Model of Channel Hot Electron Emission," International Electron Device Meeting Technical Digest, pp. 22-5, 1979.

[32] R. H. Fowler, L. Nordheim, "Electron Emission in Intense Electric Fields," in Proc. The Royal Society of London, 1928, vol. A119, pp. 81-173

[33] "IEEE standard definitions and characterization of floating gate semiconductor arrays," IEEE Std 1005-1998, 9 Feb. 1999

[34] P. E. Allen, D. R. Hoberg, CMOS Analog Circuit Design. NY: Oxford University press, pp. 323-362

[35] D. L. Schilling, C. Belove, Electronic Circuits Discrete And Integrated, 3rd edition, McGraw-Hill, 1989

[36] B. Duncan, High Performance Audio Amplifiers, Newnes, 1996

[37] L. Kitjalak, P. Pawawongsak, "DSP Application for RWDM Inverters", The 22nd Electrical Engineering Conference, Bangkok, 1999, pp. 541-544

[38] Choi et al, "A design of a 10-W single-chip class D Audio amplifier with very high efficiency using CMOS technology," IEEE Trans. Consumer electronics, vol. 45, no.3, Aug 1999

[39] C. Toumazou, F.J. Lidgey, D. Haigh, "Analogue IC Design: The current-mode Approach", Peregrinus, UK, 1990.

[40] G. Palmisano, G. Palumbo, S. Pennisi, "CMOS Current Amplifiers", Kluwer Academic Publishers, 1999.

[41] E. Abou-Allam, E.I. El-Masry, "A 200 MHz Steered current operational amplifier in 1.2-μm CMOS Technology", IEEE J. Solid-State Circuits, vol. 32, 1997, pp. 245-249.

[42] S. Jun, D.M. Kim, "Fully differential current operational amplifier", Elec. Lett., vol. 34, 1998, pp. 62-63.

[43] G. Palmisano, S. Pennisi, "Low-Voltage continuous-time CMOS current amplifier with dynamic biasing", Proc. ISCAS2001, pp. I-312-I-315.

[44] R.H. Zele, S. Lee, D.J. Allstot, "A high gain current-mode operational amplifier", Proc. ISCAS92, pp. 2852-2855.

[45] T. Kaulberg, "A CMOS current-mode operational amplifier", IEEE J. Solid-State Circuits, vol. 28, 1993, pp. 849-852.

[46] E. Bruun, "A high-speed CMOS current-mode op-amp for very low supply voltage operation", Proc. ISCAS94, pp.509-512.

[47] E. Abou-Allam, E.I. El-Masry, "High CMRR CMOS current operational amplifier", Elec. Lett., vol. 30, 1994, pp. 1042-1043.

[48] T. Shibata, T. Ohmi, "A Functional MOS Transistor Featuring Gate-Level Weighted Sum and Threshold Operations", IEEE Trans. Elec. Devices, vol. 39, 1992, pp. 1444-1455.

[49] M.A. Ibrahim, H. Kuntman, "A CMOS realization of inverting second generation current conveyor", Proc. 2002, NORDIC Signal Processing Symposium, 2002.

[50] M.T. Abdelma'Atti, N.A. Tasadduq, "New current-mode controlled filters using the controlled conveyor", Int. J. of Electronics, Vol.85, No.4, 1998, pp.483-488.

[51] U. Yodprasit, "High-precision CMOS current conveyor", Electronics Letters, Vol. 36, No. 7, March 2000, pp.609-610.

[52] B. Maundy, I. Finvers, P. Aronhime, "A low voltage CMOS current conveyor for active filter design", Proc. MWSCAS-1998, August, 1998.

[53] A. J. Lopez-Martin, J. Ramirez-Angulo, R. G. Carvajal, "Low-voltage low-power wideband CMOS current conveyors based on the flipped voltage follower", Proc. ISCAS2003, pp.I-801-804.

[54] K. Moolpho, J. Ngarmnil, K. Nundhasri, "A low-voltage wide-swing FGMOS current amplifier", Proc. ISCAS2002, May, 2002.

[55] T. Shibata, T. Ohmi, "A Functional MOS Transistor Featuring Gate-Level Weighted Sum and Threshold Operations", IEEE Trans. Elec. Devices, vol. 39, 1992, pp. 1444-1455.

[56] O. Naess, Espen A. Olsen, Y. Berg, T. S. Lande, "A low voltage second order biquad using pseudo floating-gate transistors", Proc. ISCAS2003, pp. I-125-128.

[57] J. Ramirez-Angulo, A. J. Lopez-Martin, R. G. Carvajal, C. Lackey, "Low-voltage closed-loop amplifier circuits based on quasi-floating gate transistors", Proc. ISCAS2003, pp.I-813-816.

[58] J. Ramirez-Angulo, C. Urquidi, R. G. Carvajal, A.Torralba, "Sub-volt supply analog circuits based on quasi-floating gate transistors", Proc. ISCAS2003, pp.I-781-784.

[59] I.A. Awad, A.M. Soliman, "Inverting second generation current conveyors: the missing building blocks, CMOS realizations and applications", Int. J. Electronics, Vol. 86, pp.413-432, 1999.

[60] H. Traff, "Novel approacch to high speed CMOS current comparators", Electronics Letters, Vol.28, No.3, pp.310-312, 1992.

[61] A.T.K. Tang and C. Toumazou, "High performance CMOS current comparator", Electronics Letters, Vol.30, No.1, pp.5-6, 1994.

[62] L.Ravezzi, D.Stoppaa and G.F. Dalta Betta, "Simple high-speed CMOS current comparator", Electronics Letters, Vol.33, No.22, pp.1829-1830, 1997.

[63] H. Lin, J.H. Huang and S.C. Wong, "A simple high-speed low current comparator", IEEE Trans. Circuit Syst., pp.713-716, 2000.

[64] B.M. Min and S.W. Kim, "High performance CMOS current comparator using resistive feedback network", Electronics Letters, Vol.34, No.22, pp.2074-2076, 1998.

# ผลลัพธ์จากโครงการวิจัยที่ได้รับทุนจาก สกว.

การนำผลงานวิจัยไปใช้ประโยชน์ในเชิงวิชาการโดยมี

การผลิตนักศึกษาระดับบัณฑิตศึกษาสองคน คือ

[1] นาย กฤษณพงศ์ นันทศรี ปริญญาวิศวกรรมศาสตรมหาบัณฑิต สาขาวิชาวิศวกรรมไฟฟ้า สาขาย่อยวิศวกรรมอิเล็กทรอนิกส์ สำเร็จปีการศึกษา พ.ศ. 2544

[2] นางสาว กรณิการ์ มูลโพธ์ กำลังจัดทำวิทยานิพนธ์ระดับปริญญาดุษฎีบัณฑิต สาขาวิชาวิศวกรรมไฟฟ้า สาขาย่อยวิศวกรรมอิเล็กทรอนิกส์

การนำเสนอผลงานในที่ประชุมวิชาการระดับนานาชาติ

[1] K. Nandhasri, J. Ngarmnil, "Designs of Analog and Digital Comparators with FGMOS", 2001 IEEE International Symposium on Circuits and Systems (ISCAS2001), Sydney, May, 2001.

[2] K. Moolpho, J. Ngarmnil, K. Nandhasri, "A low-voltage wide-swing FGMOS current amplifier", 2002 IEEE International Symposium on Circuits and Systems (ISCAS2002), Phoenix, May, 2002.

[3] K. Nandhasri, J. Ngarmnil, K. Moolpho, "A 2.8V RWDM BTL Class-D Amplifier using an FGMOS Comparator", 2002 IEEE International Symposium on Circuits and Systems (ISCAS2002), Phoenix, May, 2002.

[4] J. Ngarmnil, K. Nandhasri, K. Moolpho, "Floating-gate MOSFETs Analog Circuit Building Blocks: Design perspective", 2002 IEEE International Symposium on Communication and Information Technology, Thailand, October, 2002. (Invited paper)

[5] K. Moolpho, J. Ngarmnil, S. Sitjongsataporn, "A high speed low input current low voltage CMOS current comparator", 2003 IEEE International Symposium on Circuits and Systems (ISCAS2003), Bangkok, May, 2003.

[6] J. Ngarmnil, S. Ruengrungson and K. Nandhasri, 'A 100MHz ±0.75V FLOATING-GATE MOSFET CURRENT CONVEYOR', 2003 IEEE Midwest Symposium on Circuits and Systems (MWSCAS2003), Cairo, December, 2003.

# ภาคผนวก

[1] K. Nandhasri, J. Ngarmnil, "Designs of Analog and Digital Comparators with FGMOS", 2001 IEEE International Symposium on Circuits and Systems (ISCAS2001), Sydney, May, 2001.

# DESIGNS OF ANALOG AND DIGITAL COMPARATORS WITH FGMOS

*K. Nandhasri and J. Ngarmnil*

Electronic Engineering Department, Mahanakorn University of Technology, Bangkok, Thailand 10530

Email: jitkasame@ee.mut.ac.th

## ABSTRACT

Designs of analog and digital comparators are presented in this paper. We exploit the threshold voltage operation characteristic of floating-gate MOSFETs to produce a hysteresis-tunable analog voltage comparator. Consequently, the proposed analog comparator circuit is developed to a digital comparator using replacement of floating-gate MOSFETs for the input devices of which the drain currents are linear sums of the weighted multiple-input voltages which are then applied as binary bits. Simulation results on 1.2μm CMOS are demonstrated.

## 1. INTRODUCTION

Recently, many applications of floating-gate (FGMOS) devices in analog circuits have been reported [1]–[10]. However, in electronic systems, the voltage comparator is also a very widely used circuit element found in many applications. This paper presents designs for analog and digital comparators based on an exploitation of the FGMOS. A hysteresis-tunable analog comparator is constructed with an electronically tunable positive feedback factor obtained by threshold voltage tuning of the embedded FGMOSs. Recently, a design for an 8-bit digital comparator working in an analog fashion was proposed [1]. The circuit was intended for less complexity, size and improved speed. This paper also presents an alternative design of an 8-bit digital comparator featuring arithmetic functions of A>B and A≥B. The circuit essentially manipulates the proposed analog voltage comparator to produce a new digital circuit in which the signal is internally processed in an analog fashion. As a consequence, the new comparator is achieved by virtue of the analog technique.

## 2. FGMOS BASIC PRINCIPLES

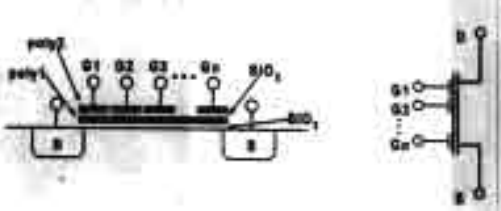



**Figure 1.** The FGMOS symbol

An FGMOS is an ordinary MOSFET except that the conventional gate on poly1 is floated. The equivalent structure, shown in Figure 1, comprises a floating gate on poly1 and input gates ($G_1$,..., $G_n$) built on poly2 which are coupled to the poly1 gate by the capacitors ($C_1$,..., $C_n$) between poly1 and poly2. With UV illumination, zero initial charge on the floating-gate can be assumed. In such a case, the drain current of the FGMOS can be written as

$$I_D = \frac{1}{2}\mu C_{ox}\frac{W}{L}\left[(k_1V_{G1}+\ldots+k_nV_{Gn})-V_S-V_{TH}\right]^2 \quad (1)$$

$$I_D = \frac{1}{2}\mu C_{ox}\frac{W}{L}\left[(k_1V_{G1}-V_S)-(V_{TH}-k_2V_{G2})\right]^2 \quad (2)$$

where $k_1$,..., $k_n$ are $C_1/C_T$,..., $C_n/C_T$ respectively and $C_T$ is the total capacitance of the floating gate. The drain current is essentially a linear sum of all the input voltages weighted by the capacitive coupling ratios. Furthermore, equation (1) can be rearranged to (2) in order to show the threshold operation when only two input gates are assumed. It is seen that $V_{G1}$ can be utilized as a signal port while $V_{G2}$ is used to tune the effective threshold voltage. These two features are exploited in this work.

## 3. HYSTERESIS ANALOG COMPARATOR

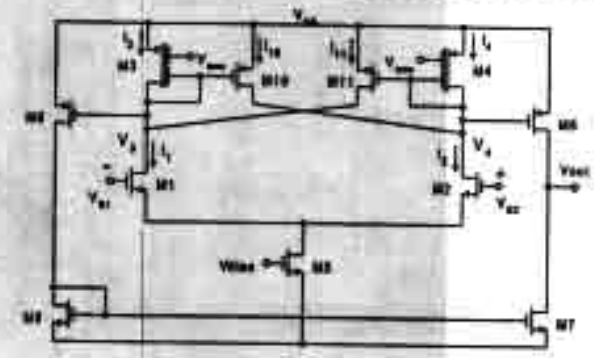



**Figure 2.** The Hysteresis Analog Comparator

A simple hysteresis analog comparator is well discussed in [11] and shown in altered form in Figure 2 where M3 and M4 are FGMOSs. The hysteresis involves two positive feedback paths provided by M10 and M11. The positive feedback occurs only when the current ratios of $I_{10}/I_3$ and $I_{11}/I_4$ are both greater than unity. If these ratios increase further, the feedback current will also increase resulting in wider positive and negative trip point voltages ($V_{TRP+}$ and $V_{TRP-}$). Hence the hysteresis can be controlled. An equation can be developed for $V_{TRP+}$ from the condition that whenever the circuit operates in the hysteresis loop, $I_2$ always equals $I_{10}$. Similarly for $V_{TRP-}$ with $I_1$ set equal to $I_{11}$. We have

$$V_{TRP+} = \sqrt{\frac{2I_3}{\beta_1}}\,\frac{\sqrt{I_{10}/I_3}-1}{\sqrt{1+I_{10}/I_3}}$$

$$V_{TRP-} = \sqrt{\frac{2I_3}{\beta_1}}\,\frac{\sqrt{I_{11}/I_4}-1}{\sqrt{1+I_{11}/I_4}} \quad (3)$$

where $\beta_1$ is the $\mu C_{ox}W/L$ for M1 which is identical to that of M2. Thus, from (2), by virtue of the FGMOSs, the ratios of $I_{D10}/I_{D3}$ and $I_{D11}/I_{D4}$ can be tuned electronically by the voltage $V_{tune}$ at the input gates $V_{G2}$ of M3 and M4. Hence $V_{TRP+}$ and $V_{TRP-}$ can be tuned orthogonally if the tuning voltage at the input gates of M3 and M4



0-7803-6685-9/01/$10.00©2001 IEEE

are different. M3 and M4 are designed with the areas of the two input gates equal to $10.8\times22.8\mu m^2$ while the conventional gate areas are set to $13.2\times2.4\ \mu m^2$, the same as those of M10 and M11. The circuit was simulated on HSPICE using 1.2μm AMI CMOS with assistance from the FGMOS macro model in [1] and supply voltage set to 5.0V. Figure 3 shows $V_{TRP+}$ and $V_{TRP-}$ vs. $V_{bias}$ varied in the range of 2.5-5.0V.

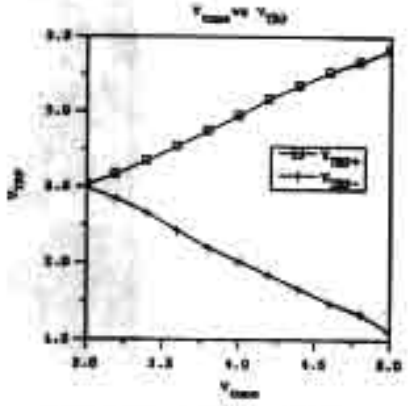


Figure 3. $V_{TRP+}$ and $V_{TRP-}$ vs. $V_{bias}$

Time-domain simulation was also performed to express the performance of the comparator in a noisy environment. The circuit was tested with a noise-modulated signal of which the noise amplitude set to $0.4V_{peak}$ while $V_{bias}$ was set to 3.8V. Simulation results are shown in comparison with those from a non-hysteresis comparator in Figure 4.

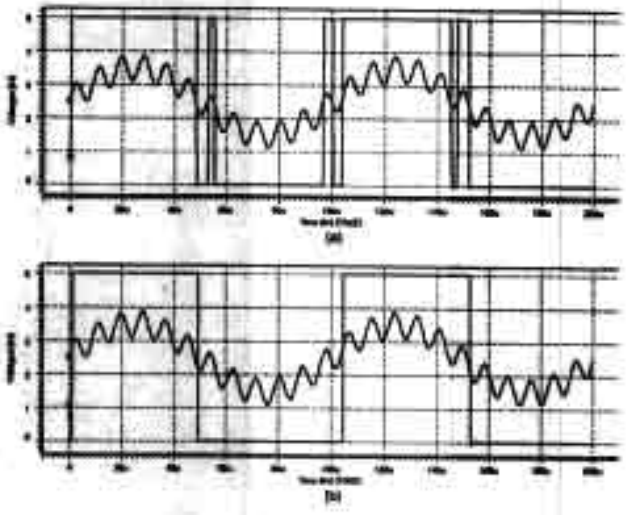


Figure 4. Comparison of results from (a) non-hysteresis and (b) hysteresis comparator

## 4. 4-BITs DIGITAL COMPARATOR

Based on the proposed opamp-based analog comparator, a new 4-bits digital comparator can also be realized by employing FGMOSs as the input devices. These 4-bit digital comparators are proposed separately as non-hysteresis and hysteresis types. Both circuits are further used for designing an 8-bit digital comparator that will be discussed in the next section. The non-hysteresis digital comparator is shown in Figure 5. It is seen that FGMOSs are employed as the input devices in order to exploit the drain current, which was written in (1) as a linear sum of the weighted multiple-input voltages that are basically binary bits of digital input data. Binary bits of '1' and '0' correspond to the voltage $V_{dd}$ and 0V at the input nodes respectively. The circuit is digital at the input and output but internally works as an analog circuit.

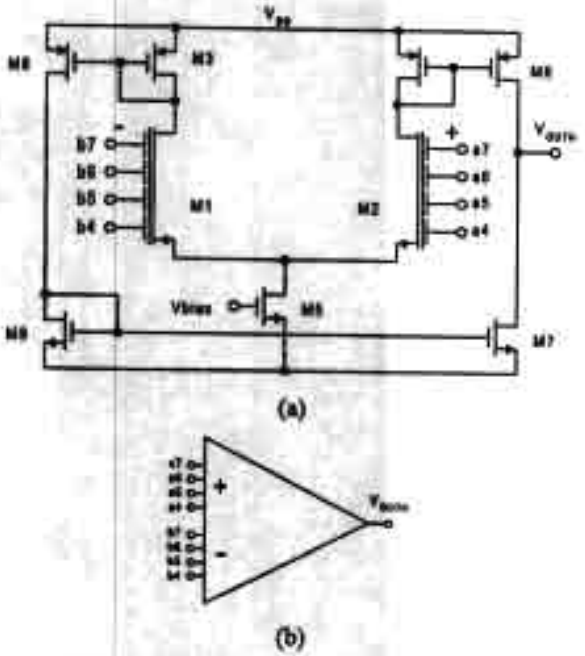



Figure 5. A Non-hysteresis 4-bit Digital Comparator

In Figure 5(a), the FGMOSs $M_1$ and $M_2$ are designed with the conventional gate areas of $12\times3\mu m^2$. Let $k_4,..,k_7$ be the weights of the input gates denoted as a4,..,a7 and b4,..,b7 respectively, where a4 and b4 are the least significant bits of this comparator. Then the input gates have the sizes set by the binary weights as in Table 1.

Table 1. Design parameters of the FGMOS

| | b4 | b5 | b6 | b7 |
|---|---|---|---|---|
| Binary weights | 1/16 | 1/8 | 1/4 | 1/2 |
| Sizes($\mu m^2$) | 10.8x22.8 | 21.6x22.8 | 43.2x22.8 | 86.4x22.8 |
| Capacitance(fF) | 159.7 | 319.5 | 638.9 | 1277.8 |

This non-hysteresis 4-bit comparator can be symbolically represented as in Figure 5(b). The circuit delivers three levels of output signal at $V_{OUT4}$. The output is logic High or $V_{dd}$ when the total weighted sum of the binary inputs at the positive terminal is higher than that of the negative terminal. The output is logic Low or GND when the total weighted sum of the binary inputs at the positive terminal is lower than that of the negative terminal. The output is $V_{dd}/2$ when the total weighted sums of the binary inputs of both terminals are equal. The latter function implies an ability to detect the equality of the binary inputs. The functionalities are confirmed by the simulation results in Figure 6.

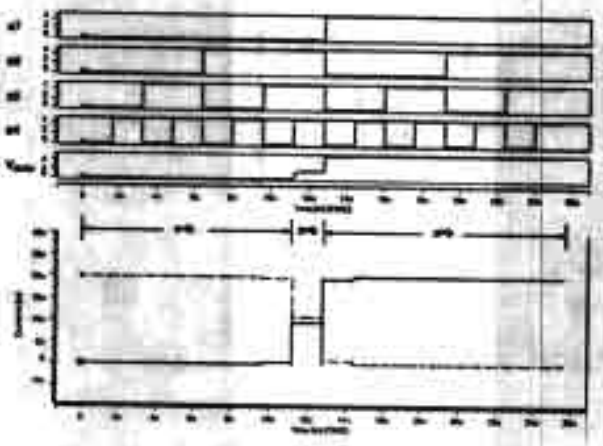
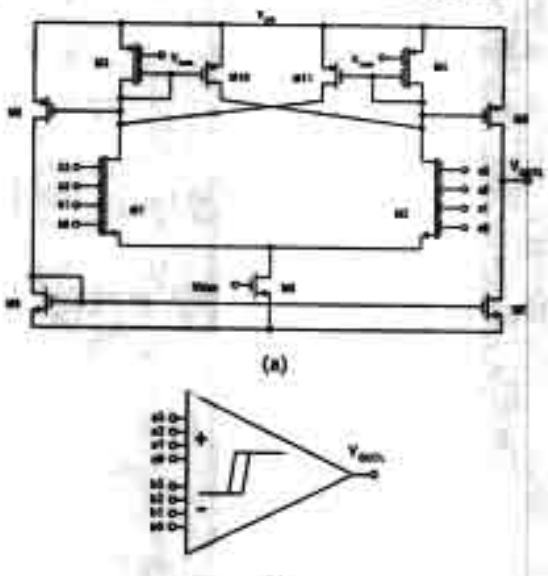


Figure 6. Results of the non-hysteresis 4-bit comparator

Figure 6 shows output signal as functions of $V_{OUTH}$ and drain currents of the input devices where the binary a7-a4 are swept digitally and the binary b7-b4 are set to #b0111. It is seen that the output voltage is at $V_{dd}/2$ and the input drain currents are equal when the binary a7-a4 equals to b7-b4. This property will also be utilized further in the design of the 8-bits comparator.

The hysteresis comparator shown in Figure 7 is similar to that of Figure 5 except that the hysteresis tuning part used in the analog comparator is employed. Because of the hysteresis operation, this circuit delivers only two levels of the output signal at high or low. As a result of the hysteresis tuning, the output signal is delivered according to the arithmetic functions of A>B or A≥B that are selected by the voltage $V_{tune}$. Using the same dimensions of all MOSFETs as in Figure5 and setting conventional gate areas of M3, M4 to 15×2.4μm$^2$, we set the input gate areas of both M3 and M4 for the input signal and for $V_{tune}$ to 77×31μm$^2$ and 11×31μm$^2$ respectively. The simulation results are shown in Figure 8.



(a)



(b)

Figure 7. Hysteresis 4-bit Digital Comparator

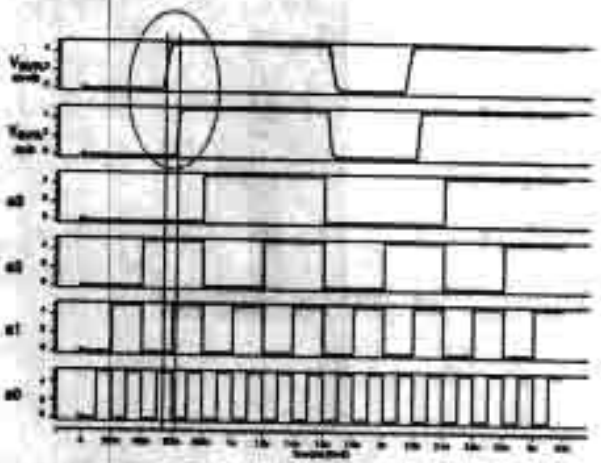


Figure 8. Simulation results of the hysteresis comparator

From Figure 8, the binary bits b3-b0 are set to #b0101 while the binary bits a3-a0 are swept digitally. It is seen that if $V_{tune}$ is set to High, the output signal $V_{OUTL}$ changes its stage when both binary sets are equal. The circuit performs the function A≥B. If $V_{tune}$ is set to Low, the comparator will perform the function A>B. In the next section, both hysteresis and non-hysteresis digital comparators will be combined in the design of an 8 bit digital comparator.

## 5. 8-BIT DIGITAL COMPARATOR

An 8-bit digital comparator is realized by using the two 4 bit comparators and another comparator as shows in Figure 9. The 8-bit binary inputs denoted as a7-a0 and b7-b0 can be defined as A and B respectively.

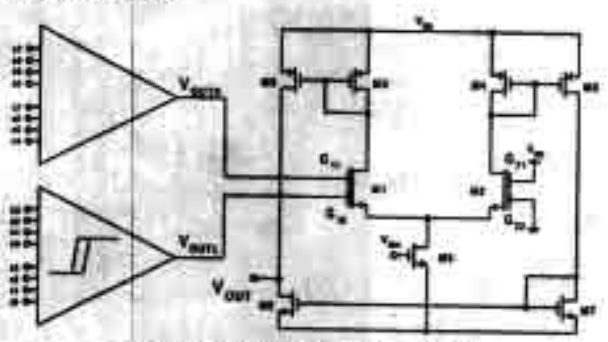


Figure 9. 8-bit digital comparator

It is seen that the 4-bit non-hysteresis comparator is used to compare the upper 4 bits where the three levels of output voltage at $V_{OUTH}$ are delivered when A>B, A<B or A=B. The 4-bit hysteresis comparator is used for the comparison of the lower 4 bits where only two levels of output voltage at $V_{OUTL}$ are delivered. The third comparator is used as the main comparator, of which the referenced input is connected to $V_{dd}$ and GND. The functions of the main comparator are summarised in table 2,

Table 2. Functions of the main comparator

| Upper 4 bits output | Lower 4 bits output | Output |
|---|---|---|
| High / $V_{dd}$ | X | High / $V_{dd}$ |
| Equal / $V_{dd}/2$ | High / $V_{dd}$ | High / $V_{dd}$ |
| Equal / $V_{dd}/2$ | Low / GND | Low / GND |
| Low / GND | X | Low / GND |

where X denotes don't care condition. It is seen that when the upper 4 bits of A are higher or lower than those of B, the output is High or Low immediately. If the upper 4 bits of A are equal to those of B, the output will correspond to the comparison result of the lower 4 bits of A and B. In order to have the functions correspond to Table 2, the main comparator must have the four input gates such as $G_{11}$, $G_{12}$, $G_{21}$, $G_{22}$ designed with proper sizes. The weights of each input are denoted as $k_{11}$, $k_{12}$, $k_{21}$, $k_{22}$, correspondingly, which are considered as in table 3.

**Table 3.** Sizing criteria for the main comparator

| Inputs | | Output | Weight sum operations |
|---|---|---|---|
| $V_{OUTH}$ | $V_{OUTL}$ | $V_{OUT}$ | |
| 5V | X | 5V | $k11\times5+k12\times0 > k21\times5+k22\times0$ <br> $\therefore k11 > k21$ |
| 0 | X | 0 | $k11\times0+k12\times5 < k21\times5+k22\times0$ <br> $\therefore k12 < k21$ |
| 2.5V | 0 | 0 | $k11\times2.5+k12\times0 < k21\times5+k22\times0$ <br> $\therefore k11 < 2\cdot k21$ |
| 2.5V | 5V | 5V | $k11\times2.5+k12\times5 > k21\times5+k22\times0$ <br> $\therefore k11+2\cdot k12 > k21$ |

where 5V and 0 stands for the logic High and Low and X denotes the don't care condition. Examining the weight sum operations, we can conclude that all weights must conform to the condition that $k_{21} < k_{11} < 2k_{21} < k_{11}+2k_{12}$. Suitable weights and sizes are summarised in Table 4.

**Table 4.** Design parameters of $G_{11}$, $G_{12}$, $G_{21}$, $G_{22}$

| | $G_{11}$ | $G_{12}$ | $G_{21}$ | $G_{22}$ |
|---|---|---|---|---|
| Binary weights | 12/16 | 4/16 | 7/16 | 9/16 |
| Sizes($\mu m^2$) | 129.6x22.8 | 43.2x22.8 | 75.6x22.8 | 97.2x22.8 |
| Capacitance(fF) | 1916.4 | 638.8 | 1117.9 | 1437.3 |

The functionalities can be demonstrated by the simulation results in Figure 10.

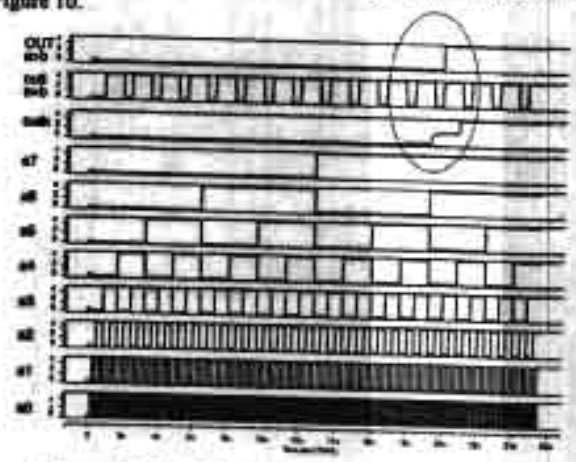


**Figure 10.** Simulation results of the 8-bits comparator

In Figure 10, the binary B is set to #b11000110 while the binary A is swept digitally from 0. It is seen that the $V_{OUTH}$ of the upper comparator delivers $V_{dd}/2$ when the upper 4-bits of the binary A equal those of B, and then the output corresponds to the $V_{OUTL}$ of the lower comparator.

## 6. CONCLUSIONS

A Hysteresis Tunable Voltage Comparator using FGMOS is proposed here. The circuit is essentially exploiting FGMOS devices in the positive feedback mode to create the hysteresis. The $V_{TH}$ tuneability of the FGMOS performs the hysteresis tuning effectively. This paper also presents a design for a non-clocked 8-bit digital comparator that essentially manipulates the proposed analog voltage comparator to realize a new digital circuit in which the signal is internally processed in an analog fashion. The proposed idea can be implemented on any standard double-poly CMOS and be useful in mixed signal and computational applications. All the simulation results confirm the functionality. The design optimizations will be determined in future studies.

## 7. REFERENCES


[1] Liming Yin, S. H. K. Embabi, E. Sanchez-Sinencio, "A floating-Gate MOSFET D/A Converter", *Proc. ISCAS'97*, Vol. 1, pp. 409-412, 1997.

[2] P. Hasler, B. A. Minch, and C. Diorio, "Floating-gate devices: they are not just for digital memories anymore", *Proc. ISCAS' 99*, Vol. 2, pp. 388-391, 1999.

[3] T. S. Lande, H. Ranjbar, M. Ismail, Y. Berg, "An analog floating-gate memory in a standard digital technology", *Proc.*, Fifth International Conference on Microelectronics for Neural Networks, pp. 271 -276, 1996.

[4] K. Yang and A. G. Andreou, "Multiple input floating-gate MOS differential amplifiers and applications for analog computation", *Proc. Midwest Symposium on Circuits and Systems*, Vol. 2, pp. 1212-1216, 1993.

[5] J. R. Angulo, S. C. Choi, G. G. Altamirno, "Low-Voltage Circuit Building Blocks Using Multiple-Input Floating-Gate Transistors", *IEEE trans. on Circuits and System, fundamental theory and applications*, Vol. 42, No. 11, pp. 971-974, Nov 1995.

[6] Y. Berg, T. S. Lande, "Tunable current mirrors for ultra low voltage" *Proc. ISCAS '99*, Vol. 2, pp. 17 -20, 1999.

[7] T. Ohmi, T. Shibata, "Intelligence implementation on silicon based on four-terminal device electronics", *Proc. MIEL'95*, Vol. 1, pp. 11 -18, Sep. 1995.

[8] H. R. Mehrvarz, C. Y. Kwok, "A large-input-dynamic-range multi-input floating-gate MOS four-quadrant analog multiplier", Digest of Technical Papers, *ISSCC' 95*, pp. 60 - 61, 1995.

[9] J.-J. Chen, S.-L. Liu, Y.-S. Hwang, "Low-voltage single power supply four-quadrant multiplier using floating-gate MOSFETs", *Proc. ISCAS' 97*, Vol. 1, pp. 237-240, 1997.

[10] J. R. Angulo, G. Gonzalez-Altamirano and S.C. Choi, "Modeling multiple-input floating-gate transistors for analog signal processing", *Proc. ISCAS' 97*, Vol. 3, pp. 2020 -2023, 1997.

[11] P. E. Allen, D. R. Hoberg, "CMOS Analog Circuit design", *Oxford Press*, NY, pp. 323-362, 1987.

[2] K. Moolpho, J. Ngarmnil, K. Nandhasri, "A low-voltage wide-swing FGMOS current amplifier", 2002 IEEE International Symposium on Circuits and Systems (ISCAS2002), Phoenix, May, 2002.

# A LOW-VOLTAGE WIDE-SWING FGMOS CURRENT AMPLIFIER

*K. Moolpho, J. Ngarmnil and K. Nandhasri*

Department of Electronic Engineering, Faculty of Engineering,
Mahanakorn University of Technology, Bangkok 10530, Thailand
Email: jitkasam@mut.ac.th

## ABSTRACT

This paper proposes a new current amplifier circuit totally formed in the class AB structure utilizing CMOS inverters and the recently proposed additive analog inverter using floating-gate MOSFETs. Operating in a negative feedback topology, the amplifier can deal with wide signal swings up to ±200μA, with 1% of the THD and 10pF of $C_L$. Designs and HSPICE simulation results are demonstrated on 0.5μm double poly CMOS processes with 1.5V and 1V power supplies to indicate high frequency and low power capabilities respectively.

## 1. INTRODUCTION

In the last decade, current-mode circuits [1] have drawn lots of interest due to their attractive features such as wide bandwidths, wide dynamic ranges and low voltage operations, all of which are very important for modern integrated circuits. Several elegant techniques for current-mode signal processing have been demonstrated successfully. These have mostly utilized current mirror cells, Gilbert gain cells and log-domain, square-root domain or translinear cells to perform filtering, multiplications, modulations, etc. For amplification purposes, current-mode amplifiers [2] based on a high open-loop current gain used for an accurate closed-loop configuration is also a very promising technique since use of a high gain device in a negative feedback loop allows large collection of transfer functions, performances of which are independent of the large but sensitive open-loop gain. So far, several high performance current amplifiers and opamps [3-9] have been proposed on CMOS technologies with various structures and topologies such as Differential Input Differential Output (DIDO), Differential Input Single-ended Output (DISO) or Single Input Differential Output (SIDO), etc. In general, the current opamp principle can be shown as a block diagram as in Fig.1, where the input current signal is firstly converted to a voltage quantity by the transimpedance amplifier (Rm) and then amplified again by the transconductance amplifiers (Gm) to produce the output current and hence the open-loop current gain. There is usually at least one high impedance node in the circuit that should be connected by a compensation capacitor for stability.

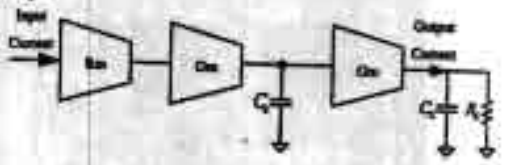


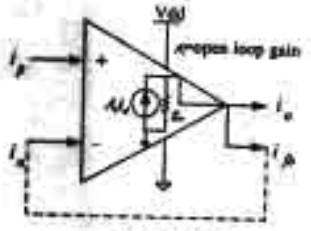

Fig.1 Current opamp principle

So far, most design efforts have been directed at the development of fully differential structures and enhancement of the open-loop gain and CMRR. In this work, we aim for a high signal swing by trying to avoid a class A circuit for which the limitation of current signal swing and slew rate is a result of the existing current sources, which also limit the charging current for the compensation capacitor at the high impedance node. Thus this paper proposes a new current amplifier circuit totally formed in the class AB structure utilizing CMOS inverters and the recently proposed additive analog inverter [10] using floating-gate MOSFETs. Since there is no biasing current source to limit the signal swing, our amplifier possesses a wide swing and high slew rate. The design is applied on a 0.5μm CMOS with 1.5 Volts power supply to demonstrate high frequency operation and with 1 Volt power supply to show the feasibility of low power operations at a lower frequency range where all MOSFETs are biased in the weak inversion region.

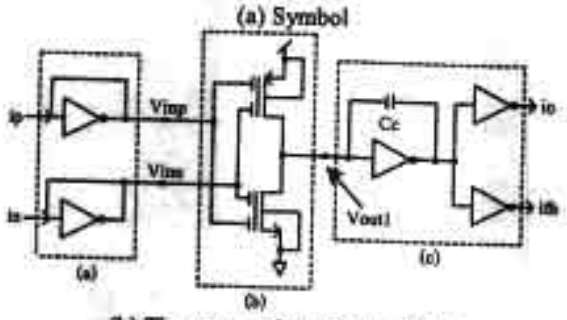
## 2. THE PROPOSED CURRENT AMPLIFIER

The proposed current amplifier, as symbolically shown in Fig.2(a), has two identical input terminals denoted as $i_p$ and $i_n$, and two output terminals delivering the same phase of the signal denoted as $i_o$ and $i_{fb}$, which are used as the output and the feedback port respectively. At the input terminals, it is noted that the input $i_n$ can only be symbolized as an inverting terminal when the amplifier is connected in the negative feedback configuration as shown by the dashed line. This will be discussed later in this section.

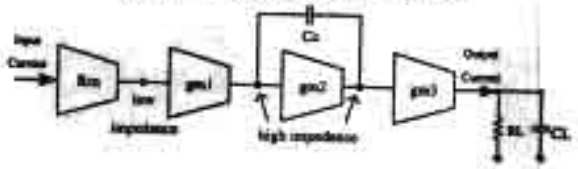
0-7803-7448-7/02/$17.00 ©2002 IEEE




(a) Symbol




(b) The proposed current amplifier




(c) Block diagram

Fig.2 The proposed current amplifier

In Fig.2(b), the amplifier comprises three circuit blocks as shown in the dashed boxes. The transimpedance amplifier is shown in box (a) and written as

$$Rm = \frac{1}{(gm_n + gm_p)} \quad (1)$$

where $gm_n$ and $gm_p$ are respectively the transconductance of NMOS and PMOS of the inverter . The additive analog inverter in box (b) is basically a two-input CMOS inverter elegantly built from the floating-gate MOSFETs and proposed in [3]. It is employed in this circuit together with the other Rm and gm blocks to work as a differential amplifier because the polarity of $i_n$ is inverse to those of $i_p$ causing the voltage at node $V_{inn}$ to be inverse to those at node $V_{inp}$. Considering only the NMOS, a large signal current equation can be written as in (2) where the coefficient of $V_{inn}$ is now negative.

$$I_D = \frac{1}{2}\mu C_{ox}\frac{W}{L}\left[\left(k_1 V_{inp} - k_2\left|V_{inn}\right|\right) - V_S - V_{TN}\right]^2 \quad (2)$$

Here k1 and k2 are the capacitive division factors [10, 11] $C_1/C_T$ and $C_2/C_T$, where $C_1$ and $C_2$ are the effective coupling capacitances between the input gates and the floating gate and $C_T$ is the total capacitance seen from the floating gate. All capacitances correspond directly to the sizes of the input gates and the floating gate areas obtained from the layout of the circuit. In this case, the equal input gate areas of $i_p$ and $i_n$ are set and result in equal values of $C_1$ and $C_2$ of 50fF and k1 and k2 of 0.5. The two-inputs CMOS inverter works as if a differential amplifier for which the small signal voltage gain between the output $V_{out1}$ and the differential inputs can be derived as

$$\frac{V_{out1}}{\left(V_{inp} - V_{inn}\right)} = -(gm_{1n} + gm_{1p})\left(r_{o1n} // r_{o1p}\right) \quad (3)$$

Here $r_{o1n}$ and $r_{o1p}$ are the respective output resistances to the floating-gate NMOS and PMOS in the dashed box (b) . With further analysis using the diagram in Fig.2(c), the open-loop current gain of the whole circuit can be derived as

$$A_i = Rm \cdot gm_1 r_{o1} gm_2 r_{o2} gm_3 \quad (4)$$

and the dominant pole frequency($\omega_d$) is

$$\omega_d = \frac{1}{r_{o1} gm_2 r_{o2} C_C} \quad (5)$$

while the GBW is

$$GBW = \frac{Rm \cdot gm_1 gm_3}{C_C} \quad (6)$$

## 3. DESIGN AND SIMULATIONS

Based on the proposed concept, the design schematic can be simplified as shown in Fig.3, where it is seen that the circuit can be designed in a modular fashion where all inverters including the additive analog inverter have the same dimensions of NMOS and PMOS correspondingly. If a higher gain of the $gm_2$ and $gm_3$ blocks is required, we simply add more cells of the identical inverters in parallel. $R_C$ and $C_C$ are employed for the frequency compensation.

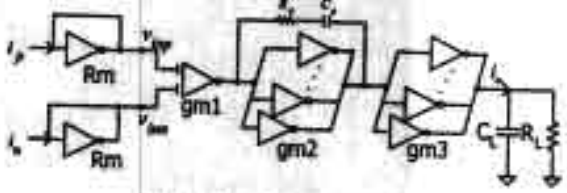
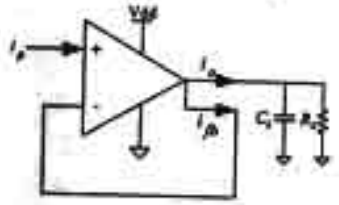


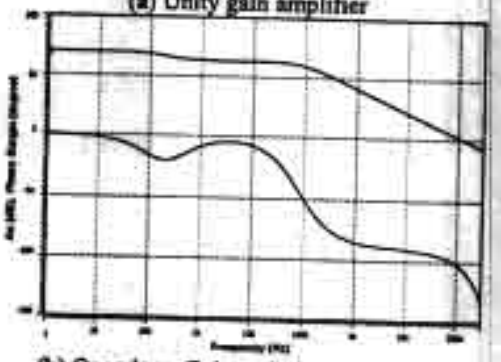

Fig.3 The design Schematic

On the Alcatel 0.5μm CMOS process, two amplifiers have been designed for $V_{DD}$ of 1.5V and 1V to demonstrate high frequency operations and low power respectively. With $V_{DD}$ of 1.5V, all NMOS and PMOS are designed with the dimensions of 6.9/0.5 and 23.6/0.5 respectively resulting in the idle currents of 30μA for each inverter. As seen in Fig.3, only one CMOS inverter is employed for each Rm and gm1 block but extra input gates on Poly2 are connected to the inverter of the gm1 block. Then four and three inverters connected in parallel are employed for the $gm_2$ block and the $gm_3$ block respectively. The amplifier is loaded with $C_L$ of 10pF and $R_L$ of 1.69k Ω that is the same value as Rm or its input resistance. To improve the phase

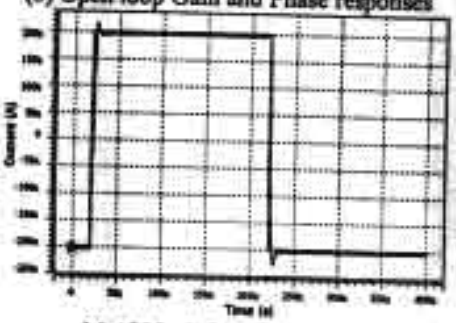
margin, $R_C$ of 1k Ohms and $C_C$ of 0.8pF are also included in the compensation scheme. The circuit was simulated on HSPICE with the performances shown in Fig.4 where 69.6dB Open-loop gain, 127MHz GBW and 74° Phase margin were achieved with a supply voltage of 1.5Volts and 635μW of power consumption. As a unity gain buffer, step response and linearity were measured at the maximum signal amplitude of ±200μA and are shown in Fig.4(d) and (e) where the 1% settling times are measured as 9.4 and 34.5 ns with and without $C_L$ respectively.



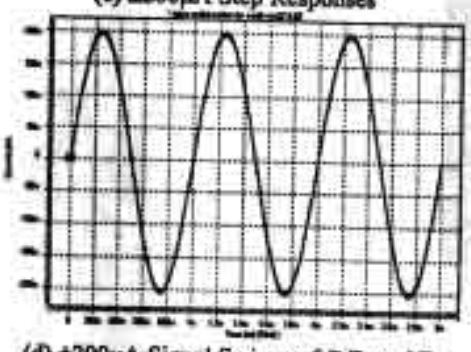
(a) Unity gain amplifier



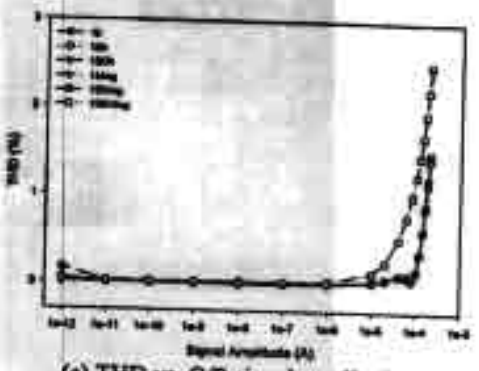
(b) Open loop Gain and Phase responses



(c) ±200μA Step Responses



(d) ±200μA Signal Swings of O/P vs. I/P



(e) THD vs. O/P signal amplitude

Fig.4 Simulation results

Another amplifier with a 1V power supply was designed including all NMOS and PMOS with the dimensions of 8/0.5 and 19.9/0.5 respectively operated in the weak inversion region. As in Fig.3, only one CMOS inverter is employed for each Rm and gm1 block. Then five and two inverters connected in parallel are employed for the $gm_2$ block and the $gm_3$ block respectively. The amplifier is loaded with $C_L$ of 10pF and $R_L$ of 47.86kΩ. From simulations, an open-loop gain of 68.3dB, with 2.68MHz GBW and 68° phase margin is achieved with 6μW power consumption. Due to space restrictions, not all performance graphs could be included here. However, in Table 1 all performances are compared with those of some earlier designs. The 1.5V $V_{DD}$ version amplifier is also tested in negative feedback structure with passive networks to set the closed loop gains higher than 1 as shown in Fig.5.

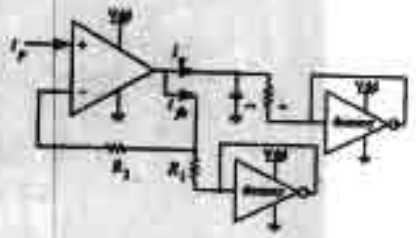


Fig.5 The amplifier in negative feedback

Fig.5 displays a non-inverting amplifier with a resistive negative feedback network. We arbitrarily put the dummy shorted input-output inverters to work as resistive loads and also to set the DC offset voltage to half of the $V_{DD}$ which is the same DC voltage at all input and output nodes. Then the closed loop gain can be derived as

$$A_{CL} = 1 + \frac{R_2 + Rm}{R_1 + Rm} \qquad (7)$$

where $R_1$ and $R_2$ are the resistances in the range of 0~10kΩ which are integrable value on a chip. The dummy inverter load is used to settle a proper dc level in order to avoid DC offset of the feedback current. From (7), Rm

with $R_1$ is the transimpedance of the dummy inverter while Rm with $R_2$ is the input resistance of the $i_{in}$ terminal. Hence all Rms are the same value. With $V_{DD}$ of 1.5V, by setting $R_1$ at 10Ω and adjusting $R_2$ for various close-loop gains, the THD of the O/P signal were measured and shown in Fig.6 where the labels in the plot show details of the input signals.

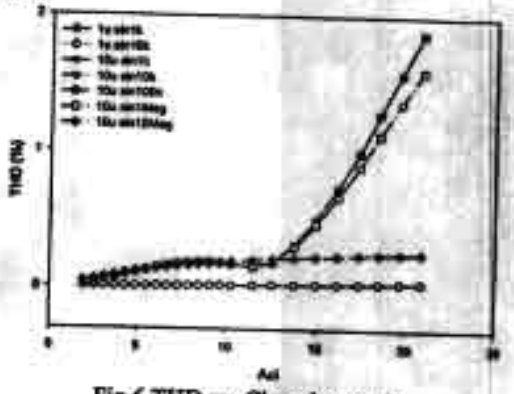


Fig.6 THD vs. Close-loop gain

## 4. CONCLUSION

This paper has proposed a new low voltage wide swing current amplifier that can receive a signal swing as large as ±200μA amplitude while a THD of about 1% is still maintained. The circuits can totally be realized in the class AB thanks to the use of CMOS inverters and the available additive analog inverter cells using floating-gate MOSFETs. An effect of complex poles and zeros around the 100Hz of the open loop gain in Fig.4 (a) can be noticed as a result from the coupling capacitors of the FGMOS devices. A deep analysis will be placed as future works. In this paper, the circuit is called a current amplifier instead of opamp due to the lack of CMRR capability, which will be part of our future works.

## 5. REFERENCES


[1] C. Toumazou, F.J. Lidgey, D. Haigh, "Analogue IC Design: The current-mode Approach", Peregrinus, UK, 1990.

[2] G. Palmisano, G. Palumbo, S. Pennisi, "CMOS Current Amplifiers", Kluwer Academic Publishers, 1999.

[3] E. Abou-Allam, E.I. El-Masry, "A 200 MHz Steered current operational amplifier in 1.2-μm CMOS Technology", IEEE J. Solid-State Circuits, vol. 32, 1997, pp. 245-249.

[4] S. Jun, D.M. Kim, "Fully differential current operational amplifier", Elec. Lett., vol. 34, 1998, pp. 62-63.

[5] G. Palmisano, S. Pennisi, "Low-Voltage continuous-time CMOS current amplifier with dynamic biasing", Proc. ISCAS2001, pp. I-312-I-315.

[6] R.H. Zele, S. Lee, D.J. Allstot, "A high gain current-mode operational amplifier", Proc. ISCAS92, pp. 2852-2855.

[7] T. Kaulberg, "A CMOS current-mode operational amplifier", IEEE J. Solid-State Circuits, vol. 28, 1993, pp. 849-852.

[8] E. Bruun, "A high-speed CMOS current-mode op-amp for very low supply voltage operation", Proc. ISCAS94, pp.509-512.

[9] E. Abou-Allam, E.I. El-Masry, "High CMRR CMOS current operational amplifier", Elec. Lett., vol. 30, 1994, pp. 1042-1043.

[10] Y. Berg, O. Naess, M. Hovin, "Ultra low voltage floating-gate transconductance amplifier with tunable gain and linearity", Proc. ISCAS2000, pp. III-343-346.

[11] T. Shibata, T. Ohmi, "A Functional MOS Transistor Featuring Gate-Level Weighted Sum and Threshold Operations", IEEE Trans. Elec. Devices, vol. 39, 1992, pp. 1444-1455.



Acknowledgement: This work has been supported by a grant from the Thailand Research Fund (TRF). Authors would like to thank the TRF for their precious support.


**TABLE 1 PERFORMANCE COMPARISONS**

| COA | [3]± | [3]⊗ | [4]± | [5]± | [6]± | [6]⊗ | [7]⊗ | [8]± | [9]± | Proposed | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Years | 1997 | 1997 | 1998 | 2001 | 1992 | 1992 | 1993 | 1994 | 1994 | 2001 | | - |
| DC Gain | 65 | 70 | 53 | 80 | 65 | 54 | 72 | 94.2 | 67 | 69.6 | 68.3 | dB |
| UGBW | 200 | 210 | 300 | 16 | 8 | 90 | 3 | 65 | 100 | 127 | 2.58 | MHz |
| FM | 60 | >45 | 50 | 68 | 60 | 60 | 60 | ~40 | 61 | 74 | 60 | ° |
| Input Resistance | 0.147 | 2 | 21 | NA | 3.65 | 5 | NA | 5.8 | 316 | 1.68 | 47.86 | KΩ |
| Output Resistance | 2.8 | 2 | 0.597 | NA | 0.899 | 0.186 | NA | 7.6 | 0.3 | 0.09 | 0.847 | MΩ |
| Settling Time (1%) | 5.1 | NA | 7.1 | 100 | 150 | 15 | NA | NA | NA | 34.5*1 | 240*2 | ns |
| Slew rate +/- | NA | NA | NA | +0.4 | NA | NA | NA | NA | NA | +145/ -170 | +0.078/ -0.1 | μA/ns |
| Rc | NA | NA | NA | NA | NA | NA | NA | NA | NA | 1 | 0.9 | KΩ |
| Cc | NA | NA | NA | 1.5 | 10 | 1.25 | 2 | NA | NA | 0.8 | 1 | pF |
| RL | NA | NA | NA | 1 | NA | NA | NA | NA | NA | 1 | 2.5 | KΩ |
| CL | NA | NA | NA | NA | NA | NA | NA | NA | NA | 10 | 10 | pF |
| Power Dissipation | NA | 4.5 | <0.86 | NA | 3.1 | 4.6 | NA | 0.03 | 4.5 | 0.635 | 0.006 | mW |
| Technology(CMOS) | 1.2 | 1.2 | 0.6 | 0.8 | 2 | 2 | 2.4 | 2 | 1.2 | 0.5 | 0.5 | μm |
| Supply | ±3 | ±3 | 3 | 1.2 | NA | NA | NA | NA | 3 | 1.5 | 1.0 | V |

± = Simulation results, ⊗ = Measured results, NA = not available, *1 = at ±200μA step i/p, *2 = at 4μA step i/p

[3] K. Nandhasri, J. Ngarmnil, K. Moolpho, "A 2.8V RWDM BTL Class-D Amplifier using an FGMOS Comparator", 2002 IEEE International Symposium on Circuits and Systems (ISCAS2002), Phoenix, May, 2002.

# A 2.8V RWDM BTL CLASS-D POWER AMPLIFIER USING AN FGMOS COMPARATOR

*K. Nandhasri, J. Ngarmnil and K. Moolpho*

Department of Electronic Engineering, Faculty of Engineering,
Mahanakorn University of Technology, Bangkok 10530, Thailand
Phone & Fax (662) 9883655 Ext.239, Email: krissana@mut.ac.th, jitkasam@mut.ac.th

## ABSTRACT

This paper presents a design of an output stage based on Class-D amplifier techniques using Rectangular Wave Delta Modulation (RWDM) topology. This amplifier has a simple structure comprised only of a hysteresis comparator and output drivers. Thanks to the use of a multiple inputs hysteresis comparator using floating-gate MOSFETs, the amplifier is capable of low voltage operations. On Alcatel 0.5μm double poly CMOS process, this amplifier demonstrated to deliver up to 0.88Watts with 95% efficiency with a 2.8 Volts power supply. This means implementation as a monolithic chip is possible, making this amplifier suitable for portable applications such as speaker driving circuits in mobile phones, hearing aids and other implantable medical devices.

## 1. INTRODUCTION

Many audio power amplifiers are designed in class-A or class-AB, and so they normally deliver a limited efficiency because their power transistors operate in the linear area where a huge biasing or idle current is normally consumed in order to be able to deliver enough power to the loads. This then results in excessive power dissipation or heat. In order to improve the efficiency, switching converter techniques such as Pulse Width Modulation (PWM) can be applied to the development of audio amplifiers, referred to as switching amplifiers or class-D type [1,2]. This type of amplifier presents several advantages over conventional class-A or AB amplifiers in their high efficiency and low internal power dissipation. In this work we present the development of a class-D amplifier based on the RWDM technique [3] utilizing a multiple input hysteresis voltage comparator using floating-gate MOSFETs to allow low voltage operation for the amplifier. The circuit is then suitable for production as a monolithic chip for battery-operate applications such as speaker driving circuits in mobile phones, hearing aids and other implantable medical devices. Designs and simulation results will be discussed in detail below.

## 2. CLASS-D AMPLIFIER

Conventionally, most class-D amplifiers are based on the Pulse Width Modulation (PWM) technique where the pulse width of the output PWM signal produced is proportional to the amplitude of the modulating signals between the audio input signal and the triangular signal. The signal at the output is recovered from the PWM signal by a low pass filter, which could be formed by a loaded resistor and an inductor inherently obtained from earphones or speakers. Fig.1 shows the basic building blocks of a conventional class D amplifier comprising triangular waveform generator, comparator and output driving stage.

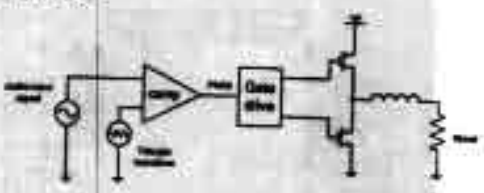


Fig. 1 Conventional PWM class-D amplifier

From Fig.1, the comparator compares the audio signal input with the triangular waveform from the waveform generator to produce a PWM signal, which is then used to control the switching timing of the output stage transistors to drive a low impedance load. The output power delivered to the load is proportional to the average output current controlled by the duty cycle of the PWM signal. The duty cycle is 50% when there is no signal at the input, thus the average output voltage is zero. PWM class-D amplifiers can dissipate less power by properly arranging the switching timing of the output power MOSFETs between the two lowest-dissipation modes such as fully on and fully off.

Another promising technique used in class-D amplifiers is the RWDM principle shown in Fig.2. In concept RWDM is similar to PWM except that the input signal denoted as $V_{in}(t)$ is compared with the feedback signal $V_{\Delta}(t)$ which is essentially the integrated signal of RWDM by a low-pass filter. Hence loading conditions from the loads are taken into account to control the RWDM signal and then to control the output power. Since there is a hysteresis in the

0-7803-7448-7/02/$17.00 ©2002 IEEE

comparator, $V_s(t)$ can track the amplitude of $V_R(t)$ within the $\pm\Delta V$ boundary as shown in Fig.2.

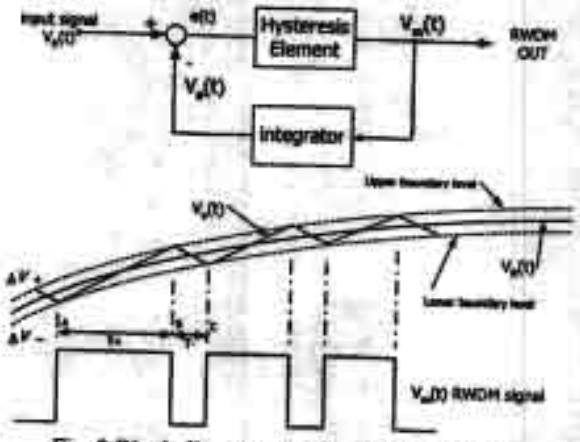



Fig. 2 Block diagram of the RWDM technique

Based on the RWDM mechanism in Fig.2, the switching frequency of the RWDM output signal can be calculated as in (1)

$$f = \frac{1}{T} = \frac{S_C}{4\Delta V}\left[1-\left(\frac{S_R(t)}{S_C}\right)^2\right] \qquad (1)$$

where $S_R$ and $S_C$ denote the slopes of the input signal $V_R(t)$ and the feedback signal $V_s(t)$ respectively and $\Delta V$ is the tracking boundary corresponding to the magnitude of the hysteresis loop which is controlled directly by the trip voltage of the hysteresis comparator. $S_C$ is also controlled by the time constant of the integrator in the feedback path.

## 3. THE PROPOSED RWDM CLASS-D AMPLIFIER

A new proposed class-D amplifier based on the RWDM technique is presented as a block diagram in Fig.3, where it is seen that the amplifier comprises only a hysteresis comparator, driving circuits and an integrator formed by the resistor inductor low-pass network. The circuit can be integrated onto a monolithic chip except for the inductor and the load resistor.

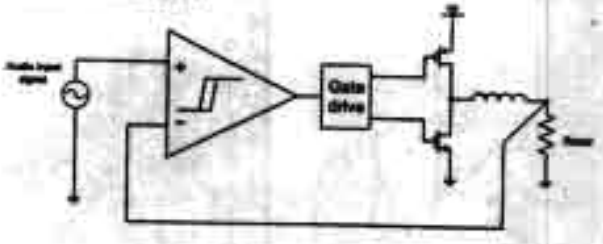



Fig.3 The Proposed Concept

From Fig.3 the audio input signal is directly connected to the input of the comparator, which is basically a high impedance node since it is the input gate of a MOSFET. Hence no loading of the signal source occurs. The comparator then compares the input signal with the feedback signal from the output. With the built-in hysteresis loop, the comparator can produce the output RWDM signal comprising only logic low or high that is then integrated by the inductor resistor network. The feedback signal as a saw-tooth-like signal is then used to compare with the input signal in the next cycle.

### 3.1 The Hysteresis Comparator

The hysteresis can be shown as the range between $V_{TRP+}$ and $V_{TRP-}$ as in Fig.4. In this paper, we expand the switching range of a hysteresis comparator to control the amount of output ripple and switching frequency of the Class-D amplifier.

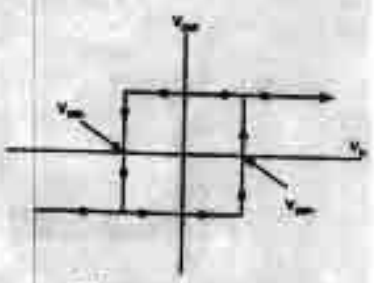


Fig.4 Hysteresis loop

An example of the hysteresis comparator [4, 5] is shown in Fig.5, where it is seen that the hysteresis is generated from a positive feedback produced by M10 and M11. The positive feedback occurs only when the current ratio of $I_{D10}/I_{D8}$ or $I_{D11}/I_{D4}$ is greater than one.

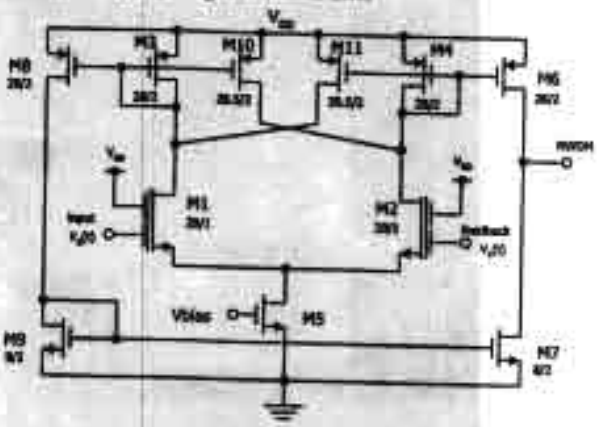



Fig.5 Rail to rail input hysteresis comparator

The hysteresis comparator shown in Fig.5 is able to receive a wide-range input signal. This particular ability is

achieved by the employment of the two-inputs floating-gate MOSFETs (FGMOS) [5, 6] as the input transistors M1 and M2 of the differential amplifier. This characteristic allows the feedback signal at the gate of M2 to track the amplitude of the input signal at the gate of M1 effectively between the supply voltage and ground. Hence low voltage operation is possible. This is results because one of the input gates of both M1 and M2 are connected to Vdd, so both FGMOSs M1 and M2 are ensured to be be turned on at all levels of the input signal. In other words, the comparator basically possesses the rail-to-rail characteristic.

### 3.2 FGMOS Basic Principles

FGMOS is an ordinary MOSFET except that the gate, which is built on the conventional poly1, is floating and then called 'Floating-Gate'. The structure of FGMOS is shown in Fig.6.

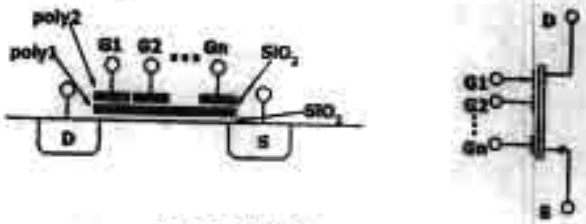



Fig.6 FGMOS structure

A multiple input MOSFET based on the FGMOS structure [6,7] is shown in Fig.6. It comprises the floating gate, and input gates (G1, G2) built on Poly2, which are coupled to the Poly1 gate by the capacitors between Poly1 and Poly2 denoted as $C_1$ and $C_2$. Assuming zero initial charge on the floating-gate, the drain current can be written as

$$I_D = \frac{1}{2}\mu C_{ox}\frac{W}{L}\left[(k_1 V_{G1} - V_S) - (V_{TN} - k_2 V_{G2})\right]^2 \qquad (2)$$

$$I_D = \frac{1}{2}\mu C_{ox}\frac{W}{L}\left[(k_1 V_{G1} + k_2 V_{G2}) - V_S - V_{TN}\right]^2 \qquad (3)$$

where $k_1$ and $k_2$ are $C_1/C_T$ and $C_2/C_T$ respectively and $C_T$ is the total capacitance of the floating gate. The drain current is essentially a linear sum of all inputs weighted by the capacitive coupling ratios. Equation (2) is arranged to show the threshold operation with only two input gates assumed. It is seen that $V_{G1}$ can be utilized as a signal port while $V_{G2}$ is used to tune the effective threshold voltage. Equation (3) is written to show a linear sum of the weighted multiple-input voltages. This operation ensures the comparator has the capability to handle large input signal swings while it still operates in the saturation region as mention before.

## 4. THE PROPOSED RWDM BTL CLASS-D

A Bridge Tied Load (BTL) class-D amplifier based on the RWDM technique is presented in Fig.7. It is basically a fully differential version of the proposed RWDM concept shown in Fig.3. With the BTL configuration the output voltage swing can be double those of the half-bridge configuration in Fig.3. The audio input signal is directly connected to the input of the comparator, which is normally in the range of 0–$V_{DD}$ so we use 3-inputs floating-gate MOSFETs as the input differential pairs of the hysteresis comparator.

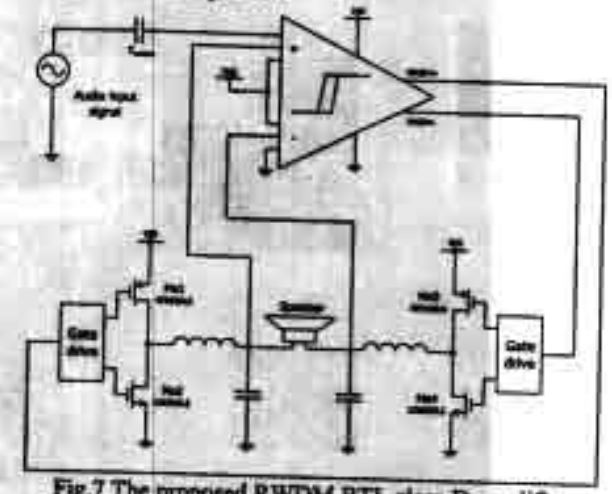


Fig.7 The proposed RWDM BTL class-D amplifier

In Fig.8, the 3-inputs fully differential hysteresis comparator comprises three-input gates FGMOS devices as the differential pairs of which the coupling capacitors are designed as $C_1$=200fF, $C_2$=128fF and $C_3$=64fF which correspond to the capacitive coupling ratios of k1, k2 and k3 to 0.5, 0.32 and 0.16 respectively. The first inputs of both plus and minus terminals having the weight factor of 0.5 are connected to $V_{DD}$ to bias the differential pairs. This results in a DC potential of $0.5V_{DD}$ at the floating-gate on Poly1 of the differential pairs. The 2nd input gates having weight of 0.32 are used as the inputs of the comparator while the 2nd gate of M1 is connected to the AC-coupled audio input signal and the 2nd gate of M2 is connected to Gnd. The weights of the 2nd inputs allow a wide input swing for the comparator. The 3rd input gates with the weight of 0.16 are connected to output nodes of the amplifier respectively. They are designed with half of the weight factor of the 2nd gates in order to make the close loop gain of the amplifier equal to 2, which is the requirement to have an output signal swing of +/- 2.8V while the input signal swing is only in the range 0–2.8V. The other advantage of this fully differential comparator is that the RWDM output signals from the comparator are exactly out of phase without any delay. The control of the

power MOSFETs of both sides of the loads will be very precise. Dimensions of all MOSFETs are also shown in the figure.

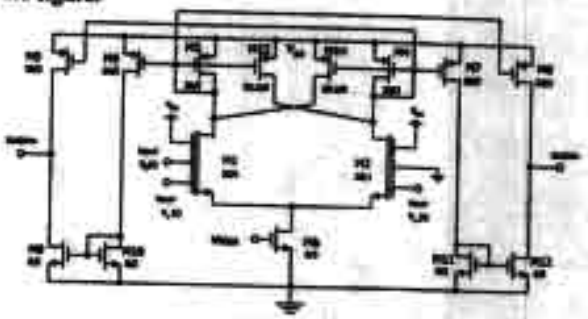


Fig.8 Fully differential comparator

## 5. SIMULATION RESULTS

Based on the proposed circuit in Fig.7, the amplifier has been designed on Alcatel 0.5μm CMOS process with 2.8 Volts power supply. The amplifier can deliver current to the 8Ω resistive loads and correspond to the output signal of $5.2V_{p-p}$. Other performances based on simulation results on HSPICE are summarized in Table 1.

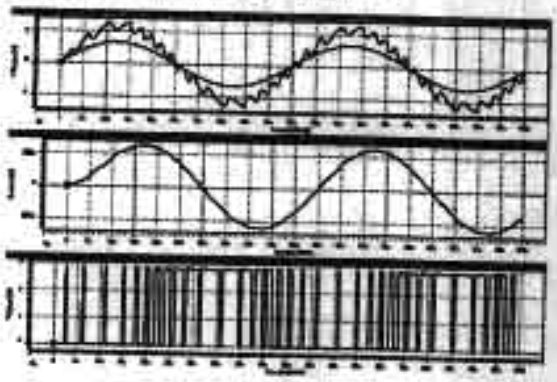


Fig.9 The voltage output signal, the current output signal and the RWDM output signal at input $1.3V_p$, 20kHz

Table 1 Summary of the proposed amplifier

| | |
|---|---|
| Process technology | Alcatel 0.5μm CMOS |
| Supply voltage | 2.8V |
| Static Power dissipation | 79.51μW |
| Maximum output swing | $5.2V_{p-p}$ |
| Output load | 8Ω |
| Maximum power | 0.88W |
| Efficiency | 95% |

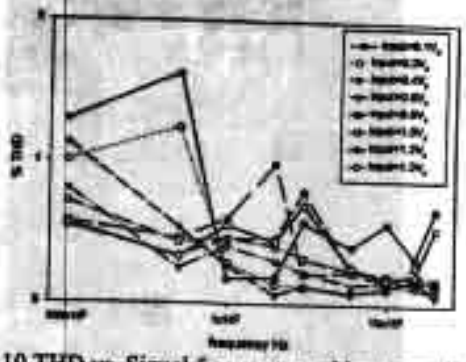


Fig.10 THD vs. Signal frequency and input amplitude

## 6. CONCLUSIONS

A single-chip low-voltage high-efficiency Class-D Power Amplifier for portable devices has been proposed The amplifier has a very simple architecture that makes it easier for it to be integrated with other circuit blocks on a system level. By virtue of the high efficiency of Class-D architecture coupled with the low voltage operation provided by the use of floating-gate MOSFET hystereais comparator, this amplifier is suitable for portable devices with battery operations. It exhibits high distortion at low input signal due to the small changing of the input signal compared to the ripple at the output. The efficiency of this circuit is 95% at 0.88Watt with a 2.8V power supply.

## 7. REFERENCES


[1] D. L. Schilling, C. Belove, "Electronic Circuits Discrete And Integrated", 3rd edition, McGraw-Hill, 1989.

[2] B. Duncan, "High Performance Audio Amplifiers", Newnes, 1996.

[3] L. Kitjalak, P. Pawawongsak, "DSP Application for RWDM Inverters", The 22nd Electrical Engineering Conference, Bangkok, 1999, pp. 541-544.

[4] P.E. Allen, D.R. Hoberg, "CMOS Analog Circuit design", Oxford Press, NY, 1987, pp.323-362.

[5] K. Nandhasri, J. Ngarmnil, "Designs of Analog and digital Comparators with FGMOS", Proc.ISCAS2001, Vol.1, pp. 25-28.

[6] K. Yang and A. G. Andreou, "Multiple input floating-gate MOS differential amplifiers and applications for analog computational", Proc. MWSCAS, Vol.2, 1993, pp.1212-1216.

[7] J. R. Angulo, G. Gonzalez-Altamirano and S.C. Choi, "Modeling multiple-input floating-gate transistors for analog signal processing", Proc. ISCAS97, Vol. 3, pp. 2020 -2023.

[8] Sung-Mo Kang, Yusef Leblebici, "CMOS digital integrated circuits analysis and design", McGraw-Hill, 1996.

[9] Choi et al, "A design of a 10-W single-chip class D Audio amplifier with very high efficiency using CMOS technology", IEEE Trans. Consumer Electronics, Vol. 45, No.3, Aug 1999.



Acknowledgement: This work has been supported by a grant from the Thailand Research Fund (TRF). The authors would like to thank the TRF for their precious support.

[4] J. Ngarmnil, K. Nandhasri, K. Moolpho, "Floating-gate MOSFETs Analog Circuit Building Blocks: Design perspective", 2002 IEEE International Symposium on Communication and Information Technology, October, 2002.

# FLOATING-GATE MOSFETS ANALOG CIRCUIT BUILDING BLOCKS: DESIGN PERSPECTIVE

*J. Ngarmnil, K. Nandhasri and K. Moolpho*

Department of Electronic Engineering, Faculty of Engineering,
Mahanakorn University of Technology, Bangkok, 10530, Thailand
Email: jitkasam@mut.ac.th

## ABSTRACT

Floating-gate MOSFET on a standard double-poly CMOS offers various new useful functions which can be used to create many novel circuits in both analog and digital circuits. This paper reviews some recently proposed FGMOS circuits, such as a hysteresis tunable voltage comparator, analog-based digital comparators, a low-voltage class AB current-mode amplifier circuit and its filtering application. Designs and HSPICE simulation results are demonstrated on standard double poly CMOS processes.

## 1. INTRODUCTION

Recently, many applications of Floating-gate MOSFET or FGMOS devices in analog circuits have been reported [1-6]. Normally playing a key role in modern integrated memories such as EEPROM and Flash, FGMOS has some unique characteristics which could be applied to design many new circuits or to enhance existing analog circuits for having extra special features such as very low voltage, low power and high complexity functions. This paper reviews the recently proposed analog and digital comparators based on an exploitation of the FGMOS. First, a hysteresis tunable analog comparator is constructed with an electronically tunable positive feedback factor obtained by threshold voltage tuning of the embedded FGMOS devices. Then, digital comparators are developed by essentially modifying the proposed analog voltage comparator to be a new digital circuits in which signal are internally processed with analog mechanism. Moreover, a high open-loop gain current amplifier circuit totally formed in the class AB structure utilizing CMOS inverters and floating-gate MOSFETs is also reviewed with its attractive features such as wide bandwidths, wide dynamic ranges and low voltage operations. Based on the high open loop gain amplifier, a single amplifier biquad is designed and demonstrated as an application of the proposed current amplifier.

## 2. FGMOS BASIC PRINCIPLE

FGMOS is an ordinary MOSFET except that the gate, which is built on the conventional poly1, is floating and then called 'Floating-Gate'. The structure of FGMOS is shown in Fig.1.


**Fig.1** *FGMOS structure*

A multiple input MOSFET based on the FGMOS structure [2-3] is shown in Fig.1, which is seen that it comprises the floating gate, and input gates ($G_1$,..,$G_n$) built on Poly2, which are coupled to the Poly1 gate by the capacitors between Poly1 and Poly2 denoted as $C_1$,..,$C_n$. Assumed with the zero initial charge on the floating-gate and only two input gates, the drain current can be written as

$$I_D = \frac{1}{2}\mu C_{ox}\frac{W}{L}\left[(k_1 V_{G1} - V_t) - (V_{TH} - k_2 V_{G2})\right]^2 \quad (1)$$

$$I_D = \frac{1}{2}\mu C_{ox}\frac{W}{L}\left[(k_1 V_{G1} + k_2 V_{G2}) - V_t - V_{TH}\right]^2 \quad (2)$$

where $k_1$ and $k_2$ are capacitive coupling ratios $C_1/C_T$ and $C_2/C_T$ respectively and $C_T$ is the total capacitance of the floating gate. The drain current is essentially a linear sum of all inputs weighted by the ratios. Equation (1) is arranged to show the threshold voltage tuning. It is seen that $V_{G1}$ can be utilized as a signal port while $V_{G2}$ is used to tune the effective threshold voltage. Equation (2) is written to show a linear sum of the weighted multiple-input voltages.

## 3. HYSTERESIS TUNABLE COMPARATOR

A hysteresis tunable comparator was proposed in [7], based on an electronically tunable positive feedback factor produced by threshold voltage tuning of the embedded FGMOS devices.

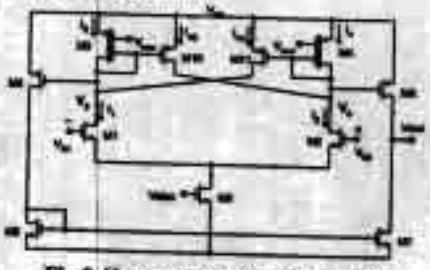


**Fig.2** *Hysteresis Analog Comparator*

power MOSFETs of both sides of the loads will be very precise. Dimensions of all MOSFETs are also shown in the figure.

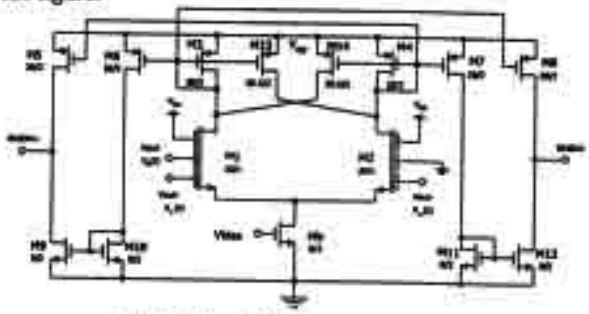


Fig.8 Fully differential comparator

## 5. SIMULATION RESULTS

Based on the proposed circuit in Fig.7, the amplifier has been designed on Alcatel 0.5μm CMOS process with 2.8 Volts power supply. The amplifier can deliver current to the 8Ω resistive loads and correspond to the output signal of $5.2V_{p-p}$. Other performances based on simulation results on HSPICE are summarized in Table 1.

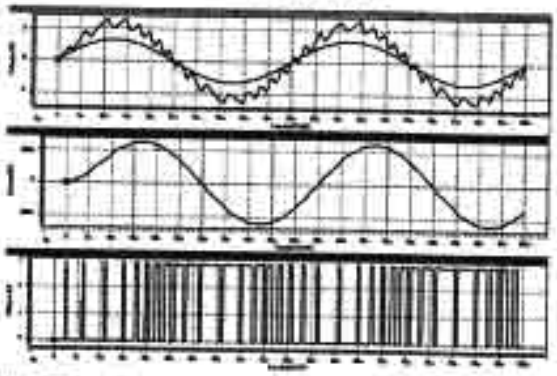


Fig.9 The voltage output signal, the current output signal and the RWDM output signal at input $1.3V_p$, 20kHz

Table 1 Summary of the proposed amplifier

| | |
|---|---|
| Process technology | Alcatel 0.5μm CMOS |
| Supply voltage | 2.8V |
| Static Power dissipation | 79.51μW |
| Maximum output swing | $5.2V_{p-p}$ |
| Output load | 8Ω |
| Maximum power | 0.88W |
| Efficiency | 95% |

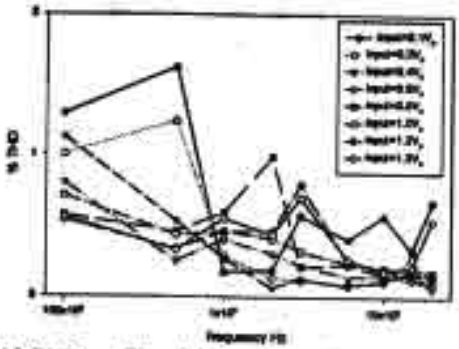


Fig.10 THD vs. Signal frequency and input amplitude

## 6. CONCLUSIONS

A single-chip low-voltage high-efficiency Class-D Power Amplifier for portable devices has been proposed The amplifier has a very simple architecture that makes it easier for it to be integrated with other circuit blocks on a system level. By virtue of the high efficiency of Class-D architecture coupled with the low voltage operation provided by the use of floating-gate MOSFET hysteresis comparator, this amplifier is suitable for portable devices with battery operations. It exhibits high distortion at low input signal due to the small changing of the input signal compared to the ripple at the output. The efficiency of this circuit is 95% at 0.88Watt with a 2.8V power supply.

## 7. REFERENCES


[1] D. L. Schilling, C. Belove, "Electronic Circuits Discrete And Integrated", 3rd edition, McGraw-Hill, 1989.

[2] B. Duncan, "High Performance Audio Amplifiers", Newnes, 1996.

[3] L. Kijjalak, P. Pawawongsak, "DSP Application for RWDM Inverters", The 22nd Electrical Engineering Conference, Bangkok, 1999, pp. 541-544.

[4] P.E. Allen, D.R. Hoberg, "CMOS Analog Circuit design", Oxford Press, NY, 1987, pp.323-362.

[5] K. Nandhasri, J. Ngarmnil, "Designs of Analog and digital Comparators with FGMOS", Proc.ISCAS2001, Vol.1, pp. 25-28.

[6] K. Yang and A. G. Andreou, "Multiple input floating-gate MOS differential amplifiers and applications for analog computational", Proc. MWSCAS, Vol.2, 1993, pp.1212-1216.

[7] J. R. Angulo, G. Gonzalez-Altamirano and S.C. Choi, "Modeling multiple-input floating-gate transistors for analog signal processing", Proc. ISCAS97, Vol. 3, pp. 2020 -2023.

[8] Sung-Mo Kang, Yusuf Leblebici, "CMOS digital integrated circuits analysis and design", McGraw-Hill, 1996.

[9] Choi et al, "A design of a 10-W single-chip class D Audio amplifier with very high efficiency using CMOS technology", IEEE Trans. Consumer Electronics, Vol. 45, No.3, Aug 1999.



Acknowledgement: This work has been supported by a grant from the Thailand Research Fund (TRF). The authors would like to thank the TRF for their precious support.

[4] J. Ngarmnil, K. Nandhasri, K. Moolpho, "Floating-gate MOSFETs Analog Circuit Building Blocks: Design perspective", 2002 IEEE International Symposium on Communication and Information Technology, October, 2002.

# FLOATING-GATE MOSFETS ANALOG CIRCUIT BUILDING BLOCKS: DESIGN PERSPECTIVE

*J. Ngarmnil, K. Nandhasri and K. Moolpho*

Department of Electronic Engineering, Faculty of Engineering,
Mahanakorn University of Technology, Bangkok, 10530, Thailand
Email: jitkasan@mut.ac.th

## ABSTRACT

Floating-gate MOSFET on a standard double-poly CMOS offers various new useful functions which can be used to create many novel circuits in both analog and digital circuits. This paper reviews some recently proposed FGMOS circuits, such as a hysteresis tunable voltage comparator, analog-based digital comparators, a low-voltage class AB current-mode amplifier circuit and its filtering application. Designs and HSPICE simulation results are demonstrated on standard double poly CMOS processes.

## 1. INTRODUCTION

Recently, many applications of Floating-gate MOSFET or FGMOS devices in analog circuits have been reported [1–6]. Normally playing a key role in modern integrated memories such as EEPROM and Flash, FGMOS has some unique characteristics which could be applied to design many new circuits or to enhance existing analog circuits for having extra special features such as very low voltage, low power and high complexity functions. This paper reviews the recently proposed analog and digital comparators based on an exploitation of the FGMOS. First, a hysteresis tunable analog comparator is constructed with an electronically tunable positive feedback factor obtained by threshold voltage tuning of the embedded FGMOS devices. Then, digital comparators are developed by essentially modifying the proposed analog voltage comparator to be a new digital circuits in which signal are internally processed with analog mechanism. Moreover, a high open-loop gain current amplifier circuit totally formed in the class AB structure utilizing CMOS inverters and floating-gate MOSFETs is also reviewed with its attractive features such as wide bandwidths, wide dynamic ranges and low voltage operations. Based on the high open loop gain amplifier, a single amplifier biquad is designed and demonstrated as an application of the proposed current amplifier.

## 2. FGMOS BASIC PRINCIPLE

FGMOS is an ordinary MOSFET except that the gate, which is built on the conventional poly1, is floating and then called 'Floating-Gate'. The structure of FGMOS is shown in Fig.1.

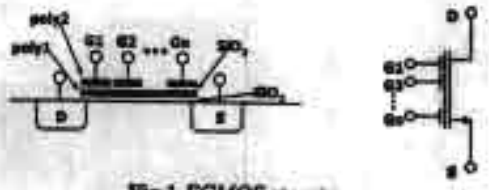



**Fig.1** *FGMOS structure*

A multiple input MOSFET based on the FGMOS structure [2-3] is shown in Fig.1, which is seen that it comprises the floating gate, and input gates ($G_1$,..,$G_n$) built on Poly2, which are coupled to the Poly1 gate by the capacitors between Poly1 and Poly2 denoted as $C_1$,..,$C_n$. Assumed with the zero initial charge on the floating-gate and only two input gates, the drain current can be written as

$$I_D = \frac{1}{2}\mu C_{ox}\frac{W}{L}\left[(k_1 V_{G1} - V_S) - (V_{TN} - k_2 V_{G2})\right]^2 \quad (1)$$

$$I_D = \frac{1}{2}\mu C_{ox}\frac{W}{L}\left[(k_1 V_{G1} + k_2 V_{G2}) - V_S - V_{TN}\right]^2 \quad (2)$$

where $k_1$ and $k_2$ are capacitive coupling ratios $C_1/C_T$ and $C_2/C_T$ respectively and $C_T$ is the total capacitance of the floating gate. The drain current is essentially a linear sum of all inputs weighted by the ratios. Equation (1) is arranged to show the threshold voltage tuning. It is seen that $V_{G1}$ can be utilized as a signal port while $V_{G2}$ is used to tune the effective threshold voltage. Equation (2) is written to show a linear sum of the weighted multiple-input voltages.

## 3. HYSTERESIS TUNABLE COMPARATOR

A hysteresis tunable comparator was proposed in [7], based on an electronically tunable positive feedback factor produced by threshold voltage tuning of the embedded FGMOS devices.

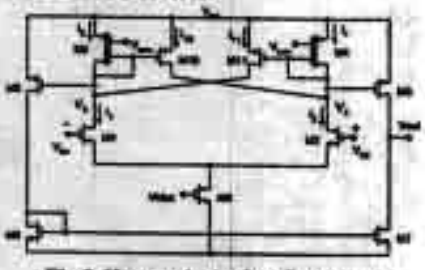


**Fig.2** *Hysteresis Analog Comparator*

The hysteresis tunable analog comparator is shown in Fig. 2 where $M_3$ and $M_4$ are FGMOSs. The hysteresis involves positive feedback produced by $M_{10}$ and $M_{11}$. The positive feedback occurs only when the current ratio of $I_{10}/I_3$ and $I_{D11}/I_{D4}$ are greater than one. If the ratio is higher, the amount of the feedback current will be increased and results in a wider of the positive and negative trip point voltage, $V_{TRP+}$ and $V_{TRP-}$. Hence the hysteresis can be controlled. The $V_{TRP+}$ and $V_{TRP-}$ can be derived from the condition that $I_2$ equals to $I_{10}$ and $I_1$ equals to $I_{11}$, correspondingly as,

$$V_{TRP+} = \sqrt{\frac{2I_3}{\beta_1}}\left(\frac{\sqrt{I_{10}/I_3}-1}{\sqrt{1+I_{10}/I_3}}\right)$$
$$V_{TRP-} = \sqrt{\frac{2I_4}{\beta_1}}\left(\frac{\sqrt{I_{11}/I_4}-1}{\sqrt{1+I_{11}/I_4}}\right) \quad (3)$$

Based on (1), since FGMOS allows us to tune drain current, the ratio of $I_{D10}/I_{D3}$ and $I_{D11}/I_{D4}$ can be tuned electronically by $V_{tune}$ at the input gate of $M_3$ and $M_4$. Also $V_{TRP+}$ and $V_{TRP-}$ can be tuned orthogonally if the tuning voltage at the input gates of $M_3$ and $M_4$ are different. $M_3$ and $M_4$ are designed with an equal area of $G_1$ and $G_2$ as $10.8\times22.8\mu m^2$ while the floating-gate area is set to $13.2\text{x}2.4\ \mu m^2$, which is also equal to those of $M_{10}$ and $M_{11}$. Fig.3 shows the simulation results of $V_{TRP+}$ and $V_{TRP-}$ vs. $V_{tune}$ varied in the range of 2.5-5.0V.

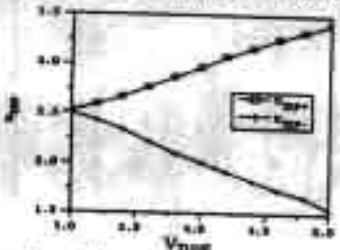



*Fig.3 $V_{TRP+}$ and $V_{TRP-}$ vs. $V_{TUNE}$*

To express the performance of the comparator in a noisy environment, the circuit was tested with a noise-modulated signal with the noise amplitude set to $0.4V_{peak}$. Simulation results are shown in comparison with those from a non-hysteresis comparator in Fig. 4.

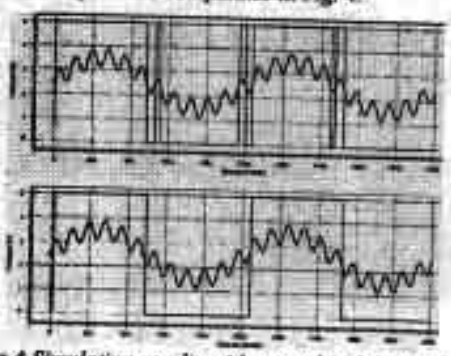


*Fig.4 Simulation results without and with hysteresis*

## 4. ANALOG-BASED DIGITAL COMPARATORS

Based on the proposed analog comparator, a new digital comparator [7] can be realized by doing a minor modification at the input devices. A hysteresis 4-bit digital comparators can be developed as in Fig.5 by employing FGMOSs as the input devices of which the sizes of the input gate are based on the significant of the binary weight. With hysteresis operation, this circuit performs two comparative functions of A>B or A≥B which depend on the level of $V_{tune}$. It is evidently shown in Fig.3 that if $V_{tune}$ is high or set to 5V, the current ratio $I_{D10}/I_{D3}$ and $I_{D11}/I_{D4}$ will be high and result in a large hysteresis. Then the comparator performs the operation A>B, where the value of A must be higher than B for some extent to cause the comparator tripping. On the other hand, If $V_{tune}$ is low or set to 0V, the positive feedback will be minimized and result in no hysteresis. Then the comparator performs the operation A≥B.

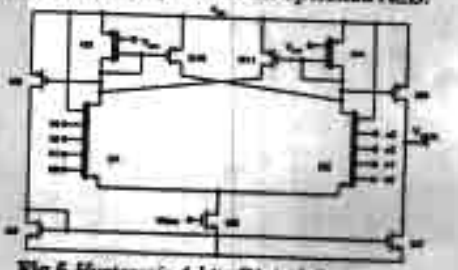


*Fig.5 Hysteresis 4-bits Digital Comparator*

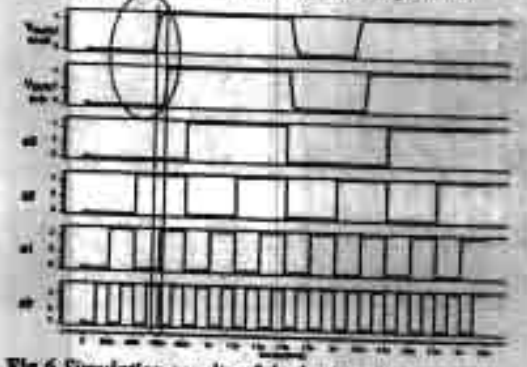


*Fig.6 Simulation results of the hysteresis comparator*

From Fig.6, the binary bits b3-b0 are set to #b0101 while the binary bits a3-a0 are swept digitally. It is seen that when $V_{tune}$ is set to Low, the output signal changes its stage when both binary sets are equal. The circuit performs the function A≥B. If $V_{tune}$ is set to High, the comparator performs the function A>B. A simple non-hysteresis digital comparator is shown in Fig.7 which is different from Fig.5 in that there is no positive feedback mechanism. The circuit performs three functions at the output node such as A<B, A>B and A=B. The output voltage is logic High or Low when the binary inputs at the positive terminal is higher or lower than that of the negative terminal respectively. The output is $V_{dd}/2$ when the binary inputs of both terminals are equal. This particular function implies an ability to detect the equality

of the binary inputs. The functionalities are confirmed by the simulation results in Fig.8.

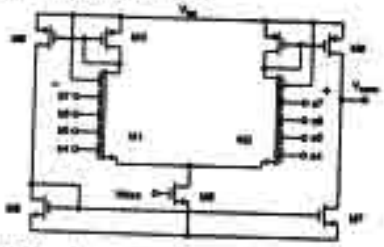


Fig.7 *Non-hysteresis 4-bits Digital Comparator*

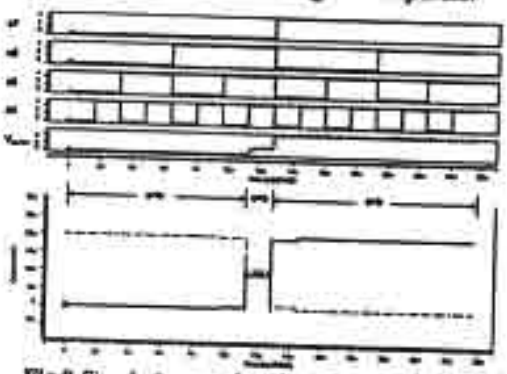
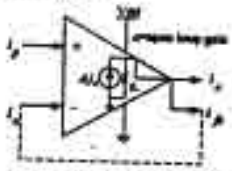


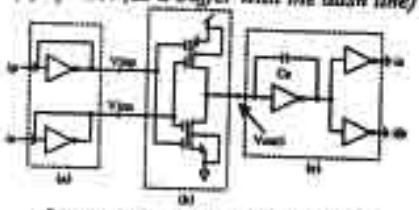
Fig.8 *Simulation results of the non-hysteresis comparator*

## 5. LOW VOLTAGE CURRENT AMPLIFIER

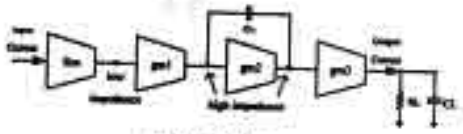
A current amplifier circuit [8] totally formed in the class AB structure utilizing CMOS inverters and FGMOS devices is presented here on 0.5μm double poly CMOS processes with 1.5V. As a buffer, the amplifier can deal with wide signal swings up to ±200μA, with 1% of the THD and 10pF of $C_L$. The proposed current amplifier, as symbolically shown in Fig.9(a), has two identical input terminals denoted as $i_p$ and $i_n$ and two output terminals delivering the same phase of the signal denoted as $i_o$ and $i_{fb}$, which are used as the output and the feedback port respectively. It is noted that the input $i_n$ can only be symbolized as an inverting terminal when the amplifier is connected in the negative feedback configuration as shown by the dashed line.



*(a) Symbol (as a buffer with the dash line)*



*(b) The proposed current amplifier*



*(c) Block diagram*

Fig.9 *The proposed current amplifier*

In Fig.9(b), the amplifier comprises three circuit blocks as shown in the dashed boxes. The trans-impedance amplifier is shown in box (a) and written as

$$Rm = \frac{1}{(gm_n + gm_p)} \tag{4}$$

where $gm_n$ and $gm_p$ are respectively the transconductance of NMOS and PMOS of the inverter . The additive analog inverter in box (b) is basically a two-input CMOS inverter elegantly built from the floating-gate MOSFETs and proposed in [9]. It is employed in this circuit together with the other Rm blocks to work as a differential amplifier. Hence the polarity of $i_{in}$ is inverse to those of $i_{ip}$ causing the voltage at node $V_{inn}$ to be inverse to those at node $V_{inp}$. Based on the diagram in Fig.9(c), the open-loop current gain of the whole circuit can be derived as

$$A_i = Rm \cdot gm_1 r_{o1} gm_2 r_{o2} gm_3 \tag{5}$$

where $r_{o1}$, $r_{o2}$ are the output resistance of $gm_1$, $gm_2$ stages while the GBW is

$$GBW = \frac{Rm \cdot gm_1 gm_3}{C_C} \tag{6}$$

The final design schematic can be illustrated in Fig.10, where it is seen that the circuit can be designed in a modular fashion where all inverters including the additive analog inverter have the same dimensions of NMOS and PMOS correspondingly. If a higher gain of the $gm_2$ and $gm_3$ blocks is required, we simply add more cells of the identical inverters in parallel. $R_C$ and $C_C$ are employed for the frequency compensation.

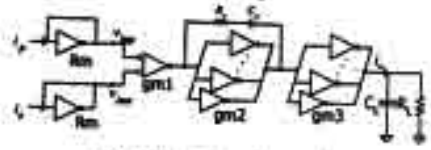


Fig.10 *Design schematic*

On the Alcatel 0.5μm CMOS process, the amplifiers have been designed with $V_{DD}$ of 1.5V. All NMOS and PMOS are designed with the dimensions of 6.9/0.5 and 23.6/0.5 respectively resulting in the idle currents of 30μA for each inverter. Four and three inverters connected in parallel are employed for the $gm_2$ block and the $gm_3$ block respectively to increase the gain. The amplifier is loaded with $C_L$ of 10pF and $R_L$ of 1.69kΩ, while $R_C$ of 1kΩ and $C_C$ of 0.8pF are set in the compensation scheme. The circuit was simulated on HSPICE with the performances shown in Fig.11 where 69.6dB Open-loop gain, 127MHz GBW and 74° PM were achieved with 635μW power consumption.

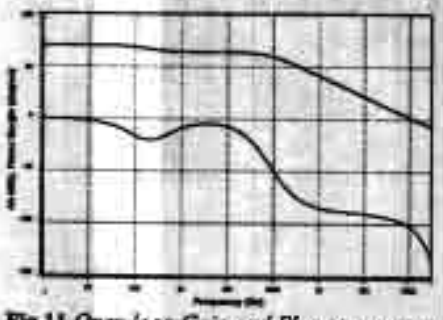


**Fig.11** *Open loop Gain and Phase responses*

A current-mode filter implementation using the current amplifier is demonstrated as an application, based on the general single amplifier network configuration with dual feedback in Fig.12 [10-11]. To demonstrate a design example, we assume filter specifications as,

$$f_{-3dB} = 2MHz \quad Q_p = 1 \quad H_p = 1 \qquad (7)$$

which correspond to the design parameters of $R_a$, $R_b$, $C_1$, $C_2$, $R_1$, $R_2$ and $R_3$ for various cut-off frequencies in the range of 1-10 MHz in Table 1. The simulation results are shown in Fig.13 and in comparison with an ideal case in Table 1. It is seen that the simulation results show a good agreement with the ideal case.

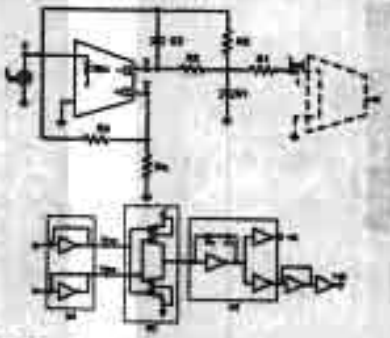


**Fig.12** *Single-ended input dual-feedback Biquad*

## 6. CONCLUSIONS

We have reviewed the designs of analog and digital comparators which exploit the threshold voltage operation characteristic of FGMOS to produce a hysteresis-tunable analog comparator. Consequently, the proposed analog comparator circuit is developed to a digital comparator using replacement of FGMOSs for the input devices of which the drain currents are linear sums of the weighted multiple-input binaries. Design and application of the low voltage current-mode amplifier using inverters and FGMOSs are also presented. Simulation results are demonstrated to confirm the functionalities. It is seen that FGMOS is a useful device for low voltage and electronically tuning applications.

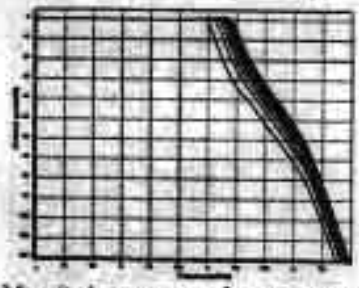


**Fig.13** Magnitude responses of current-mode biquad

## 7. REFERENCES


[1] T. Shibata, T. Ohmi, "A Functional MOS Transistor Featuring Gate-Level Weighted Sum and Threshold Operations", IEEE Trans. Elec. Devices, vol. 39, 1992, pp. 1444-1455.

[2] J. R. Angulo, G. Gonzalez-Altamirano, S.C. Choi, "Modeling multiple-input floating-gate transistors for analog signal processing", ISCAS97, Vol. 3, pp. 2020 -2023.

[3] Liming Yin, S. H. K. Embabi, E. Sanchez-Sinencio, "A floating-Gate MOSFET D/A Converter", ISCAS'97, Vol. 1, pp. 409-412.

[4] P. Hasler, B. A. Minch, and C. Diorio, "Floating-gate devices: they are not just for digital memories anymore", ISCAS99, Vol. 2, pp. 388-391.

[5] A. Veeravalli, E. Sanchez-Sinencio, J. Silva-Martinez, "Transconductance amplifier structures with very small transconductances: a comparative design approach" J. Solid-State Circuits, Vol. 37, Issue. 11 May 2002, pp. 530-532.

[6] K. Nandhasri, J. Ngarmnil, K. Moolpho, "A 2.8V RWDM BTL Class-D Power Amplifier using an FGMOS Comparator", ISCAS2002, Vol. 5, pp. 261-264.

[7] K. Nandhasri, J. Ngarmnil, "Designs of Analog and Digital Comparators with FGMOS", ISCAS2001, pp.I-25-I28.

[8] K. Moolpho, J. Ngarmnil, K. Nandhasri, "A low-voltage wide-swing FGMOS current amplifier", ISCAS2002, Vol. 4 pp.659-662.

[9] Y. Berg, O. Naess, M. Hovin, "Ultra low voltage floating-gate transconductance amplifier with tunable gain and linearity", ISCAS2000, pp.343-346.

[10] H.P. Schmid, G.S.Moschytz, "Active-MOSFET-C single-amplifier biquadratic filters for video frequencies", IEE Proc.-Circuits Devices Syst., Vol. 147, No. 1, 2000, pp. 35-41.

[11] G.S.Moschytz, A.Carlosena, "A Classification of Current-Mode Single-Amplifier Biquads Based on a Voltage-to-Current Transformation", IEEE Trans. On CAS, Vol.41, no. 2, pp. 151-156


**Table 1** *Design parameters and simulation results*

| Design parameters | | | | | | Simulation results | | Ideal case calculations | |
|---|---|---|---|---|---|---|---|---|---|
| $f_{-3dB}$ (MHz) | $C_1$(pF) | $C_2$(pF) | $R_1$(kΩ) | $R_2$(kΩ) | $R_3$(kΩ) | DC gain (dB) | $f_{-3dB}$ (MHz) | DC gain (dB) | $f_{-3dB}$ (MHz) |
| 1 | 160 | 80 | 2.459 | 0.819 | 1.809 | 0.109 | 1.12 | 0.010 | 1.27 |
| 2 | 80 | 40 | 2.459 | 0.819 | 1.809 | 0.109 | 2.21 | 0.010 | 2.54 |
| 3 | 52 | 26 | 2.522 | 0.805 | 1.851 | 0.140 | 3.24 | -0.854 | 3.80 |
| 4 | 40 | 20 | 2.459 | 0.819 | 1.809 | 0.109 | 4.24 | 0.010 | 5.09 |
| 5 | 32 | 16 | 2.459 | 0.819 | 1.809 | 0.109 | 5.17 | 0.010 | 6.37 |
| 6 | 26 | 13 | 2.522 | 0.840 | 1.851 | 0.140 | 6.02 | -0.554 | 7.80 |
| 7 | 22 | 11 | 2.555 | 0.851 | 1.872 | 0.155 | 6.82 | 0.009 | 8.90 |
| 8 | 20 | 10 | 2.459 | 0.819 | 1.809 | 0.109 | 7.82 | 0.010 | 10.2 |
| 9 | 18 | 9 | 2.429 | 0.809 | 1.780 | 0.093 | 8.35 | 0.001 | 11.4 |
| 10 | 16 | 8 | 2.459 | 0.819 | 1.809 | 0.109 | 8.03 | 0.010 | 12.7 |

[5] K. Moolpho, J. Ngarmnil, S. Sitjongsatapom, "A high speed low input current low voltage CMOS current comparator", 2003 IEEE International Symposium on Circuits and Systems (ISCAS2003), Bangkok, May, 2003.

# A High Speed Low Input Current Low Voltage CMOS Current Comparator

*K. Moolpho, J. Ngarmnil, S. Sitjongsataporn*

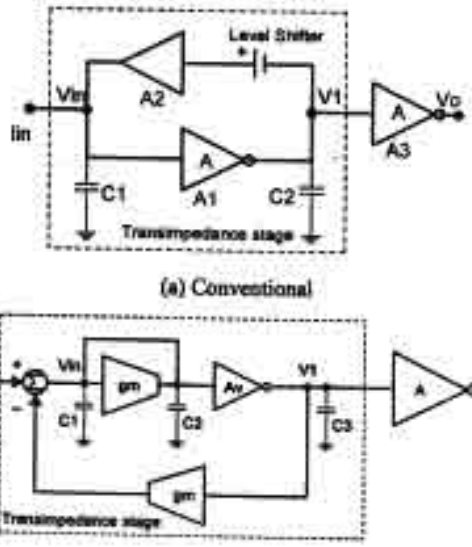
Electronic Engineering Department
Mahanakorn University of Technology, Bangkok, Thailand, 10530
Email: jitkasam@mut.ac.th

## ABSTRACT

A new high speed low input current comparator is proposed in this paper. Based on a simple negative feedback scheme around the transimpedance stage with an emphasis on a very large loop-gain, the transformed voltage signal is maintained at the lowest swing that results in a speed improvement. On a 0.25um TSMC CMOS process, simulation results demonstrate propagation delays of 3.6ns with ±100nA input current and 1.5Volts power supply, while the smallest input current is ±50pA. Performances are also shown with other $V_{DD}$ such as 1.0, 1.8 Volts.

## 1. INTRODUCTION

In the last decade, current-mode circuits [1]-[3] have drawn lots of interest for modern integrated circuits and sensory systems. This is due to their attractive features such as high speed, wide dynamic ranges and low voltage operation, all of which are mainly due to the fact that all node voltages swing are very low. In analogue and mixed signal processing, the current comparator is also one of the key elements. The circuit is not purely in a current-mode operation since although the input signal is current the output signal is digital logics or rail to rail voltage signal. Obviously there is a requirement to transform the input current to a large voltage signal. Thus to design a high speed current comparator, one has to take care of the voltage swing carefully since it directly determines the propagation delay. Conventionally, most reported current comparators [4]-[7] are based on the concept shown as a block diagram in Figure 1(a), where the input current signal is converted to the voltage $V_{in}$ and $V_1$ by the transimpedance stage comprising inverter amplifier $A_1$ and voltage buffer $A_2$. The resulting voltage $V_1$ is then amplified by the latter high gain inverter amplifiers $A_3$ to produce output logic voltage. There exist parasitic capacitors at all nodes. Ideally for high speed comparators, the signal swing at $V_1$ should be maintained as small as possible and situated exactly around the inverter threshold voltage of the inverter $A_3$. However, the reported works were relating to improve the lowest input current acquiring ability by arranging a proper biasing to turn on the MOSFETs of the buffer $A_2$ all the time. Most of them utilized diode connected MOSFETs as a level shifter to create $V_{GS}$ of the buffer MOSFETs. It is seen that although the transimpedance stage is formed in a negative feedback loop a much larger loop gain has not been exploited to keep the signal $V_{in}$ and $V_1$ as low as possible. Moreover with a larger loop gain, the input impedance at node $V_{in}$ could be much lower and receive a much smaller input current in the pico Amps range. The so called dead zone which is the smallest input current range to which comparators are insensitive is then minimized. However, a drawback of having the small voltage swing at $V_1$ is that the gain of the latter inverter amplifier must be necessarily high with hence a higher power consumption. Obviously, there is a conflict that if a speed as a result of a small voltage swing of the tranresistance stage is desired, a very high gain of the latter inverter amplifier will be necessary to provide the rail to rail output swing. In this paper, we propose an idea based on Figure 1(b), where a much higher loop gain is emphasized to gain speed and then trade power to the latter high gain inverter amplifier. The circuit utilizes only CMOS inverters and is suitable for a low $V_{DD}$ operation.




(a) Conventional

(b) Proposed

**Figure 1** Current comparator concepts

0-7803-7763-1/03/$17.00 ©2003 IEEE

## 2. THE PROPOSED CIRCUIT

As discussed above, we concentrate on a high speed or smallest average propagation delays and low input current acquiring capability or smallest dead zone. In this work, we trade off power for the required speed by maintaining the lowest voltage swing of the transimpedance stage and then providing high power to build up the latter high gain stage using inverter amplifiers. We then focus on the two separated circuit blocks as follows.

### 2.1 TRANSIMPEDANCE STAGE

The transimpedance stage, shown as the dashed block in Figure 2, plays the most important role in determining the speed of the comparator. It is seen that the whole stage is formed in a negative feedback loop by observing the polarities of output voltages and currents of each inverter. $A_1$ as a shorted input-output transconductance amplifier or inverter is basically an equivalent grounded resistor with the value of 1/gm. $A_2$ and $A_3$ are two high voltage gain amplifiers constructed from two cascaded inverters. Since there are two high impedance nodes in the loop RC frequency compensation is necessary to make the circuit stable. Capacitor C is set to 0.1pF while the resistor R is set to 1.6k Ohms. Note that the C and R could be made from a parasitic capacitor and a triode MOSFET respectively. The transconductance amplifier $A_4$ is used to provide negative feedback current to the input node. All amplifiers $A_1$ to $A_4$ are CMOS inverters designed with the same dimensions which are 2.1um/0.25um and 7um/0.25um for W/L of NMOS and PMOS respectively.

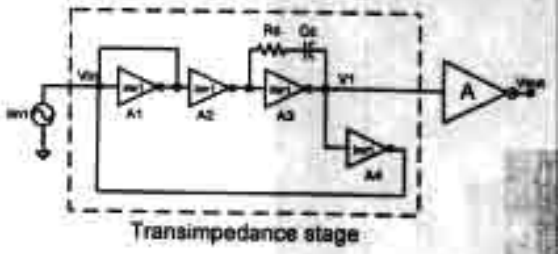



Figure 2 Transimpedance stage

Constructed in the feedback loop, the input resistance at node $V_{in}$ can be derived as.

$$R_{in} = \frac{1}{gm_T} \frac{1}{\left(1 + A_{vv}^2\right)} \quad (1)$$

where $gm_T$ is an equivalent transconductance of $A_1$ and and $A_{vv}$ is a voltage gain of the amplifier $A_2$ and $A_3$. Note that all inverters have the same transconductance and voltage gain because they have the same dimensions. It is seen that the input resistance $R_{in}$ is very small which results in a minimum voltage swing at node $V_{in}$ and also the same value of $V_1$ at the output of $A_3$. Figure 3 shows an open loop gain and phase of the feedback current to the input current. It is seen that dc gain of 56dB, GBW of 906MHz and PM of 45° are achieved in the open loop transconductance stage. With this specification, we have enough loop gain to suppress signals for the lowest voltage swings at $V_{in}$ and $V_1$ as shown in Figure 4. The negative feedback also stabilizes the common-mode voltage at all nodes to $V_{DD}/2$ which is set by the node $V_{in}$. This property is crucial for assuring that the signal swing is very small and also situated right at the center of the gate threshold voltage of the latter inverter of the gain stage.

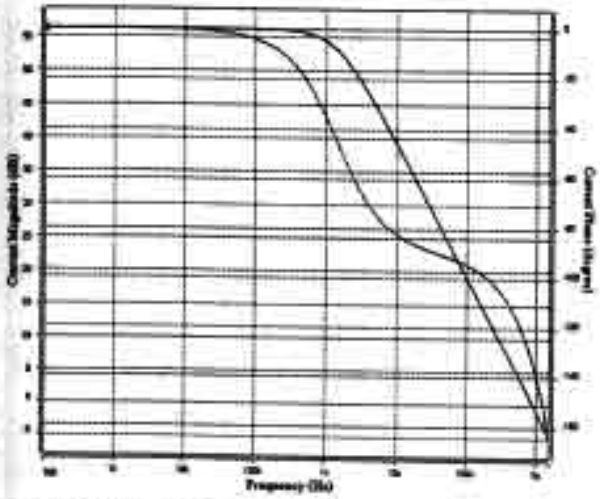


Figure 3 Open-loop responses of the transconductance stage

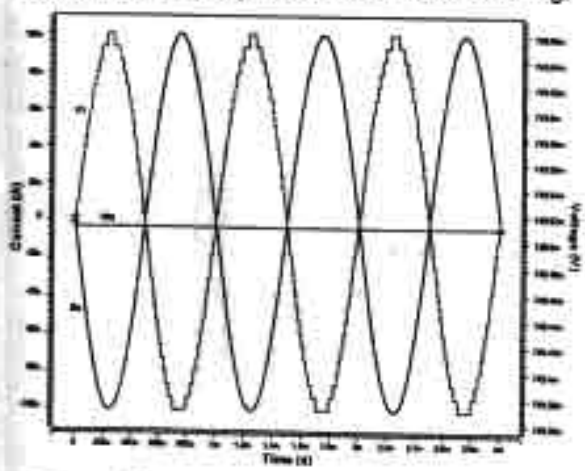


Figure 4 Voltage swings at $V_{in}$ and $V_1$ vs. input current

### 2.2 GAIN STAGES

We have now a very small voltage swing $V_1$ at the input of $A_5$ of the gain stage. The main aim in designing this part is to construct high voltage gain to produce rail to rail output logic. Based on the use of the same dimension inverters, we can construct the high gain stage in a modular fashion. INV1 has the same dimension as those in the

transconductance stage. INV2 has smaller dimensions than those of INV1 by half, i.e. 1um/0.25um and 3.5um/0.25um for W/L of NMOS and PMOS respectively. The modules could be placed in parallel for higher gain. For $A_5$, there are six INV1s connected in parallel, where each INV1 possesses an output current equal to $I_{in}$. $A_9$ and $A_{10}$ are only needed when $I_{in}$ is lower than 10nA. Cascading many stages of the inverter does not deteriorate the speed much because each inverter has a very small propagation delay which is less than 1ns. So as discussed earlier the major contributor to the delay is the transimpedance stage.

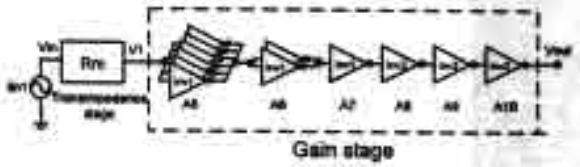
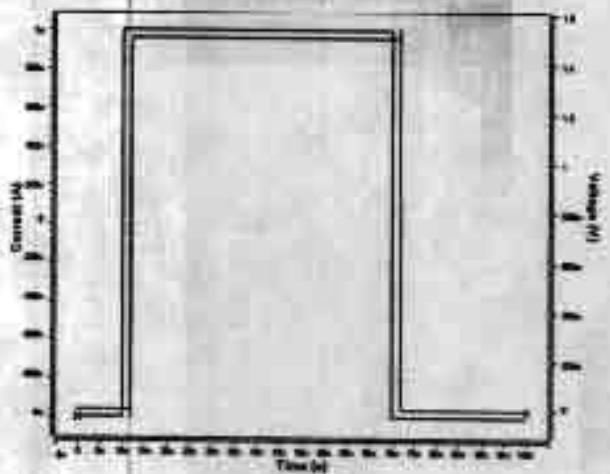


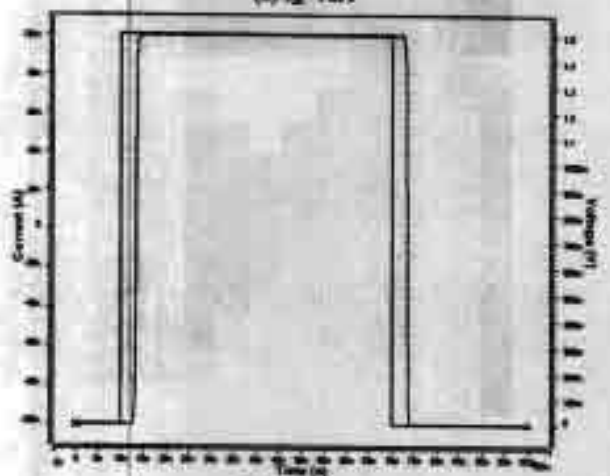

Figure 3 Gain stage

## 3. SIMULATION RESULTS

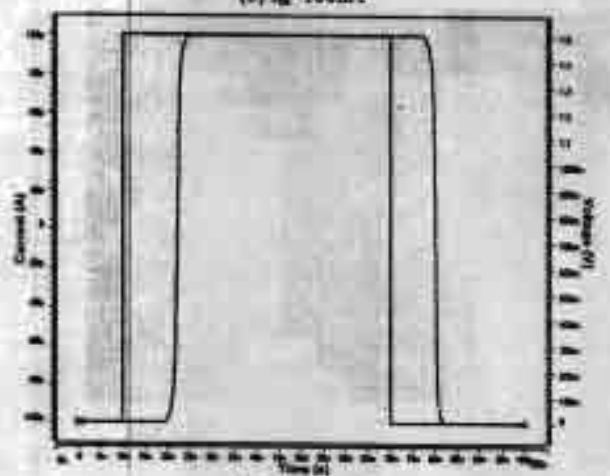
The proposed current comparator has been designed on a 0.25um TSMC CMOS process and tested with various power supplies and input current amplitudes. On HSPICE and with $V_{DD}$ set to 1.5V, the comparator responses of three input current amplitudes of 1uA, 100nA and 100pA are shown in Figure 5 where the average propagation delays are 1.95ns, 3.6ns and 10.7ns respectively. Performances vs the input current amplitudes at 1.5V $V_{DD}$ such as average propagation delay, static power and power delay product (PDP) are shown in Figure 6. It is seen that the lowest input current amplitude is at ±50pA thanks to the small input resistance as a result of the negative feedback with high loop gain. The average propagation delay is inversely proportional to the input current amplitudes since the voltage swing at the output of the transconductance stage is small. With small input current amplitudes, the static power also increases because all node voltages are around the common-mode value or $V_{DD}/2$ where most MOSFETs of the inverters are fully turned on. Propagation delays at various $V_{DD}$ and input signal amplitudes are shown in Figure 7. Performance comparisons among many reported circuits are listed in Table 1. It is seen that the power is higher than those from some earlier designs because the scaling down of the $V_{DD}$ normally degrades some properties of the inverter such as average drain current, voltage gain and propagation delay. Thus more power has to be pumped into the circuits in order to achieve the required speed and rail to rail output voltage swing.



(a) $I_{in}$=1uA



(b) $I_{in}$=100nA



(c) $I_{in}$=100pA

Figure 5 Transient Response of $V_{OUT}$ vs. $I_{in}$ at 1.5V $V_{DD}$

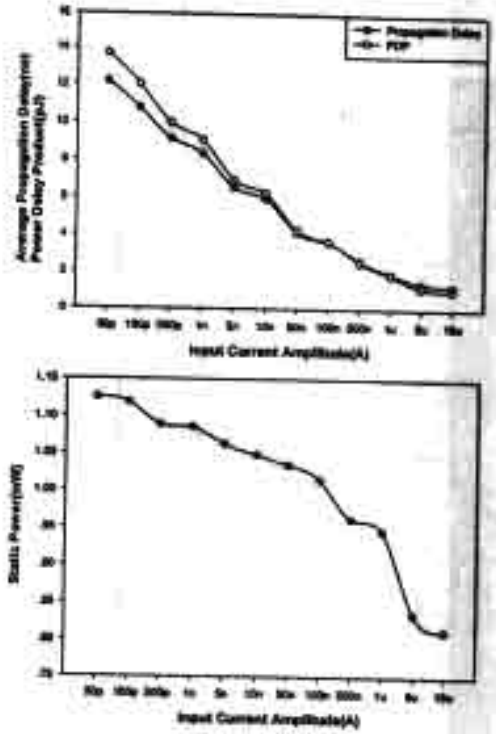


Figure 6 Performances at 1.5V $V_{DD}$

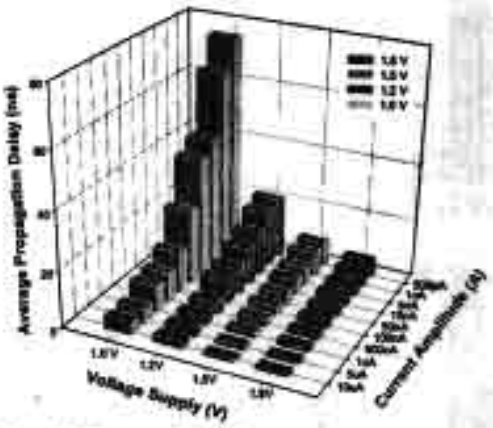


Figure 7 Propagation delays at $V_{DD}$ 1.0-1.8 Volts

## 4. SUMMARY

A new high speed low input current low voltage current comparator has been demonstrated on a 0.25um TSMC CMOS process. Based on the concept of a high speed current-mode technique, we exploit a negative feedback scheme around the transimpedance stage with an emphasis on a very large loop-gain to produce a very small transformed voltage swing which is situated at the center of the gate threshold voltage of the latter stage. This will ensure the fastest response time. The same dimension inverters are used in all amplifier stages. They are fast and simple and suitable for low voltage operation. There is no extra biasing circuit and stacked transistor, thus the same design can be applied with various $V_{DD}$ - ie there is no need to readjust the design.

## 5. REFERENCES


[1] C. Toumazou, F.J. Lidgey, D. Haigh, "Analogue IC Design: The current-mode Approach", Peregrinus, UK, 1990.

[2] G. Palmisano, S. Pennisi, "Low-Voltage continuous-time CMOS current amplifier with dynamic biasing", *Proc. ISCAS2001*, Sydney, May 2001, pp. I-312-I-315.

[3] K. Moolpho, J. Ngarmnil, K. Nandhasri, "A low-voltage wide-swing FGMOS current amplifier", *Proc. ISCAS2002*, Phoenix, May, 2002, pp.713-716.

[4] H. Traff, "Novel approach to high speed CMOS current comparators", *Electronics Letters*, Vol.28, No.3, pp.310-312, 1992.

[5] A.T.K. Tang and C. Toumazou, "High performance CMOS current comparator", *Electronics Letters*, Vol.30, No.1, pp.5-6, 1994.

[6] L.Ravezzi, D.Stoppas and G.F. Dalta Betta, "Simple high-speed CMOS current comparator", *Electronics Letters*, Vol.33, No.22, pp.1829-1830, 1997.

[7] H. Lin, J.H. Huang and S.C. Wong, "A simple high-speed low current comparator", *IEEE Trans. Circuit Syst.*, pp.713-716, 2000.

[8] B.M. Min and S.W. Kim, "High performance CMOS current comparator using resistive feedback network", *Electronics Letters*, Vol.34, No.22, pp.2074-2076, 1998.



ACKNOWLEDGEMENT This work has been supported by a grant from the Thailand Research Fund (TRF).


Table 1 Performance comparisons

| | Traff [4] | Tang [5] | Ravezzi[6] | Min [8] | Lin [7] | Proposed circuit | | |
|---|---|---|---|---|---|---|---|---|
| Year | 1992 | 1994 | 1997 | 1998 | 2000 | 2002 | 2002 | 2002 |
| Power Supply (V) | 5 | 5 | 5 | 3 | 3 | 1.5 | 1.0 | 1.8 |
| Process (μm) | 2 | 1.6 | 2.5 | 0.35 | 0.35 | 0.25 | 0.25 | 0.25 |
| Minimum Input Current Amplitude (nA) | 10 | 10 | 100 | 10 | 1 | 0.05 | 0.05 | 0.5 |
| Propagatino delay | ±1μA/ 10ns | ±0.1μA/ 11ns | ±0.1μA/ 19ns | ±0.1μA/ 7ns | ±0.1μA/ 2.8ns | ±0.1μA/ 3.5ns | ±0.1μA/ 14.65ns | ±0.1μA/ 2.6ns |
| Power consumption (mW) (at 0.1μA) | 0.390 | 1.4 | NA | 0.45 | 0.58 | 1.01 | 0.022 | 2.73 |
| PDP (pJ) | NA | NA | NA | 3.15 | 1.4 | 3.648 | 0.32 | 7.25 |

[6] J. Ngarmnil, S. Ruengrungson and K. Nandhasri, 'A 100MHz ±0.75V FLOATING-GATE MOSFET CURRENT CONVEYOR', 2003 IEEE Midwest Symposium on Circuits and Systems (MWSCAS2003), Cairo, December, 2003.

# A 100MHz ±0.75V Floating-gate MOSFET Current Conveyor

J. Ngarmnil, S. Ruengrungson and K. Nandhasri

Department of Electronic Engineering, Faculty of Engineering,
Mahanakorn University of Technology, Bangkok 10530, Thailand
Email: jitkasam@mut.ac.th

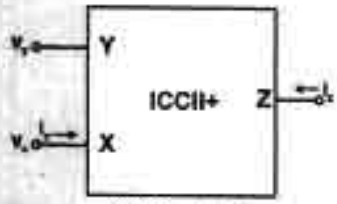
**Abstract-This paper proposes a low voltage inverting second eration current conveyor working up to a 100MHz with 5V power supply. The circuit is formed in class AB structure g CMOS inverters and a pseudo floating-gate MOSFETs itive analog inverter facilitating a negative feedback loop to ilate accurate signal tracking of the terminal voltage X to Y the terminal current Z to X. Simulation results on 0.5μm ble poly CMOS processes confirm high precision conveying ares, wide signal swing and low voltage capabilities of the ent conveyor.**

## I. INTRODUCTION

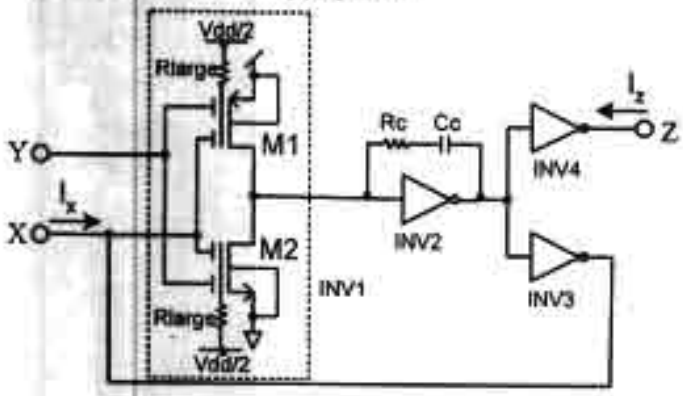
Recently, several signal processing techniques [1-2] id on second generation current conveyors (CCII) have n demonstrated successfully such as filtering, log-domain slinear, squarer and rectifier and multiplier circuits. Most erted CCII structures are based on a translinear cell which acked on current mirror circuits. A high precision CMOS I [3] was also realized with voltage follower and current ors with an emphasis on local negative feedback loop ind $v_y$ and $v_x$ terminals. All these circuits have ountered with limitation on low voltage applications since circuits are based on stacking topology of transistors. For voltage applications, a CMOS CCII [4] was proposed ly using CMOS inverters allowing only two stacked ces between the supply rails. The circuit is in a class-AB n of which the current signal swing can be very high ause there is not any fixed bias current source to limit the al swing. However, the circuit is restricted to applications re the Y input is only referenced to signal ground. A ped voltage follower based CCII was also proposed ntly in [5] exhibiting performances on low voltage and pactness. However, the current signal swing of terminal X Z are limited to the fix bias current source.

In this paper, we proposes a new inverting second eration current conveyor 'positive' (ICCII+) totally ted in the class AB structure utilizing CMOS inverters and recently proposed additive analog inverter [6-7] using ido or Quasi floating-gate MOSFETs, of which the offset age of the floating gate terminal can be weakly controlled ctively via a large valued resistor thanks to the inventions posed in [8-11]. The design is emphasized on negative lback with a high loop gain to enhance the conveying isions relating to $v_y$ to $v_x$ and $i_x$ to $i_z$. Thanks to the class AB topology, the circuit is also capable with wide swing signals. The design is applied on a 0.5μm double poly CMOS with ±0.75V power supply demonstrating low voltage capability and high frequency operation up to 100MHz.

## II. THE PROPOSED ICCII+




(a) Symbol




(b) Schematic

Fig.1 The proposed ICCII+

The proposed ICCII+ is shown in Fig.1 of which the port relations [12] among voltage and current terminals are described as,

$$\begin{bmatrix} i_y \\ v_x \\ i_z \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ -1 & 0 & 0 \\ 0 & 1 & 0 \end{bmatrix} \begin{bmatrix} v_y \\ i_x \\ v_z \end{bmatrix} \quad (1)$$

where terminal Y is a high impedance node and does not draw any input current. Terminal X is a low impedance node with voltage value $v_x$ equal to $-v_y$. Terminal Z is a high impedance node with the terminal current $i_z$ equal to $i_x$. These properties are transformed to the proposed ICCII+ shown in Fig.1. It is

n that Y is connected to the input gate of floating-gate )SFETs and is perfectly a high impedance node. Z is nected to the output node of an inverter which is obviously igh impedance node with current driving capability. It will shown later on that there is an internal negative feedback p from Y terminal to X terminal. By virtue of the negative fback loop, X can be derived as a low impedance node a current driving capability by inverter INV3 which is wn in Fig.1(b).

In Fig.1(b), the ICCII+ comprises four circuit blocks ignated as INV1, INV2, INV3 and INV4. The INV1 is an itive analog inverter or basically a two-input CMOS erter built from floating-gate MOSFETs M1 and M2 and proposed in [6-7]. Based on the idea of Pseudo or Quasi ting-gate MOSFET in [9-11], large value resistors urge) are shown to connect the floating-gate terminals of and M2 to Vdd/2 thus the DC offset of the floating-gate )SFETs can be effectively controlled and the complicated ial charge programming scheme such as UV removal can avoided. The resistors are built from reverse-biased diode nected PMOSs. The INV1 is employed in this circuit ether with INV2 and INV3 blocks to mimic the function of erential amplifier which allows the output of INV3 to atively feedback to the node X. Since voltage polarity of /3 output is inversed to those of $v_y$ causing the voltage at e $v_x$ to be inversed to those at node $v_y$ hence the function nverting CCII to copy the voltage $-v_y$ to $v_x$ can be fulfilled. reover, the diode connected PMOSs are always in reverse because voltage at the floating-gate is small as a result of negative feedback. A modulated AC voltage at the ting-gate can be written in (2) where the coefficient of $v_x$ egative as a result of the negative feedback via INV2 and /3.

$$v_{FG} = k_1 v_y - k_2 |v_x| \tag{2}$$

e k1 and k2 are the capacitive division factors $C_1/C_T$ and $C_T$, where $C_1$ and $C_2$ are the input coupling capacitances of and M2. $C_T$ is the total capacitance seen from the floating . All capacitances correspond directly to the sizes of the t coupled gates. In this case, the equal input coupling $C_1$ $C_2$ of M1 and M2 are set to 60fF and 100fF respectively result in approximated equal values $k_1$ and $k_2$ of 0.5. A ll signal voltage gain between the output $V_{out,INV1}$ and the erential inputs can be derived as

$$\frac{\partial V_{out,INV1}}{\partial (V_y - V_x)} = -(gm_{1n} + gm_{1p})(r_{o1n} // r_{o1p}) \tag{3}$$

re $gm_{1n}$, $gm_{1p}$ and $r_{o1n}$, $r_{o1p}$ are the respective sconductance and output resistances of M1 and M2 ectively. The voltage transfer of $v_y$ to $v_x$ is derived as

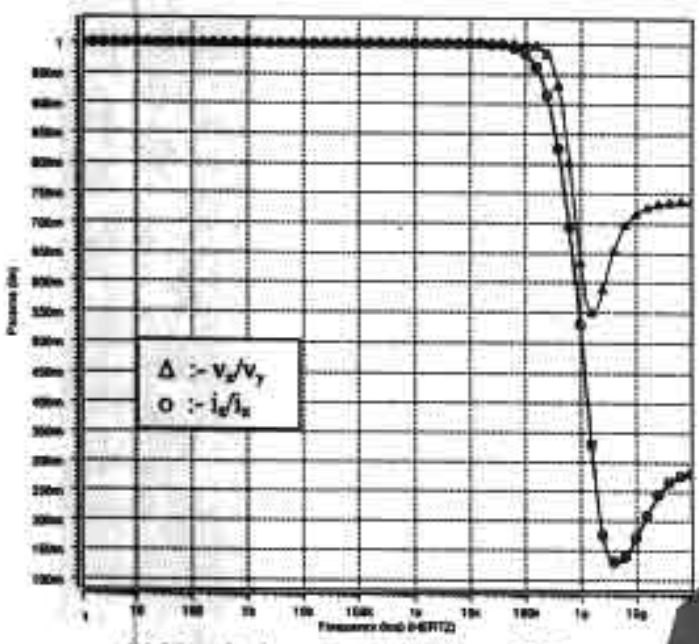
$$\frac{v_x}{v_y} = \frac{-gm_1 r_{o1} gm_2 r_{o2} gm_3 r_{o3}}{1 + gm_1 r_{o1} gm_2 r_{o2} gm_3 r_{o3}} \approx -1 \tag{4}$$

where $gm_1 r_{o1}$, $gm_2 r_{o2}$, $gm_3 r_{o3}$ are the intrinsic voltage gain of the INV1, INV2 and INV3 respectively. We can also derive the output resistance of terminal X as $r_x$ in (5) which is low as a result of the negative feedback.

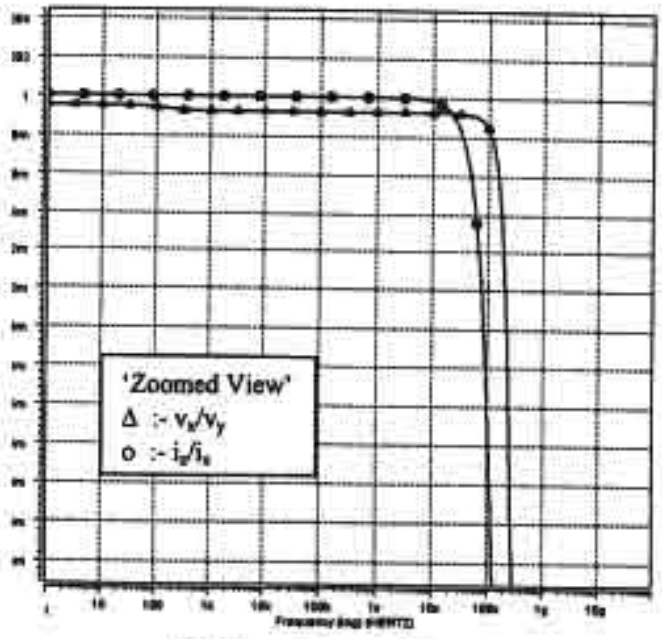
$$r_x = \frac{r_{o3}}{1 + gm_1 r_{o1} gm_2 r_{o2} gm_3 r_{o3}} \tag{5}$$

## III. SIMULATION RESULTS

Based on the proposed schematic in Fig.1(b), the circuit can be designed in a modular fashion where all inverters including the additive analog inverter have the same dimensions of NMOS and PMOS correspondingly. If a higher gain of any inverter blocks is required, we simply add more cells of the identical inverters in parallel. The circuit has been designed on the Alcatel 0.5μm double poly CMOS process with ±0.75V power supply. For each inverter module, NMOS and PMOS are designed with the dimensions of 8.4/0.5 and 24/0.5 respectively corresponding to $gm_n$ of 344uA/V and $gm_p$ of 314uA/V and resulting in the idle currents of 34μA for each inverter. The compensation network with $R_C$ of 500 Ohms and $C_C$ of 0.35pF are employed for stability since there are two high impedance nodes across INV2. In this circuit, we employ only one CMOS inverter for the additive inverter INV1 block. There are nine inverters connected in parallel for INV2 and three parallel inverters for INV3 and INV4 blocks hence making $i_z$ equals to $i_x$. Both X and Z terminals are loaded with external resistors of 1kΩ. Fig.2 shows frequency responses of the ratio $v_x/v_y$ and $i_z/i_x$ which are seen that the circuit contributes very low tracking errors of $v_x/v_y$ to less than 1% and those of $i_z/i_x$ to 1.6% at the frequency of 100MHz.




(a) Magnitude response of $v_x/v_y$ and $i_z/i_x$




(b) Zoomed view of (a)

Fig.2 Magnitude responses of $v_x/v_y$ and $i_z/i_x$

The magnitude responses of the X terminal output itance $r_x$ was derived in (5) and is shown in Fig.3. The e is less than 1 Ohms at DC rising to 500 Ohms at MHz. It is increasing dependent to the frequency in the frequency range because the loop gain of the negative back is decreasing at high frequency. However, the ating frequency of the circuit is bound to 100MHz.

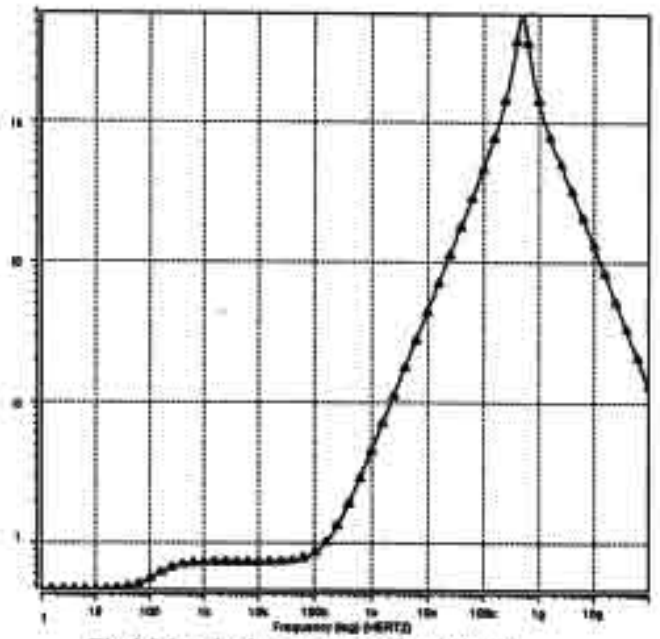
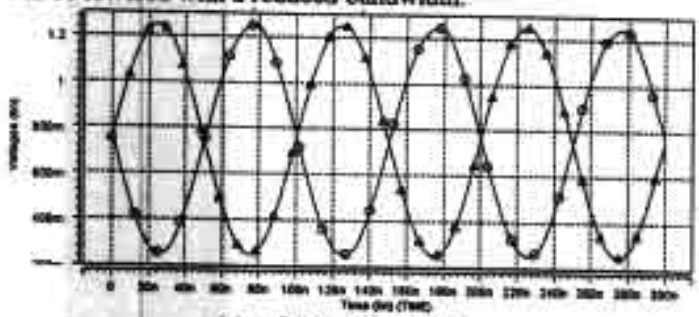
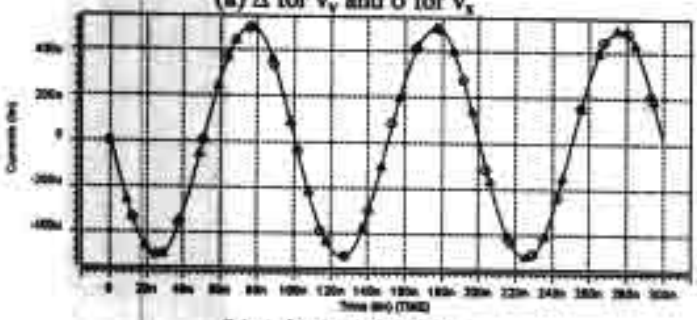


Fig.3 Magnitude response of $r_x$ (Ohms)

l shows the transient responses at 10MHz of $v_y$ vs. $v_x$ and $i_z$. In Fig.4(a) the responses of $v_y$ vs. $v_x$ confirm well (4). It is seen that the signal swing is as large as mV. Fig.4(b) shows a perfect matching of $i_x$ vs. $i_z$ with the current swing as large as ±500uA. For high frequency capability, Fig.5 shows the transient responses at 100MHz. In Fig.5(a) shows the responses of $v_y$ vs. $v_x$ with signal swing of ±200mV. Fig.5(b) shows the responses of $i_x$ vs. $i_z$ with the current swing of ±200uA. It is seen that the corresponding signals $v_y$ vs. $v_x$ and $i_x$ vs. $i_z$ are still matched but with a small phase shift. All signal amplitudes are set to confine the THD to less than 1%. Total power consumption is 816μW which can be lowered with a reduced bandwidth.

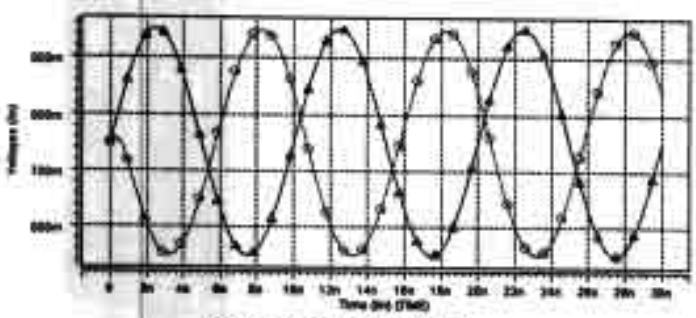


(a) Δ for $v_y$ and o for $v_x$

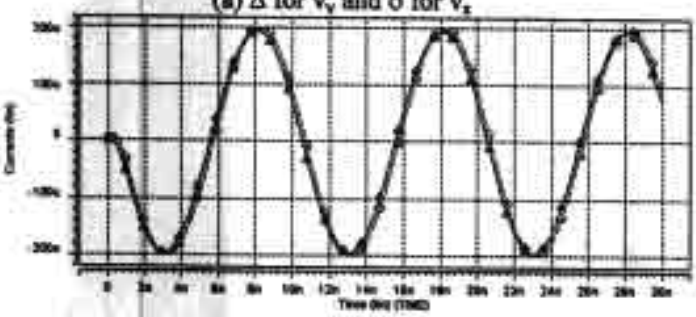


(b) Δ for $i_x$ and o for $i_z$

Fig.4 Transient responses at 10MHz with THD<1%



(a) Δ for $v_y$ and o for $v_x$



(b) Δ for $i_x$ and o for $i_z$

Fig.5 Transient responses at 100MHz with THD<1%

In many current conveyor applications, there is a need to have both polarities of output current $i_Z$ or multiple outputs $i_{Z+}$ and $i_{Z-}$. In some conventional CCII, this facility is usually

formed using additional current mirrors to copy and invert arity of the output current $i_Z$. However non-ideal racteristics of current mirror always introduce some king error between the current $i_{Z+}$ and $i_{Z-}$. In the similar on this topology, we can not straightforwardly cascade itional inverters at the output Z terminal in order to make inverted-direction current $i_Z$ since there is usually an ess phase shift that causing an unperfected tracking veen the currents $i_{Z+}$ and $i_{Z-}$. In this case, we demonstrate a allel connected ICCII+s as shown Fig.6. The perfected king in both magnitude and out of phase of $i_{Z+}$ and $i_{Z-}$ are wn in Fig.7(b) confirming a high precision property of this II+.

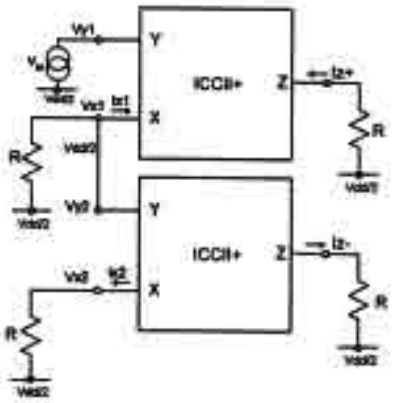
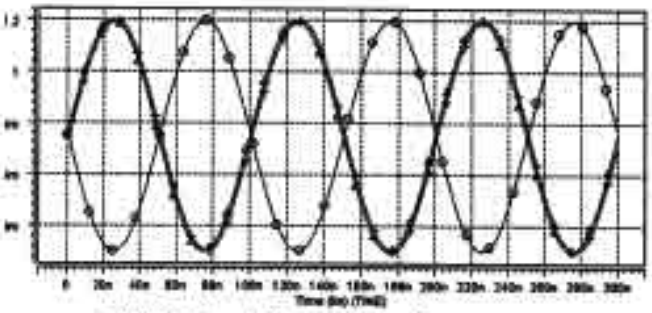
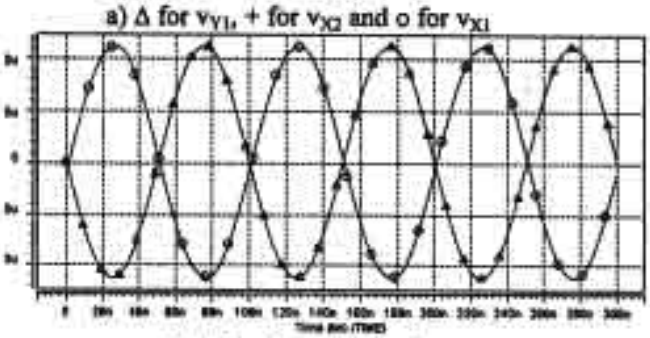



Fig.6 Parallel connected ICCII+s



a) Δ for $v_{Y1}$, + for $v_{X2}$ and o for $v_{X1}$



(b) Δ for $i_{Z-}$ and o for $i_{Z+}$.

Fig.7 Transient responses at 10MHz with THD<1%

## IV. CONCLUSION

paper has presented a low voltage wide swing inverting nd generation CMOS current conveyor of which the gn focuses on the use of CMOS inverters and the negative feedback to enhance conveying precisions, signal linearity and low output resistance property at the terminal X. The circuit is totally realized in class AB thanks to the use of CMOS inverters and the available floating-gate MOSFET additive analog inverter cell which facilitates the negative feedback channel to the normal CMOS inverter. With the programming approach of pseudo or quasi floating-gate MOSFET, DC offset of the floating-gate inverter can be effectively controlled to Vdd/2 and the complicated initial charge programming schemes could be avoided. The diode connected PMOSs producing the large resistors are always in reverse bias because the voltage at the floating-gate is small as a result of the negative feedback. With ±0.75V supply, the circuit can handle signal swing as large as ±500μA amplitude through X and Z terminals and ±500mV at Y and X terminals while the THD is maintained to less then 1%. The circuit is designed to operate up to 100MHz signal frequency.

## V. REFERENCES


[1] M.A. Ibrahim, H. Kuntman, "A CMOS realization of inverting second generation current conveyor", Proc. 2002, NORDIC Signal Processing Symposium, 2002.

[2] M.T. Abdelma'Atti, N.A. Tasadduq, "New current-mode controlled filters using the controlled conveyor", Int. J. of Electronics, Vol.85, No.4, 1998, pp.483-488.

[3] U. Yodprasit, "High-precision CMOS current conveyor", Electronics Letters, Vol. 36, No. 7, March 2000, pp.609-610.

[4] B. Maundy, I. Finvers, P. Aronhime, "A low voltage CMOS current conveyor for active filter design", Proc. MWSCAS-1998, August, 1998.

[5] A. J. Lopez-Martin, J. Ramirez-Angulo, R. G. Carvajal, "Low-voltage low-power wideband CMOS current conveyors based on the flipped voltage follower", Proc. ISCAS2003, pp.I-801-804.

[6] Y. Berg, O. Naess, M. Hovin, "Ultra low voltage floating-gate transconductance amplifier with tunable gain and linearity", Proc. ISCAS2000, pp. III-343-346.

[7] K. Moolpho, J. Ngarmnil, K. Nundhasri, "A low-voltage wide-swing FGMOS current amplifier", Proc. ISCAS2002, May, 2002.

[8] T. Shibata, T. Ohmi, "A Functional MOS Transistor Featuring Gate-Level Weighted Sum and Threshold Operations", IEEE Trans. Elec. Devices, vol. 39, 1992, pp. 1444-1455.

[9] O. Naess, Espen A. Olsen, Y. Berg, T. S. Lande, "A low voltage second order biquad using pseudo floating-gate transistors", Proc. ISCAS2003, pp. I-125-128.

[10] J. Ramirez-Angulo, A. J. Lopez-Martin, R. G. Carvajal, C. Lackey, "Low-voltage closed-loop amplifier circuits based on quasi-floating gate transistors", Proc. ISCAS2003, pp.I-813-816.

[11] J. Ramirez-Angulo, C. Urquidi, R. G. Carvajal, A.Torralba, "Sub-volt supply analog circuits based on quasi-floating gate transistors", Proc. ISCAS2003, pp.I-781-784.

[12] I.A. Awad, A.M. Soliman, "Inverting second generation current conveyors: the missing building blocks, CMOS realizations and applications", Int. J. Electronics, Vol. 86, pp.413-432, 1999.



Acknowledgement: This work has been supported by a grant from the Thailand Research Fund (TRF). Authors are grateful to the TRF for their precious support.