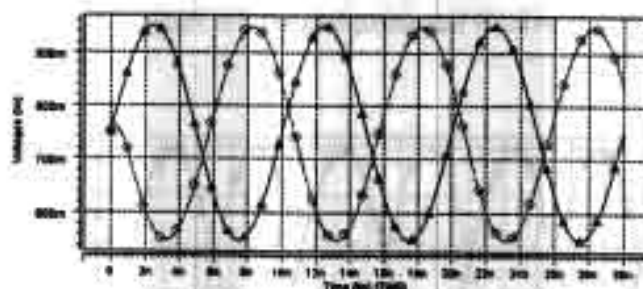
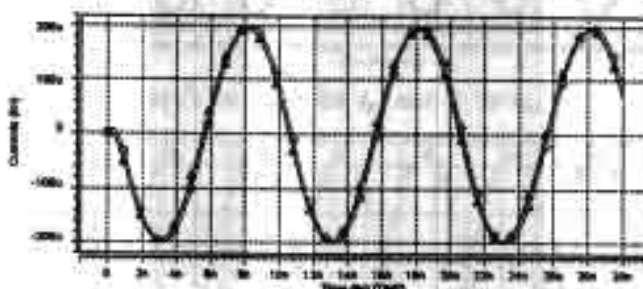


(b) Δ for i_z and $\circ$ for i_z

Figure 8.4 Transient responses at 10MHz with THD<1%



(a) Δ for v_y and $\circ$ for v_x



(b) Δ for i_z and $\circ$ for i_z

Figure 8.5 Transient responses at 100MHz with THD<1%

In many current conveyor applications, there is a need to have both polarities of output current i_z or multiple outputs i_{z+} and i_{z-} . In some conventional CCII, this facility is usually performed using additional current mirrors to copy and invert polarity of the output current i_z . However non-ideal characteristics of current mirror always introduce some tracking error between the current i_{z+} and i_{z-} . In the similar way on this topology, we can not straightforwardly cascade additional inverters at the output Z terminal in order to make an inverted-direction current i_{z-} since there is usually an excess phase shift that causing an unperfected tracking between the currents i_{z+} and i_{z-} . In this case, we demonstrate a parallel connected ICCII+s as shown Fig.8.6. Fig.8.7 (a) shows a perfected tracking of the voltage signal at terminals v_{y1} , v_{x1} and v_{x2} . The perfected tracking in both magnitude and out of phase of i_{z+} and i_{z-} are shown in Fig.8.7 (b) confirming a high precision property of this ICCII+.

connected PMOSs producing the large resistors are always in reverse bias because the voltage at the floating-gate is small as a result of the negative feedback. With $\pm 0.75\text{V}$ supply, the circuit can handle signal swing as large as $\pm 500\mu\text{A}$ amplitude through X and Z terminals and $\pm 500\text{mV}$ at Y and X terminals while the THD is maintained to less than 1%. The circuit is designed to operate up to 100MHz signal frequency.

9. A HIGH SPEED LOW INPUT CURRENT LOW VOLTAGE CMOS CURRENT COMPARATOR

In the last decade, current-mode circuits [39, 43, 54] have drawn lots of interest for modern integrated circuits and sensory systems. This is due to their attractive features such as high speed, wide dynamic ranges and low voltage operation, all of which are mainly due to the fact that all node voltages swing are very low. In analogue and mixed signal processing, the current comparator is also one of the key elements. The circuit is not purely in a current-mode operation since although the input signal is current the output signal is digital logics or rail to rail voltage signal. Obviously there is a requirement to transform the input current to a large voltage signal. Thus to design a high speed current comparator, one has to take care of the voltage swing carefully since it directly determines the propagation delay. Conventionally, most reported current comparators [60-63] are based on the concept shown as a block diagram in Fig.9.1 (a), where the input current signal is converted to the voltage V_{in} and V_1 by the transimpedance stage comprising inverter amplifier A_1 and voltage buffer A_2 . The resulting voltage V_1 is then amplified by the latter high gain inverter amplifiers A_3 to produce output logic voltage. There exist parasitic capacitors at all nodes. Ideally for high speed comparators, the signal swing at V_1 should be maintained as small as possible and situated exactly around the inverter threshold voltage of the inverter A_3 . However, the reported works were relating to improve the lowest input current acquiring ability by arranging a proper biasing to turn on the MOSFETs of the buffer A_2 all the time. Most of them utilized diode connected MOSFETs as a level shifter to create V_{GS} of the buffer MOSFETs. It is seen that although the transimpedance stage is formed in a negative feedback loop a much larger loop gain has not been exploited to keep the signal V_{in} and V_1 as low as possible. Moreover with a larger loop gain, the input impedance at node V_{in} could be much lower and receive a much smaller input current in the pico Amps range. The so called dead zone which is the smallest input current range to which comparators are insensitive is then minimized. However, a drawback of having the small voltage swing at V_1 is that the gain of the latter inverter amplifier must be necessarily high with hence a higher power consumption. Obviously, there is a conflict that if a speed as a result of a small voltage swing of the transresistance stage is desired, a very high gain of the latter inverter amplifier will be necessary to provide the rail to rail output swing. In this paper, we propose an idea based on Fig.9.1 (b), where a much higher loop gain is emphasized to gain speed and then trade power to the latter

high gain inverter amplifier. The circuit utilizes only CMOS inverters and is suitable for a low V_{DD} operation.

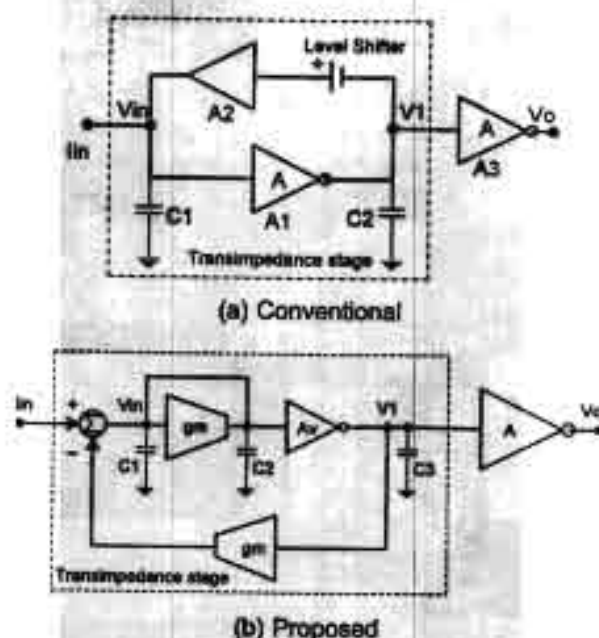


Figure 9.1 Current comparator concepts

9.1 THE PROPOSED CIRCUIT

As discussed above, we concentrate on a high speed or smallest average propagation delays and low input current acquiring capability or smallest dead zone. In this work, we trade off power for the required speed by maintaining the lowest voltage swing of the transimpedance stage and then providing high power to build up the latter high gain stage using inverter amplifiers. We then focus on the two separated circuit blocks as follows.

9.1.1 TRANSIMPEDANCE STAGE

The transimpedance stage, shown as the dashed block in Fig.9.2, plays the most important role in determining the speed of the comparator. It is seen that the whole stage is formed in a negative feedback loop by observing the polarities of output voltages and currents of each inverter. A_1 as a shorted input-output transconductance amplifier or inverter is basically an equivalent grounded resistor with the value of $1/g_m$. A_2 and A_3 are two high voltage gain amplifiers constructed from two cascaded inverters. Since there are two high impedance nodes in the loop RC frequency compensation is necessary to make the circuit stable. Capacitor C is set to 0.1pF while the resistor R is set to 1.6k Ohms. Note that the C and R could be made from a parasitic capacitor and a triode MOSFET respectively. The transconductance amplifier A_4 is used to provide

negative feedback current to the input node. All amplifiers A_1 to A_4 are CMOS inverters designed with the same dimensions which are $2.1\mu\text{m}/0.25\mu\text{m}$ and $7\mu\text{m}/0.25\mu\text{m}$ for W/L of NMOS and PMOS respectively.

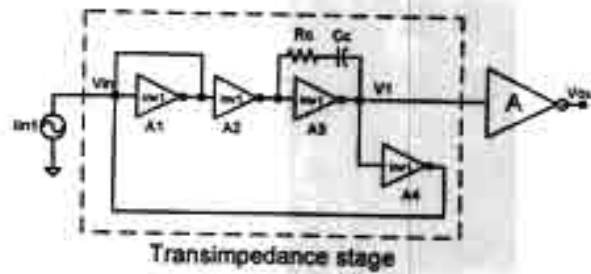


Figure 9.2 Transimpedance stage

Constructed in the feedback loop, the input resistance at node V_{in} can be derived as.

$$R_{in} = \frac{1}{g_{m_T} (1 + A_{vo}^2)} \quad (9.1)$$

where g_{m_T} is an equivalent transconductance of A_1 and A_{vo} is a voltage gain of the amplifier A_2 and A_3 . Note that all inverters have the same transconductance and voltage gain because they have the same dimensions. It is seen that the input resistance R_{in} is very small which results in a minimum voltage swing at node V_{in} and also the same value of V_1 at the output of A_3 . Fig.9.3 shows an open loop gain and phase of the feedback current to the input current. It is seen that dc gain of 56dB, GBW of 906MHz and PM of 45° are achieved in the open loop transconductance stage. With this specification, we have enough loop gain to suppress signals for the lowest voltage swings at V_{in} and V_1 as shown in Fig.9.4. The negative feedback also stabilizes the common-mode voltage at all nodes to $V_{DD}/2$ which is set by the node V_{in} . This property is crucial for assuring that the signal swing is very small and also situated right at the center of the gate threshold voltage of the latter inverter of the gain stage.

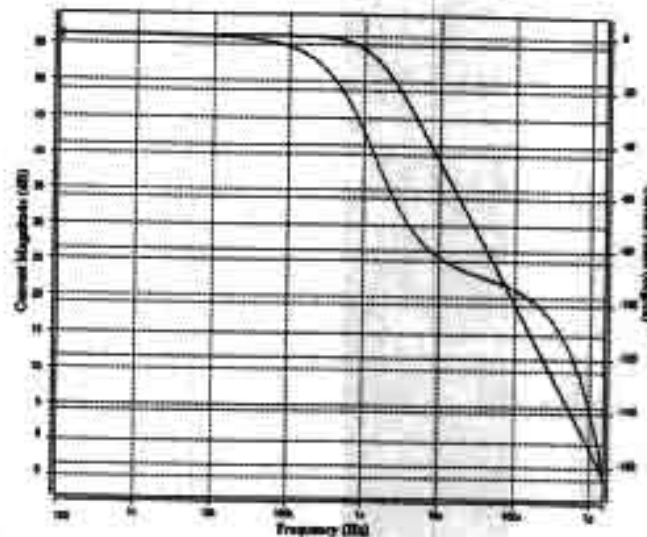


Figure 9.3 Open-loop responses of the transconductance stage

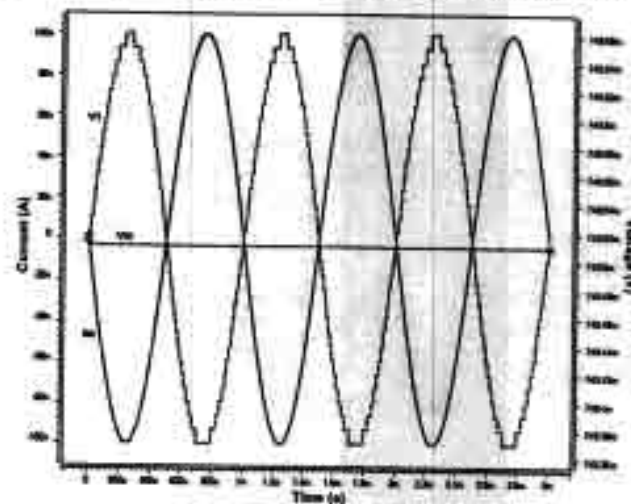


Figure 9.4 Voltage swings at V_{in} and V_i vs. input current

9.1.2 GAIN STAGES

We have now a very small voltage swing V_i at the input of A_5 of the gain stage. The main aim in designing this part is to construct high voltage gain to produce rail to rail output logic. Based on the use of the same dimension inverters, the high gain stage can be constructed in a modular fashion as shown in Fig.9.5. INV1 has the same dimension as those in the transconductance stage. INV2 has smaller dimensions than those of INV1 by half, i.e. $1\mu\text{m}/0.25\mu\text{m}$ and $3.5\mu\text{m}/0.25\mu\text{m}$ for W/L of NMOS and PMOS respectively. The modules could be placed in parallel for higher gain. For A_5 , there are six INV1s connected in parallel, where each INV1 possesses an output current equal to I_{in} . A_5 and A_{10} are only needed when I_{in} is lower than 10nA. Cascading many stages of the inverter does not deteriorate the speed much because each inverter has a very small propagation delay which is less than 1ns. So as discussed earlier the major contributor to the delay is the transimpedance stage.

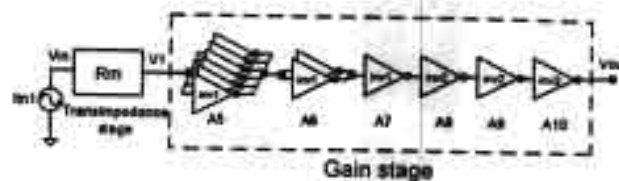
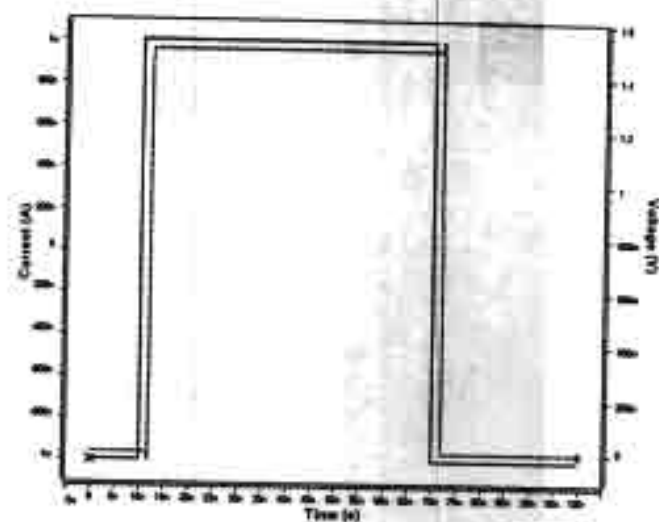


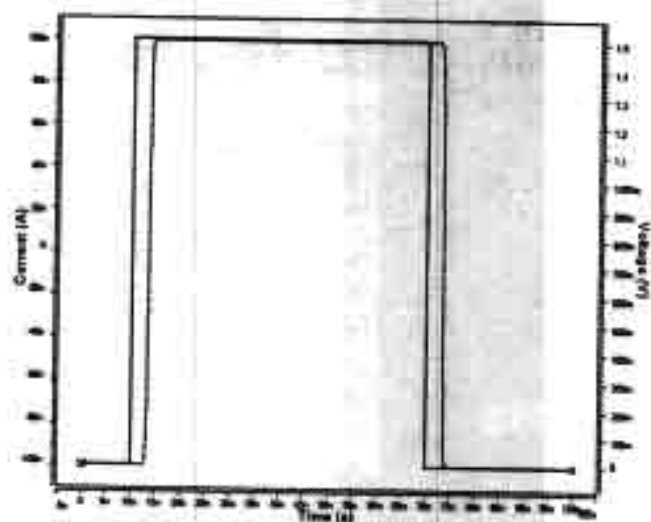
Figure 9.5 Gain stage

9.2 SIMULATION RESULTS

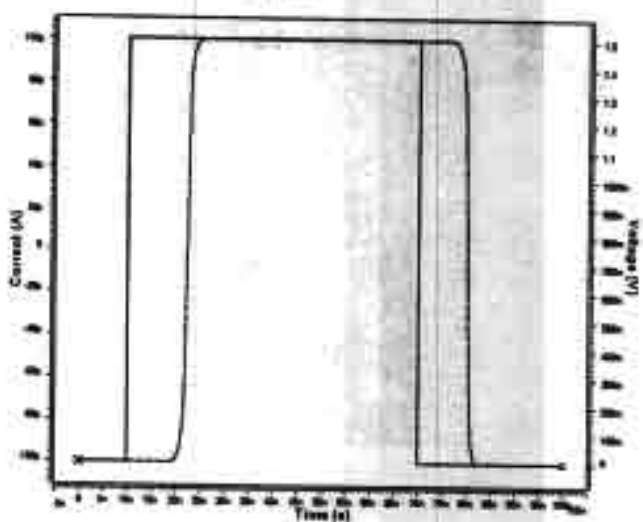
The proposed current comparator has been designed on a 0.25 μ m TSMC CMOS process and tested with various power supplies and input current amplitudes. On HSPICE and with V_{DD} set to 1.5V, the comparator responses of three input current amplitudes of 1 μ A, 100nA and 100pA are shown in Fig.9.6 where the average propagation delays are 1.95ns, 3.6ns and 10.7ns respectively. Performances vs the input current amplitudes at 1.5V V_{DD} such as average propagation delay, static power and power delay product (PDP) are shown in Fig.9.7. It is seen that the lowest input current amplitude is at ± 50 pA thanks to the small input resistance as a result of the negative feedback with high loop gain. The average propagation delay is inversely proportional to the input current amplitudes since the voltage swing at the output of the transconductance stage is small. With small input current amplitudes, the static power also increases because all node voltages are around the common-mode value or $V_{DD}/2$ where most MOSFETs of the inverters are fully turned on. Propagation delays at various V_{DD} and input signal amplitudes are shown in Fig.9.8. Performance comparisons among many reported circuits are listed in Table 9.1. It is seen that the power is higher than those from some earlier designs because the scaling down of the V_{DD} normally degrades some properties of the inverter such as average drain current, voltage gain and propagation delay. Thus more power has to be pumped into the circuits in order to achieve the required speed and rail to rail output voltage swing.



(a) $I_{in} = 1 \mu A$



(b) $I_{in} = 100 nA$



(c) $I_{in} = 100 pA$

Figure 9.6 Transient Response of V_{out} vs. I_{in} at 1.5V V_{DD}

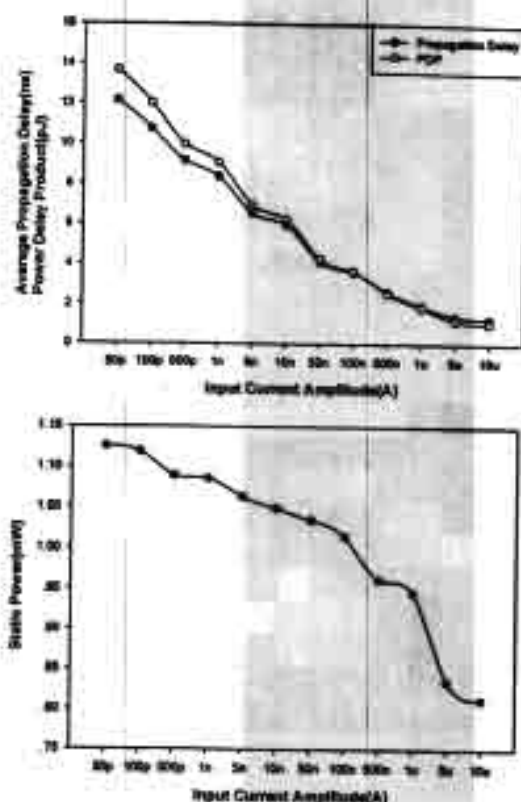


Figure 9.7 Performances at 1.5V V_{DD}

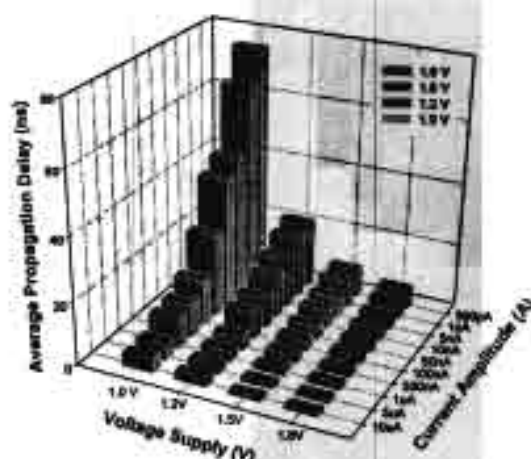


Figure 9.8 Propagation delays at V_{DD} 1.0-1.8 Volts

A new high speed low input current low voltage current comparator has been demonstrated on a 0.25 μ m TSMC CMOS process. Based on the concept of a high speed current-mode technique, we exploit a negative feedback scheme around the transimpedance stage with an emphasis on a very large loop-gain to produce a very small transformed voltage swing which is situated at the center of the gate threshold voltage of the latter stage. This will ensure the fastest response time. The same dimension inverters are used in all amplifier stages. They are fast and simple and suitable for low voltage operation. There is no extra biasing circuit and stacked

transistor, thus the same design can be applied with various V_{DD} - ie there is no need to readjust the design.

Table 9.1 Performance comparisons								
	Traff [60]	Tang [61]	Ravezzl[62]	Min [64]	Lin [63]	Proposed circuit		
Year	1992	1994	1997	1998	2000	2002	2002	2002
Power Supply (V)	5	5	5	3	3	1.5	1.0	1.8
Process (μm)	2	1.6	2.5	0.35	0.35	0.25	0.25	0.25
Minimum Input Current Amplitude (nA)	10	10	100	10	1	0.05	0.05	0.5
Propagation delay	$\pm 1\mu\text{A}/10\text{ns}$	$\pm 0.1\mu\text{A}/11\text{ns}$	$\pm 0.1\mu\text{A}/19\text{ns}$	$\pm 0.1\mu\text{A}/7\text{ns}$	$\pm 0.1\mu\text{A}/2.6\text{ns}$	$\pm 0.1\mu\text{A}/3.5\text{ns}$	$\pm 0.1\mu\text{A}/14.65\text{ns}$	$\pm 0.1\mu\text{A}/2.6\text{ns}$
Power consumption (mW) (at $0.1\mu\text{A}$)	0.390	1.4	NA	0.45	0.58	1.01	0.022	2.73
PDP (pJ)	NA	NA	NA	3.15	1.4	3.648	0.32	7.25

10. CONCLUSION

A floating-gate MOSFET or FGMOS on a standard double-poly CMOS offers various new useful functions which can be used to create many novel circuits such as low voltage low power circuits, analogue computational circuits and etc. This report gives a review of FGMOS such as the principle properties, functional characteristics and modeling for simulation tools. FGMOS device is basically a multiple-input device of which the main properties can be very useful for analog and digital computational circuits. It has unique and attractive characteristics of which the most important properties to be applied in this research and report are as follows: 1) As a multiple-input gate device, the voltage appears at the floating gate is a linear summation of its input voltage at all input terminals. This characteristic makes the device suitable for multiple signal computation. 2) The effective threshold voltage (V_{th}) seen at the input gate is tunable. These two phenomena are very attractive to analog designers. The first feature of the multiple-input gates allows analog designers to design a novel or to adapt many existing circuits to work with more complexity function without adding power consumption, while the second feature allows FGMOS devices to be operated at a very low the supply voltage as a result of the threshold voltage tunability. Both low voltage and low power operations are the most important requirement for biomedical applications. In this research, several analog signal processing building blocks have been proposed. They are very useful to various applications in biomedical systems such as biologically inspired circuits, electronic cochlea, silicon retina and analogue neural networks.

A Hysteresis Tunable Voltage Comparator using FGMOS is already proposed. The circuit is essentially exploiting FGMOS devices in the positive feedback scheme to create the hysteresis. Based on the tunability of the FGMOS, the current ratio of I_{D10}/I_{D3} and I_{D11}/I_{D4} corresponding to the amount of feedback current is used to tune the hysteresis effectively. An experiment of the back-gate tuning of M3 and M4 has also been investigated with a result showing that the range of V_{TRP+} and V_{TRP-} are not as wide as those offered by the circuit employing FGMOS. Also, the back-gate biasing always experiences an amount of leakage current because the bulk terminal is not fully isolated as in the case of poly1 and poly2 gates. The proposed idea can be implemented on any standard double-poly CMOS processes. The work has been performed on AMI 1.2 μ m CMOS process available through MOSIS. All the simulation

results confirm well the functionality. Performance optimizing will be placed as future works. Following the design of the Hysteresis Tunable Voltage Comparator, a non-clocked 8-bits digital comparator is also presented. It essentially manipulates the proposed analog voltage comparator to realize the new digital circuit in which the signal is internally processed in an analogue fashion. The proposed idea can be implemented on any standard double-poly CMOS and be useful to mixed signal and computational applications. All the simulation results confirm well the functionality.

As an application of a multiple input voltage comparator, designs of a single-chip low-voltage high-efficiency Class-D Power Amplifier for portable devices has been proposed. The amplifier has a very simple architecture that makes it easier to be integrated with other circuit blocks on a system level. By virtue of the high efficiency of Class-D architecture coupled with the low voltage operation provided by the use of floating-gate MOSFET hysteresis comparator, this amplifier is suitable for portable devices with battery operations. It exhibits high distortion at low input signal due to the small changing of the input signal compared to the ripple at the output. The efficiency of this circuit is 95% at 0.88Watt with a 2.8V power supply.

In this research, a novel approach in exploitation of CMOS inverter in a negative feedback form is presented. Normally, the CMOS Inverter has only one input terminal which is not convenience to be used in a negative feedback form. However, the negative feedback can be performed successfully via an assistance of the floating-gate additive analog inverter. A new low voltage wide swing current amplifier is then proposed. It can receive a signal swing as large as $\pm 200\mu\text{A}$ amplitude while a THD of about 1% is still maintained. The circuits can totally be realized in the class AB thanks to the use of CMOS inverters and the available additive analog inverter cells using floating-gate MOSFETs. The circuit is called a current amplifier instead of opamp due to the lack of CMRR capability, which will be part of our future works. Based on the same concept of designing CMOS inverter circuits in a negative feedback form, a low voltage wide swing inverting second generation CMOS current conveyor of which the design focuses on the use of CMOS inverters and the negative feedback to enhance conveying precisions, signal linearity and low output resistance property at the terminal X. The circuit is totally realized in class AB thanks to the use of CMOS inverters and the available floating-gate MOSFET additive analog inverter cell which facilitates the negative feedback channel to the normal CMOS inverter. With the programming approach of pseudo or quasi floating-gate MOSFET, DC offset of the floating-gate

inverter can be effectively controlled to $V_{dd}/2$ and the complicated initial charge programming schemes could be avoided. The diode connected PMOSs producing the large resistors are always in reverse bias because the voltage at the floating-gate is small as a result of the negative feedback. With $\pm 0.75V$ supply, the circuit can handle signal swing as large as $\pm 500\mu A$ amplitude through X and Z terminals and $\pm 500mV$ at Y and X terminals while the THD is maintained to less than 1%. The circuit is designed to operate up to 100MHz signal frequency.

A new high speed low input current low voltage current comparator has also been proposed and demonstrated on a 0.25 μm TSMC CMOS process. Based on the concept of a high speed current-mode technique, a negative feedback scheme has been exploited around the transimpedance stage with an emphasis on a very large loop-gain to produce a very small transformed voltage swing which is situated at the center of the gate threshold voltage of the latter stage. This will ensure the fastest response time. The same dimension inverters are used in all amplifier stages. They are fast and simple and suitable for low voltage operation. There is no extra biasing circuit and stacked transistor, thus the same design can be applied with various V_{DD} - ie there is no need to readjust the design.

This research works have been leading the way to exploit the floating-gate MOSFET device in various low voltage low power applications based on the fundamental concepts of analog signal processing and current mode circuit designs. All proposed analog building blocks are useful for micro power system designs and integrations. The first attempt in using the CMOS inverter in negative feedback form has been pointed out and should be exploited further for future works.

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ผลลัพธ์จากโครงการวิจัยที่ได้รับทุนจาก สกว.

การนำผลงานวิจัยไปใช้ประโยชน์ในเชิงวิชาการโดยมี

การผลิตนักศึกษาระดับบัณฑิตศึกษาสองคน คือ

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การนำเสนอผลงานในที่ประชุมวิชาการระดับนานาชาติ

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DESIGNS OF ANALOG AND DIGITAL COMPARATORS WITH FGMOS

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ABSTRACT

Designs of analog and digital comparators are presented in this paper. We exploit the threshold voltage operation characteristic of floating-gate MOSFETs to produce a hysteresis-tunable analog voltage comparator. Consequently, the proposed analog comparator circuit is developed to a digital comparator using replacement of floating-gate MOSFETs for the input devices of which the drain currents are linear sums of the weighted multiple-input voltages which are then applied as binary bits. Simulation results on 1.2µm CMOS are demonstrated.

1. INTRODUCTION

Recently, many applications of floating-gate (FGMOS) devices in analog circuits have been reported [1]–[10]. However, in electronic systems, the voltage comparator is also a very widely used circuit element found in many applications. This paper presents designs for analog and digital comparators based on an exploitation of the FGMOS. A hysteresis-tunable analog comparator is constructed with an electronically tunable positive feedback factor obtained by threshold voltage tuning of the embedded FGMOSs. Recently, a design for an 8-bit digital comparator working in an analog fashion was proposed [1]. The circuit was intended for less complexity, size and improved speed. This paper also presents an alternative design of an 8-bit digital comparator featuring arithmetic functions of A>B and A2B. The circuit essentially manipulates the proposed analog voltage comparator to produce a new digital circuit in which the signal is internally processed in an analog fashion. As a consequence, the new comparator is achieved by virtue of the analog technique.

2. FGMOS BASIC PRINCIPLES

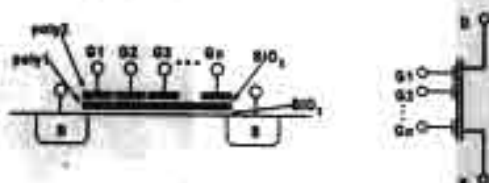


Figure 1. The FGMOS symbol

An FGMOS is an ordinary MOSFET except that the conventional gate on poly1 is floated. The equivalent structure, shown in Figure 1, comprises a floating gate on poly1 and input gates ($G_1, \dots, G_n$) built on poly2 which are coupled to the poly1 gate by the capacitors ($C_1, \dots, C_n$) between poly1 and poly2. With UV illumination, zero initial charge on the floating-gate can be assumed. In such a case, the drain current of the FGMOS can be written as

$$I_D = \frac{1}{2} \mu C_{ox} \frac{W}{L} [(k_1 V_{G1} + \dots + k_n V_{Gn}) - V_s - V_{TH}]^2 \quad (1)$$

$$I_D = \frac{1}{2} \mu C_{ox} \frac{W}{L} [(k_1 V_{G1} - V_s) - (V_{TH} - k_2 V_{G2})]^2 \quad (2)$$

where $k_1, \dots, k_n$ are $C_1/C_T, \dots, C_n/C_T$ respectively and C_T is the total capacitance of the floating gate. The drain current is essentially a linear sum of all the input voltages weighted by the capacitive coupling ratios. Furthermore, equation (1) can be rearranged to (2) in order to show the threshold operation when only two input gates are assumed. It is seen that V_{G1} can be utilized as a signal port while V_{G2} is used to tune the effective threshold voltage. These two features are exploited in this work.

3. HYSTERESIS ANALOG COMPARATOR

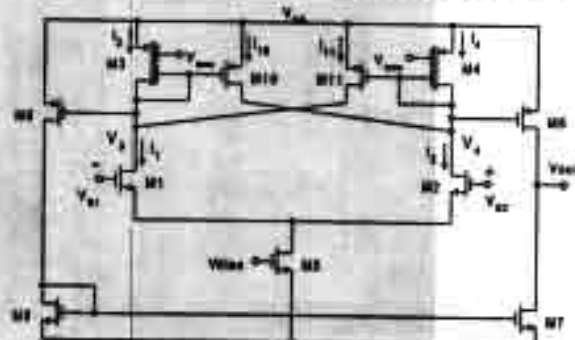


Figure 2. The Hysteresis Analog Comparator

A simple hysteresis analog comparator is well discussed in [11] and shown in altered form in Figure 2 where M3 and M4 are FGMOSs. The hysteresis involves two positive feedback paths provided by M10 and M11. The positive feedback occurs only when the current ratios of I_{D10}/I_3 and I_{D11}/I_4 are both greater than unity. If these ratios increase further, the feedback current will also increase resulting in wider positive and negative trip point voltages (V_{TRP+} and V_{TRP-}). Hence the hysteresis can be controlled. An equation can be developed for V_{TRP+} from the condition that whenever the circuit operates in the hysteresis loop, I_3 always equals I_{D10} . Similarly for V_{TRP-} with I_4 set equal to I_{D11} . We have

$$\begin{aligned} V_{TRP+} &= \frac{\sqrt{2I_3}}{\beta_1} \frac{\sqrt{I_{D10}/I_3} - 1}{\sqrt{1 + I_{D10}/I_3}} \\ V_{TRP-} &= \frac{\sqrt{2I_4}}{\beta_1} \frac{\sqrt{I_{D11}/I_4} - 1}{\sqrt{1 + I_{D11}/I_4}} \end{aligned} \quad (3)$$

where β_1 is the $\mu C_{ox} W/L$ for M1 which is identical to that of M2. Thus, from (2), by virtue of the FGMOSs, the ratios of I_{D10}/I_3 and I_{D11}/I_4 can be tuned electronically by the voltage V_{tun} at the input gates V_{G2} of M3 and M4. Hence V_{TRP+} and V_{TRP-} can be tuned orthogonally if the tuning voltage at the input gates of M3 and M4

are different. M3 and M4 are designed with the areas of the two input gates equal to $10.8 \times 22.8 \mu\text{m}^2$ while the conventional gate areas are set to $13.2 \times 2.4 \mu\text{m}^2$, the same as those of M10 and M11. The circuit was simulated on HSPICE using $1.2 \mu\text{m}$ AMI CMOS with assistance from the FGMOS macro model in [1] and supply voltage set to 5.0V. Figure 3 shows V_{TRP+} and V_{TRP-} vs. V_{TDC} varied in the range of 2.5-5.0V.

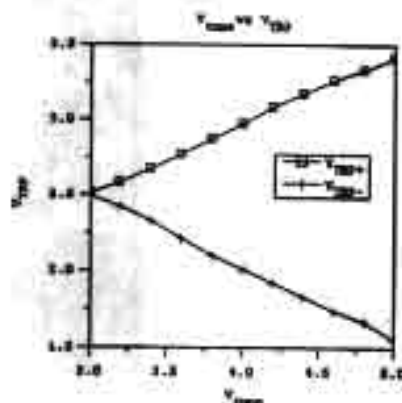


Figure 3. V_{TRP+} and V_{TRP-} vs. V_{TDC}

Time-domain simulation was also performed to express the performance of the comparator in a noisy environment. The circuit was tested with a noise-modulated signal of which the noise amplitude set to $0.4V_{DD}$ while V_{TDC} was set to 3.8V. Simulation results are shown in comparison with those from a non-hysteresis comparator in Figure 4.

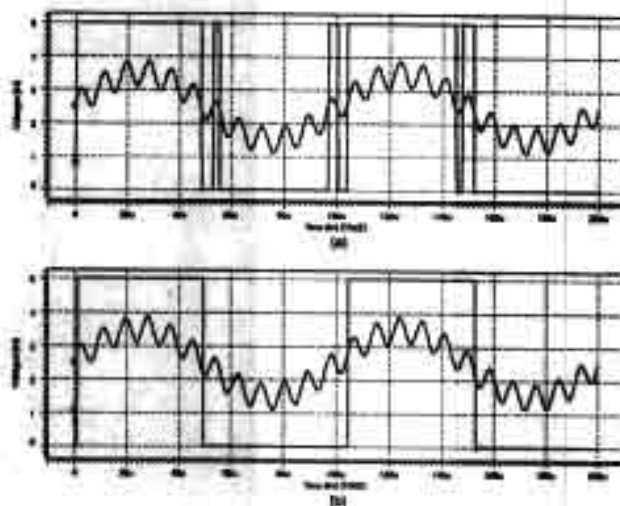


Figure 4. Comparison of results from (a) non-hysteresis and (b) hysteresis comparator

4. 4-BITS DIGITAL COMPARATOR

Based on the proposed opamp-based analog comparator, a new 4-bits digital comparator can also be realized by employing FGMOSs as the input devices. These 4-bit digital comparators are proposed separately as non-hysteresis and hysteresis types. Both circuits are

further used for designing an 8-bit digital comparator that will be discussed in the next section. The non-hysteresis digital comparator is shown in Figure 5. It is seen that FGMOSs are employed as the input devices in order to exploit the drain current, which was written in (1) as a linear sum of the weighted multiple-input voltages that are basically binary bits of digital input data. Binary bits of '1' and '0' correspond to the voltage V_{DD} and 0V at the input nodes respectively. The circuit is digital at the input and output but internally works as an analog circuit.

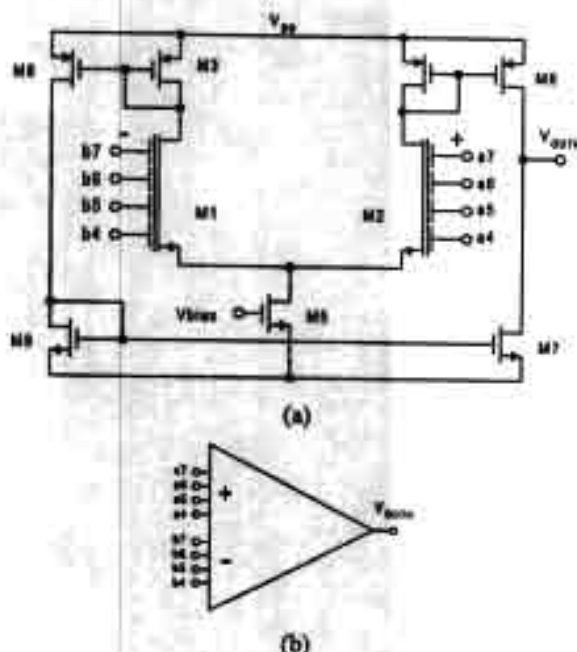


Figure 5. A Non-hysteresis 4-bit Digital Comparator

In Figure 5(a), the FGMOSs M_1 and M_2 are designed with the conventional gate areas of $12 \times 3 \mu\text{m}^2$. Let k_{a4}, k_{a7} be the weights of the input gates denoted as $a4, a7$ and $b4, b7$ respectively, where $a4$ and $b4$ are the least significant bits of this comparator. Then the input gates have the sizes set by the binary weights as in Table 1.

Table 1. Design parameters of the FGMOS

	b4	b5	b6	b7
Binary weights	1/16	1/8	1/4	1/2
Size(μm^2)	10.8x22.8	21.6x22.8	43.2x22.8	86.4x22.8
Capacitance(fF)	159.7	319.3	638.9	1277.8

This non-hysteresis 4-bit comparator can be symbolically represented as in Figure 5(b). The circuit delivers three levels of output signal at V_{OUT} . The output is logic High or V_{DD} when the total weighted sum of the binary inputs at the positive terminal is higher than that of the negative terminal. The output is logic Low or GND when the total weighted sum of the binary inputs at the positive terminal is lower than that of the negative terminal. The output is $V_{DD}/2$ when the total weighted sums of the binary inputs of both terminals are equal. The latter function implies an ability to detect the equality of the binary inputs. The functionalities are confirmed by the simulation results in Figure 6.

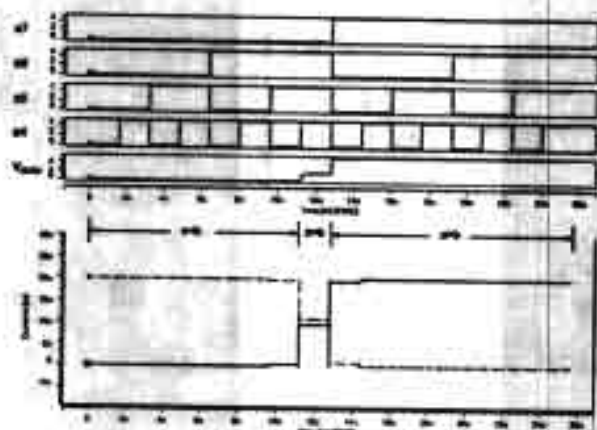


Figure 6. Results of the non-hysteresis 4-bit comparator

Figure 6 shows output signal as functions of V_{OUT} and drain currents of the input devices where the binary a7-a4 are swept digitally and the binary b7-b4 are set to #b0111. It is seen that the output voltage is at $V_{DD}/2$ and the input drain currents are equal when the binary a7-a4 equals to b7-b4. This property will also be utilized further in the design of the 8-bits comparator.

The hysteresis comparator shown in Figure 7 is similar to that of Figure 5 except that the hysteresis tuning part used in the analog comparator is employed. Because of the hysteresis operation, this circuit delivers only two levels of the output signal at high or low. As a result of the hysteresis tuning, the output signal is delivered according to the arithmetic functions of $A > B$ or $A \geq B$ that are selected by the voltage V_{TUNE} . Using the same dimensions of all MOSFETs as in Figure 5 and setting conventional gate areas of M3, M4 to $15 \times 2.4 \mu\text{m}^2$, we set the input gate areas of both M3 and M4 for the input signal and for V_{TUNE} to $77 \times 31 \mu\text{m}^2$ and $11 \times 31 \mu\text{m}^2$ respectively. The simulation results are shown in Figure 8.

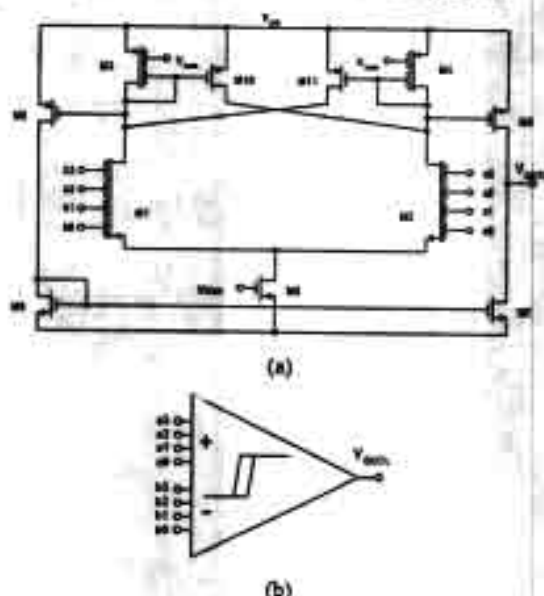


Figure 7. Hysteresis 4-bit Digital Comparator

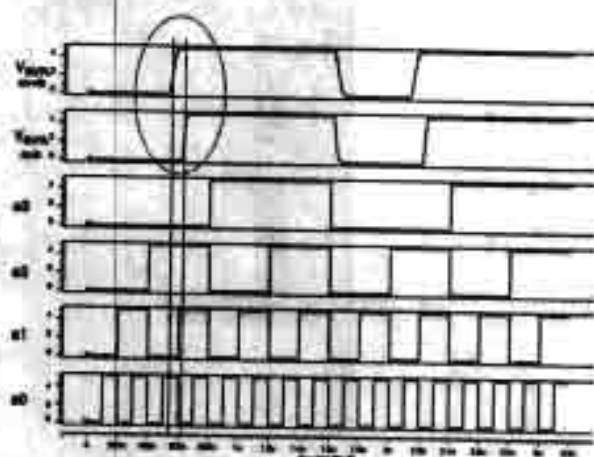


Figure 8. Simulation results of the hysteresis comparator

From Figure 8, the binary bits b3-b0 are set to #b0101 while the binary bits a3-a0 are swept digitally. It is seen that if V_{TUNE} is set to High, the output signal V_{OUT} changes its stage when both binary sets are equal. The circuit performs the function $A \geq B$. If V_{TUNE} is set to Low, the comparator will perform the function $A > B$. In the next section, both hysteresis and non-hysteresis digital comparators will be combined in the design of an 8 bit digital comparator.

5. 8-BIT DIGITAL COMPARATOR

An 8-bit digital comparator is realized by using the two 4 bit comparators and another comparator as shown in Figure 9. The 8-bit binary inputs denoted as a7-a0 and b7-b0 can be defined as A and B respectively.

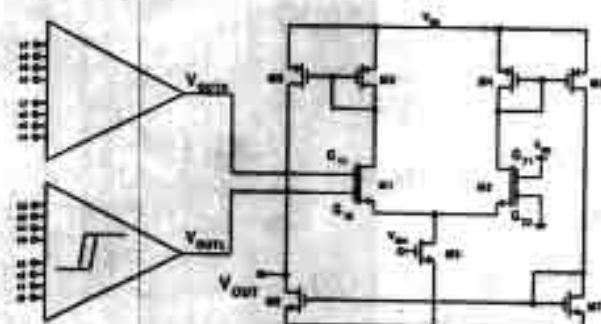


Figure 9. 8-bit digital comparator

It is seen that the 4-bit non-hysteresis comparator is used to compare the upper 4 bits where the three levels of output voltage at V_{OUT1} are delivered when $A > B$, $A < B$ or $A = B$. The 4-bit hysteresis comparator is used for the comparison of the lower 4 bits where only two levels of output voltage at V_{OUT2} are delivered. The third comparator is used as the main comparator, of which the referenced input is connected to V_{DD} and GND. The functions of the main comparator are summarized in table 2.

Table 2. Functions of the main comparator

Upper 4 bits output	Lower 4 bits output	Output
High / V_{DD}	X	High / V_{DD}
Equal / $V_{DD}/2$	High / V_{DD}	High / V_{DD}
Equal / $V_{DD}/2$	Low / GND	Low / GND
Low / GND	X	Low / GND

where X denotes don't care condition. It is seen that when the upper 4 bits of A are higher or lower than those of B, the output is High or Low immediately. If the upper 4 bits of A are equal to those of B, the output will correspond to the comparison result of the lower 4 bits of A and B. In order to have the functions correspond to Table 2, the main comparator must have the four input gates such as G_{11} , G_{12} , G_{21} , G_{22} designed with proper sizes. The weights of each input are denoted as k_{11} , k_{12} , k_{21} , k_{22} , correspondingly, which are considered as in table 3.

Table 3. Sizing criteria for the main comparator

Inputs		Output	Weight sum operations
V_{out1}	V_{out2}	V_{out}	
5V	X	5V	$k_{11} \times 5 + k_{12} \times 0 > k_{21} \times 5 + k_{22} \times 0$ $\therefore k_{11} > k_{21}$
0	X	0	$k_{11} \times 0 + k_{12} \times 5 < k_{21} \times 5 + k_{22} \times 0$ $\therefore k_{12} < k_{21}$
2.5V	0	0	$k_{11} \times 2.5 + k_{12} \times 0 < k_{21} \times 5 + k_{22} \times 0$ $\therefore k_{11} < 2 \times k_{21}$
2.5V	5V	5V	$k_{11} \times 2.5 + k_{12} \times 5 > k_{21} \times 5 + k_{22} \times 0$ $\therefore k_{11} + 2 \times k_{12} > k_{21}$

where 5V and 0 stands for the logic High and Low and X denotes the don't care condition. Examining the weight sum operations, we can conclude that all weights must conform to the condition that $k_{21} < k_{11} < 2k_{21} < k_{11} + 2k_{12}$. Suitable weights and sizes are summarized in Table 4.

Table 4. Design parameters of G_{11} , G_{12} , G_{21} , G_{22}

	G_{11}	G_{12}	G_{21}	G_{22}
Binary weights	12/16	4/16	3/16	9/16
Sizes(μm^2)	129.6 $\pm$ 22.8	43.2 $\pm$ 22.8	75.6 $\pm$ 22.8	97.2 $\pm$ 22.8
Capacitance(fF)	1916.4	638.8	1117.9	1437.3

The functionalities can be demonstrated by the simulation results in Figure 10.

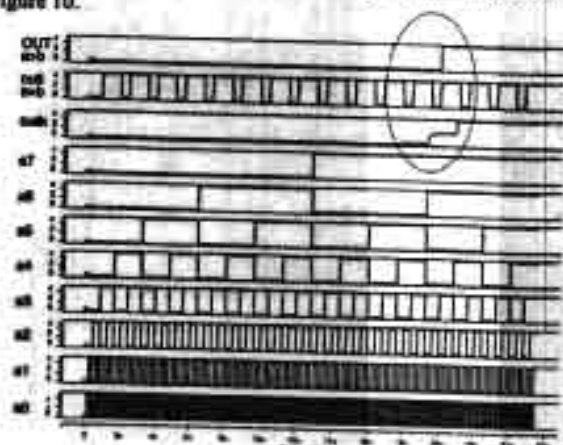


Figure 10. Simulation results of the 8-bits comparator

In Figure 10, the binary B is set to #b1000110 while the binary A is swept digitally from 0. It is seen that the V_{out1} of the upper comparator delivers $V_{dd}/2$ when the upper 4-bits of the binary A equal those of B, and then the output corresponds to the V_{out1} of the lower comparator.

6. CONCLUSIONS

A Hysteresis Tunable Voltage Comparator using FGMOS is proposed here. The circuit is essentially exploiting FGMOS devices in the positive feedback mode to create the hysteresis. The V_{TH} tunability of the FGMOS performs the hysteresis tuning effectively. This paper also presents a design for a non-clocked 8-bit digital comparator that essentially manipulates the proposed analog voltage comparator to realize a new digital circuit in which the signal is internally processed in an analog fashion. The proposed idea can be implemented on any standard double-poly CMOS and be useful in mixed signal and computational applications. All the simulation results confirm the functionality. The design optimizations will be determined in future studies.

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A LOW-VOLTAGE WIDE-SWING FGMOS CURRENT AMPLIFIER

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ABSTRACT

This paper proposes a new current amplifier circuit totally formed in the class AB structure utilizing CMOS inverters and the recently proposed additive analog inverter using floating-gate MOSFETs. Operating in a negative feedback topology, the amplifier can deal with wide signal swings up to $\pm 200\mu\text{A}$, with 1% of the THD and 10pF of C_L . Designs and HSPICE simulation results are demonstrated on 0.5 μm double poly CMOS processes with 1.5V and 1V power supplies to indicate high frequency and low power capabilities respectively.

1. INTRODUCTION

In the last decade, current-mode circuits [1] have drawn lots of interest due to their attractive features such as wide bandwidths, wide dynamic ranges and low voltage operations, all of which are very important for modern integrated circuits. Several elegant techniques for current-mode signal processing have been demonstrated successfully. These have mostly utilized current mirror cells, Gilbert gain cells and log-domain, square-root domain or translinear cells to perform filtering, multiplications, modulations, etc. For amplification purposes, current-mode amplifiers [2] based on a high open-loop current gain used for an accurate closed-loop configuration is also a very promising technique since use of a high gain device in a negative feedback loop allows large collection of transfer functions, performances of which are independent of the large but sensitive open-loop gain. So far, several high performance current amplifiers and opamps [3-9] have been proposed on CMOS technologies with various structures and topologies such as Differential Input Differential Output (DIDO), Differential Input Single-ended Output (DISO) or Single Input Differential Output (SIDO), etc. In general, the current opamp principle can be shown as a block diagram as in Fig.1, where the input current signal is firstly converted to a voltage quantity by the transimpedance amplifier (R_m) and then amplified again by the

transconductance amplifiers (G_m) to produce the output current and hence the open-loop current gain. There is usually at least one high impedance node in the circuit that should be connected by a compensation capacitor for stability.

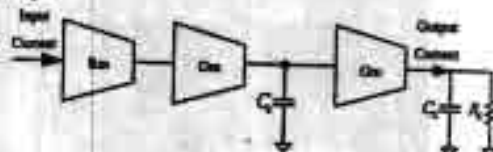
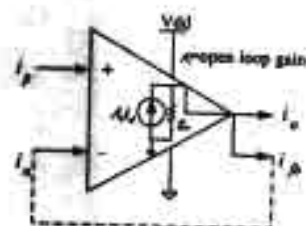


Fig.1 Current opamp principle

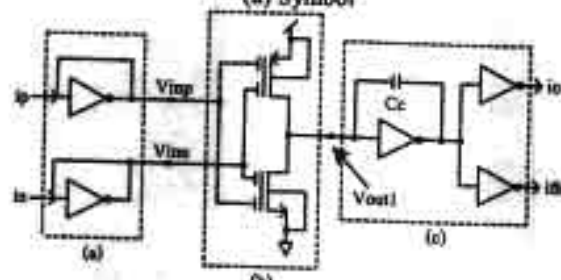
So far, most design efforts have been directed at the development of fully differential structures and enhancement of the open-loop gain and CMRR. In this work, we aim for a high signal swing by trying to avoid a class A circuit for which the limitation of current signal swing and slew rate is a result of the existing current sources, which also limit the charging current for the compensation capacitor at the high impedance node. Thus this paper proposes a new current amplifier circuit totally formed in the class AB structure utilizing CMOS inverters and the recently proposed additive analog inverter [10] using floating-gate MOSFETs. Since there is no biasing current source to limit the signal swing, our amplifier possesses a wide swing and high slew rate. The design is applied on a 0.5 μm CMOS with 1.5 Volts power supply to demonstrate high frequency operation and with 1 Volt power supply to show the feasibility of low power operations at a lower frequency range where all MOSFETs are biased in the weak inversion region.

2. THE PROPOSED CURRENT AMPLIFIER

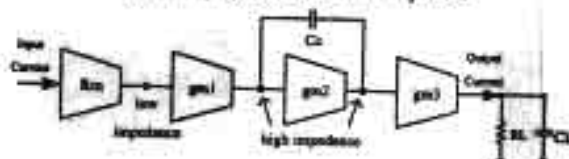
The proposed current amplifier, as symbolically shown in Fig.2(a), has two identical input terminals denoted as i_p and i_n and two output terminals delivering the same phase of the signal denoted as i_o and i_n , which are used as the output and the feedback port respectively. At the input terminals, it is noted that the input i_n can only be symbolized as an inverting terminal when the amplifier is connected in the negative feedback configuration as shown by the dashed line. This will be discussed later in this section.



(a) Symbol



(b) The proposed current amplifier



(c) Block diagram

Fig.2 The proposed current amplifier

In Fig.2(b), the amplifier comprises three circuit blocks as shown in the dashed boxes. The transimpedance amplifier is shown in box (a) and written as

$$R_m = \frac{1}{(g_{m_n} + g_{m_p})} \quad (1)$$

where g_{m_n} and g_{m_p} are respectively the transconductance of NMOS and PMOS of the inverter. The additive analog inverter in box (b) is basically a two-input CMOS inverter elegantly built from the floating-gate MOSFETs and proposed in [3]. It is employed in this circuit together with the other R_m and gm blocks to work as a differential amplifier because the polarity of i_n is inverse to those of i_p , causing the voltage at node V_{inn} to be inverse to those at node V_{imp} . Considering only the NMOS, a large signal current equation can be written as in (2) where the coefficient of V_{inn} is now negative.

$$I_D = \frac{1}{2} \mu C_{ox} \frac{W}{L} \left[(k_1 V_{imp} - k_2 |V_{inn}|) - V_s - V_{TH} \right]^2 \quad (2)$$

Here k_1 and k_2 are the capacitive division factors [10, 11] C_1/C_T and C_2/C_T , where C_1 and C_2 are the effective coupling capacitances between the input gates and the floating gate and C_T is the total capacitance seen from the floating gate. All capacitances correspond directly to the sizes of the input gates and the floating gate areas obtained from the layout of the circuit. In this case, the equal input

gate areas of i_p and i_n are set and result in equal values of C_1 and C_2 of 50fF and k_1 and k_2 of 0.5. The two-inputs CMOS inverter works as if a differential amplifier for which the small signal voltage gain between the output V_{out1} and the differential inputs can be derived as

$$\frac{V_{out1}}{(V_{imp} - V_{inn})} = -(g_{m_{in}} + g_{m_{ip}})(r_{o_{in}} // r_{o_{ip}}) \quad (3)$$

Here $r_{o_{in}}$ and $r_{o_{ip}}$ are the respective output resistances to the floating-gate NMOS and PMOS in the dashed box (b). With further analysis using the diagram in Fig.2(c), the open-loop current gain of the whole circuit can be derived as

$$A_i = R_m \cdot g_{m_1} r_{o_1} g_{m_2} r_{o_2} g_{m_3} \quad (4)$$

and the dominant pole frequency(ω_d) is

$$\omega_d = \frac{1}{r_{o_1} g_{m_2} r_{o_2} C_c} \quad (5)$$

while the GBW is

$$GBW = \frac{R_m \cdot g_{m_1} g_{m_3}}{C_c} \quad (6)$$

3. DESIGN AND SIMULATIONS

Based on the proposed concept, the design schematic can be simplified as shown in Fig.3, where it is seen that the circuit can be designed in a modular fashion where all inverters including the additive analog inverter have the same dimensions of NMOS and PMOS correspondingly. If a higher gain of the gm_2 and gm_3 blocks is required, we simply add more cells of the identical inverters in parallel. R_c and C_c are employed for the frequency compensation.

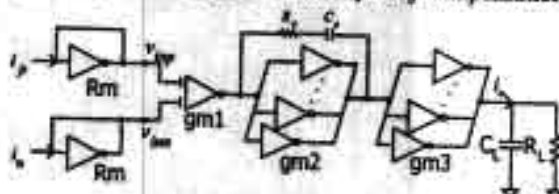
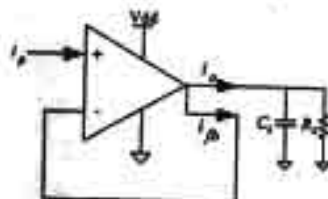


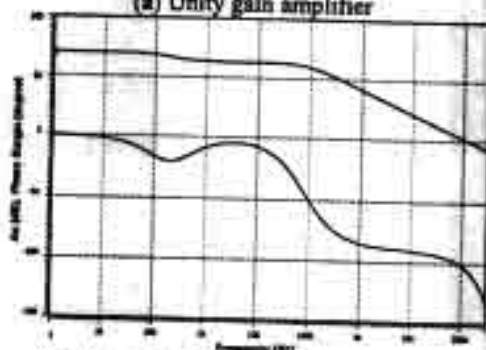
Fig.3 The design Schematic

On the Alcatel 0.5 μ m CMOS process, two amplifiers have been designed for V_{DD} of 1.5V and 1V to demonstrate high frequency operations and low power respectively. With V_{DD} of 1.5V, all NMOS and PMOS are designed with the dimensions of 6.9/0.5 and 23.6/0.5 respectively resulting in the idle currents of 30 μ A for each inverter. As seen in Fig.3, only one CMOS inverter is employed for each R_m and gm_1 block but extra input gates on Poly2 are connected to the inverter of the gm_1 block. Then four and three inverters connected in parallel are employed for the gm_2 block and the gm_3 block respectively. The amplifier is loaded with C_L of 10pF and R_L of 1.69k Ω that is the same value as R_m or its input resistance. To improve the phase

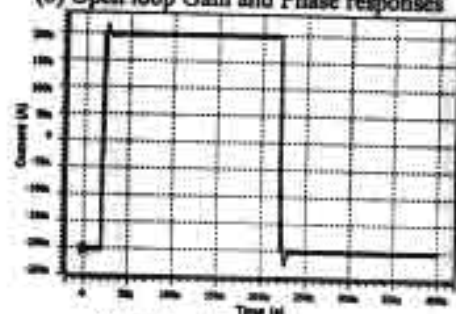
margin, R_C of 1k Ohms and C_C of 0.8pF are also included in the compensation scheme. The circuit was simulated on HSPICE with the performances shown in Fig.4 where 69.6dB Open-loop gain, 127MHz GBW and 74° Phase margin were achieved with a supply voltage of 1.5Volts and 635μW of power consumption. As a unity gain buffer, step response and linearity were measured at the maximum signal amplitude of ±200μA and are shown in Fig.4(d) and (e) where the 1% settling times are measured as 9.4 and 34.5 ns with and without C_L respectively.



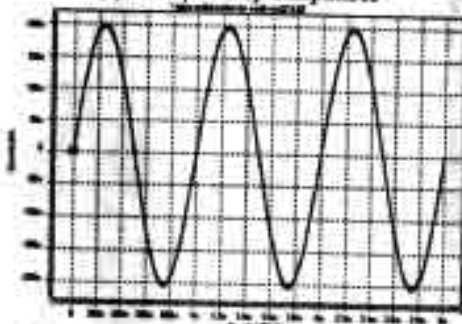
(a) Unity gain amplifier



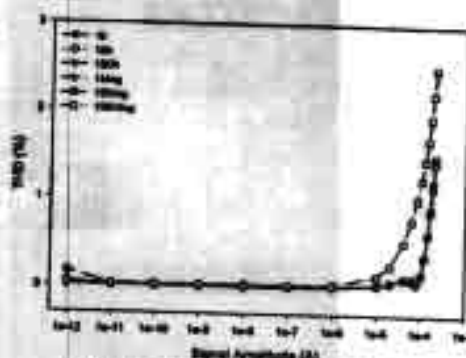
(b) Open loop Gain and Phase responses



(c) ±200μA Step Responses



(d) ±200μA Signal Swings of O/P vs. I/P



(e) THD vs. O/P signal amplitude

Fig.4 Simulation results

Another amplifier with a 1V power supply was designed including all NMOS and PMOS with the dimensions of 8/0.5 and 19.9/0.5 respectively operated in the weak inversion region. As in Fig.3, only one CMOS inverter is employed for each R_m and g_{m1} block. Then five and two inverters connected in parallel are employed for the g_{m2} block and the g_{m3} block respectively. The amplifier is loaded with C_L of 10pF and R_L of 47.86kΩ. From simulations, an open-loop gain of 68.3dB, with 2.68MHz GBW and 68° phase margin is achieved with 6μW power consumption. Due to space restrictions, not all performance graphs could be included here. However, in Table 1 all performances are compared with those of some earlier designs. The 1.5V V_{DD} version amplifier is also tested in negative feedback structure with passive networks to set the closed loop gains higher than 1 as shown in Fig.5.

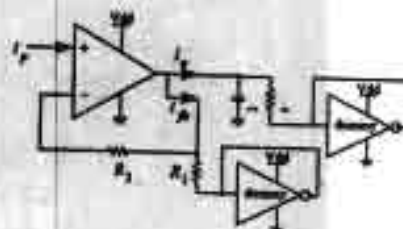


Fig.5 The amplifier in negative feedback

Fig.5 displays a non-inverting amplifier with a resistive negative feedback network. We arbitrarily put the dummy shorted input-output inverters to work as resistive loads and also to set the DC offset voltage to half of the V_{DD} which is the same DC voltage at all input and output nodes. Then the closed loop gain can be derived as

$$A_{CL} = 1 + \frac{R_2 + R_m}{R_1 + R_m} \quad (7)$$

where R_1 and R_2 are the resistances in the range of 0–10kΩ which are integrable value on a chip. The dummy inverter load is used to settle a proper dc level in order to avoid DC offset of the feedback current. From (7), R_m

with R_1 is the transimpedance of the dummy inverter while R_{in} with R_2 is the input resistance of the i_b terminal. Hence all R_{ins} are the same value. With V_{DD} of 1.5V, by setting R_1 at 10Ω and adjusting R_2 for various close-loop gains, the THD of the O/P signal were measured and shown in Fig.6 where the labels in the plot show details of the input signals.

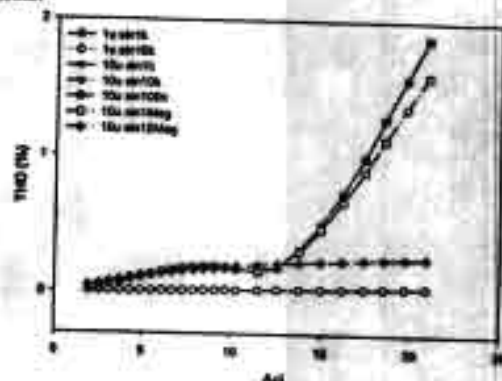


Fig.6 THD vs. Close-loop gain

4. CONCLUSION

This paper has proposed a new low voltage wide swing current amplifier that can receive a signal swing as large as $\pm 200\mu A$ amplitude while a THD of about 1% is still maintained. The circuits can totally be realized in the class AB thanks to the use of CMOS inverters and the available additive analog inverter cells using floating-gate MOSFETs. An effect of complex poles and zeros around the 100Hz of the open loop gain in Fig.4 (a) can be noticed as a result from the coupling capacitors of the FG MOS devices. A deep analysis will be placed as future works. In this paper, the circuit is called a current

amplifier instead of opamp due to the lack of CMRR capability, which will be part of our future works.

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TABLE 1 PERFORMANCE COMPARISONS

COA	[3] $\pm$	[3] $\otimes$	[4] $\pm$	[5] $\pm$	[6] $\pm$	[6] $\otimes$	[7] $\otimes$	[8] $\pm$	[9] $\pm$	Proposed	Units
Years	1997	1997	1998	2001	1992	1992	1993	1994	1994	2001	-
DC Gain	65	70	53	80	65	54	72	94.2	67	69.6	dB
UGBW	200	210	300	16	8	90	3	65	100	127	MHz
FM	60	>45	50	68	60	60	60	-40	61	74	°
Input Resistance	0.147	2	21	NA	3.65	5	NA	3.8	316	1.68	K Ω
Output Resistance	2.8	2	0.597	NA	0.899	0.186	NA	7.6	0.3	0.09	M Ω
Settling Time (1%)	5.1	NA	7.1	100	150	15	NA	NA	NA	34.5*	ns
Slew rate +/-	NA	NA	NA	+0.4	NA	NA	NA	NA	NA	+145/-170	$\mu A/ns$
R_c	NA	NA	NA	NA	NA	NA	NA	NA	NA	1	K Ω
C_c	NA	NA	NA	1.5	10	1.25	2	NA	NA	0.8	pF
R_L	NA	NA	NA	1	NA	NA	NA	NA	NA	1	K Ω
C_L	NA	NA	NA	NA	NA	NA	NA	NA	NA	10	pF
Power Dissipation	NA	4.5	<0.86	NA	3.1	4.6	NA	0.03	4.5	0.635	mW
Technology(CMOS)	1.2	1.2	0.6	0.8	2	2	2.4	2	1.2	0.5	μm
Supply	+3	+3	3	1.2	NA	NA	NA	NA	3	1.5	V

$\pm$ = Simulation results, $\otimes$ = Measured results, NA = not available, * = at $\pm 200\mu A$ step i/p, ** = at $4\mu A$ step i/p

- [3] K. Nandhasri, J. Ngarmnil, K. Moolpho, "A 2.8V RWDM BTL Class-D Amplifier using an FGMOS Comparator", 2002 IEEE International Symposium on Circuits and Systems (ISCAS2002), Phoenix, May, 2002.

A 2.8V RWDM BTL CLASS-D POWER AMPLIFIER USING AN FGMOS COMPARATOR

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ABSTRACT

This paper presents a design of an output stage based on Class-D amplifier techniques using Rectangular Wave Delta Modulation (RWDM) topology. This amplifier has a simple structure comprised only of a hysteresis comparator and output drivers. Thanks to the use of a multiple inputs hysteresis comparator using floating-gate MOSFETs, the amplifier is capable of low voltage operations. On Alcatel 0.5 μ m double poly CMOS process, this amplifier demonstrated to deliver up to 0.88Watts with 95% efficiency with a 2.8 Volts power supply. This means implementation as a monolithic chip is possible, making this amplifier suitable for portable applications such as speaker driving circuits in mobile phones, hearing aids and other implantable medical devices.

1. INTRODUCTION

Many audio power amplifiers are designed in class-A or class-AB, and so they normally deliver a limited efficiency because their power transistors operate in the linear area where a huge biasing or idle current is normally consumed in order to be able to deliver enough power to the loads. This then results in excessive power dissipation or heat. In order to improve the efficiency, switching converter techniques such as Pulse Width Modulation (PWM) can be applied to the development of audio amplifiers, referred to as switching amplifiers or class-D type [1,2]. This type of amplifier presents several advantages over conventional class-A or AB amplifiers in their high efficiency and low internal power dissipation. In this work we present the development of a class-D amplifier based on the RWDM technique [3] utilizing a multiple input hysteresis voltage comparator using floating-gate MOSFETs to allow low voltage operation for the amplifier. The circuit is then suitable for production as a monolithic chip for battery-operate applications such as speaker driving circuits in mobile phones, hearing aids and other implantable medical devices. Designs and simulation results will be discussed in detail below.

2. CLASS-D AMPLIFIER

Conventionally, most class-D amplifiers are based on the Pulse Width Modulation (PWM) technique where the pulse width of the output PWM signal produced is proportional to the amplitude of the modulating signals between the audio input signal and the triangular signal. The signal at the output is recovered from the PWM signal by a low pass filter, which could be formed by a loaded resistor and an inductor inherently obtained from earphones or speakers. Fig.1 shows the basic building blocks of a conventional class D amplifier comprising triangular waveform generator, comparator and output driving stage.

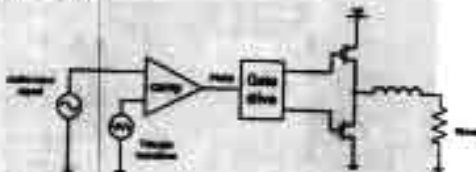


Fig. 1 Conventional PWM class-D amplifier

From Fig.1, the comparator compares the audio signal input with the triangular waveform from the waveform generator to produce a PWM signal, which is then used to control the switching timing of the output stage transistors to drive a low impedance load. The output power delivered to the load is proportional to the average output current controlled by the duty cycle of the PWM signal. The duty cycle is 50% when there is no signal at the input, thus the average output voltage is zero. PWM class-D amplifiers can dissipate less power by properly arranging the switching timing of the output power MOSFETs between the two lowest-dissipation modes such as fully on and fully off.

Another promising technique used in class-D amplifiers is the RWDM principle shown in Fig.2. In concept RWDM is similar to PWM except that the input signal denoted as $V_A(t)$ is compared with the feedback signal $V_F(t)$ which is essentially the integrated signal of RWDM by a low-pass filter. Hence loading conditions from the loads are taken into account to control the RWDM signal and then to control the output power. Since there is a hysteresis in the

comparator, $V_e(t)$ can track the amplitude of $V_R(t)$ within the $\pm\Delta V$ boundary as shown in Fig.2.

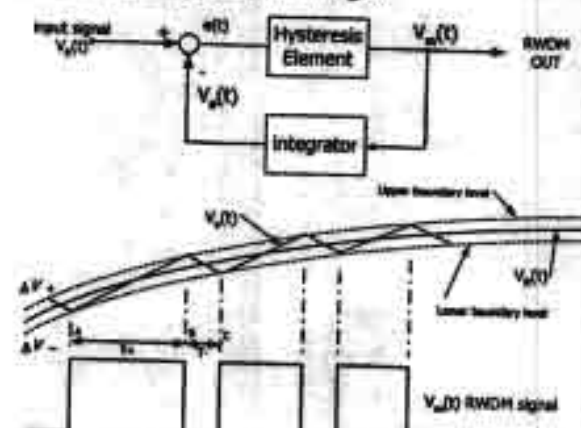


Fig. 2 Block diagram of the RWDM technique

Based on the RWDM mechanism in Fig.2, the switching frequency of the RWDM output signal can be calculated as in (1)

$$f = \frac{1}{T} = \frac{S_C}{4\Delta V} \left[1 - \left(\frac{S_R(t)}{S_C} \right)^2 \right] \quad (1)$$

where S_R and S_C denote the slopes of the input signal $V_R(t)$ and the feedback signal $V_e(t)$ respectively and ΔV is the tracking boundary corresponding to the magnitude of the hysteresis loop which is controlled directly by the trip voltage of the hysteresis comparator. S_C is also controlled by the time constant of the integrator in the feedback path.

3. THE PROPOSED RWDM CLASS-D AMPLIFIER

A new proposed class-D amplifier based on the RWDM technique is presented as a block diagram in Fig.3, where it is seen that the amplifier comprises only a hysteresis comparator, driving circuits and an integrator formed by the resistor inductor low-pass network. The circuit can be integrated onto a monolithic chip except for the inductor and the load resistor.

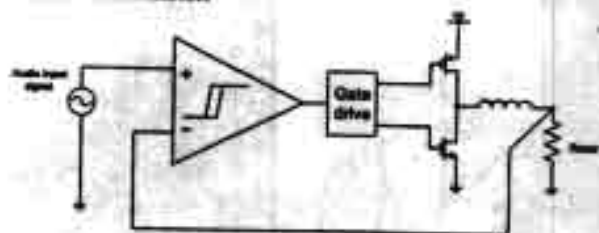


Fig.3 The Proposed Concept

From Fig.3 the audio input signal is directly connected to the input of the comparator, which is basically a high impedance node since it is the input gate of a MOSFET. Hence no loading of the signal source occurs. The comparator then compares the input signal with the feedback signal from the output. With the built-in hysteresis loop, the comparator can produce the output RWDM signal comprising only logic low or high that is then integrated by the inductor resistor network. The feedback signal as a saw-tooth-like signal is then used to compare with the input signal in the next cycle.

3.1 The Hysteresis Comparator

The hysteresis can be shown as the range between V_{TRP+} and V_{TRP-} as in Fig.4. In this paper, we expand the switching range of a hysteresis comparator to control the amount of output ripple and switching frequency of the Class-D amplifier.

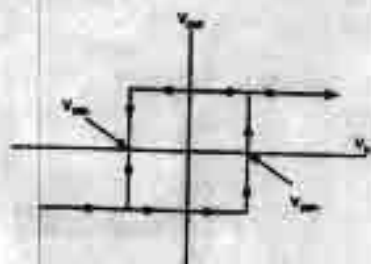


Fig.4 Hysteresis loop

An example of the hysteresis comparator [4, 5] is shown in Fig.5, where it is seen that the hysteresis is generated from a positive feedback produced by M10 and M11. The positive feedback occurs only when the current ratio of I_{D10}/I_{D11} or I_{D11}/I_{D4} is greater than one.

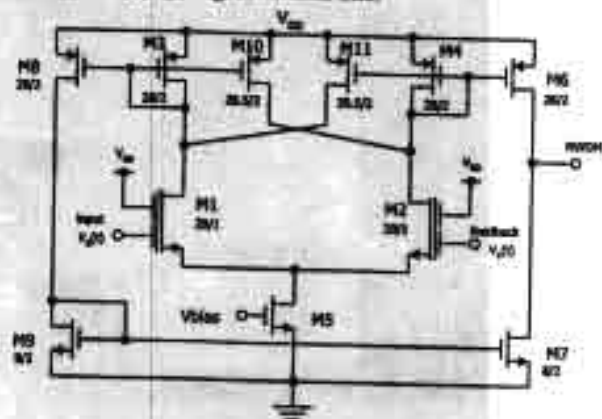


Fig.5 Rail to rail input hysteresis comparator

The hysteresis comparator shown in Fig.5 is able to receive a wide-range input signal. This particular ability is

achieved by the employment of the two-inputs floating-gate MOSFETs (FGMOS) [5, 6] as the input transistors M1 and M2 of the differential amplifier. This characteristic allows the feedback signal at the gate of M2 to track the amplitude of the input signal at the gate of M1 effectively between the supply voltage and ground. Hence low voltage operation is possible. This is results because one of the input gates of both M1 and M2 are connected to V_{DD} , so both FGMOSs M1 and M2 are ensured to be turned on at all levels of the input signal. In other words, the comparator basically possesses the rail-to-rail characteristic.

3.2 FGMOS Basic Principles

FGMOS is an ordinary MOSFET except that the gate, which is built on the conventional poly1, is floating and then called 'Floating-Gate'. The structure of FGMOS is shown in Fig.6.

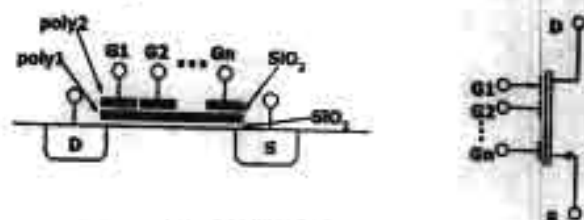


Fig.6 FGMOS structure

A multiple input MOSFET based on the FGMOS structure [6,7] is shown in Fig.6. It comprises the floating gate, and input gates (G1, G2) built on Poly2, which are coupled to the Poly1 gate by the capacitors between Poly1 and Poly2 denoted as C_1 and C_2 . Assuming zero initial charge on the floating-gate, the drain current can be written as

$$I_D = \frac{1}{2} \mu C_{ox} \frac{W}{L} [(k_1 V_{G1} - V_s) - (V_{th} - k_2 V_{G2})]^2 \quad (2)$$

$$I_D = \frac{1}{2} \mu C_{ox} \frac{W}{L} [(k_1 V_{G1} + k_2 V_{G2}) - V_s - V_{th}]^2 \quad (3)$$

where k_1 and k_2 are C_1/C_T and C_2/C_T respectively and C_T is the total capacitance of the floating gate. The drain current is essentially a linear sum of all inputs weighted by the capacitive coupling ratios. Equation (2) is arranged to show the threshold operation with only two input gates assumed. It is seen that V_{G1} can be utilized as a signal port while V_{G2} is used to tune the effective threshold voltage. Equation (3) is written to show a linear sum of the weighted multiple-input voltages. This operation ensures the comparator has the capability to handle large input signal swings while it still operates in the saturation region as mention before.

4. THE PROPOSED RWDM BTL CLASS-D

A Bridge Tied Load (BTL) class-D amplifier based on the RWDM technique is presented in Fig.7. It is basically a fully differential version of the proposed RWDM concept shown in Fig.3. With the BTL configuration the output voltage swing can be double those of the half-bridge configuration in Fig.3. The audio input signal is directly connected to the input of the comparator, which is normally in the range of $0-V_{DD}$ so we use 3-inputs floating-gate MOSFETs as the input differential pairs of the hysteresis comparator.

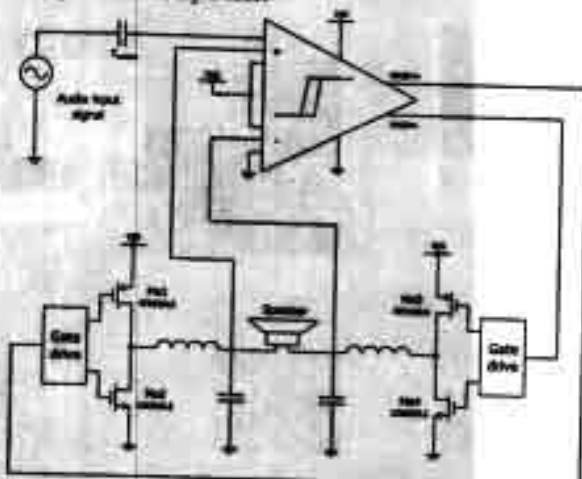


Fig.7 The proposed RWDM BTL class-D amplifier

In Fig.8, the 3-inputs fully differential hysteresis comparator comprises three-input gates FGMOS devices as the differential pairs of which the coupling capacitors are designed as $C_1=200fF$, $C_2=128fF$ and $C_3=64fF$ which correspond to the capacitive coupling ratios of k_1 , k_2 and k_3 to 0.5, 0.32 and 0.16 respectively. The first inputs of both plus and minus terminals having the weight factor of 0.5 are connected to V_{DD} to bias the differential pairs. This results in a DC potential of $0.5V_{DD}$ at the floating-gate on Poly1 of the differential pairs. The 2nd input gates having weight of 0.32 are used as the inputs of the comparator while the 2nd gate of M1 is connected to the AC-coupled audio input signal and the 2nd gate of M2 is connected to Gnd. The weights of the 2nd inputs allow a wide input swing for the comparator. The 3rd input gates with the weight of 0.16 are connected to output nodes of the amplifier respectively. They are designed with half of the weight factor of the 2nd gates in order to make the close loop gain of the amplifier equal to 2, which is the requirement to have an output signal swing of $\pm 2.8V$ while the input signal swing is only in the range $0-2.8V$. The other advantage of this fully differential comparator is that the RWDM output signals from the comparator are exactly out of phase without any delay. The control of the

power MOSFETs of both sides of the loads will be very precise. Dimensions of all MOSFETs are also shown in the figure.

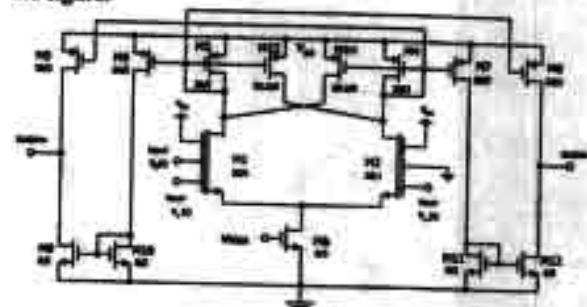


Fig.8 Fully differential comparator

5. SIMULATION RESULTS

Based on the proposed circuit in Fig.7, the amplifier has been designed on Alcatel 0.5 μ m CMOS process with 2.8 Volts power supply. The amplifier can deliver current to the 8 Ω resistive loads and correspond to the output signal of 5.2V_{pp}. Other performances based on simulation results on HSPICE are summarized in Table 1.

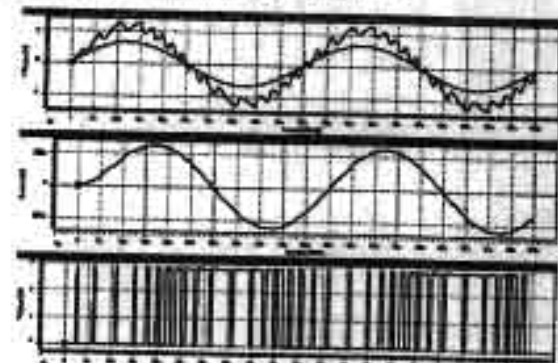


Fig.9 The voltage output signal, the current output signal and the RWDm output signal at input 1.3V_p, 20kHz

Table 1 Summary of the proposed amplifier

Process technology	Alcatel 0.5 μ m CMOS
Supply voltage	2.8V
Static Power dissipation	79.51 μ W
Maximum output swing	5.2V _{pp}
Output load	8 Ω
Maximum power	0.88W
Efficiency	95%

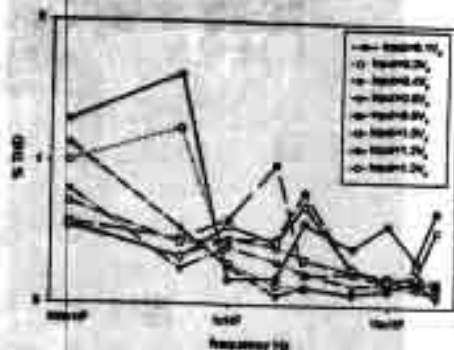


Fig.10 THD vs. Signal frequency and input amplitude

6. CONCLUSIONS

A single-chip low-voltage high-efficiency Class-D Power Amplifier for portable devices has been proposed. The amplifier has a very simple architecture that makes it easier for it to be integrated with other circuit blocks on a system level. By virtue of the high efficiency of Class-D architecture coupled with the low voltage operation provided by the use of floating-gate MOSFET hysteresis comparator, this amplifier is suitable for portable devices with battery operations. It exhibits high distortion at low input signal due to the small changing of the input signal compared to the ripple at the output. The efficiency of this circuit is 95% at 0.88Watt with a 2.8V power supply.

7. REFERENCES

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FLOATING-GATE MOSFETS ANALOG CIRCUIT BUILDING BLOCKS: DESIGN PERSPECTIVE

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ABSTRACT

Floating-gate MOSFET on a standard double-poly CMOS offers various new useful functions which can be used to create many novel circuits in both analog and digital circuits. This paper reviews some recently proposed FGMOS circuits, such as a hysteresis tunable voltage comparator, analog-based digital comparators, a low-voltage class AB current-mode amplifier circuit and its filtering application. Designs and HSPICE simulation results are demonstrated on standard double poly CMOS processes.

1. INTRODUCTION

Recently, many applications of Floating-gate MOSFET or FGMOS devices in analog circuits have been reported [1-6]. Normally playing a key role in modern integrated memories such as EEPROM and Flash, FGMOS has some unique characteristics which could be applied to design many new circuits or to enhance existing analog circuits for having extra special features such as very low voltage, low power and high complexity functions. This paper reviews the recently proposed analog and digital comparators based on an exploitation of the FGMOS. First, a hysteresis tunable analog comparator is constructed with an electronically tunable positive feedback factor obtained by threshold voltage tuning of the embedded FGMOS devices. Then, digital comparators are developed by essentially modifying the proposed analog voltage comparator to be a new digital circuits in which signal are internally processed with analog mechanism. Moreover, a high open-loop gain current amplifier circuit totally formed in the class AB structure utilizing CMOS inverters and floating-gate MOSFETs is also reviewed with its attractive features such as wide bandwidths, wide dynamic ranges and low voltage operations. Based on the high open loop gain amplifier, a single amplifier biquad is designed and demonstrated as an application of the proposed current amplifier.

2. FGMOS BASIC PRINCIPLE

FGMOS is an ordinary MOSFET except that the gate, which is built on the conventional poly1, is floating and then called 'Floating-Gate'. The structure of FGMOS is shown in Fig. 1.



Fig.1 FGMOS structure

A multiple input MOSFET based on the FGMOS structure [2-3] is shown in Fig.1, which is seen that it comprises the floating gate, and input gates ($G_1, \dots, G_n$) built on Poly2, which are coupled to the Poly1 gate by the capacitors between Poly1 and Poly2 denoted as $C_1, \dots, C_n$. Assumed with the zero initial charge on the floating-gate and only two input gates, the drain current can be written as

$$I_D = \frac{1}{2} \mu C_{ox} \frac{W}{L} [(k_1 V_{G1} - V_t) - (V_{th} - k_2 V_{G2})]^2 \quad (1)$$

$$I_D = \frac{1}{2} \mu C_{ox} \frac{W}{L} [(k_1 V_{G1} + k_2 V_{G2}) - V_t - V_{th}]^2 \quad (2)$$

where k_1 and k_2 are capacitive coupling ratios C_1/C_T and C_2/C_T respectively and C_T is the total capacitance of the floating gate. The drain current is essentially a linear sum of all inputs weighted by the ratios. Equation (1) is arranged to show the threshold voltage tuning. It is seen that V_{G1} can be utilized as a signal port while V_{G2} is used to tune the effective threshold voltage. Equation (2) is written to show a linear sum of the weighted multiple-input voltages.

3. HYSTERESIS TUNABLE COMPARATOR

A hysteresis tunable comparator was proposed in [7], based on an electronically tunable positive feedback factor produced by threshold voltage tuning of the embedded FGMOS devices.

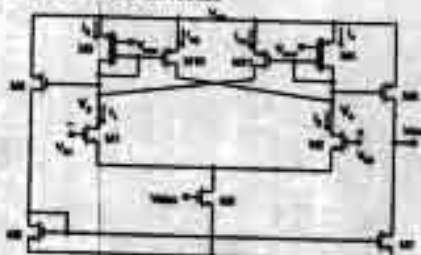


Fig.2 Hysteresis Analog Comparator

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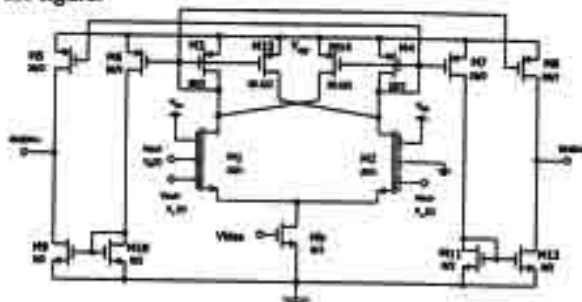


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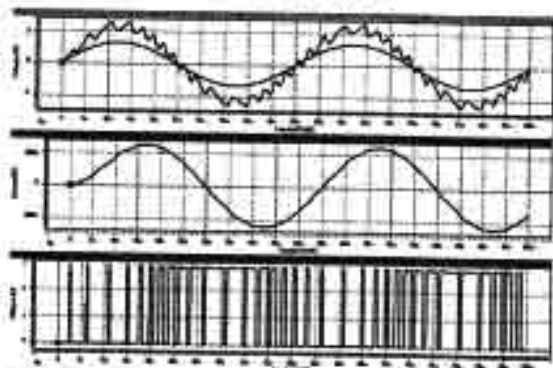


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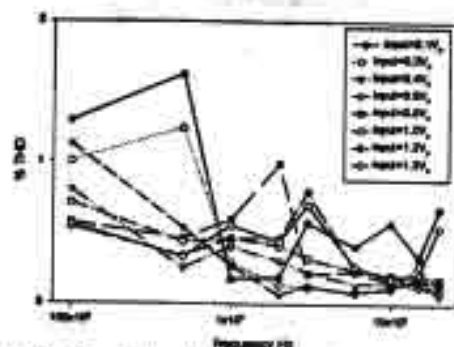


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FLOATING-GATE MOSFETS ANALOG CIRCUIT BUILDING BLOCKS: DESIGN PERSPECTIVE

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ABSTRACT

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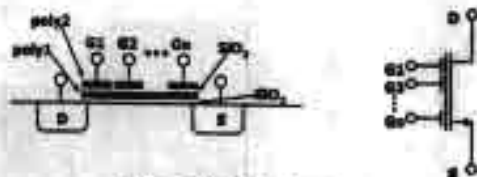


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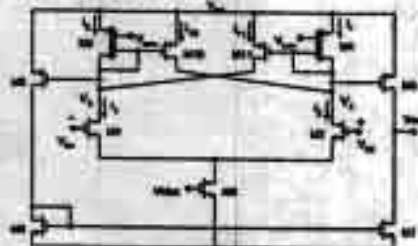


Fig.2 Hysteresis Analog Comparator

The hysteresis tunable analog comparator is shown in Fig. 2 where M_3 and M_4 are FGMOSs. The hysteresis involves positive feedback produced by M_{10} and M_{11} . The positive feedback occurs only when the current ratio of I_{10}/I_3 and I_{11}/I_4 are greater than one. If the ratio is higher, the amount of the feedback current will be increased and results in a wider of the positive and negative trip point voltage, V_{TRP+} and V_{TRP-} . Hence the hysteresis can be controlled. The V_{TRP+} and V_{TRP-} can be derived from the condition that I_2 equals to I_{10} and I_1 equals to I_{11} , correspondingly as,

$$\begin{aligned} V_{TRP+} &= \sqrt{\frac{2I_2}{\beta_1}} \left(\frac{\sqrt{I_{10}/I_3} - 1}{\sqrt{1 + I_{10}/I_3}} \right) \\ V_{TRP-} &= \sqrt{\frac{2I_2}{\beta_1}} \left(\frac{\sqrt{I_{11}/I_4} - 1}{\sqrt{1 + I_{11}/I_4}} \right) \end{aligned} \quad (3)$$

Based on (1), since FGMOS allows us to tune drain current, the ratio of I_{10}/I_3 and I_{11}/I_4 can be tuned electronically by V_{toss} at the input gate of M_3 and M_4 . Also V_{TRP+} and V_{TRP-} can be tuned orthogonally if the tuning voltage at the input gates of M_1 and M_2 are different. M_3 and M_4 are designed with an equal area of G_1 and G_2 as $10.8 \times 22.8 \mu\text{m}^2$ while the floating-gate area is set to $13.2 \times 2.4 \mu\text{m}^2$, which is also equal to those of M_{10} and M_{11} . Fig. 3 shows the simulation results of V_{TRP+} and V_{TRP-} vs. V_{toss} varied in the range of 2.5-5.0V.

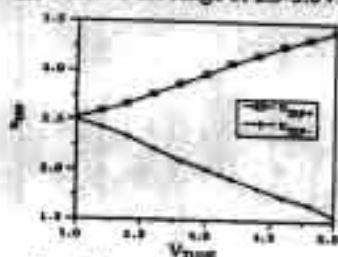


Fig. 3 V_{TRP+} and V_{TRP-} vs. V_{toss}

To express the performance of the comparator in a noisy environment, the circuit was tested with a noise-modulated signal with the noise amplitude set to $0.4V_{DD}$. Simulation results are shown in comparison with those from a non-hysteresis comparator in Fig. 4.

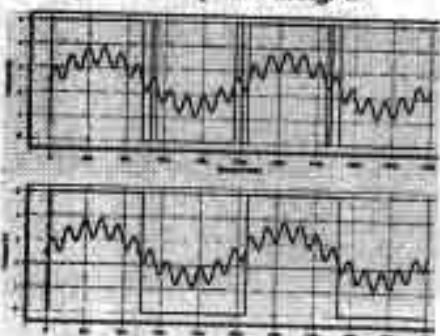


Fig. 4 Simulation results without and with hysteresis

4. ANALOG-BASED DIGITAL COMPARATORS

Based on the proposed analog comparator, a new digital comparator [7] can be realized by doing a minor modification at the input devices. A hysteresis 4-bit digital comparators can be developed as in Fig. 5 by employing FGMOSs as the input devices of which the sizes of the input gate are based on the significant of the binary weight. With hysteresis operation, this circuit performs two comparative functions of $A > B$ or $A \geq B$ which depend on the level of V_{toss} . It is evidently shown in Fig. 3 that if V_{toss} is high or set to 5V, the current ratio I_{10}/I_3 and I_{11}/I_4 will be high and result in a large hysteresis. Then the comparator performs the operation $A > B$, where the value of A must be higher than B for some extent to cause the comparator tripping. On the other hand, if V_{toss} is low or set to 0V, the positive feedback will be minimized and result in no hysteresis. Then the comparator performs the operation $A \geq B$.

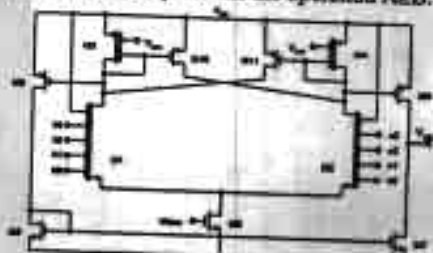


Fig. 5 Hysteresis 4-bits Digital Comparator

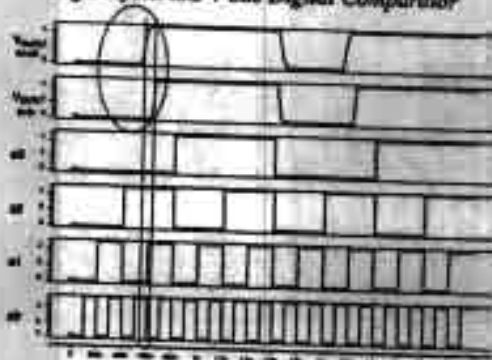


Fig. 6 Simulation results of the hysteresis comparator

From Fig. 6, the binary bits b3-b0 are set to #b0101 while the binary bits a3-a0 are swept digitally. It is seen that when V_{toss} is set to Low, the output signal changes its stage when both binary sets are equal. The circuit performs the function $A \geq B$. If V_{toss} is set to High, the comparator performs the function $A > B$. A simple non-hysteresis digital comparator is shown in Fig. 7 which is different from Fig. 5 in that there is no positive feedback mechanism. The circuit performs three functions at the output node such as $A < B$, $A > B$ and $A = B$. The output voltage is logic High or Low when the binary inputs at the positive terminal is higher or lower than that of the negative terminal respectively. The output is $V_{DD}/2$ when the binary inputs of both terminals are equal. This particular function implies an ability to detect the equality

of the binary inputs. The functionalities are confirmed by the simulation results in Fig. 8.

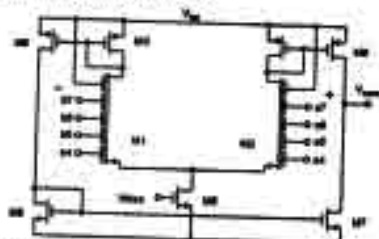


Fig. 7 Non-hysteresis 4-bits Digital Comparator

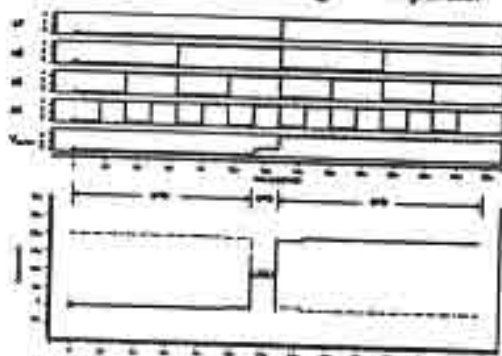
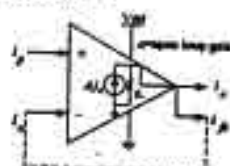


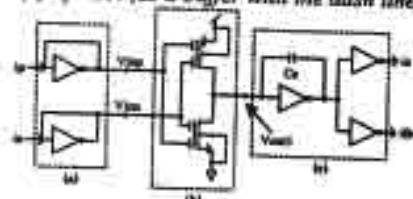
Fig. 8 Simulation results of the non-hysteresis comparator

5. LOW VOLTAGE CURRENT AMPLIFIER

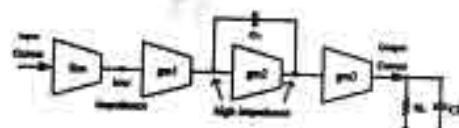
A current amplifier circuit [8] totally formed in the class AB structure utilizing CMOS inverters and FG MOS devices is presented here on 0.5 μ m double poly CMOS processes with 1.5V. As a buffer, the amplifier can deal with wide signal swings up to $\pm 200\mu$ A, with 1% of the THD and 10pF of C_L . The proposed current amplifier, as symbolically shown in Fig. 9(a), has two identical input terminals denoted as i_p and i_n and two output terminals delivering the same phase of the signal denoted as i_o and i_{fb} , which are used as the output and the feedback port respectively. It is noted that the input i_n can only be symbolized as an inverting terminal when the amplifier is connected in the negative feedback configuration as shown by the dashed line.



(a) Symbol (as a buffer with the dash line)



(b) The proposed current amplifier



(c) Block diagram

Fig. 9 The proposed current amplifier

In Fig. 9(b), the amplifier comprises three circuit blocks as shown in the dashed boxes. The transimpedance amplifier is shown in box (a) and written as

$$R_m = \frac{1}{(g_{m_n} + g_{m_p})} \quad (4)$$

where g_{m_n} and g_{m_p} are respectively the transconductance of NMOS and PMOS of the inverter. The additive analog inverter in box (b) is basically a two-input CMOS inverter elegantly built from the floating-gate MOSFETs and proposed in [9]. It is employed in this circuit together with the other R_m blocks to work as a differential amplifier. Hence the polarity of i_{fb} is inverse to those of i_p , causing the voltage at node V_{in} to be inverse to those at node V_{out} . Based on the diagram in Fig. 9(c), the open-loop current gain of the whole circuit can be derived as

$$A_i = R_m \cdot g_{m_1} r_{o1} g_{m_2} r_{o2} g_{m_3} \quad (5)$$

where r_{o1} , r_{o2} are the output resistance of g_{m_1} , g_{m_2} stages while the GBW is

$$GBW = \frac{R_m \cdot g_{m_1} g_{m_2}}{C_c} \quad (6)$$

The final design schematic can be illustrated in Fig. 10, where it is seen that the circuit can be designed in a modular fashion where all inverters including the additive analog inverter have the same dimensions of NMOS and PMOS correspondingly. If a higher gain of the g_{m_2} and g_{m_3} blocks is required, we simply add more cells of the identical inverters in parallel. R_c and C_c are employed for the frequency compensation.

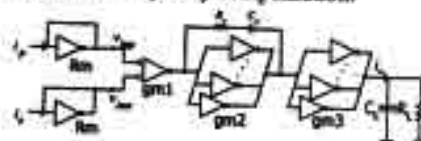


Fig. 10 Design schematic

On the Alcatel 0.5 μ m CMOS process, the amplifiers have been designed with V_{DD} of 1.5V. All NMOS and PMOS are designed with the dimensions of 6.9/0.5 and 23.6/0.5 respectively resulting in the idle currents of 30 μ A for each inverter. Four and three inverters connected in parallel are employed for the g_{m_2} block and the g_{m_3} block respectively to increase the gain. The amplifier is loaded with C_L of 10pF and R_L of 1.69k Ω , while R_c of 1k Ω and C_c of 0.8pF are set in the compensation scheme. The circuit was simulated on HSPICE with the performances shown in Fig. 11 where 69.6dB Open-loop gain, 127MHz GBW and 74° PM were achieved with 635 μ W power consumption.

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A High Speed Low Input Current CMOS

Current Comparator

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ABSTRACT

A new high speed low input current comparator is proposed in this paper. Based on a simple negative feedback scheme around the transimpedance stage with an emphasis on a very large loop-gain, the transformed voltage signal is maintained at the lowest swing that results in a speed improvement. On a 0.25µm TSMC CMOS process, simulation results demonstrate propagation delays of 3.6ns with $\pm 100\mu\text{A}$ input current and 1.5Vdc power supply, while the smallest input current is $\pm 50\mu\text{A}$. Performances are also shown with other V_{DD} as such as 1.0, 1.8 Vdc.

1. INTRODUCTION

In the last decade, current-mode circuits [1]-[3] have drawn lots of interest for modern integrated circuits and sensory systems. This is due to their attractive features such as high speed, wide dynamic ranges and low voltage operation, all of which are mainly due to the fact that all node voltages swing are very low. In analogue and mixed signal processing, the current comparator is also one of the key elements. The circuit is not purely in a current-mode operation since although the input signal is current the output signal is digital logic or rail to rail voltage signal. Obviously there is a requirement to transform the input current to a large voltage signal. Thus to design a high speed current comparator, one has to take care of the voltage swing carefully since it directly determines the propagation delay. Conventionally, most reported current comparators [4]-[7] are based on the concept shown as a block diagram in Figure 1(a), where the input current signal is converted to the voltage V_{in} and V_1 by the transimpedance stage comprising inverter amplifier A_1 and voltage buffer A_2 . The resulting voltage V_1 is then amplified by the latter high gain inverter amplifiers A_3 to produce output logic voltage. There exist parasitic capacitors at all nodes. Ideally for high speed comparators, the signal swing at V_1 should be maintained as small as possible and situated exactly around the inverter threshold voltage of the buffer A_2 . However, the reported works were relating to improve the lowest input current acquiring ability by arranging a proper biasing to turn on the MOSFETs of the buffer A_2 all the time. Most of them

utilized diode connected MOSFETs as a level shifter to create V_{OS} of the buffer MOSFETs. It is seen that although the transimpedance stage is formed in a negative feedback loop a much larger loop gain has not been exploited to keep the signal V_{in} and V_1 as low as possible. Moreover with a larger loop gain, the input impedance at node V_{in} could be much lower and receive a much smaller input current in the pico Amps range. The so called dead zone which is the smallest input current range to which comparators are insensitive is then minimized. However, a drawback of having the small voltage swing at V_1 is that the gain of the latter inverter amplifier must be necessarily high with hence a higher power consumption. Obviously, there is a conflict that if a speed as a result of a small voltage swing of the transimpedance stage is desired, a very high gain of the latter inverter amplifier will be necessary to provide the rail to rail output swing. In this paper, we propose an idea based on Figure 1(b), where a much higher loop gain is emphasized to gain speed and then trade power to the latter high gain inverter amplifier. The circuit utilizes only CMOS inverters and is suitable for a low V_{DD} operation.

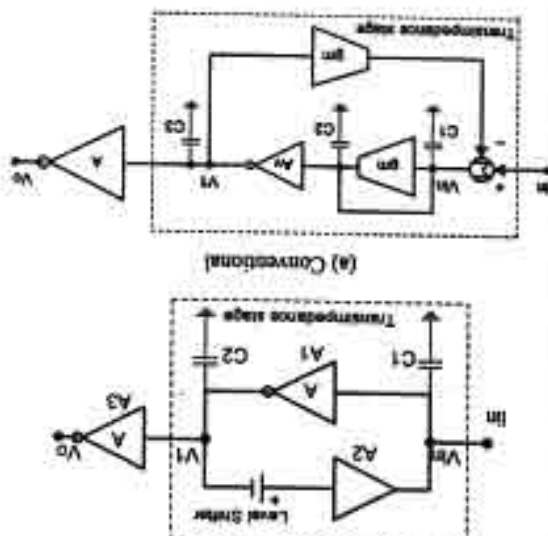


Figure 1 Current comparator concepts

2. THE PROPOSED CIRCUIT

As discussed above, we concentrate on a high speed or smallest average propagation delays and low input current acquiring capability or smallest dead zone. In this work, we trade off power for the required speed by maintaining the lowest voltage swing of the transimpedance stage and then providing high power to build up the latter high gain stage using inverter amplifiers. We then focus on the two separated circuit blocks as follows.

2.1. TRANSMIMPEDANCE STAGE

The transimpedance stage, shown as the dashed block in Figure 2, plays the most important role in determining the speed of the comparator. It is seen that the whole stage is formed in a negative feedback loop by observing the polarities of output voltages and currents of each inverter. A_1 as a shorted input-output transconductance amplifier or inverter is basically an equivalent grounded resistor with the value of $1/g_{m1}$. A_2 and A_3 are two high voltage gain amplifiers constructed from two cascaded inverters. Since there are two high impedance nodes in the loop RC frequency compensation is necessary to make the circuit stable. Capacitor C is set to 0.1 pF while the resistor R is set to 1.6 kΩ. Note that the C and R could be made from a parasitic capacitor and a triode MOSFET respectively. The transconductance amplifier A_4 is used to provide negative feedback current to the input node. All amplifiers A_1 to A_4 are CMOS inverters designed with the same dimensions which are $2.1\mu\text{m}/0.25\mu\text{m}$ and $7\mu\text{m}/0.25\mu\text{m}$ for W/L of NMOS and PMOS respectively.

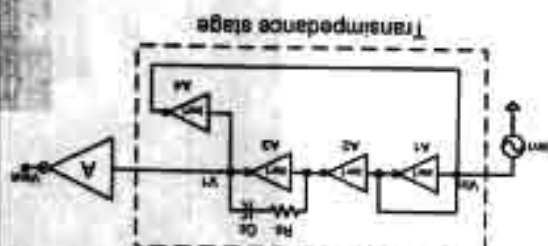


Figure 2 Transimpedance stage

Constructed in the feedback loop, the input resistance at node V_{in} can be derived as

$$R_{in} = \frac{1}{1 + g_{m1} (1 + A_2^2)} \quad (1)$$

where g_{m1} is an equivalent transconductance of A_1 and A_2 is a voltage gain of the amplifier A_2 and A_3 . Note that all inverters have the same transconductance and voltage gain because they have the same dimensions. It is seen that the input resistance R_{in} is very small which results in a minimum voltage swing at node V_{in} and also the same value of V_{in} at the output of A_4 . Figure 3 shows an

open loop gain and phase of the feedback current to the input current. It is seen that the gain of 56 dB, GBW of 906 MHz and PM of 45° are achieved in the open loop transconductance stage. With this specification, we have enough loop gain to suppress signals for the lowest voltage swings at V_{in} and V_{out} as shown in Figure 4. The negative feedback also stabilizes the common-mode voltage at all nodes to $V_{DD}/2$ which is set by the node V_{in} . This property is crucial for assuring that the signal swing is very small and also situated right at the center of the gate threshold voltage of the latter inverter of the gain stage.

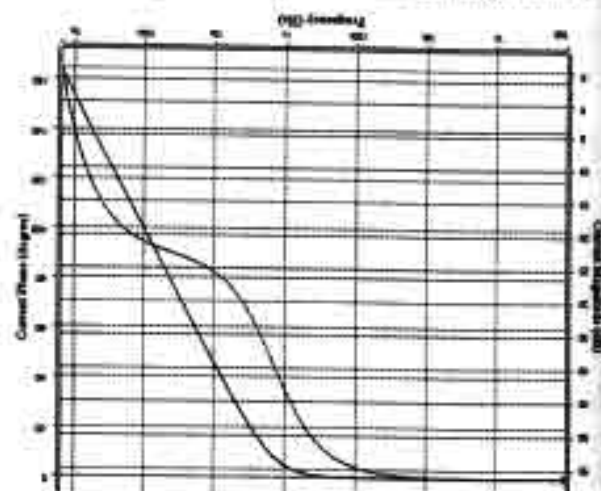


Figure 3 Open-loop responses of the transconductance stage

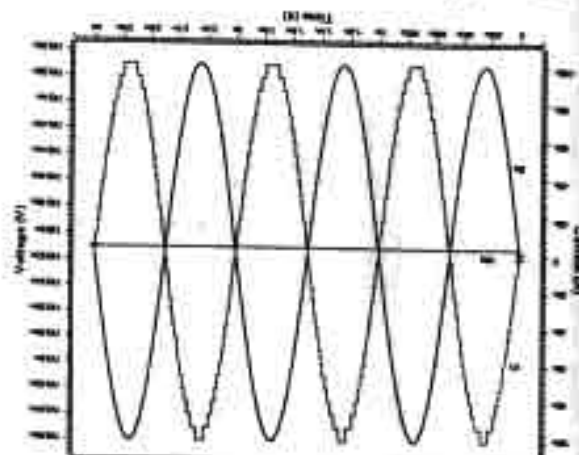


Figure 4 Voltage swings at V_{in} and V_{out} vs. input current

2.2. GAIN STAGES

We have now a very small voltage swing V_{in} at the input of A_4 of the gain stage. The main aim in designing this part is to construct high voltage gain to produce rail to rail output logic. Based on the use of the same dimension inverters, we can construct the high gain stage in a modular fashion. INV1 has the same dimension as those in the

transconductance stage. INV2 has smaller dimensions than those of INV1 by half, i.e. $1\mu\text{m}/0.25\mu\text{m}$ and $3.5\mu\text{m}/0.25\mu\text{m}$ for W/L of NMOS and PMOS respectively. The modules could be placed in parallel for higher gain. For A_5 , there are six INV1s connected in parallel, where each INV1 possesses an output current equal to I_{in} . A_9 and A_{10} are only needed when I_{in} is lower than 10nA . Cascading many stages of the inverter does not deteriorate the speed much because each inverter has a very small propagation delay which is less than 1ns . So as discussed earlier the major contributor to the delay is the transimpedance stage.

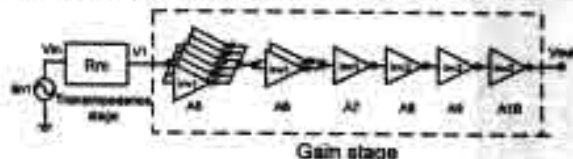


Figure 3 Gain stage

3. SIMULATION RESULTS

The proposed current comparator has been designed on a $0.25\mu\text{m}$ TSMC CMOS process and tested with various power supplies and input current amplitudes. On HSPICE and with V_{DD} set to 1.5V , the comparator responses of three input current amplitudes of $1\mu\text{A}$, 100nA and 100pA are shown in Figure 5 where the average propagation delays are 1.95ns , 3.6ns and 10.7ns respectively. Performances vs the input current amplitudes at 1.5V V_{DD} such as average propagation delay, static power and power delay product (PDP) are shown in Figure 6. It is seen that the lowest input current amplitude is at $\pm 50\text{pA}$ thanks to the small input resistance as a result of the negative feedback with high loop gain. The average propagation delay is inversely proportional to the input current amplitudes since the voltage swing at the output of the transconductance stage is small. With small input current amplitudes, the static power also increases because all node voltages are around the common-mode value or $V_{DD}/2$ where most MOSFETs of the inverters are fully turned on. Propagation delays at various V_{DD} and input signal amplitudes are shown in Figure 7. Performance comparisons among many reported circuits are listed in Table 1. It is seen that the power is higher than those from some earlier designs because the scaling down of the V_{DD} normally degrades some properties of the inverter such as average drain current, voltage gain and propagation delay. Thus more power has to be pumped into the circuits in order to achieve the required speed and rail to rail output voltage swing.

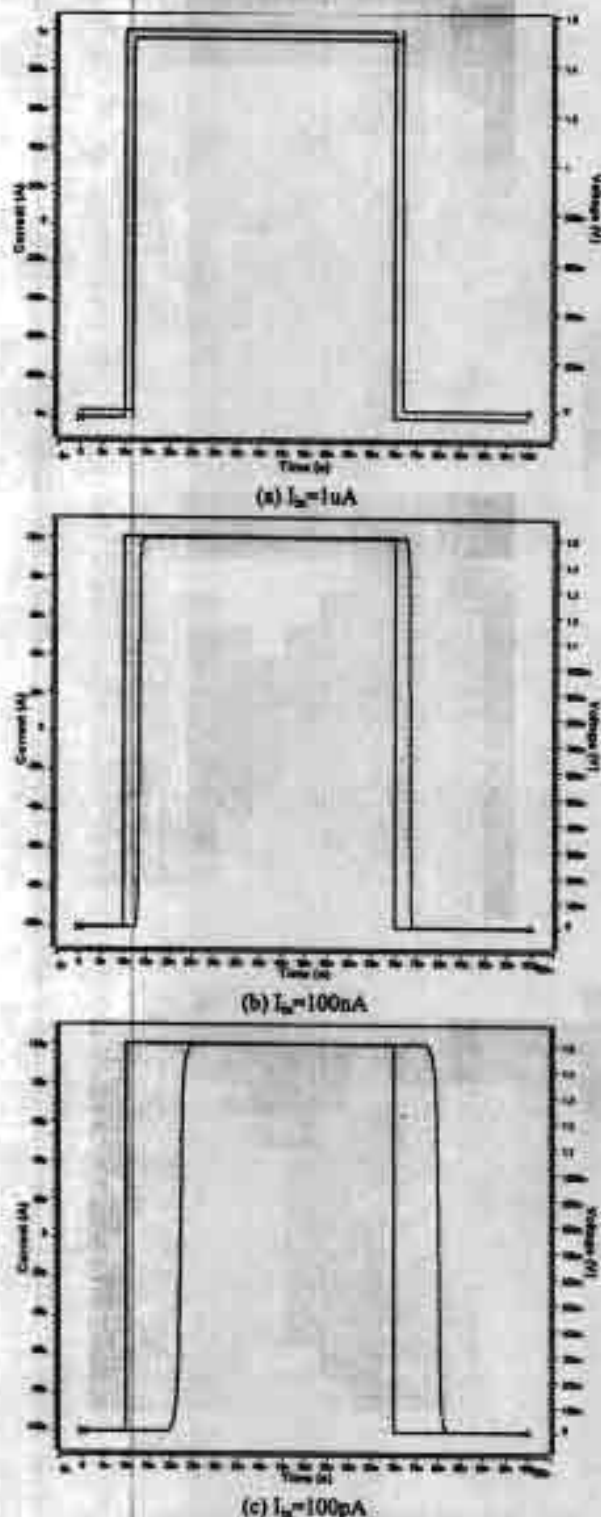


Figure 5 Transient Response of V_{out} vs. I_{in} at 1.5V V_{DD}

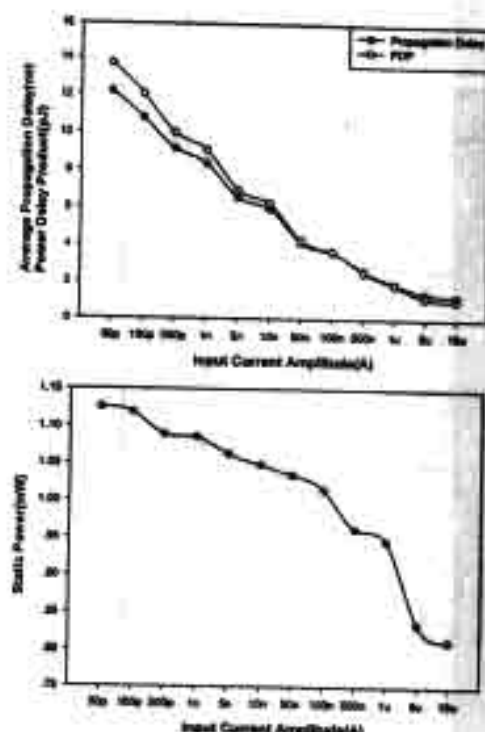


Figure 6 Performances at 1.5V V_{DD}

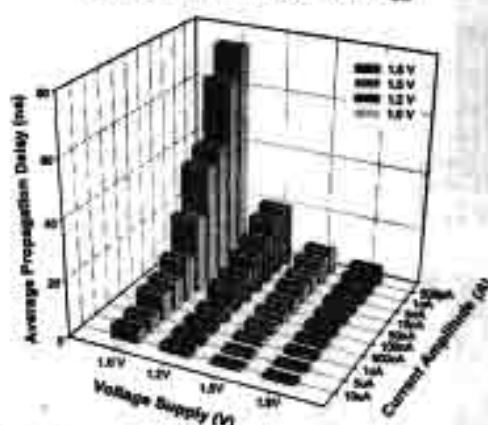


Figure 7 Propagation delays at V_{DD} 1.0-1.8 Volts

4. SUMMARY

A new high speed low input current low voltage current comparator has been demonstrated on a 0.25 μ m TSMC CMOS process. Based on the concept of a high speed current-mode technique, we exploit a negative feedback scheme around the transimpedance stage with an emphasis on a very large loop-gain to produce a very small transformed voltage swing which is situated at the center of the gate threshold voltage of the latter stage. This will ensure the fastest response time. The same dimension inverters are used in all amplifier stages. They are fast and simple and suitable for low voltage operation. There is no extra biasing circuit and stacked transistor, thus the same design can be applied with various V_{DD} - in there is no need to readjust the design.

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Table 1 Performance comparisons

	Traff [4]	Tang [5]	Ravazzi [6]	Min [8]	Lin [7]	Proposed circuit		
Year	1992	1994	1997	1998	2000	2002	2002	2002
Power Supply (V)	5	5	5	3	3	1.5	1.0	1.8
Process (μ m)	2	1.6	2.5	0.35	0.35	0.25	0.25	0.25
Minimum Input Current Amplitude (nA)	10	10	100	10	1	0.05	0.05	0.5
Propagation delay	$\pm 1\mu$ A/ 10ns	$\pm 0.1\mu$ A/ 11ns	$\pm 0.1\mu$ A/ 19ns	$\pm 0.1\mu$ A/ 7ns	$\pm 0.1\mu$ A/ 2.8ns	$\pm 0.1\mu$ A/ 3.5ns	$\pm 0.1\mu$ A/ 14.65ns	$\pm 0.1\mu$ A/ 2.6ns
Power consumption (mW) (at 0.1 μ A)	0.390	1.4	NA	0.45	0.58	1.01	0.022	2.73
PDP (pJ)	NA	NA	NA	3.15	1.4	3.648	0.32	7.35

[6] J. Ngarmnil, S. Ruengrungson and K. Nandhasri, 'A 100MHz $\pm 0.75V$ FLOATING-GATE MOSFET CURRENT CONVEYOR', 2003 IEEE Midwest Symposium on Circuits and Systems (MWSCAS2003), Cairo, December, 2003.

A 100MHz $\pm 0.75V$ Floating-gate MOSFET Current Conveyor

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Abstract—This paper proposes a low voltage inverting second generation current conveyor working up to a 100MHz with 5V power supply. The circuit is formed in class AB structure using CMOS inverters and a pseudo floating-gate MOSFETs additive analog inverter facilitating a negative feedback loop to relate accurate signal tracking of the terminal voltage X to Y the terminal current Z to X . Simulation results on 0.5 μ m double poly CMOS processes confirm high precision conveying area, wide signal swing and low voltage capabilities of the current conveyor.

I. INTRODUCTION

Recently, several signal processing techniques [1-2] based on second generation current conveyors (CCII) have been demonstrated successfully such as filtering, log-domain linear, squarer and rectifier and multiplier circuits. Most reported CCII structures are based on a translinear cell which are stacked on current mirror circuits. A high precision CMOS CCII [3] was also realized with voltage follower and current sources with an emphasis on local negative feedback loop and v_y and v_x terminals. All these circuits have suffered with limitation on low voltage applications since these circuits are based on stacking topology of transistors. For low voltage applications, a CMOS CCII [4] was proposed by using CMOS inverters allowing only two stacked devices between the supply rails. The circuit is in a class-AB mode of which the current signal swing can be very high since there is not any fixed bias current source to limit the signal swing. However, the circuit is restricted to applications where the Y input is only referenced to signal ground. A pseudo voltage follower based CCII was also proposed recently in [5] exhibiting performances on low voltage and compactness. However, the current signal swing of terminal X and Z are limited to the fixed bias current source.

In this paper, we propose a new inverting second generation current conveyor 'positive' (ICCI⁺) totally based in the class AB structure utilizing CMOS inverters and recently proposed additive analog inverter [6-7] using pseudo or Quasi floating-gate MOSFETs, of which the offset voltage of the floating gate terminal can be weakly controlled actively via a large valued resistor thanks to the inventions proposed in [8-11]. The design is emphasized on negative feedback with a high loop gain to enhance the conveying properties relating to v_y to v_x and i_x to i_z . Thanks to the class

AB topology, the circuit is also capable with wide swing signals. The design is applied on a 0.5 μ m double poly CMOS with $\pm 0.75V$ power supply demonstrating low voltage capability and high frequency operation up to 100MHz.

II. THE PROPOSED ICCI⁺

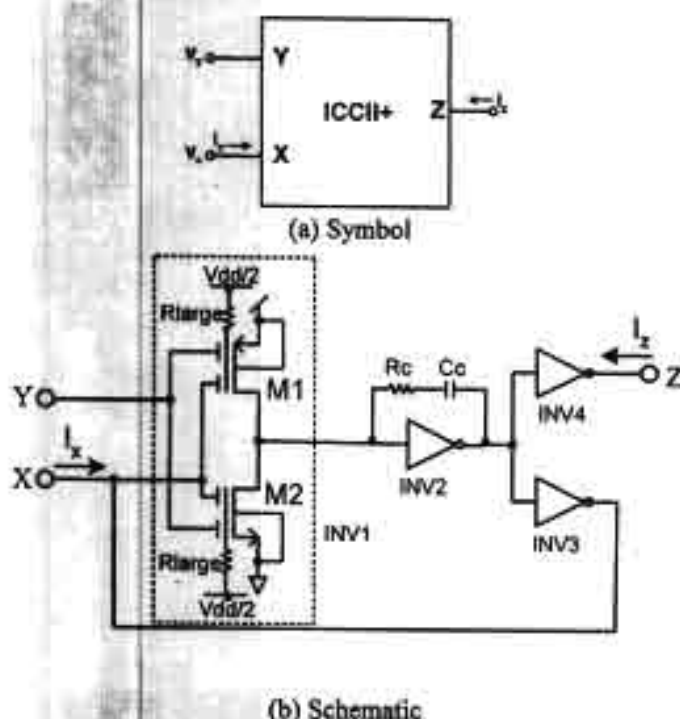


Fig.1 The proposed ICCI⁺

The proposed ICCI⁺ is shown in Fig.1 of which the port relations [12] among voltage and current terminals are described as

$$\begin{bmatrix} i_y \\ v_x \\ i_z \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ -1 & 0 & 0 \\ 0 & 1 & 0 \end{bmatrix} \begin{bmatrix} v_y \\ i_x \\ v_z \end{bmatrix} \quad (1)$$

where terminal Y is a high impedance node and does not draw any input current. Terminal X is a low impedance node with voltage value v_x equal to $-v_y$. Terminal Z is a high impedance node with the terminal current i_z equal to i_x . These properties are transformed to the proposed ICCI⁺ shown in Fig.1. It is

n that Y is connected to the input gate of floating-gate MOSFETs and is perfectly a high impedance node. Z is connected to the output node of an inverter which is obviously a high impedance node with current driving capability. It will be shown later on that there is an internal negative feedback loop from Y terminal to X terminal. By virtue of the negative feedback loop, X can be derived as a low impedance node with a current driving capability by inverter INV3 which is shown in Fig.1(b).

In Fig.1(b), the ICCII+ comprises four circuit blocks designated as INV1, INV2, INV3 and INV4. The INV1 is an additive analog inverter or basically a two-input CMOS inverter built from floating-gate MOSFETs M1 and M2 and proposed in [6-7]. Based on the idea of Pseudo or Quasi-floating-gate MOSFET in [9-11], large value resistors (large) are shown to connect the floating-gate terminals of M1 and M2 to $V_{DD}/2$ thus the DC offset of the floating-gate MOSFETs can be effectively controlled and the complicated charge programming scheme such as UV removal can be avoided. The resistors are built from reverse-biased diode connected PMOSs. The INV1 is employed in this circuit together with INV2 and INV3 blocks to mimic the function of differential amplifier which allows the output of INV3 to provide negative feedback to the node X. Since voltage polarity of INV3 output is inverted to those of v_y , causing the voltage at node v_x to be inverted to those at node v_y , hence the function of inverting CCII to copy the voltage $-v_y$ to v_x can be fulfilled. Moreover, the diode connected PMOSs are always in reverse bias because voltage at the floating-gate is small as a result of negative feedback. A modulated AC voltage at the floating-gate can be written in (2) where the coefficient of v_x is negative as a result of the negative feedback via INV2 and INV3.

$$v_{FG} = k_1 v_y - k_2 v_x \quad (2)$$

where k_1 and k_2 are the capacitive division factors C_1/C_T and C_2/C_T , where C_1 and C_2 are the input coupling capacitances of M1 and M2. C_T is the total capacitance seen from the floating gate. All capacitances correspond directly to the sizes of the gate coupled gates. In this case, the equal input coupling C_1 and C_2 of M1 and M2 are set to 60fF and 100fF respectively result in approximated equal values k_1 and k_2 of 0.5. A differential signal voltage gain between the output $V_{out,INV1}$ and the differential inputs can be derived as

$$\frac{\partial V_{out,INV1}}{\partial (V_y - V_x)} = -(g_{m1n} + g_{m1p})(r_{o1n} // r_{o1p}) \quad (3)$$

where g_{m1n} , g_{m1p} and r_{o1n} , r_{o1p} are the respective transconductance and output resistances of M1 and M2 respectively. The voltage transfer of v_y to v_x is derived as

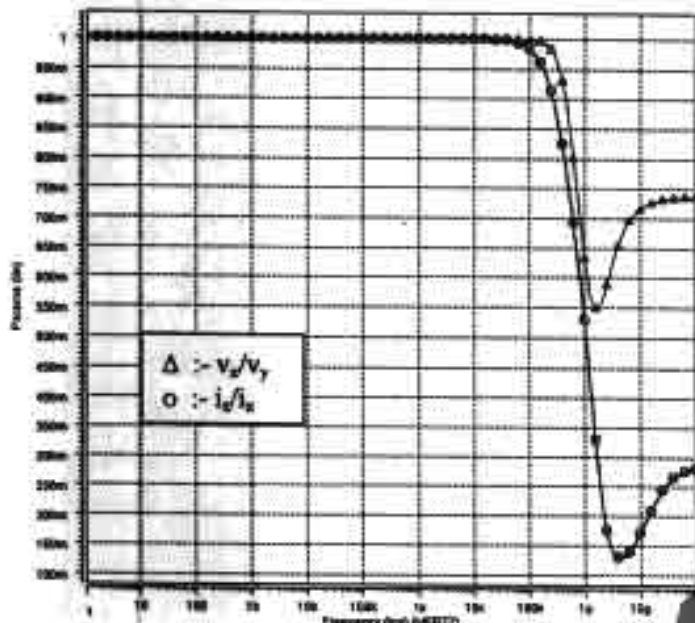
$$\frac{v_x}{v_y} = \frac{-g_{m1n} r_{o1n} g_{m2} r_{o2} g_{m3} r_{o3}}{1 + g_{m1n} r_{o1n} g_{m2} r_{o2} g_{m3} r_{o3}} \approx -1 \quad (4)$$

where g_{m1n} , g_{m2} , g_{m3} are the intrinsic voltage gain of the INV1, INV2 and INV3 respectively. We can also derive the output resistance of terminal X as r_x in (5) which is low as a result of the negative feedback.

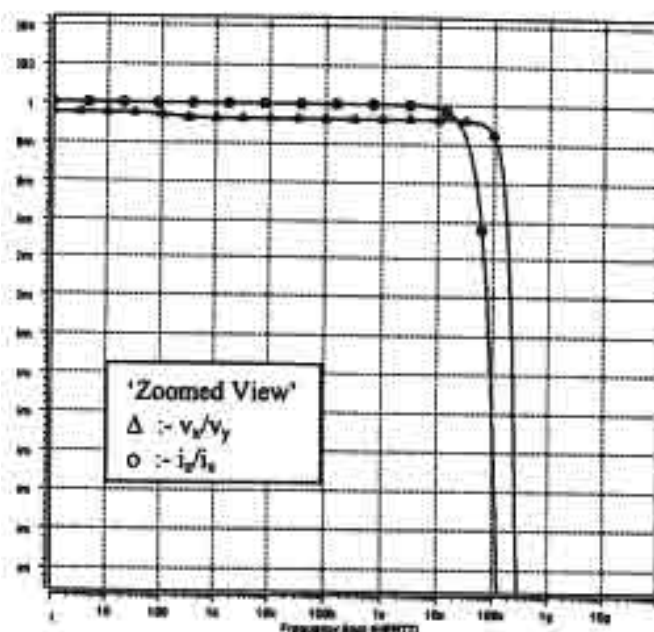
$$r_x = \frac{r_{o3}}{1 + g_{m1n} r_{o1n} g_{m2} r_{o2} g_{m3} r_{o3}} \quad (5)$$

III. SIMULATION RESULTS

Based on the proposed schematic in Fig.1(b), the circuit can be designed in a modular fashion where all inverters including the additive analog inverter have the same dimensions of NMOS and PMOS correspondingly. If a higher gain of any inverter blocks is required, we simply add more cells of the identical inverters in parallel. The circuit has been designed on the Alcatel 0.5μm double poly CMOS process with ±0.75V power supply. For each inverter module, NMOS and PMOS are designed with the dimensions of 8.4/0.5 and 24/0.5 respectively corresponding to g_{m_n} of 344μA/V and g_{m_p} of 314μA/V and resulting in the idle currents of 34μA for each inverter. The compensation network with R_C of 500 Ohms and C_C of 0.35pF are employed for stability since there are two high impedance nodes across INV2. In this circuit, we employ only one CMOS inverter for the additive inverter INV1 block. There are nine inverters connected in parallel for INV2 and three parallel inverters for INV3 and INV4 blocks hence making i_n equals to i_p . Both X and Z terminals are loaded with external resistors of 1kΩ. Fig.2 shows frequency responses of the ratio v_x/v_y and i_p/i_n which are seen that the circuit contributes very low tracking errors of v_x/v_y to less than 1% and those of i_p/i_n to 1.6% at the frequency of 100MHz.



(a) Magnitude response of v_x/v_y and i_p/i_n



(b) Zoomed view of (a)

Fig.2 Magnitude responses of v_x/v_y and i_x/i_z

The magnitude responses of the X terminal output resistance r_x was derived in (5) and is shown in Fig.3. The r_x is less than 1 Ohms at DC rising to 500 Ohms at MHz. It is increasing dependent to the frequency in the frequency range because the loop gain of the negative back is decreasing at high frequency. However, the operating frequency of the circuit is bound to 100MHz.

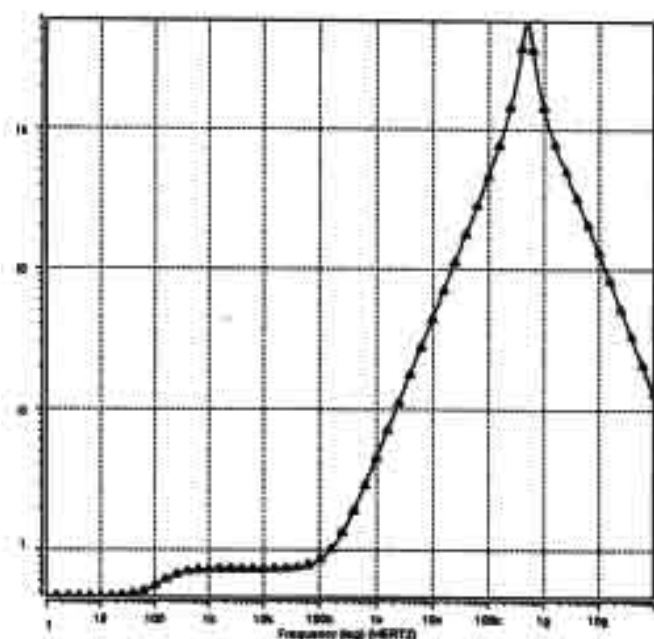
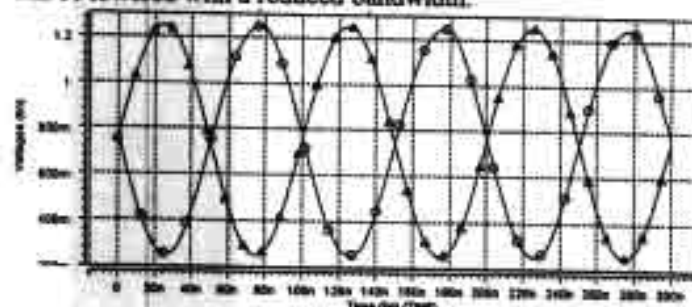


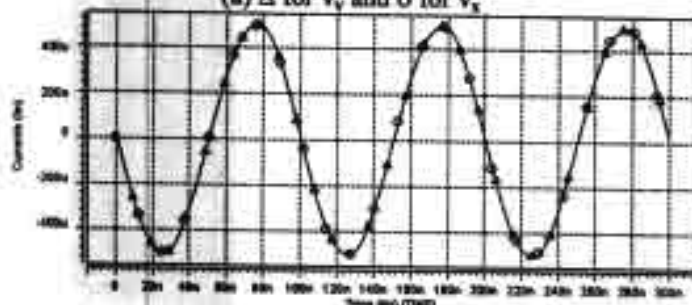
Fig.3 Magnitude response of r_x (Ohms)

Fig.4 shows the transient responses at 10MHz of v_y vs. v_x and i_x vs. i_z . In Fig.4(a) the responses of v_y vs. v_x confirm well (4). It is seen that the signal swing is as large as 1mV. Fig.4(b) shows a perfect matching of i_x vs. i_z with

the current swing as large as $\pm 500\mu A$. For high frequency capability, Fig.5 shows the transient responses at 100MHz. In Fig.5(a) shows the responses of v_y vs. v_x with signal swing of $\pm 200mV$. Fig.5(b) shows the responses of i_x vs. i_z with the current swing of $\pm 200\mu A$. It is seen that the corresponding signals v_y vs. v_x and i_x vs. i_z are still matched but with a small phase shift. All signal amplitudes are set to confine the THD to less than 1%. Total power consumption is $816\mu W$ which can be lowered with a reduced bandwidth.

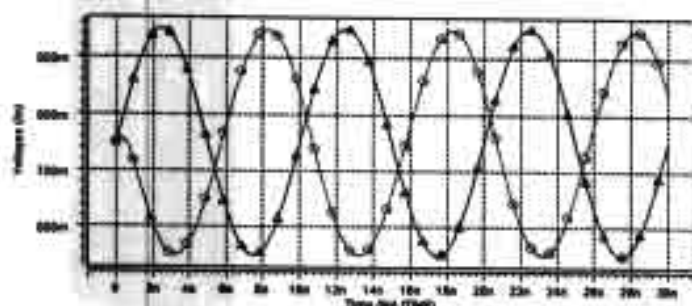


(a) Δ for v_y and ϕ for v_x

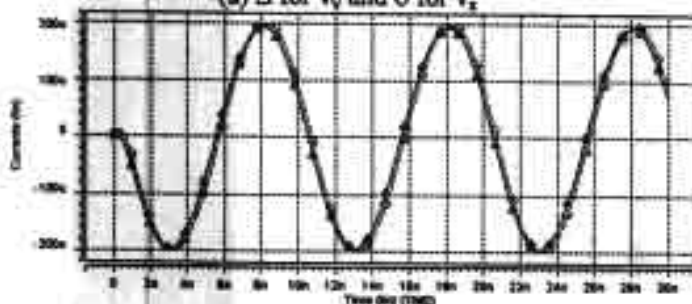


(b) Δ for i_x and ϕ for i_z

Fig.4 Transient responses at 10MHz with THD<1%



(a) Δ for v_y and ϕ for v_x



(b) Δ for i_x and ϕ for i_z

Fig.5 Transient responses at 100MHz with THD<1%

In many current conveyor applications, there is a need to have both polarities of output current i_z or multiple outputs i_z and i_z . In some conventional CCII, this facility is usually

formed using additional current mirrors to copy and invert the output current i_z . However non-ideal characteristics of current mirror always introduce some tracking error between the current i_{z+} and i_{z-} . In the similar way on this topology, we can not straightforwardly cascade additional inverters at the output Z terminal in order to make inverted-direction current i_z since there is usually an essential phase shift that causing an unperfected tracking between the currents i_{z+} and i_{z-} . In this case, we demonstrate a parallel connected ICCII+s as shown Fig.6. The perfected tracking in both magnitude and out of phase of i_{z+} and i_{z-} are shown in Fig.7(b) confirming a high precision property of this II+.

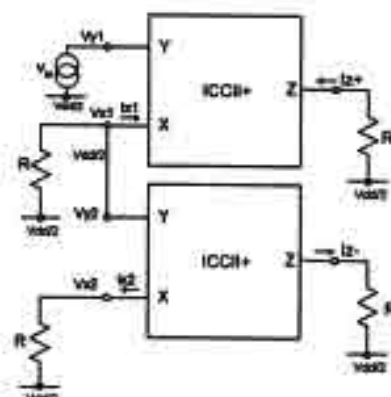


Fig.6 Parallel connected ICCII+s

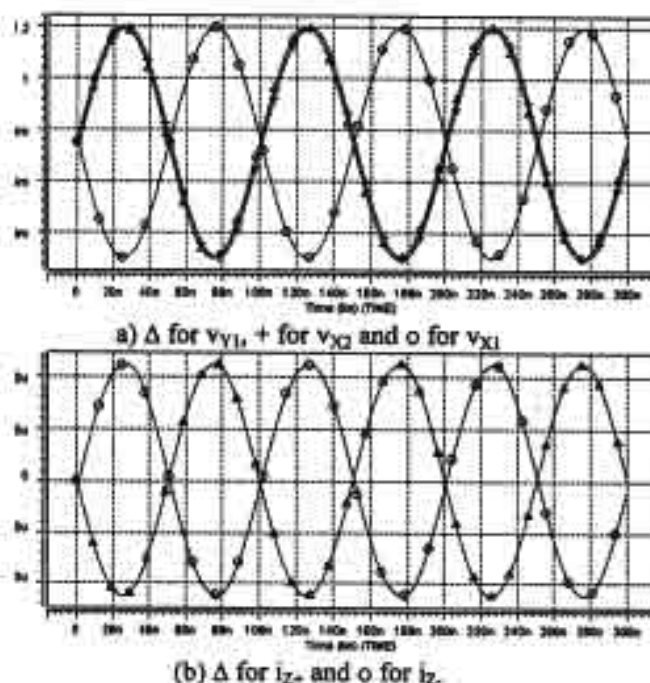


Fig.7 Transient responses at 10MHz with THD<1%

IV. CONCLUSION

This paper has presented a low voltage wide swing inverting second generation CMOS current conveyor of which the design focuses on the use of CMOS inverters and the negative

feedback to enhance conveying precisions, signal linearity and low output resistance property at the terminal X. The circuit is totally realized in class AB thanks to the use of CMOS inverters and the available floating-gate MOSFET additive analog inverter cell which facilitates the negative feedback channel to the normal CMOS inverter. With the programming approach of pseudo or quasi floating-gate MOSFET, DC offset of the floating-gate inverter can be effectively controlled to $V_{dd}/2$ and the complicated initial charge programming schemes could be avoided. The diode connected PMOSs producing the large resistors are always in reverse bias because the voltage at the floating-gate is small as a result of the negative feedback. With $\pm 0.75V$ supply, the circuit can handle signal swing as large as $\pm 500\mu A$ amplitude through X and Z terminals and $\pm 500mV$ at Y and X terminals while the THD is maintained to less than 1%. The circuit is designed to operate up to 100MHz signal frequency.

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