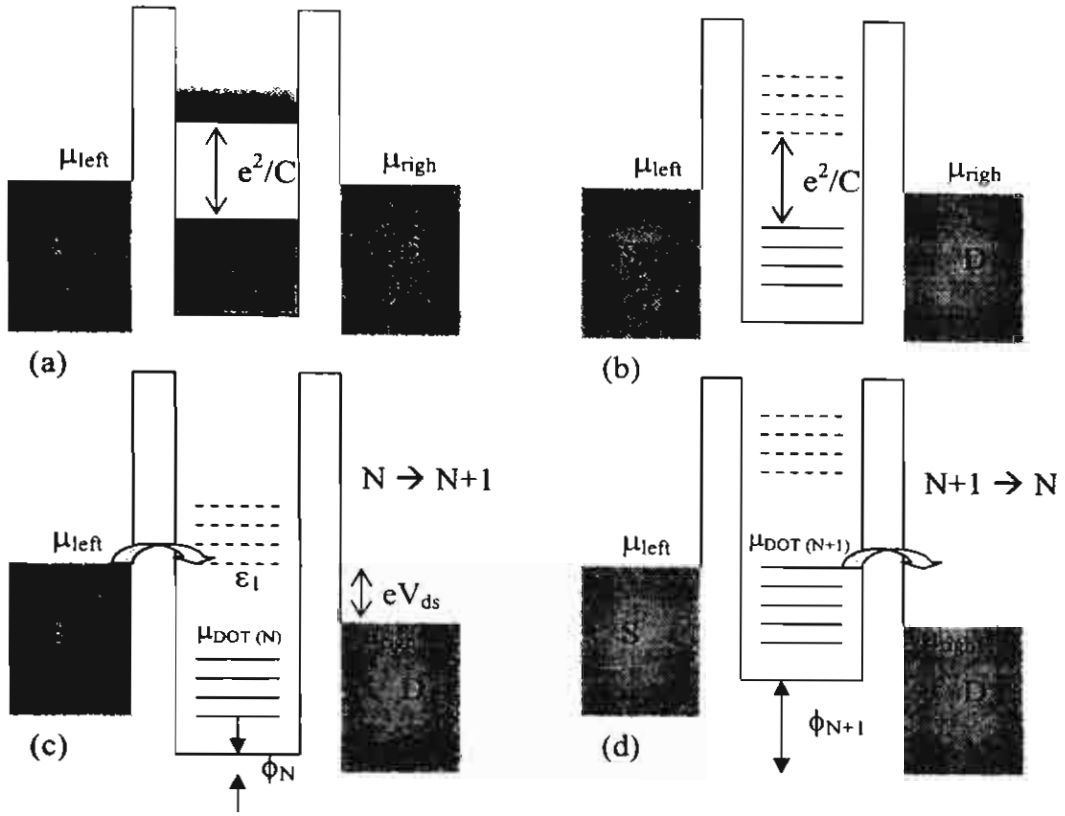


Figure 16. Potential landscape along a quantum dot showing occupied states in the leads and the dot. (a) Classical case where continuous energy levels in the dot are assumed. (b) shows discrete energy levels in the dot in Coulomb blockade, which is lifted (c) when ϕ_N is adjusted such that ε_1 lies between μ_{left} and μ_{right}. An excess electron on the island from the left lead causes potential in the dot to be raised by $e^2/2C$ (d). Consequently, the excess electron can tunnel off the island to the right lead because $\mu_{DOT}(N+1) > \mu_{right}$. The cycle repeats ($N \rightarrow N+1 \rightarrow N\ldots$) and the system starts passing current.

Biased appropriately, the electrons from the left lead can tunnel across the barrier into one of the discrete energy levels in the quantum dot. For simplicity, these levels are assumed to be equally spaced with zero width, the tunnel rate which in the classical case is given by (17) is now (assuming $E_C >> \Delta\varepsilon$) [20]:

$$\Gamma = \frac{\Delta\varepsilon}{e^2 R}\sum_{n=0}^{+\infty}\left[\left(1+e^{a}\right)\cdot\left(1+e^{b}\right)\right]^{-1};\begin{cases} a = (-\Delta E + E_o + n\Delta\varepsilon)/k_B T \\ b = -(E_o + n\Delta\varepsilon)/k_B T \end{cases} \tag{28}$$

where E_o is the ground state energy and ΔE is defined as in (18).

An example of simulated I-V_{ds} characteristics for $\Delta\varepsilon$ = 0.4meV is shown in Fig. 17. The gate-source voltage is swept from 0 to 3 V while V_{ds} is kept constant for each V_{gs} sweep. The V_{ds} is varied between 1 mV to 5 mV in 0.1 mV steps. The simulation results in current oscillation with the expected broad period of e/C_g ~ 1 V with embedded fine oscillations that deserve further analyses.

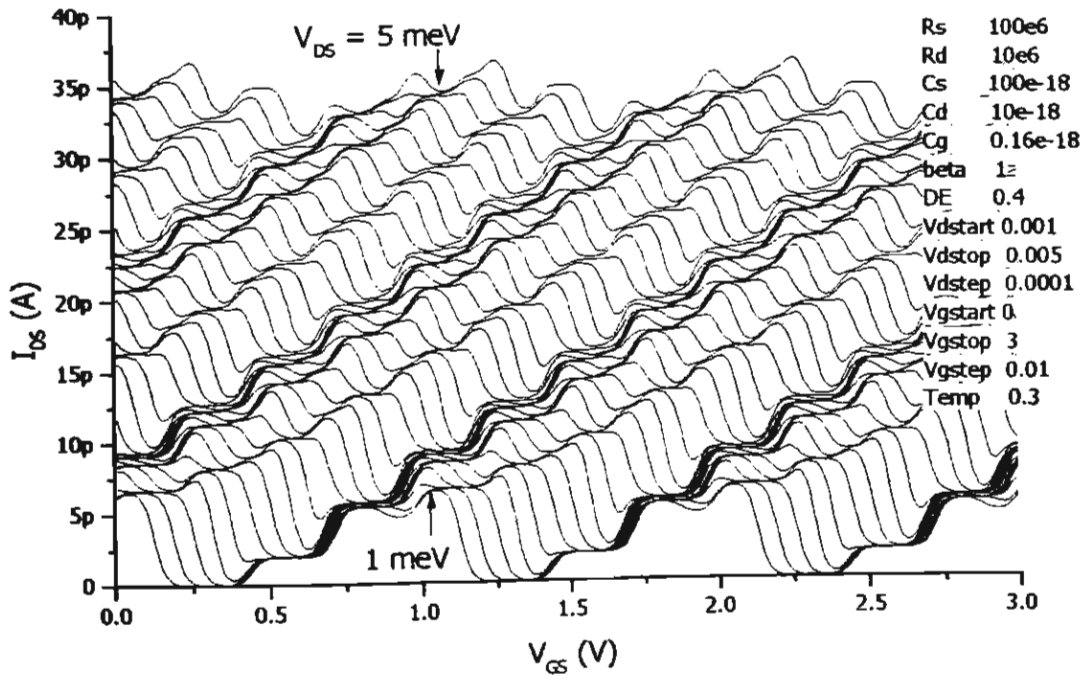


Figure 17. Coulomb oscillations in asymmetrical, semiconducting quantum dot transistor with energy level spacing in the dot of 0.4meV, see inset and text for other parameters.

3.5 Dual-Gate Quantum Dot Transistors

3.5.1 Structure and Electrical Characteristics

A quantum dot system is one in which the geometrical size of the dot is so small that quantum-sized effects are significant, particularly at low temperatures. In metallic systems the corresponding size is a few nanometers. In semiconductors, the electron density is much smaller; therefore, quantum effects can be seen in structures as large as 100 nm. When these nanoscale dots are connected to external terminals, source (S) and drain (D), charge transport through the dot is possible. One or more gate electrode (G) can thus be placed nearby to control the source-drain current. The electrodes together with the dot are collectively called a quantum dot transistor, see Fig. 18(a). The equivalent circuit diagram in Fig. 18(b) shows the tunnel junctions represented by a resistor and a capacitor while the coupling between the gate and the dot is capacitive in nature. The quantum dot is represented by the dotted box in the figure, enclosing n electrons.

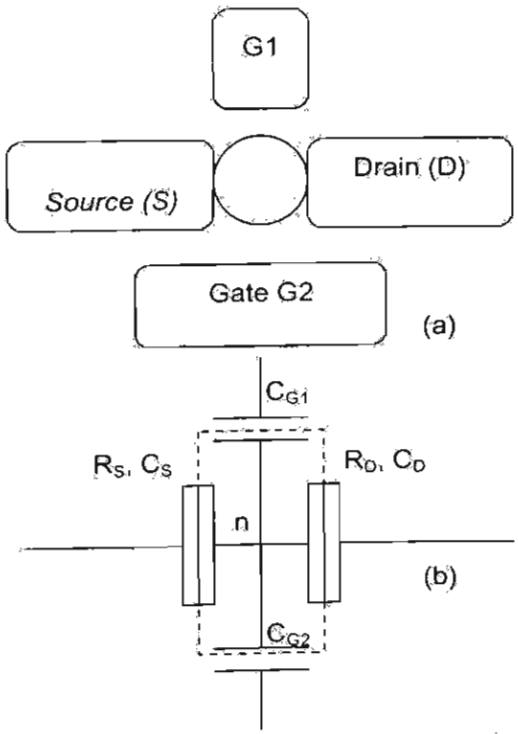


Figure 18. (a) Schematic of a dual-gate quantum dot transistor. The gates (G1 and G2) control the current passing through the dot between the source (S) and drain (D) terminals. (b) Its equivalent circuit diagram: R and C represents the modelled resistive and capacitive equivalence of the source, drain or gates with subscripts S, D, or G1 and G2 respectively.

Current through double-barrier systems is suppressed at low voltages due to Coulombic forces: electrons already stored in the dot prevent external electrons from entering. At a voltage (V_{DS}) larger than a blockade voltage (V_{CB}), however, the energy of the external electrons can overcome the repulsive forces and the current starts to flow. This is called Coulomb blockade phenomena earlier explained in section 2. The charging energy (E_C) required to overcome the blockade depends entirely on the total capacitance of the island (*i.e.* the capacitance between the island and the rest of the environment) and is given by $E_C = e^2/2C$ where e is the electronic charge and C is the island capacitance.

It is clear from the relationship that as the island gets smaller (and C is lowered) the charging energy, and thus the operating temperature of the device, increases. At room temperature, electrons have sufficient thermal energy and can thus tunnel across the tunnel junctions unimpeded. At cryogenic temperatures, however, electron energy is low and external voltage(s) has to be supplied in order to move electrons across the structure.

Holding V_{DS} constant and sweeping the gate voltage causes electrons to be expelled out of, or injected into the dot one by one depending on the sweep direction. The current thus increases and decreases as the gate voltage is swept. The oscillatory nature was first observed by Scott-Thomas *et al.* [3].

The programming code in the previous section which can handle (single-gate) quantum dot transistors has been modified to include more than one gate input allowing the simulation of dual-gate structure shown in Fig. 18. Indeed, changes can also be made to the source code to cover multiple gate designs where the number of gates is unlimited. In practice, however, the number of gates will be limited by the resolution of fabrication processes.

The modified program allows for double gate features which can have arbitrary shapes. The coupling between the gates and the dot is capacitive in nature with electric fields spanning across the gate-to-dot junction in three dimensions: above the plane level (in air or ambience at which the device operates), in plane (this can be air or

whatever material which physically connect the gates to the dot), and under the plane (via the substrate). The capacitances of the two gates, denoted C_{GX} and C_{GY}, thus do not have to be identical.

In order to probe the accuracy of the modified program, a set of simulation tasks is carried out and results shown in Figs. 19 and 20. The simulations for metallic system where $\Delta\varepsilon$ is set to zero is shown in Fig. 19. The drain-to-source voltage is kept constant at 1 mV. The source and drain junctions are asymmetric with the source junction being ten times more resistive and capacitive than the drain junction. The total gate capacitance of the system is 0.4aF which comprises 0.1aF of C_{GX} and 0.3aF of C_{GY}.

Simple calculation in line with theoretical formulation in section 2 indicates that by sweeping gate X the period of the Coulomb oscillation should be $e/C_{GX} \approx 1.6$V. Similarly, sweeping gate Y should result in a period of ~ 0.5V. And if both gates are coupled (connected together such that they are at the same potential), the period should be $e/(C_{GX}+C_{GY}) \approx 0.4$V. All these periods can clearly be seen in Fig. 19 which implies that the modified simulation program can correctly model the dual-gate structure.

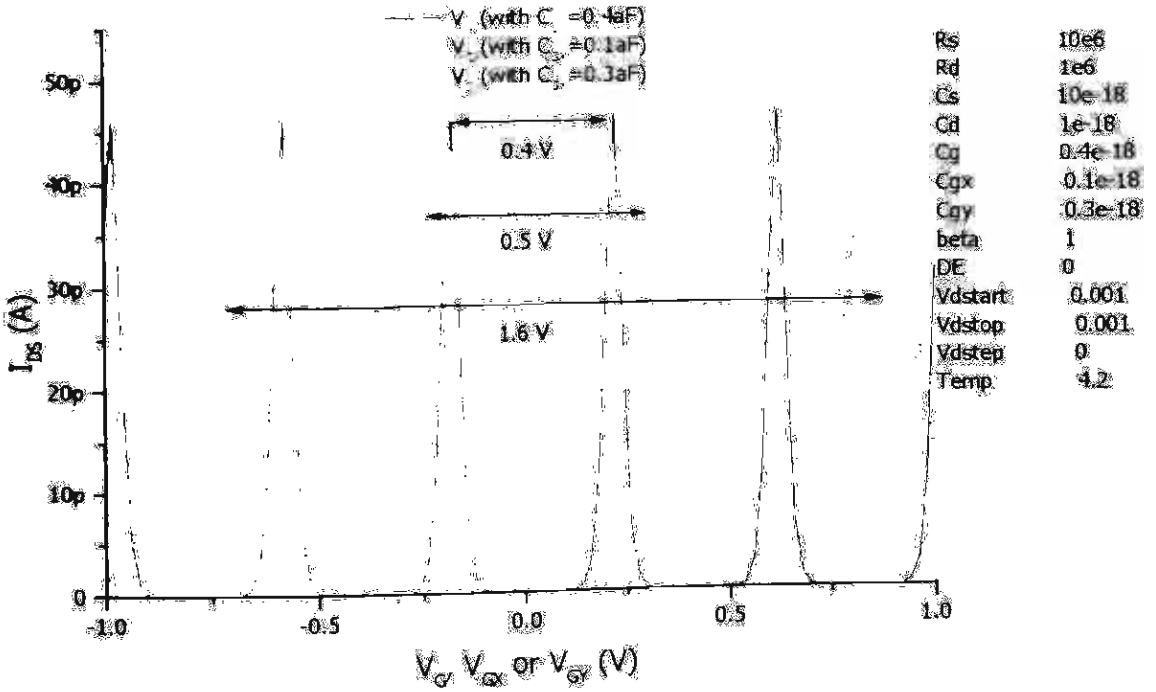


Figure 19. Drain-to-source current as functions of gate X voltage (V_{GX} with $C_{GX} = 0.1$aF), or gate Y (V_{GY} with $C_{GY} = 0.3$aF), or the voltage when both gates are connected together (V_G with $C_{GX} + C_{GY} = 0.4$aF).

The simulations for semiconducting system where $\Delta\varepsilon$ is set to 0.4meV is shown in Fig. 20. Both single-gate and dual-gate results are shown in the same plot for comparison. The parameters for the single-gate case are the same as those used in Fig. 17 with total capacitance of 0.16aF. The parameters for the dual-gate case use the same source and drain parameters and symmetrical gates with each having effective capacitance of 0.08aF. The peak amplitude of the current for both cases are 6.5pA, in good agreement with the previously simulated results in Fig. 17. Furthermore, the periodicity of the oscillations when sweeping gates X and Y doubles that of the single-gate case, as expected due to the fact that the capacitances for gates X and Y are halved that of the single gate.

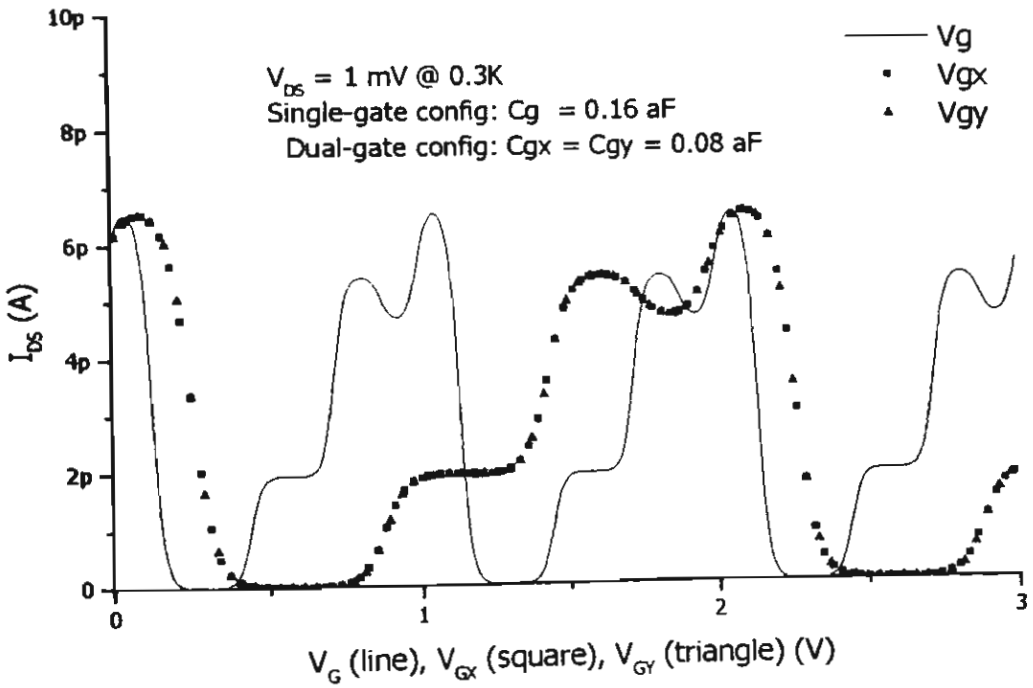
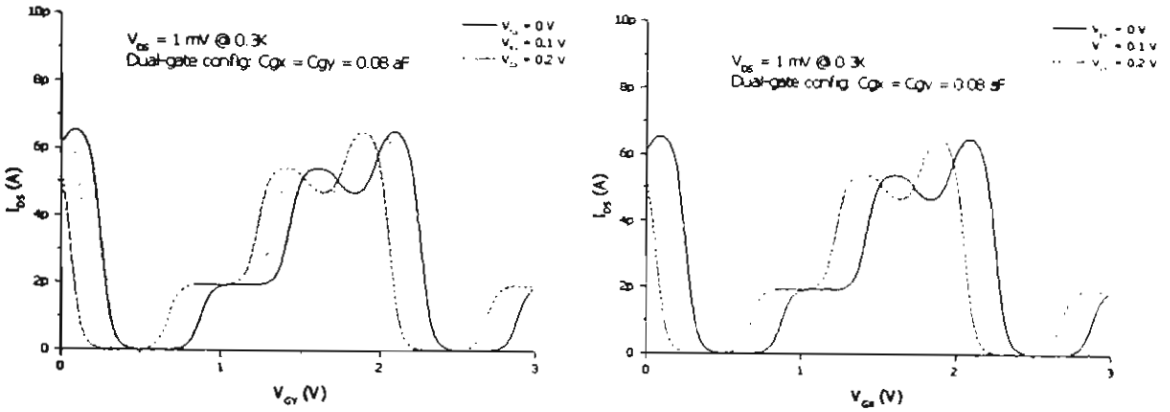


Figure 20. Drain-to-source current oscillations using parameters similar to those used in Fig. 17. The modified program can now handle two gate inputs with gate X sweep (▪), gate Y sweep (▲), or when X and Y are tied and swept together (—).

When V_{ds} is fixed, the tunnel current which shuttles between the source and drain will depend on the charge state of the quantum dot which in turn depends on the potentials of the gate electrodes. Therefore, if the gates are identical (C_{GX} = C_{GY} = 0.08aF in the simulation to follow), the changes in I_{DS} when gate voltages are swept should also be identical. This is the case in another set of simulations shown in Fig. 21

with current oscillations as functions of V_{GY} and V_{GX} shown in Fig. 21(a) and (b) respectively.

The results show that the modified program can correctly calculate the tunnel currents in symmetrical systems. The next set of simulations will provide further evidence that the program also correctly calculate the tunnel currents for asymmetrical systems.



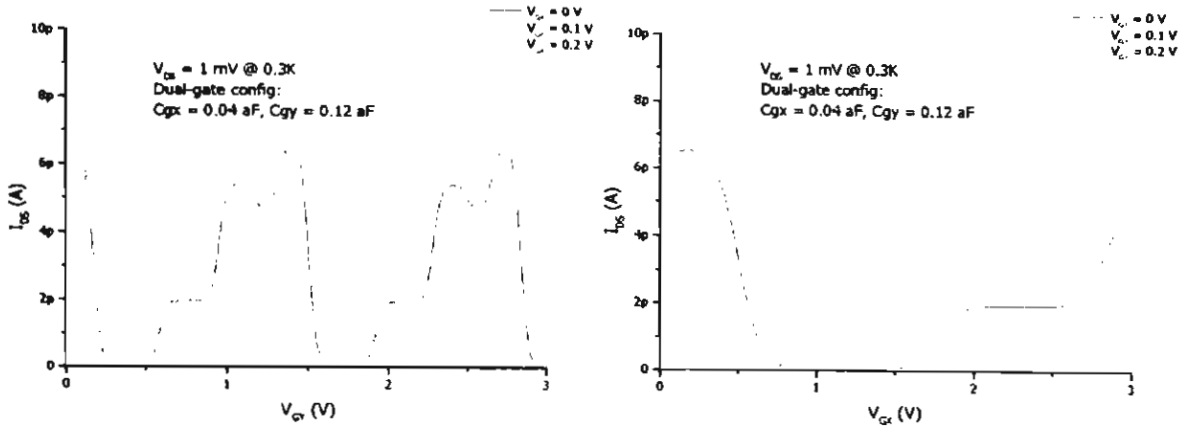
(a) (b)

Figure 21. Drain-to-source current oscillations when sweeping (a) gate Y at different values of V_{GX} and (b) gate X at different values of V_{GY}.

Using high-resolution lithography and careful alignment, it is possible to control the fabrication of a real dual-gate quantum dot system to a degree that doubling or tripling of gate area of one gate as compared to the other is achievable without much difficulty. The next set of simulations uses the same source and drain parameters as above. The gate capacitances, however, are different and, for illustrative purposes, set as follows: $C_{GX} = 0.04aF$ and $C_{GY} = 0.12aF$. Since gate Y is three times as capacitive as gate X, it is expected that sweeping V_{GY} would result in a current oscillation with a period which is one third that of sweeping V_{GX}. This follows the fact that the period is given by e/C_G. Figure 22(a) shows that the period of the oscillation when gate Y is swept is 1.2V, approximately three times the period seen in Fig. 22(b).

Due to the generally imperfect control during growth or fabrication of small nanostructures, quantum dots vary in size and, as explained in section 3.4 earlier, the discrete energy levels $\Delta\varepsilon$ in the dots cannot be decided upon and created with absolute

precision. In fact, a slight change in geometry of small structure result in significant changes of corresponding energy levels. The next set of simulations show the effect of varying $\Delta\varepsilon$ on Coulomb oscillation.



(a) (b)

Figure 22. Drain-to-source current oscillations of asymmetrical junctions when sweeping (a) gate Y at different values of V_{GX} and (b) gate X at different values of V_{GY}.

The following simulations assume symmetrical dual-gate quantum dot structure with tunnel resistance of 50MΩ, tunnel capacitance of 50aF, and gate capacitances of 0.08aF each. The dot itself is assumed to have energy levels which are spaced 0.4meV apart, i.e. $\Delta\varepsilon$ = 0.4meV. V_{DS} is swept from -3mV to 3mV in 0.02mV steps. V_{GX} is swept from -2V to 2V in 0.02V steps. The temperature is set at 0.3K.

The presentation of the results in Fig. 23 is commonly referred to as a diamond plot and it makes use of colour and intensity to reflect the amplitude of the tunnel current: red being positive and blue being negative current. And in both cases, the darker the colour the higher the current: dark red = +0.2pA and dark blue = -0.2pA. It can be seen in the figure that, apart from the usual Coulomb oscillation with a broad period of 2V (= e/C_{GX}), there exist periodic oscillations which are embedded in the broad oscillatory characteristic. The finer oscillatory features have a period of 0.4mV (in V_{DS}) which indicates that the finer oscillations embedded in the diamond may result from the energy levels $\Delta\varepsilon$ in the quantum dot.

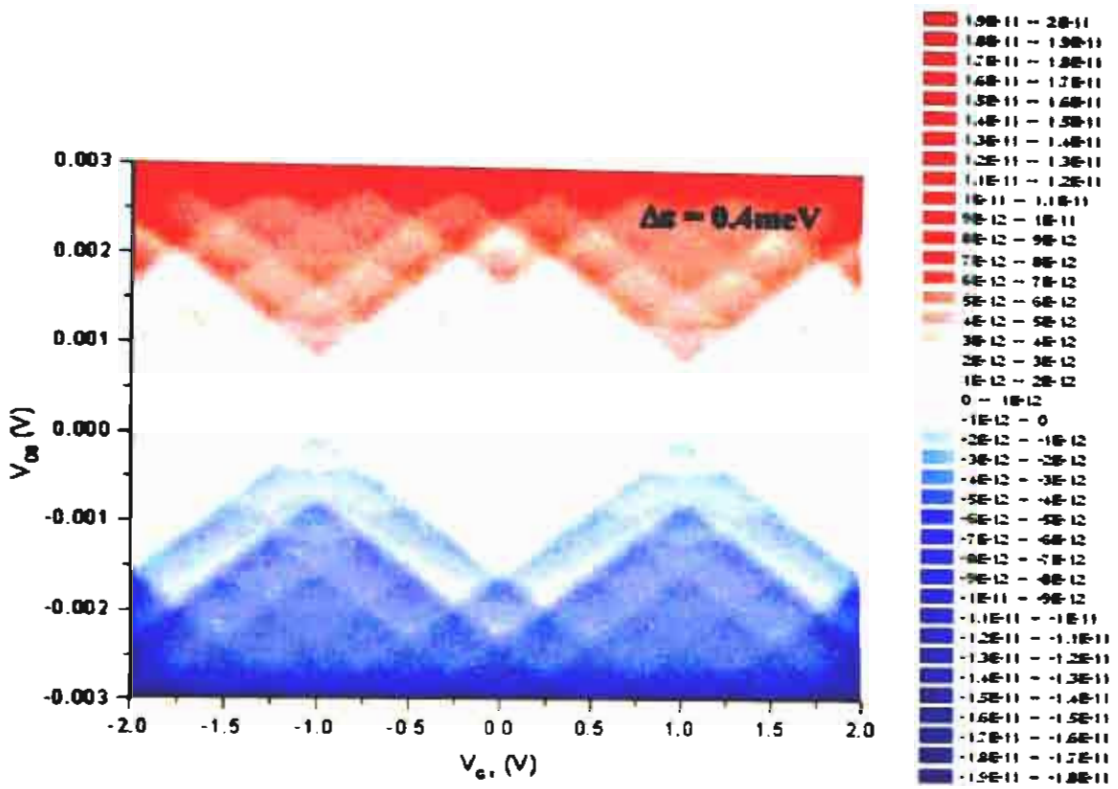


Figure 23. Colour plot of drain-to-source current as functions of V_{DS} and V_{GX} of symmetrical semiconducting quantum dot transistor. See text for simulation parameters. Colour code with varying intensity at right gives the amplitude of current in Ampere.

In order to gain a more thorough understanding of what is taking place in the dot, two more simulations are carried out with almost the same parameters. However, the energy levels are now increased to 0.6 and 0.8meV. The results shown in Fig. 24(a) and (b) for $\Delta\varepsilon$ = 0.6 and 0.8meV show that the finer oscillations have periods of 0.6 and 0.8mV in V_{DS} respectively. These clearly indicate that the finer oscillations do originate from resonant tunnelling via the energy levels of the dot.

It is important to note that the parameters used in the simulations above ($\Delta\varepsilon$ = 0.4, 0.6 and 0.8meV) can result from seemingly identical quantum dots. This is due to the fact that the surface states of the dots can deplete the charge carriers around the edges of the dots and thus the active volume inside each dot can vary greatly. A factor of two difference in energy levels of similar-sized nanostructures is not uncommon.

In the case of asymmetric dual-gate system where $\Delta\varepsilon$ is a non-zero value and C_{GX} and C_{GY} differ, the diamond characteristic can be complicated. The next set of simulations are carried out for a double-gated single-electron transistor whose junction

properties differ by a factor of ten: $R_s = 10R_d = 100$ MΩ, $C_s = 10C_d = 100$ aF. The two side gates are capacitively coupled to the dot. The coupling for the two gates differ by a factor of three, a realistic figure resulting from the difference in the effective areas of the gates and the distance of each gate from the dot, which can be independently controlled during the fabrication process. The dot is assumed to have discrete energy levels, instead of a continuum as is the case in metallic systems. The energy-level spacing is 0.4 meV and the temperature is 0.3 K.

Figures 25(a) and (b) show the simulation results of the system described above when sweeping the low- and high coupling-capacitance gates ($C_{GX} = 0.04$ aF, $C_{GY} = 0.12$ aF), respectively. The figures only illustrate a fraction of the Coulomb blockade regions, and only positive bias results are shown when the blockade is lifted.

Both figures illustrate the rich feature in the I-V characteristics. The plateaux results from two sources: the discrete energy levels in the dot and the asymmetry of the tunnel junctions. The former can be varied by changing the size of the dot, while the latter is somewhat more difficult to control as explained previously.

Corresponding results of Figs. 25(a) and 25(b) with wider voltage ranges to cover positive and negative drain bias are plotted in the colour plots in Figs. 26(a) and 26(b) respectively. At a fixed V_{ds}, varying gate voltage results in an oscillatory change in the drain current. However, the drain-current oscillation obtained from the asymmetrical case differs strongly from the symmetrical case. In the latter case, the oscillation is almost sinusoidal in nature with a single peak in each cycle. In the former case, however, each cycle contains several peaks and troughs. In some cases, plateaux can be obtained. This may find applications in multi-level logic since current plateaux are well defined.

The diamond plots shown in the case of symmetrical system in Fig. 24 and in the case of asymmetrical system in Fig. 26 above are very useful and informative as they show clearly where a certain bias condition operates.

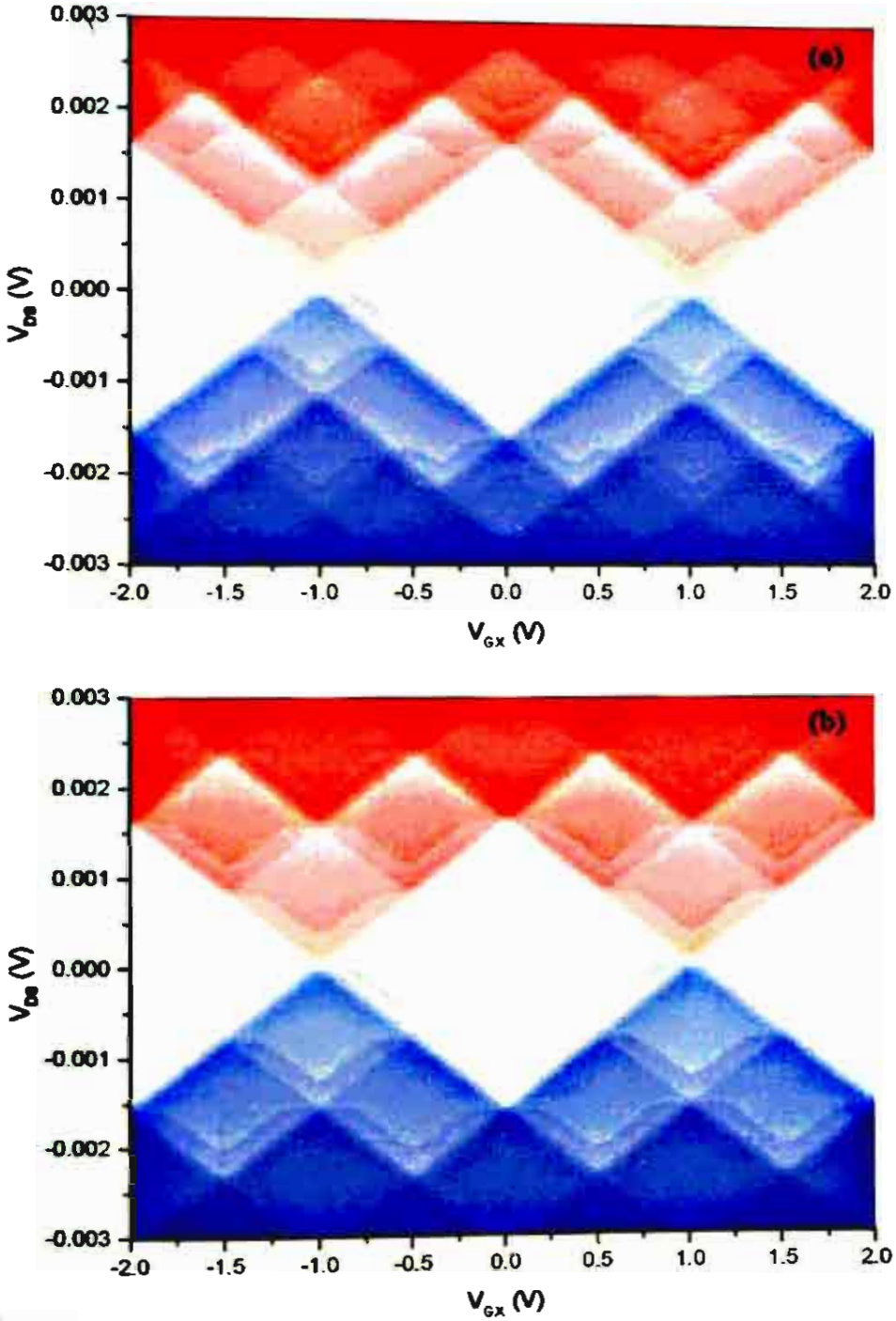
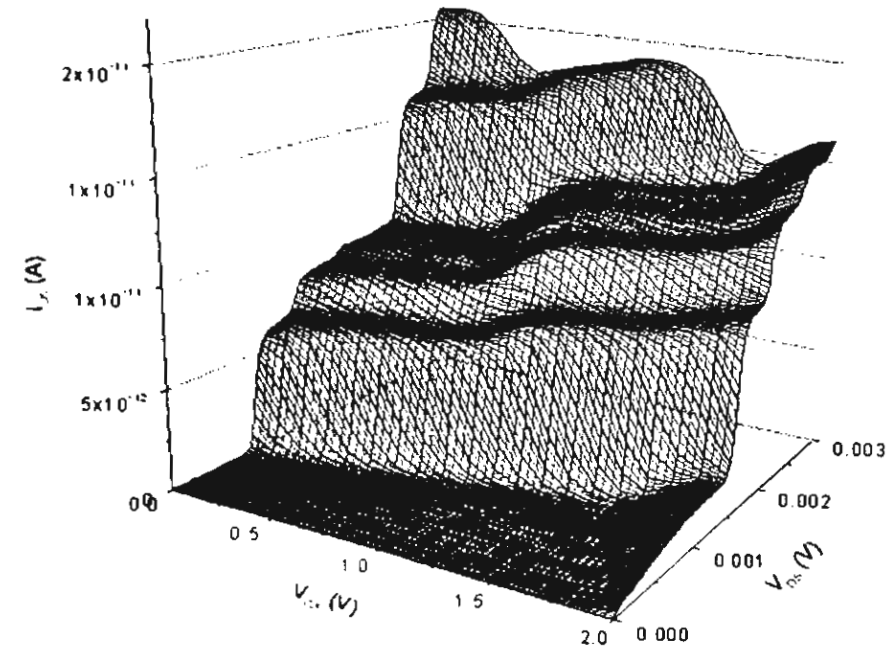
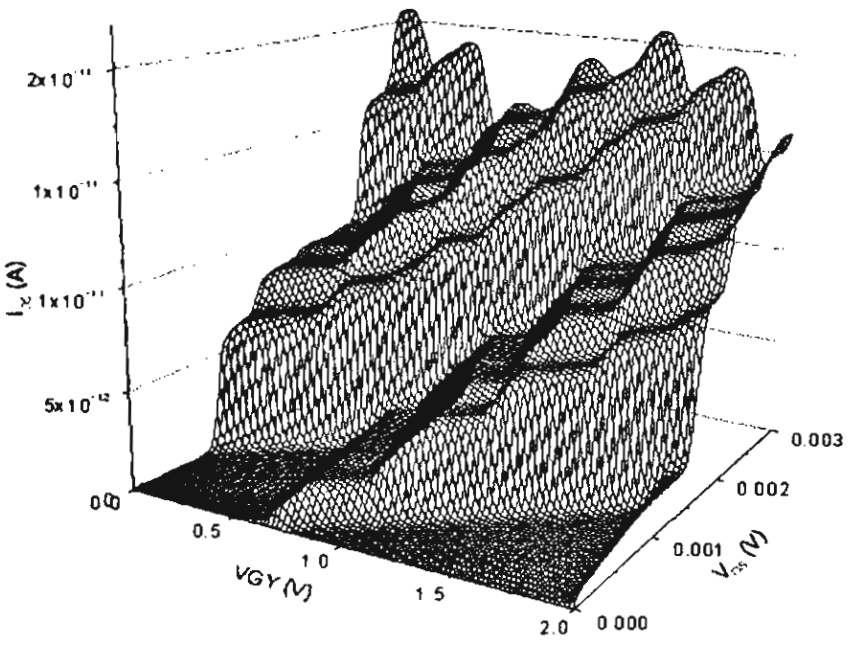


Figure 24. Colour plot of drain-to-source current as functions of V_{DS} and V_{GX} of symmetrical semiconducting quantum dot transistor, with the same simulation parameters as those used in Fig. 23, except for the value of $\Delta\varepsilon$ which is changed to (a) 0.6meV or (b) 0.8meV.



(a)



(b)

Figure 25. Drain-to-source current (wireframe) plot for asymmetrical single-electron transistor as functions of V_{DS} and (a) low coupling-capacitance gate voltage V_{GX}, and (b) high coupling-capacitance gate voltage V_{GY}. See text for simulation parameters.

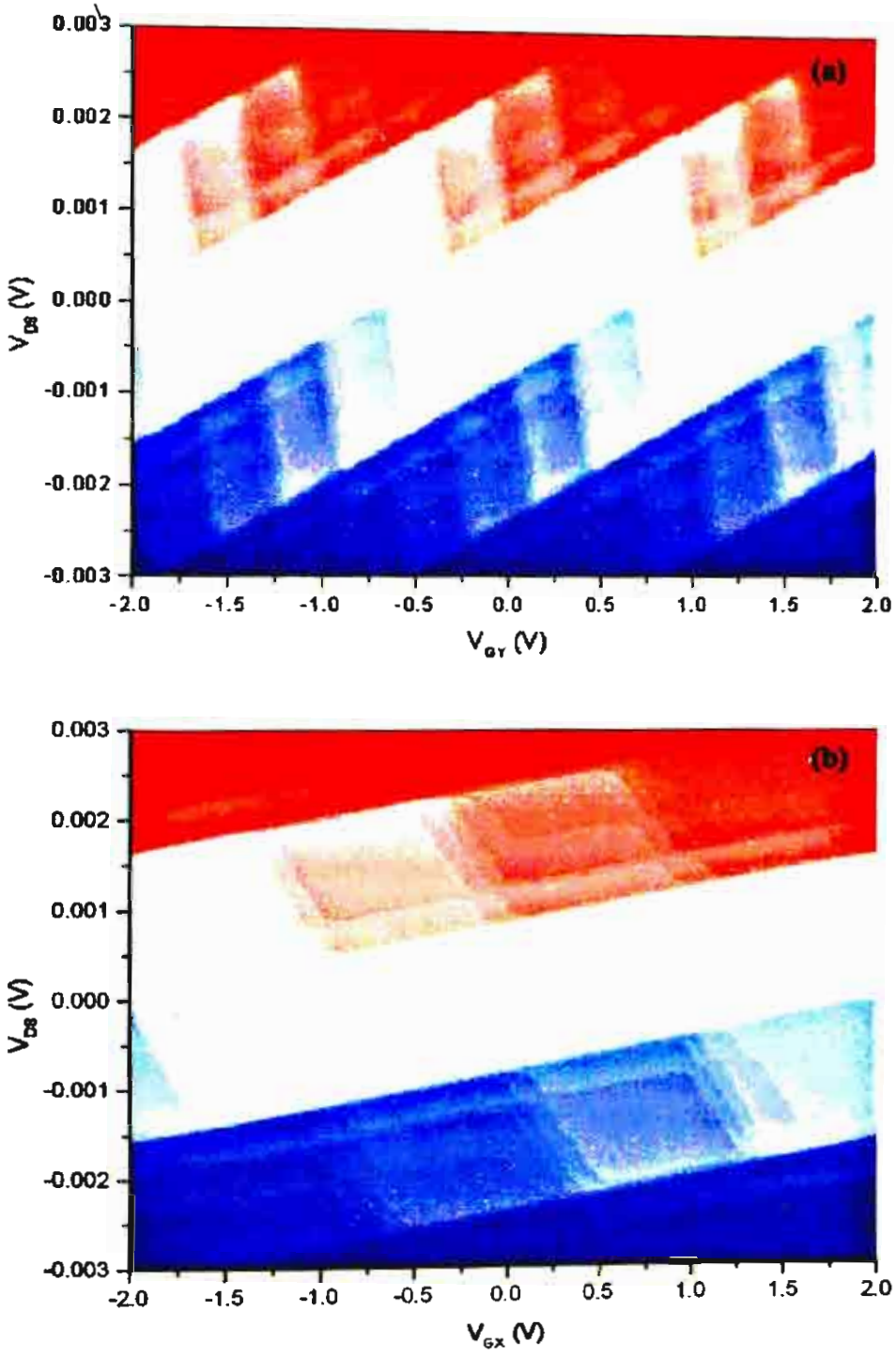


Figure 26. Drain-to-source current (colour) plot for asymmetrical single-electron transistor as functions of V_{DS} and (a) low coupling-capacitance gate voltage V_{GX}, and (b) high coupling-capacitance gate voltage V_{GY}. See text for simulation parameters.

3.5.2 Application: Low-Power Mixers

To operate as a mixer, the dual-gate quantum dot transistor takes inputs from the two gates in a similar fashion to the dual-gate device demonstrated by Collier *et al.* [21]. The output is taken from the variation in I_{DS}. Two input signals of the same or different frequencies, one applied to G1 and the other to G2, influence the electrostatic potential of the quantum dot by means of capacitive coupling through the substrate. As a result, the energy levels in the quantum dot are effectively adjusted by both input signals resulting in an output current (I_{DS}) whose magnitude depends on the state of the dot. In order to show that the proposed methodology can be performed experimentally, a previously published result of a dual-gate transistor will also be considered here.

The material used in the experiment previously carried out by Kanjanachuchai *et al.* [22] consists of a 50-nm thick silicon-germanium (SiGe) layer grown on a silicon-on-insulator (SOI) substrate by low-pressure chemical vapour deposition at 800°C. Device fabrication involves an electron-beam lithography stage, where critical dimensions are defined, and a conventional photolithography stage, for device isolation and bond pads. The finished device has a 50-nm dot as its active region. Two gates are placed close to the dot; they are separated from the dot by approximately 50 nm and 100 nm, see Fig. 18(a).

Electrical measurements in the experiment were conducted at atmospheric pressure in a helium dewar, i.e. at 4.2 K, using a HP4156A parameter analyzer. Coulomb blockade characteristics of the device have been confirmed, indicating that the quantum dot transistor operated as expected. Only Coulomb oscillations (changes in drain-source current I_{DS} as a function of gate voltage $V_{G1\text{-}G2}$) are considered in this work. Note that $V_{G1\text{-}G2}$ represents a coupled-gate configuration where both gates are connected.

Figure 27 shows the I_{DS}-$V_{G1\text{-}G2}$ characteristics of the QDT as a function of V_{DS}. The coupled gate is swept from 8 to 10 V while V_{DS} is kept constant during each trace: at +3 mV, +1 mV, −1 mV and −3 mV. Coulomb oscillations for all biases are clearly visible; the periodic nature of the results is obvious to the eye although fast Fourier

transforms have been performed on these sets of data where periodicity in all traces has been confirmed. The most stable oscillations can be observed at around $V_{G1+G2} = 9.1$ V (for $V_{DS} = -3$ mV, shown as dotted rectangle in the figure); therefore, electrical response of the device around this point will be used to demonstrate frequency mixing operations. Figure 28 illustrates the expanded view of the measured characteristic (shown as open circles) around the region enclosed in the box in Fig. 27, and the best sinusoidal fit (line) which has been modelled by the equation:

$$I_{DS}\,(\text{nA}) = -0.25\times\cos(89.7\times V_{G1+G2} - 0.75) - 1 \qquad (29)$$

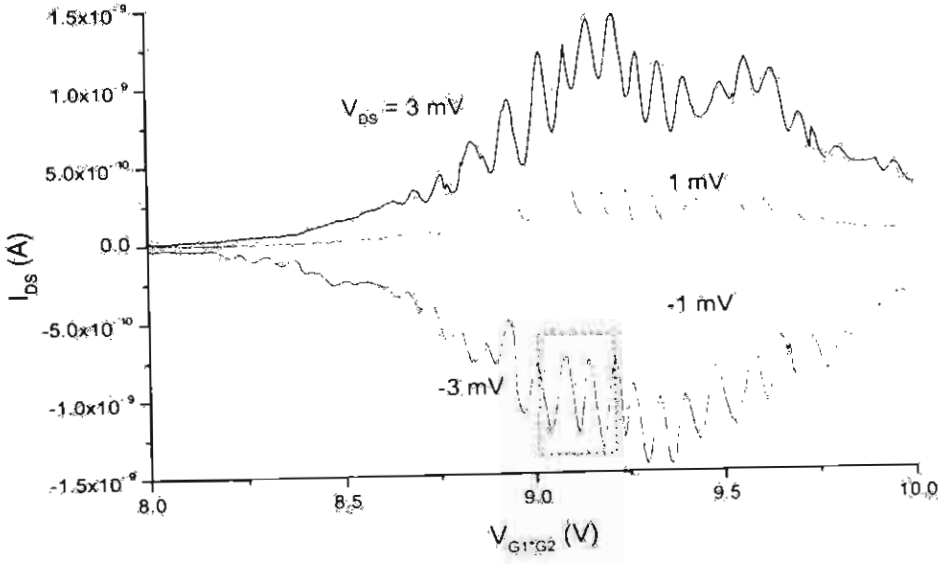


Figure 27. Souce-drain current of the quantum dot transistor as the coupled gate is swept from 8 to 10 V. The source-drain voltage is kept constant during each trace: at +3 mV, +1 mV, –1 mV and –3 mV as indicated.

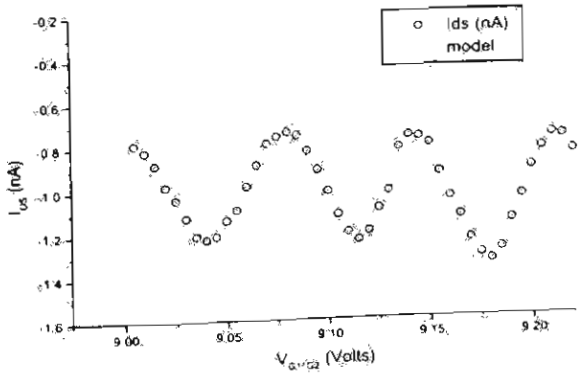


Figure 28. Expanded view of the section enclosed by the dotted box in Fig. 27. The measured characteristic (open circles) is sinusoidal in nature and can be modelled by an a.c. component superimposed onto a d.c. current centred at around –1 nA (see text for detail).

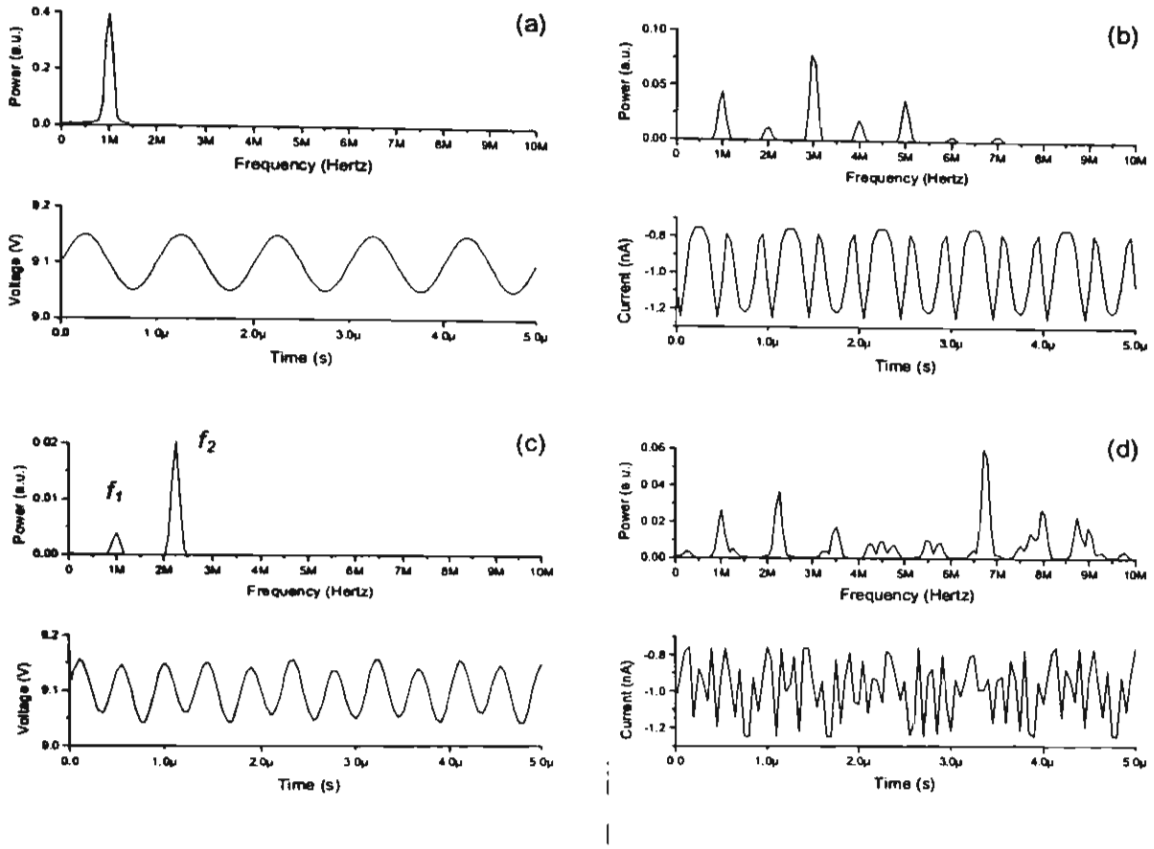


Figure 29. The frequency (upper panel) and time (lower panel) components of the one-frequency input voltage (a) and output current (b), and the two-frequency input voltage (c) and output current (d). The time data are generated mathematically. The frequency data are obtained using fast Fourier transform.

Knowing the electrical response of the quantum dot to varying gate potential, the dot's output current can be simulated out of any mathematically-generated input voltages. Shown in Figs. 29(a) and 29(c) are mathematically-generated input voltages as a function of time with one and two principal frequencies, respectively. The upper/lower panels of each figure illustrate the frequency/time data. In the case of one-frequency input (1 MHz), the output current can be readily calculated from the equation since the input voltage is fed directly to the coupled gate. Similarly, output current from the two-frequency input (1 and 2.25 MHz) can be calculated from the same equation, with some corrections on the magnitude due to different gate-to-dot capacitance of the two gates. However, such corrections do not affect frequency data and are thus ignored. The simulated output currents from the one- and two-frequency input signals are shown in Figs. 29(b) and 29(d) respectively.

The output response, Fig. 29(b), from the one-frequency input shows that together with the principal input frequency (1 MHz) there are also several frequency components (most notably the 3 and 5 MHz peaks) which are reflected in the output current. In the two-frequency input (f_1 = 1 MHz and f_2 = 2.25 MHz), modulation of the two frequencies according to $mf_1 \pm nf_2$, where m and n are integers, is obtained. The three most strong peaks are at 6.75, 8 and 8.75 MHz which correspond to $0f_1 + 3f_2$, $4f_2 - 1f_1$ and $2f_1 + 3f_2$ respectively. Similarly, other peaks can be explained using different sets of m and n.

In order to have a better understanding of the mixing operation and the selection of operating points of each device, the time-dependent simulations above have to be supplemented with additional information regarding tunnel current as functions of gate voltages V_{GX} and V_{GY} when the drain-source voltage V_{DS} is fixed. Two sets of simulations for symmetrical and asymmetrical systems will be considered.

In the case of symmetrical junctions, the parameters are the same as those used in the simulation of Fig. 23, i.e. with tunnel resistance of 50MΩ, tunnel capacitance of 50aF, and gate capacitances of 0.08aF each. The dot itself is assumed to have energy levels which are spaced 0.4meV apart, i.e. $\Delta\varepsilon$ = 0.4meV. Both gate voltages V_{GX} and V_{GY} are swept from -2V to 2V in 0.02V steps. The temperature is set at 0.3K. V_{DS} is kept constant in each simulation to conform with the fact that V_{DS} has to be kept constant throughout mixing operation.

Figure 30 shows colour plots of tunnel current with varying intensity (red represents high positive current, blue no current; there is no negative current because V_{DS} is positive, see colour code in the figure for details). The fixed value of V_{DS} in each simulation is kept at 1, 2 and 3mV in Figs. 30(a), 30(b) and 30(c), respectively.

The plots show that the tunnel current in symmetrical system varies with gate voltages in characteristic 45° stripes. This is a direct result of C_{GX} being equal to C_{GY}. Although the three plots show that the stripes have the same orientation, closer examinations reveal that the degree to which tunnel currents fluctuate between the peaks (red) and troughs (blue) do vary significantly.

For mixing applications where a linear relationship between the inputs and output is desireable, device operation based on Fig. 30(a) is the most appropriate of the three because the spacing among the peaks and troughs are sinusoidal and linear. Thus the V_{DS} in this particular system should be biassed at 1mV for mixing applications.

On the other hand, if signals amplification is also required, the rate of change of current should be as fast as possible in order to obtain high gain. In this case, the result shown in Fig. 30(b) is the most appropriate biassing condition of the three.

In the case of asymmetrical junctions, the stripes will not exhibit a 45° characteristic in a similar plot to those shown in Fig. 30. Instead, the divergence from the 45° angle will be determined by the degree of asymmetry. Figure 31 shows the tunnel current as functions of V_{GX} and V_{GY} for a system with the following asymmetrical properties: $R_S = 10R_D = 100M\Omega$, $C_{GY} = 3C_{GX} = 0.12aF$, $\Delta\varepsilon = 0.4meV$, $T = 0.3K$, $V_{DS} = 1mV$. Another interesting feature which is not present in the symmetrical case above is that the stripes exhibit an oscillatory feature which is off-axis. This feature requires further explanation and experimental observations which have to be carried out at cryogenic temperatures. Applications of such feature may include single-electron pumps [23], in addition to single-electron mixers.

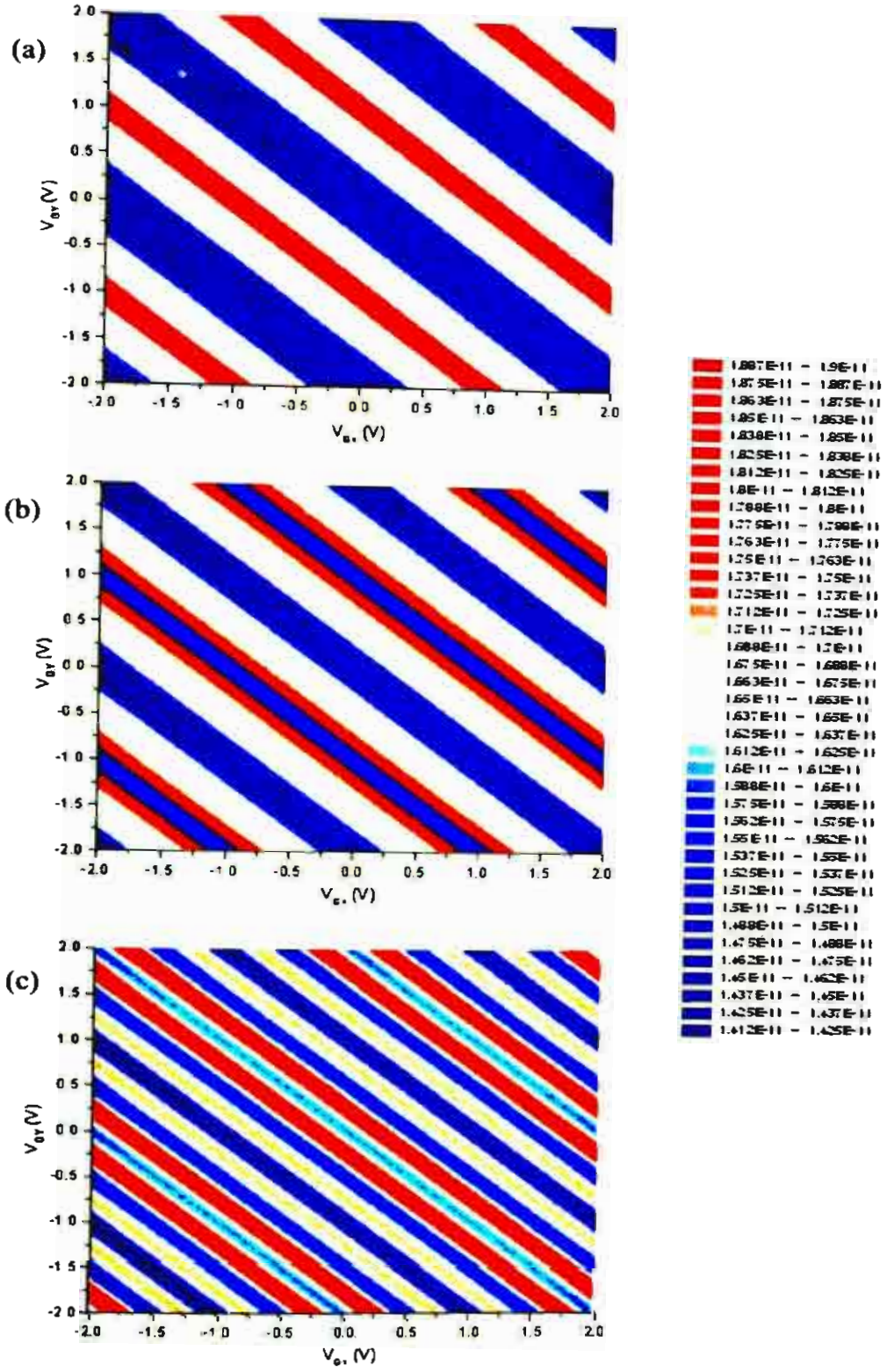


Figure 30. Drain-to-source currents of *symmetrical*, semiconducting quantum dot transistor as functions of gate biasses. V_{DS} is set to (a) 1mV, (b) 2mV or (c) 3mV.

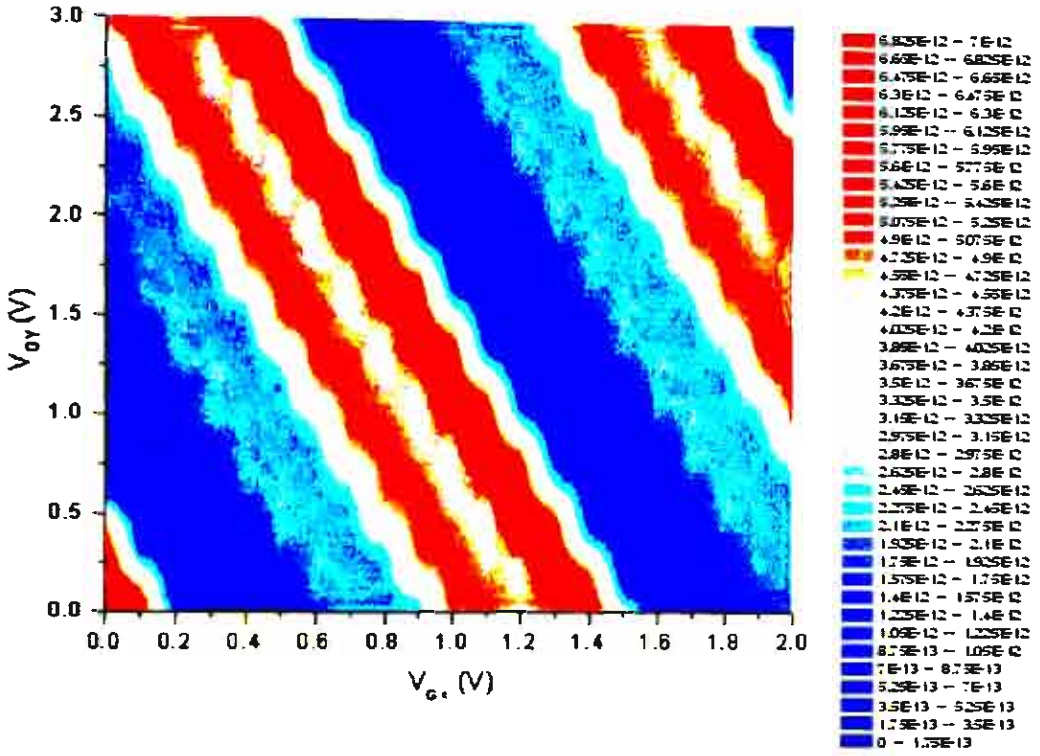


Figure 31. Drain-to-source currents of *asymmetrical*, semiconducting quantum dot transistor as functions of gate biasses. V_{DS} is set to 1mV. See text for other simulation parameters.

4. Conclusion

To summarise, the report provides background on theoretical aspects of current conduction in quantum dots, starting from the treatment of simple single-tunnel junctions to more complicated double-tunnel junctions. Analytical solution for the current-voltage characteristic is then given. The extension of the solution to include dual-gate quantum dot configuration is given in Chapter 3 where detailed simulations of quantum-dot transistors are carried out.

The most important signatures of single-electron charging effects are the Coulomb blockade characteristics, the Coulomb staircase in the case of asymmetric junctions, and the Coulomb oscillation in the current-gate voltage sweep. All these features are present in the simulated results.

A proposal to use the quantum dot transistor configuration as a signal mixer is explained in detail. The sinusoidal response of I_{DS} to varying gate voltage in a quantum dot transistor provides the basis for frequency manipulation, on a quantum scale. The semi-empirical simulations in section 3.4 show that for one-frequency input, the QDT may function as a frequency multiplier – provided that the required frequency is singled out using a proper band-pass filter. And for two-frequency input, modulation and demodulation functions are feasible, i.e. the QDT effectively operates as a mixer. These may lead to QDTs being adopted in various analog circuits, particularly in low-power high-density applications.

Despite the promises of having useful analog devices, proof-of-principle experiments are necessary before any conclusion can be made with regard to room temperature operation and subsequent applications.

References

[1] ITRS for public: http://public.itrs.net

[2] M. Amman, R. Wilkins, E. Ben-Jacob, P. D. Maker, and R. C. Jaklevic, "Analytic solution for the current-voltage characteristic of two mesoscopic tunnel junctions coupled in series", *Phys. Rev. B* **43**, 1146 (1991).

[3] J. H. F. Scott-Thomas, S. B. Field, M. A. Kastner, H. I. Smith, and D. A. Antoniadis, "Conductance oscillation periodic in the density of a one-dimensional electron gas", *Phys. Rev. Lett.* **62**, 583 (1989).

[4] M. A. Kastner, "The single-electron transistor", *Rev. Mod. Phys.* **64**, 849 (1992).

[5] Boeuf F, Jehl X, Sanquer M, Skotnicki T, "Controlled single-electron effects in nonoverlapped ultra-short silicon field effect transistors", *IEEE Trans. on Nanotechnology* **2** (3), 144-148 (2003).

[6] Nakajima F, Miyoshi Y, Motohisa J, Fukui T, "Single-electron AND/NAND logic circuits based on a self-organized dot network", *Appl Phys Lett* **83** (13), 2680-2682 (2003).

[7] Duan XF, Huang Y, Cui Y, Wang JF, Lieber CM, "Indium phosphide nanowires as building blocks for nanoscale electronic and optoelectronic devices", *Nature* **409** (6816), 66-69 (2001).

[8] Yu ZR, Aceves M, Carrillo J, Flores F, "Single electron charging in Si nanocrystals embedded in silicon-rich oxide", *Nanotechnology* **14** (9), 959-964 (2003).

[9] Marty L, Bouchiat V, Naud C, Chaumont M, Fournier T, Bonnot AM, "Schottky barriers and Coulomb blockade in self-assembled carbon nanotube FETs", *Nano Lett* **3** (8), 1115-1118 (2003).

[10] Wakayama Y, Kubota T, Suzuki H, Kamikado T, Mashiko S, "Molecular Coulomb islands for single-electron tunneling in SiO2/molecular layer/SiO2 multilayers on Si(100)", *J Appl Phys* **94** (7), 4711-4713 (2003).

[11] D. V. Averin and K. K. Likharev, "Coulomb blockade of single-electron tunnelling, and coherent osciallations in small tunnel junctions", *J. Low Temp. Phys.* **62**, 345 (1986); see also, K. K. Likharev, "Single-electron transistors: electrostatic analogs of the DC SQUIDs", *IEEE Trans. Mag.* **MAG-23**, 1142 (1987); and, D. V. Averin, A. N. Korotkov, and K. K. Likharev, "Theory of single-electron charging of quantum wells and dots", *Phys. Rev. B* **44**, 6199 (1991).

[12] See, for example, *Single Charge Tunnelling – Coulomb Blockade Phenomena in Nanostructures*, NATO ASI Series B, Edited by H. Grabert and M. H. Devoret (Plenum, New York, 1992).

[13] U. Meirav and E. B. Foxman, "Single-electron phenomena in semiconductors", *Semicond. Sci. Technol.* **11**, 255 (1996).

[14] L. P. Kouwenhoven, C. M. Marcus, P. L. MaEuen, S. Tarucha, R. M. Westervelt, and N. S. Wingreen, "Electron transport in quantum dots", in *Mesoscopic Electron Transport*, edited by L. L. Sohn *et al.* (Kluwer Academic, Netherlands, 1997).

[15] G.-L. Ingold and Yu. V. Nazarov, "Charge tunnelling rates in ultrasmall junctions", in *Single Charge Tunnelling – Coulomb Blockade Phenomena in Nanostructures*, NATO ASI Series B, Edited by H. Grabert and M. H. Devoret (Plenum, New York, 1992).

[16] D. V. Averin and K. K. Likharev, in Mesoscopic Phenomena in Solids, edited by B. L. Altshuler, P. A. Lee, and R. A. Webb (Elsevier Science, North Holland, 1991), p. 173.

[17] T. A. Fulton and G. J. Dolan, "Observation of single-electron charging effects in small tunnel junctions", *Phys. Rev. Lett.* **59**, 109 (1987).

[18] T. J. Thornton, M. Pepper, H. Ahmed, D. Andrews, and G. J. Davies, "1D conduction in the 2DEG of a GaAs/AlGaAs heterojunction", *Phys. Rev. Lett.* **56**, 1198 (1986).

[19] D. Ali and H. Ahmed, "Coulomb blockade in a silicon tunnel junction device", *Appl. Phys. Lett.* **64**, 2119 (1994).

[20] K. Mullen, E. Ben-Jacob, R. C. Jaklevic, and Z. Schuss, "I-V characteristics of coupled ultrasmall-capacitance normal tunnel junctions", *Phys. Rev. B* **37**, 98 (1988) ; see also, [2]

[21] N. J. Collier and J. R. A. Cleaver, "A novel dual-gate high electron mobility transistor using a split-gate structure", *Appl. Phys. Lett.* **71**, 2958 (1997).

[22] S. Kanjanachuchai, J. M. Bonar, and H. Ahmed, "Single charge tunnelling in n- and p-type strained silicon germanium on silicon-on-insulator", *Semicond. Sci. Technol.* **14**, 1065 (1999).

[23] Shimada H, Ono K, Ootuka Y, "Driving the single-electron device with a magnetic field (invited)", *J Appl Phys* **93**, 8259-8264 (2003).

Appendix A

Source Code for Analytical Solution for Current-Voltage Characteristics of Single-Electron Transistors

```
#include <stdio.h>
#include <math.h>
#include <stdlib.h>     /* for atof */
#include <ctype.h>      /* for isalpha */
#include <string.h>     /* for strcmp*/
#define TRUE 1
#define FALSE 0
#define MAXLINE 1000
#define MAXVDS 500
#define MAXVGS 500
const int S2DOT=1;      /* Directions of tunnelling */
const int D2DOT=2;
const int DOT2S=3;
const int DOT2D=4;

const double e=1.60217733e-19;          /* electronic charge */
const double kB=1.380658e-23;  /* Boltzmann constant */

char *OutFile;
double Eo,DE,Rs,Rd,Cs,Cd,Cg,Temp,alpha,beta,eta,period,
double Vdstart,Vdstop,Vdstep,Vgstart,Vgstop,Vgstep;
double C;                               /* Total capacitance */
double Ec;                              /* Coulomb Charging energy */
double cf;                              /* Correction factor for Gamma */
int NewPzero,                           /* Ps( * I(  */
int nMAX,                               /* MAX # of electrons */
double P[100];                          /* Prob  of n el-h in the dot */

int GetInput(char *line);
int Find_nMAX(int x,int y,double a,double b);
double CFactor(double n, double p);
double Vs(int n,double Vds,double Vg);
double Vd(int n,double Vds,double Vg);
double deltaE(int n,double Vds,double Vg,int direction);
double Gamma(int n,double Vds,double Vg,int direction);
double InGamma(int n,double Vds,double Vg);
double OutGamma(int n,double Vds,double Vg);
double Pn(int n,double Vds,double Vg);
double I(double Vds,double Vg);

main(int argc, char *argv[])

{
  FILE *fp;
  extern double Rs,Rd,Cs,Cd,Cg,Temp;
  extern double beta,period;
  extern double Vdstart,Vdstop,Vdstep,Vgstart,Vgstop,Vgstep;
  extern double C,Ec;
  extern double cf;
  extern char *OutFile;
  extern int NewPzero,nMAX;
  double VDS[MAXVDS],VGS[MAXVGS],IDS[MAXVDS][MAXVGS];
  double offset;
  char line[MAXLINE],input[MAXLINE];
  int x=0,y=0;  /* Various counters */
  int i,j;


/*================ Input Handling ======================*/

  if (argc==1) printf("No input: Program terminated\n");
  else if (fp = fopen(*++argv,"r")) ==NULL) {
               printf("Can't open %s\n",*argv);
               return 1; }
       else    while ((fgets(line, MAXLINE,fp)) != NULL)
               GetInput(line);
  fclose(fp);

/*==================== Initialisation ======================*/

  cf = 1;                       /* Set correction factor to 1 */
  C = Cs + Cd + Cg;             /* Total capacitance */
  Ec = (e*e)/(2*C);             /* Charging energy */
  period = e/Cg;                /* mostly ! */
  NewPzero = FALSE;
printf("-------------------------------------\n");
printf("Rs/Rd = %4.0f Cs/Cd = %4.0f\n",Rs/Rd,Cs/Cd);
printf("C=%e Ec=%e kB*T=%e period=%e V\n",C,Ec,kB*Temp,period);
printf("DE/Ec=%2.3f/%2.3f meV/meV=%2.3f\n",DE,1000*Ec/e,DE*e/(1000*Ec));
printf("Period due to SEC = %3.3f mV\n",2000*Ec/e);
printf("Period due to  DE = %3.3f mV\n",DE);
printf("-------------------------------------\n");

  if (Vdstep != 0) x=(Vdstop-Vdstart)/Vdstep;
  else x=0;
  if (Vgstep != 0) y=(Vgstop-Vgstart)/Vgstep;
  else y=0;
```

```
  nMAX = Find_nMAX(x,y,e/C,e/Cg);
  printf("nMAX=%d\n",nMAX);

/*====================== Maths ==================================*/

  printf("x=%d y=%d\n",x,y);
  if (x>MAXVDS || y> MAXVGS)
       printf("WARNING: may have storage problem!!\n");

  fp = fopen(OutFile,"w");
  fprintf(fp,"Temp=%e K Eo=%e meV DE=%e meV\n",Temp,Eo,DE);
  fprintf(fp,"alpha=%f beta=%f eta=%f\n",alpha,beta,eta);
  fprintf(fp,"Rs=%e Ohms Rd=%e Ohms\n",Rs,Rd);
  fprintf(fp,"Cs=%g Cd=%g Cg=%g\n",Cs,Cd,Cg);
  fprintf(fp,"Vdstart=%e Vdstop=%e Vdstep=%e\n",Vdstart,Vdstop,Vdstep);
  fprintf(fp,"Vgstart=%e Vgstop=%e Vgstep=%e\n",Vgstart,Vgstop,Vgstep);
  fprintf(fp,"--------------------------\n");
  fprintf(fp,"Rs/Rd = %4.0f Cs/Cd = %4.0f\n",Rs/Rd,Cs/Cd);
  fprintf(fp,"DE/Ec=%2.3f/%2.3f meV/meV=%2.3f\n",DE,1000*Ec/e,DE*e/(1000*Ec));
  fprintf(fp,"Period due to SEC = %3.3f mV\n",2000*Ec/e);
  fprintf(fp,"Period due to  DE = %3.3f mV\n",DE);
  fprintf(fp,"--------------------------\n");

  offset=0e-9;

/*---- Sweeping Vds ------------------*/
  if (x>y) {
     fprintf(fp,"Vds(V) ");
     for(j=0;j<=y;++j)  {
        VGS[j]=Vgstart+j*Vgstep;
        fprintf(fp,"I@Vgs=%2.3f ",VGS[j]);
        for(i=0;i<=x;++i) {
                VDS[i]=Vdstart+i*Vdstep;
                IDS[i][j]=I(VDS[i],VGS[j]);
                }
        }
     fprintf(fp,"\n");
     for(i=0;i<=x;++i) {
        fprintf(fp,"%e ",VDS[i]);
        for(j=0;j<=y;++j)
                fprintf(fp,"%e ",IDS[i][j]+j*offset);
        fprintf(fp,"\n");
        }
     }
/*---- Sweeping Vgs ------------------*/
  else if ((x<y) && (beta==1)) {      /* normal Vgs run */
     fprintf(fp,"Vgs(V) ");
     for(i=0;i<=x;++i)  {
        VDS[i]=Vdstart+i*Vdstep;
        fprintf(fp,"I@Vds=%2.3f ",VDS[i]);
        for(j=0;j<=y;++j) {
                VGS[j]=Vgstart+j*Vgstep;
                IDS[j][i]=I(VDS[i],VGS[j]);
                }
        }
     fprintf(fp,"\n");
     for(j=0;j<=y;++j) {
        fprintf(fp,"%g ",VGS[j]);
        for(i=0;i<=x;++i) {
                fprintf(fp,"%g ",IDS[j][i]+i*offset);}
        fprintf(fp,"\n");
        }
     }
  else if ((x<y) && (beta!=1)) {

     double i_smallest;
     double Vgs_smallest;
     double Vgstart0;
     double temp=0;

     if (Vgstep<0) {printf("WARNING: must use +ve Vgstep!\n");return 0;}
     i_smallest=1;

     for(j=0;(j*Vgstep)<period;++j) { /* Assuming +ve Vgs */
        VGS[j]=Vgstart+j*Vgstep;
        IDS[j][0]=I(Vdstart,VGS[j]);
        temp = fabs(IDS[j][0]);
        if (temp<i_smallest) {i_smallest=temp; Vgs_smallest=VGS[j];}
        }

     Vgstart0=Vgs_smallest;
     y=(Vgstop-Vgstart0)/Vgstep+1;

     fprintf(fp,"Vgs(V) ");
     for(i=0;i<=x;++i)  {
        VDS[i]=Vdstart+i*Vdstep;
        fprintf(fp,"I@Vds=%2.3f ",VDS[i]);
```

```
        for(j=0;j<=y;j++) {
            cf=cFactor(j*Vgstep/period);
            VGS[j]=Vgstart0+j*Vgstep;
            IDS[j][a]=I(VDS[i],VGS[j]);
            }
        }
      fprintf(fp,"\n");
      for(j=0;j<=y;++j) {
         fprintf(fp,"%g ",VGS[j]);
         for(i=0;i<=x;++i)
                fprintf(fp,"%g ",IDS[j][i]*scaleFactor);
         fprintf(fp,"\n");
         }
   }

   fclose(fp);
   return 0;
}

/*-------------------------------------------------------------------------*/

int GetInput(char *line)
{
   extern double Es,Ed,Ds,Dd,Eg Temp,alpha,beta,eta;
   extern double Vdstart,Vdstop,Vdstep,Vgstart,Vgstop,Vgstep;
   extern char *OutFile;
   int i=0,j=0;
   char *s;
   char input[MAXLINE];

        for(i=0; isdigit(line[i]) && isspace(line[i]) &&
                line[i]!='\0' && line[i]!='\n';i++);
                input[j++]=line[i];
        if(isspace(line[i])) input[j]='\0';
        input[j]='\0';
        s=&line[i];

        if(strcmp(input,"Temp")==0)   Temp = atof(s);
        else if(strcmp(input,"Es")==0)   Es = atof(s);
        else if(strcmp(input,"Ds")==0)   Ds = atof(s);
        else if(strcmp(input,"alpha")==0)   alpha = atof(s);
        else if(strcmp(input,"beta")==0)   beta = atof(s);
        else if(strcmp(input,"eta")==0)   eta = atof(s);
        else if(strcmp(input,"Ed")==0)   Ed = atof(s);
        else if(strcmp(input,"Dd")==0)   Dd = atof(s);
        else if(strcmp(input,"Eg")==0)   Eg = atof(s);
        else if(strcmp(input,"Dg")==0)   Dg = atof(s);
        else if(strcmp(input,"Vdstart")==0)  Vdstart = atof(s);
        else if(strcmp(input,"Vdstop")==0)   Vdstop = atof(s);
        else if(strcmp(input,"Vdstep")==0)   Vdstep = atof(s);
        else if(strcmp(input,"Vgstart")==0)  Vgstart = atof(s);
        else if(strcmp(input,"Vgstop")==0)   Vgstop = atof(s);
        else if(strcmp(input,"Vgstep")==0)   Vgstep = atof(s);
        else if(strcmp(input,"OutFile")==0)
                while(isspace(line[i])) i++;
                for(j=0;line[i]!='\n' && line[i]!='\0';)
                        input[j++]=line[i++];
                input[j]='\0';
                OutFile = input;
                }
        else printf("Warning: Unknown parameter %s\n",input);

}

/*-------------------------------------------------------------------------*/

int Find_nMAX(int x,int y,double a,double s)
{
   extern double Vdstop,Vgstop,Vdstart,Vgstart;
   int n;
   double c;

   if (x>=y) {
         c=fabs(Vdstop-Vdstart)/a;
         for(n=0;c>=0;n++) c=c-1.;
   else if(x<y) {
         c=fabs(Vgstop-Vgstart)/a;
         for(n=0;c>=0;n++) c=c-1.;}

   if (n>0 && n<5) return 5;    /* minimum # electrons */
   else if (n<96) return n+3;
   else if (n>96) {
         printf("WARNING: Too high bias!\n");
         printf("\tReduce Vdstop or Vgstop\n");
         return 99;}
```

```
}

/*------------------ Correction Factor -------------------------------*/

double CFactor(double n, double p)
{
  extern double beta;
  double c;
  int i;

  c=n;
  for(i=0;fabs(c/p)>1;) {c=c-p;++i;}
  return pow(beta,i);
}

/*------------------ Vs and Vd ---------------------------------*/

double Vs(int n,double V,double Vg)
{ extern double Cs,Cd,Cg,C;
  return ((Cd/C)*V + (Cg/C)*Vg - (n*e/C));}

double Vd(int n,double V,double Vg)
{ extern double Cs,Cd,Cg,C;
  return (((Cs + Cg)/C)*V - (Cg/C)*Vg + (n*e)/C);}

/*-----------------------------------------------------------------*/

double deltaE(int n,double Vds,double Vg,int direction)
{
  extern double Ec;

  if (direction == S2DOT)      return ( e*Vs(n,Vds,Vg)-Ec);
  else if(direction == DOT2S) return (-e*Vs(n,Vds,Vg)-Ec);
  else if(direction == DOT2D) return ( e*Vd(n,Vds,Vg)-Ec);
  else if(direction == D2DOT) return (-e*Vd(n,Vds,Vg)-Ec);
  else {printf("Error in deltaE\n"); return 0;}
}

/*-----------------------------------------------------------------*/

double Gamma(int n,double Vds,double Vg,int direction)
{
  extern double Temp,Eo,DE,Rs,Rd,alpha,eta,cf,period;
  double Rt,dE,E,EO,sum;
  double rtn;  /* Gamma prior to correction */
  double perV; /* Changes in Rt per Vg */
  double a,b;
  int c;

  sum=0;a=0;b=0;
  dE=deltaE(n,Vds,Vg,direction);
  E=DE*0.001*e;                /* Level spacing in meV */
  EO=Eo*0.001*e;       /* Ground state energy in meV */

  if (direction==S2DOT || direction==DOT2S) {
       perV=(eta*Rs)/(100*period);
       Rt=Rs+perV*Vg; }
  else if (direction==D2DOT || direction==DOT2D) {
       perV=(eta*Rd)/(100*period);
       Rt=Rd+perV*Vg; }

  if (DE==0) { /* Metals */
    if (dE>(100*kB*Temp)) rtn = dE/(e*e*Rt);
    else if (dE<(-100*kB*Temp)) rtn = (-dE/(e*e*Rt))*exp(dE/(kB*Temp));
    else rtn = (dE/(e*e*Rt))*1/(1-1/exp(dE/(kB*Temp))); }
  else {               /* Semiconductors */
    for(c=0;c<50;++c) {
       a=1+exp((EO+c*E-dE)/(kB*Temp));
       b=1+1/exp((EO+c*E)/(kB*Temp));
       sum += 1/(a*b);}
    rtn = (sum*E)/(e*e*Rt);
  }

  return cf*(rtn+alpha*pow(Vds,3)/Rt);

}

/*-------------- Tunnel rates into/outof the dot --------------*/

double InGamma(int n,double Vds,double Vg)
{ return Gamma(n,Vds,Vg,S2DOT)+Gamma(n,Vds,Vg,D2DOT);}

double OutGamma(int n,double Vds,double Vg)
{ return Gamma(n,Vds,Vg,DOT2S)+Gamma(n,Vds,Vg,DOT2D);}

/*-----------------------------------------------------------------
        Probability of finding n electrons/holes in the dot.
```

```
                \
        Summing over +/- 5 is good enough
   ------------------------------------------------------------------------*/

double Pn(int n,double Vds,double Vg)

{
  extern double P[];
  extern int NewPzero,nMAX;
  double NewPo;
  int b,c,m,middle;
  double sum=0;
  double Po=1; /* for 0 electrons/holes */


  middle = nMAX;
  c=n+middle;  /* P[middle] is for 0 el/h */

  if (NewPzero == FALSE) {
        P[middle]=Po;
        for (b=middle+1;b<=2*nMAX;++b)  { m=b-middle;
                P[b]=(P[b-1])*(InGamma(m-1,Vds,Vg)/OutGamma(m,Vds,Vg));}
        for (b=middle-1;b>=0;--b)    { m=b-middle;
                P[b]=(P[b+1])*(OutGamma(m+1,Vds,Vg)/InGamma(m,Vds,Vg));}

        for (b=0;b<=2*nMAX;++b)
                sum += P[b];
        NewPo = 1/sum;
        NewPzero = TRUE;
        for (b=0;b<=2*nMAX;++b)
                P[b] *= NewPo;

        return P[c];
        }
  else if (NewPzero == TRUE) return P[c];
  else (*Warning: Error in Pn()\n");
}

/*-------------------------------------------------------------*/

double I(double Vds,double Vg)

{
  extern int NewPzero,nMAX;
  double i=0;
  int n;        /* counters */

  NewPzero = FALSE;

  for(n=-nMAX;n<=nMAX;++n){
    i+=(e*(Gamma(n,Vds,Vg,S2DOT)-Gamma(n,Vds,Vg,DOT2S))*Pn(n,Vds,Vg));}

  return i;

}
```

Appendix B

Publications

1. 26th Electrical Engineering Conference (domestic)
2. 2002 IEEE International Conference on Industrial Technology

Novel Dual-Gate Quantum-Dot Mixers

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Abstract
Quantum dot transistor is proposed here as a frequency processing device, of which mixing applications are a possibility. Measured electrical characteristics of the transistor are used as a basis for simulations using mathematically-generated input voltage signals. The simulated output currents show that modulation and demodulation of the input frequencies can be achieved, with proper biasing of the transistor.

Keywords: Quantum dot transistors, Coulomb blockade, Coulomb oscillations, dual-gate, mixers.

1. Introduction

When the channel length of a metal-oxide-semiconductor field-effect transistor (MOSFET) is reduced to the sub-0.1 μm regime, charge transport along its inversion layer becomes highly sensitive to the locations of individual dopant atoms, defects and impurities. Scott-Thomas *et al.* measured the current-voltage characteristics of narrow dual-gate MOSFETs and found them to behave in an oscillatory fashion [1]; van Houten and Beenaker later explained the results in terms of single-electron tunnelling across two potential barriers formed in the vicinity of charge impurities [2]. The nonuniformity causes the electron current to oscillate as a function of gate voltage when the latter is swept in order to change the state of the nanoscale transistors from on to off, and vice versa.

Since then, single charge (either electron or hole, depending on the type of majority carriers) phenomena have been extensively studied [3], especially in quantum dot systems [4] where logic [5] and memory [6] applications have been demonstrated. This work explains how the usefulness of quantum dots may be extended to cover analogue applications such as mixers. Section 2 describes the principle of quantum dot transistors (QDT). Section 3 shows the electrical characteristics of a dual-gate QDT. Mixing mechanisms in the QDT are demonstrated via measured electrical response of the device, a set of mathematically generated input voltages, and simulated output currents, shown in section 4. Conclusions are given in section 5.

2. Quantum Dot Transistors (QDTs)

A quantum dot system is one in which the geometrical size of the dot is so small that quantum-sized effects are significant, particularly at low temperatures. In metallic systems the corresponding size is a few nanometers.In semiconductors, the electron density is much smaller; therefore, quantum effects can be seen in structures as large as 100 nm. When these nanoscale dots are connected to external terminals, source (S) and drain (D), charge transport through the dot is possible. One or more gate electrode (G) can thus be placed nearby to control the source-drain current. The electrodes together with the dot are collectively called a quantum dot transistor, see Fig. 1 (a). The equivalent circuit diagram in Fig. 1(b) shows the tunnel junctions represented by a resistor and a capacitor while the coupling between the gate and the dot is entirely capacitive. The quantum dot is represented by the dotted box in the figure, enclosing n electrons

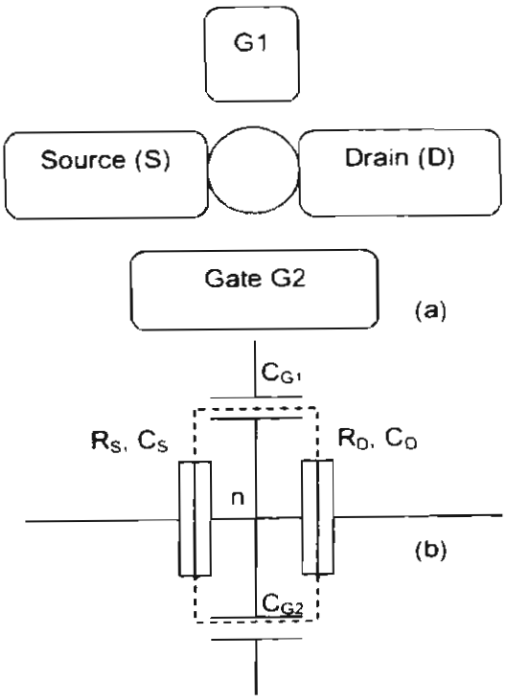

Fig 1. (a) Schematic of a quantum dot transistor. The gates (G1 and G2) control the current passing through the dot between the source (S) and drain (D) terminals (b) Its equivalent circuit diagram: R and C are respectively resistor and capacitor components of S, D, G1 or G2, shown as subscripts.

Current through double-barrier systems is suppressed at low voltages due to Coulombic forces: electrons already stored in the dot prevent external electrons from entering. At a voltage (V_{DS}) larger than a

blockade voltage (V_{CB}), however, the energy of the external electrons can overcome the repulsive forces and the current starts to flow. This is called Coulomb blockade phenomena. The charging energy (E_C) required to overcome the blockade depends entirely on the total capacitance of the island (*i.e.* the capacitance between the island and the rest of the environment) and is given by $E_C = e^2/2C$ where e is the electronic charge and C is the island capacitance.

It is clear from the relationship that as the island gets smaller (and C is lowered) the charging energy, and thus the operating temperature of the device, increases. At room temperature, electrons have sufficient thermal energy and can thus tunnel across the tunnel junctions unimpeded. At cryogenic temperatures, however, electron energy is low and external voltage(s) has to be supplied in order to move electrons across the structure.

Holding V_{DS} constant and sweeping the gate voltage causes electrons to be expelled out of, or injected into the dot one by one depending on the sweep direction. The current thus increases and decreases as the gate voltage is swept. The oscillatory nature was first observed by Scott-Thomas *et al* [1].

3. Device and Electrical Characteristics

The material used in the experiment consists of a 50-nm thick silicon-germanium (SiGe) layer grown on a silicon-on-insulator (SOI) substrate by low-pressure chemical vapour deposition at 800°C [7]. Device fabrication involves an electron-beam lithography stage, where critical dimensions are defined, and a conventional photolithgraphy stage, for device isolation and bond pads. The finished device has a 50-nm dot as its active region. Two gates are placed close to the dot; they are separated from the dot by approximately 50 nm and 100 nm, see Fig. 1(a).

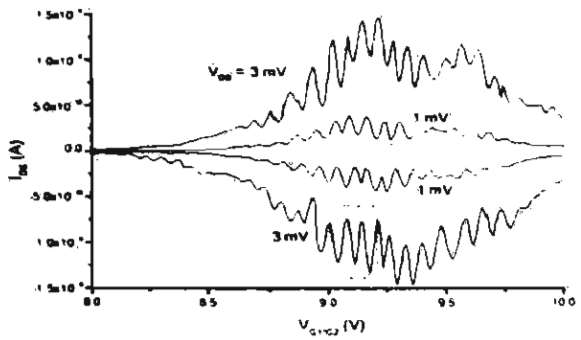

Fig. 2. Souce-drain current of the quantum dot transistor as the coupled gate is swept from 8 to 10 V. The source-drain voltage is kept constant during each trace: at +3 mV, +1 mV, -1 mV and -3 mV as indicated.

Electrical measurements were conducted at atmospheric pressure in a helium dewar, i.e. at 4.2 K, using a HP4156A parameter analyzer. Coulomb blockade characteristics of the device have been confirmed [7], indicating that the quantum dot transistor operated as expected. Only Coulomb oscillations (changes in drain-source current I_{DS} as a function of gate voltage V_{G1+G2}) are considered in this work. Note that V_{G1+G2} represents a coupled-gate configuration where both gates are connected.

Figure 2 shows the I_{DS}-V_{G1+G2} characteristics of the QDT as a function of V_{DS}. The coupled gate is swept from 8 to 10 V while V_{DS} is kept constant during each trace: at +3 mV, +1 mV, -1 mV and -3 mV. Coulomb oscillations for all biases are clearly visible; the periodic nature of the results is obvious to the eye although fast Fourier transforms have been performed on these sets of data where periodicity in all traces has been confirmed. The most stable oscillations can be observed at around V_{G1+G2} = 9.1 V (for V_{DS} = -3 mV, shown as dotted rectangle in the figure); therefore, electrical response of the device around this point will be used to demonstrate frequency mixing operations. Figure 3 illustrates the expanded view of the measured characteristic (shown as open circles) around the region enclosed in the box in Fig. 2., and the best sinusoidal fit (line) which has been modelled by the equation:

$$I_{DS}\,(\text{nA}) = -0.25\times\cos(89.7\times V_{G1+G2} - 0.75) - 1$$

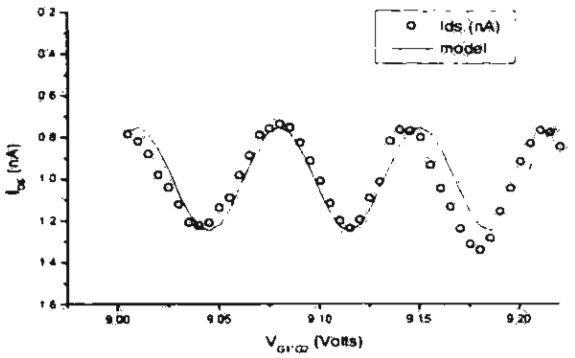

Fig. 3. Expanded view of the section enclosed by the dotted box in Fig. 2. The measured characteristic (open circles) is sinusoidal in nature and can be modelled by an a.c. component superimposed onto a d.c. current centred at around -1 nA (see text for detail).

4. Mixing Mechanism

To operate as a mixer, the quantum dot transistor takes input from the dual-gate in a similar fashion to the dual-gate device demonstrated by Collier *et al.* [8]. The output is taken from the variation in I_{DS}. Two input signals of the same or different frequencies, one applied to G1 and the other to G2, influence the electrostatic potential of the quantum dot by means of capacitive coupling through the substrate. As a result, the energy levels in the quantum dot are effectively adjusted by both input signals resulting in an output current (I_{DS}) whose magnitude depends on the state of the dot.

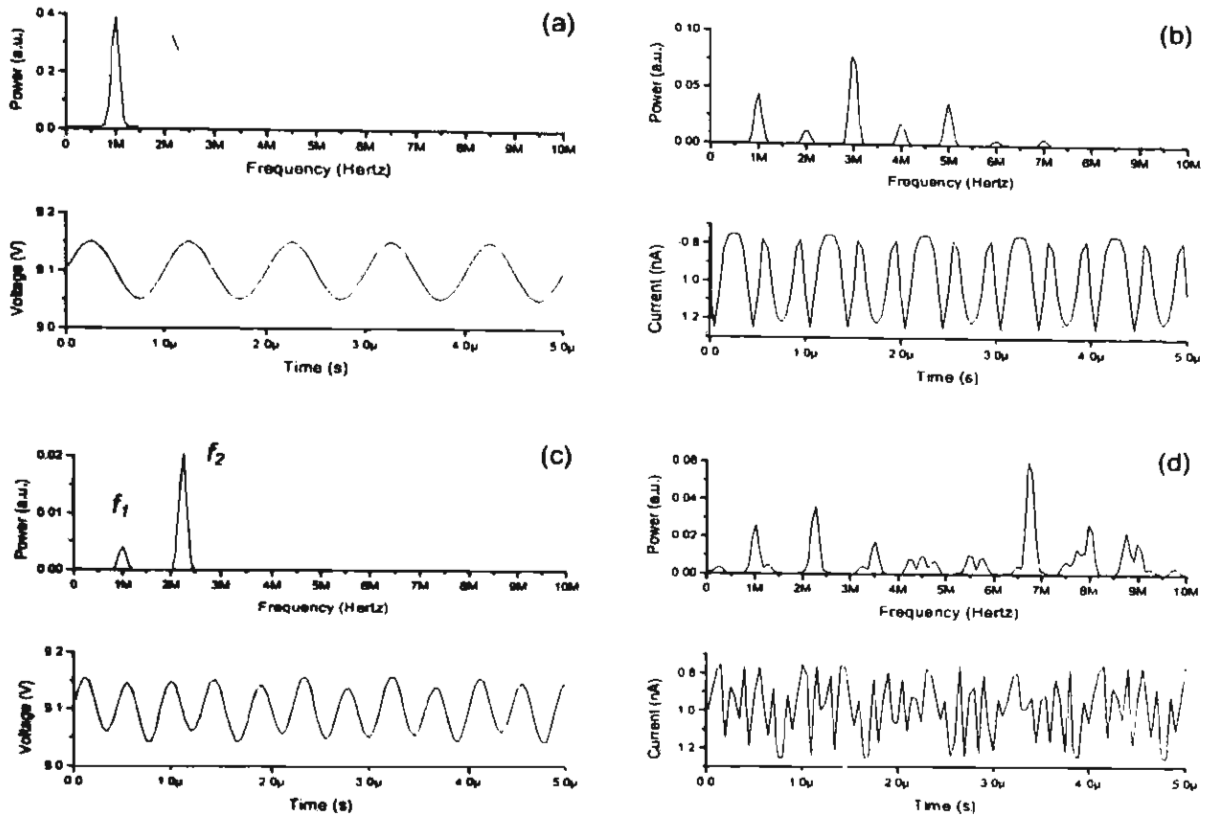

Fig. 4. The frequency (upper panel) and time (lower panel) components of the one-frequency input voltage (a) and output current (b), and the two-frequency input voltage (c) and output current (d). The time data are generated mathematically. The frequency data are obtained using fast Fourier transform.

Knowing the electrical response of the quantum dot to varying gate potential, the dot's output current can be simulated out of any mathematically-generated input voltages. Shown in Figs. 4(a) and 4(c) are mathematically-generated input voltages as a function of time with one and two principal frequencies, respectively. The upper/lower panels of each figure illustrate the frequency/time data. In the case of one-frequency input (1 MHz), the output current can be readily calculated from the equation since the input voltage is fed directly to the coupled gate. Similarly, output current from the two-frequency input (1 and 2.25 MHz) can be calculated from the same equation, with some corrections on the magnitude due to different gate-to-dot capacitance of the two gates. However, such corrections do not affect frequency data and are thus ignored. The simulated output currents from the one- and two-frequency input signals are shown in Figs. 4(b) and 4(d) respectively.

The output response, Fig. 4(b), from the one-frequency input shows that together with the principal input frequency (1 MHz) there are also several frequency components (most notably the 3 and 5 MHz peaks) which are reflected in the output current. In the two-frequency input (f_1 = 1 MHz and f_2 = 2.25 MHz), modulation of the two frequencies according to $mf_1 \pm nf_2$, where m and n are integers, is obtained. The three most strong peaks are at 6.75, 8 and 8.75 MHz which correspond to $0f_1 + 3f_2$, $4f_2 - 1f_1$ and $2f_1 + 3f_2$ respectively. Similarly, other peaks can be explained using different sets of m and n.

5. Conclusions

The sinusoidal response of I_{DS} to varying gate voltage in a quantum dot transistor provides the basis for frequency manipulation, in a quantum scale. Our semi-empirical simulations show that for one-frequency input, the QDT may function as a frequency multiplier – provided that the required frequency is singled out using a proper band-pass filter. And for two-frequency input, modulation and demodulation functions are feasible, i.e. the QDT effectively operates as a mixer. These may lead to QDTs being adopted in various analog circuits, particularly in low-power high-density applications.

References

[1] J. H. F. Scott-Thomas, S. B. Field, M. A. Kastner, H. I. Smith, and D. A. Antoniadis, "Conductance oscillation periodic in the density of a one-dimensional electron gas", *Phys. Rev. Lett.* **62**, 583 (1989).

[2] H. van Houten and C. W. J. Beenakker, Comment on "Conductance oscillation periodic in the density of a one-dimensional electron gas", *Phys. Rev. Lett.* **63**, 1893 (1989).

[3] M. A. Kastner, "The single-electron transistor", *Rev. Mod. Phys.* **64**, 849 (1992).

[4] S. Luryi, J. M. Xu, and A. Zaslavsky, *Future Trends in Microelectronics: The Road Ahead* (Wiley, New York, 1999).

[5] C. S. Lent and P. D. Tougaw, "A device architecture for computing with quantum dots", *Proc. IEEE* **85**, 541 (1997).

[6] S. Tiwari, F. Raha, H. Hanafi, A. Hartstein, E. F. Crabbe, and K. Chan, "A silicon nanocrystals based memory", *Appl. Phys. Lett.* **68**, 1377 (1996); see also, S. Tiwari, F. Raha, K. Chan, L. Shi, and H. Hanafi, "Single charge and confinement effects in nano-crystal memories", *Appl. Phys. Lett.* **69**, 1232 (1996).

[7] S. Kanjanachuchai, J. M. Bonar, and H. Ahmed, "Single charge tunnelling in n- and p-type strained silicon germanium on silicon-on-insulator", *Semicond. Sci. Technol.* **14**, 1065 (1999).

[8] N. J. Collier and J. R. A. Cleaver, "A novel dual-gate high electron mobility transistor using a split-gate structure", *Appl. Phys. Lett.* **71**, 2958 (1997).

Beyond CMOS: Single-Electron Transistors

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Abstract
Current microelectronics technology relies on continued shrinkage of transistor features. At a certain point in the miniaturization drive, conventional transistors will behave differently with different current conduction mechanisms. This paper sheds a light on how electrical conduction takes place in a nanoscale transistor.

1. Introduction

Continued miniaturization of metal-oxide-semiconductor field-effect transistor (MOSFET) technology is one of the driving forces behind the electronics industry. The semiconductor industry association has predicted that by the year 2016, the gate length will be reduced to as small as 13 nm [1]. At such small geometry, random dopant distribution in the substrate and charge impurity in the oxide are likely to cause the channel connecting the source and the drain to be irregular. This spatial variation in electrical characteristic result in regions of high and low electrical conductivity. Low conductivity region forms a barrier to charge transport. Early experiments have shown the presence of tunnel barriers along narrow conducting channel [2]. If two closely-spaced tunnel barriers are present along the channel, the confined region between the barriers can be considered as a dot or a reservoir of charges, provided the channel is populated with charges.

The principle of electrical conduction of nanometre-scale transistors differs from that of micrometre-scale transistors which are the building block of the current complementary MOS circuits. In micro-scale transistors, charge carriers are transported via the inversion layer along the channel. But in a nano-scale transistor, where a single dot is placed between source and drain, the transfer of individual electrons through the dot is possible via a nearby gate electrode; the structure is now known as a single-electron transistor [3].

2 Device structure

The structure investigated is one of gated double-barrier systems in which the source and drain regions are separated by two tunnel barriers with a small region of no larger than 100 nm, usually called a dot, in between. A nearby electrode (gate) controls the electrostatic potential of the dot, see Fig.1. The source, drain and dot are doped heavily, beyond the metal-insulator transition. However, conduction between the source and drain is impeded by the presence of the two tunnel barriers.

Each barrier is characterized by a tunnel resistance R_T and a junction capacitance C_J. When R_T is small, charge transport is due to the typical drift process. However, when R_T is larger than the quantum resistance R_k ($= h/e^2 \sim 25\ k\Omega$), charge transport across the barrier is possible via tunnelling mechanism. Since only discrete number of charges can be transported, a single negative charge (electron) or positive charge (hole) can be transferred from source to drain, and vice versa.

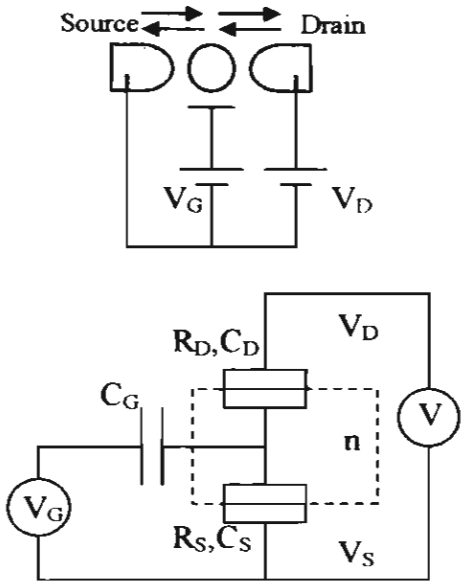

Fig. 1. The single-electron transistor and its equivalent circuit diagram. The dashed box encloses the island with n excess/deficit electrons.

3 Transport Theory

Electrical conduction theory in the double-barrier system has been widely studied. The so-called orthodox theory [4] assumes that (i) shapes and dimensions of tunnel junctions are irrelevant, (ii) the tunnelling process is instantaneous, (iii) charge redistribution after tunnelling event is instantaneous, and (iv) energy spectra of reservoirs (source, drain) including that of dots are continuous.

The current depends on the drain-source bias V and gate voltage V_G according to:

$$I(V, V_G) = e \sum_{n=-\infty}^{+\infty} p(n, V, V_G) \times [\vec{\Gamma}_s(n, V, V_G) - \overleftarrow{\Gamma}_s(n, V, V_G)]$$

where e is the electronic charge, p is the probability of having n electrons in the dot, and Γ_s is the tunnel rate across the source junction in the direction indicated by the arrow. The tunnel rate across a junction with tunnel resistance R_T is given by the golden rule [5]:

$$\overrightarrow{\Gamma_i} = \frac{1}{e^2 R_i} \times \frac{\overrightarrow{\Delta E}}{1 - \exp\left(-\overrightarrow{\Delta E} / k_B T\right)}$$

where k_B is the Boltzmann's constant, T is the temperature, and ΔE is the change in the energy after a tunnelling event.

The orthodox theory allows for an accurate calculation of current-voltage (I-V) relationship for metallic systems where high electron densities in the source and drain satisfy the assumptions above. In semiconductor systems, however, the electron energies in the dot cannot be described as continuous, but rather as discrete. The tunnel rate now depends on the discrete energy-level spacing $\Delta\varepsilon$ in the dot according to [6]:

$$\Gamma = \frac{\Delta\varepsilon}{e^2 R} \sum_{n=0}^{+\infty} \left[\left(1 + e^{a}\right) \cdot \left(1 + e^{b}\right)\right]^{-1}$$

$$\text{where} \begin{cases} a = (-\Delta E + E_o + n\Delta\varepsilon)/k_B T \\ b = -(E_o + n\Delta\varepsilon)/k_B T \end{cases}$$

where E_0 is the ground-state energy and ΔE is as defined previously.

4. Results and Discussion

Simulations undertaken can be categorized into two cases: for symmetrical and asymmetrical systems. In the former, both tunnel junctions are identical; hence, conductions under positive and negative biases are symmetrical. In the latter, more realistic, case where the two junctions differ in their resistances, or their capacitances, or both, I-V characteristics may develop a distinct feature known as Coulomb staircase resulting from the nature of charge carriers that prefer movements in only one direction. In our simulations in the latter case, the differences in junction parameters are deliberately made large, typical of lithographically-defined quantum dot systems where observations of Coulomb staircase are widely reported.

4.1 Symmetrical SET

Silicon quantum dots with lateral dimension of 50 nm can be reliably grown by molecular-beam epitaxy, or they can be fabricated by direct e-beam writing and reactive ion etching. The capacitance of such small dot is often below 1 aF and other capacitances often overwhelms the total capacitance.

Figure 2 shows the simulation result of drain current as functions of gate- and drain-to-source voltages of a quantum dot system having symmetrical junctions. Junction parameters are R_T = 50 MΩ, C_J = 50 aF and C_{Gate} = 0.16 aF. V_{GS} is swept from -2 to 2 V in 0.02-V steps. V_{DS} is swept from -3 to 3 mV in 20-μV steps. The temperature is 0.3 K. At a fixed V_{DS}, the drain current oscillates when the gate voltage is swept. Each cycle of the oscillations corresponds to an addition or a removal of a single electron to or from the dot. This can be seen at the lower left hand corner of the figure.

Another alternative representation of the above result is illustrated in the grayscale plot of Fig. 3 where high-current regions are darker than low-current regions. This diamond shape characteristic indicates that current conduction is not allowed when the device is biased in the central diamond region.

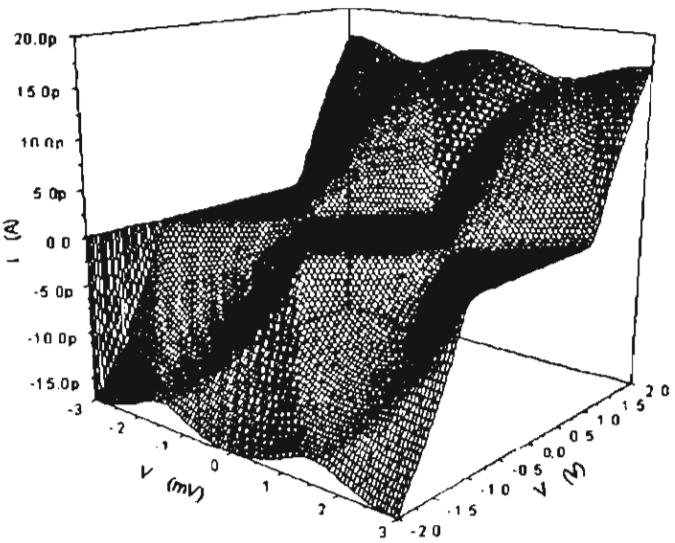

Fig. 2. Drain-to-source current (I_{DS}) of a single-electron transistor as functions of V_{DS} and V_{GS}. Tunnel junctions are identical. See text for simulation parameters.

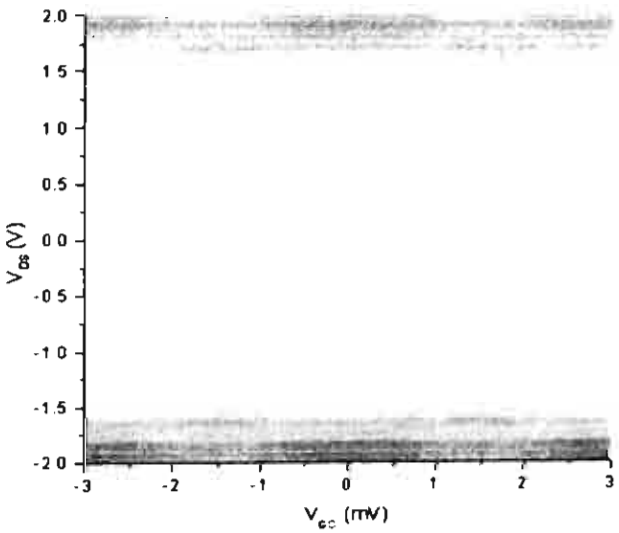

Fig. 3. Grayscale plot of Fig. 2. Low current is represented as white, high current as dark.

When electrons are concentrated in a small confined space, an addition or a removal of a single electron into or out of the space will result in the change in the electrostatic energy of the system. This energy has to be supplied or dissipated by external means, via biasing. Without sufficient energy from external biasing, the system resists the changes in its electrostatic energy giving rise to non-conducting states as seen above. This is known as Coulomb blockade phenomenon.

4.2 Asymmetrical SET

Most lithographically-defined SETs do not have identical junction characteristics as assumed above. Efforts to precisely control tunnel resistances and junction capacitances are, at best, partially successful. Reactive ion etching is useful in defining confined space with good geometrical control. However, the destructive nature of the process results in damaged sidewalls whose electrical properties (depletion layer) are not controllable. Hence, geometrically identical shapes more often do not have the same electrical characteristics.

Numerical simulations are carried out for a double-gated single-electron transistor whose junction properties differ by a factor of ten: $R_s = 10R_d = 100$ MΩ, $C_s = 10C_d = 100$ aF. The two side gates are capacitively coupled to the dot. The coupling for the two gates differ by a factor of three, a realistic figure resulting from the difference in the effective areas of the gates and the distance of each gate from the dot, which can be independently controlled during the fabrication process. The dot is assumed to have discrete energy levels, instead of a continuum as is the case in metallic systems. The energy-level spacing is 0.4 meV and the temperature is 0.3 K.

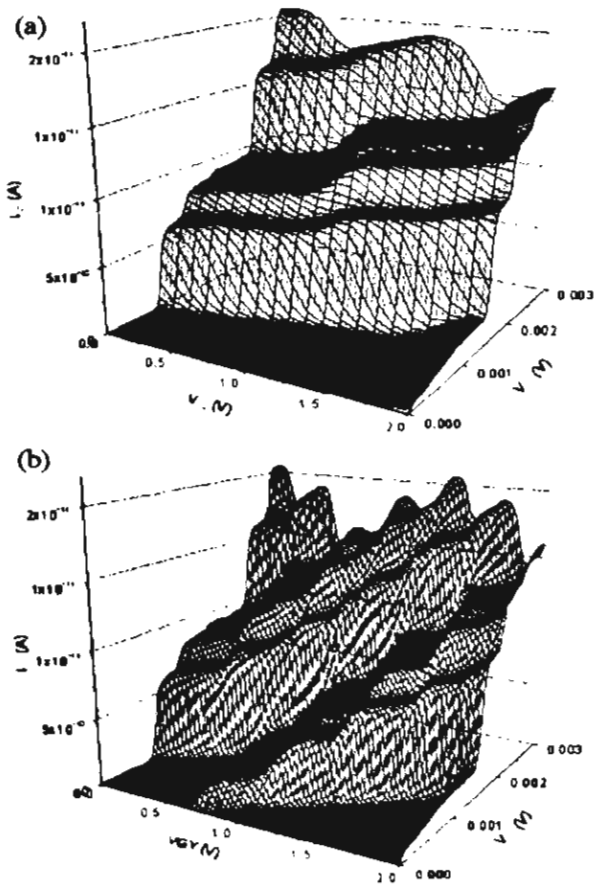

Fig. 4. Drain current plot for asymmetrical single-electron transistor as functions of V_{DS} and (a) V_{GX}, low coupling-capacitance gate voltage, and (b) V_{GY}, high coupling-capacitance gate voltage.

Figures 4(a) and 4(b) show the simulation results of the system described above when sweeping the low- and high coupling-capacitance gates (C_{GX} = 0.04 aF, C_{GY} = 0.12 aF), respectively. The figures only illustrate a fraction of the Coulomb blockade regions, and only positive bias results are shown when the blockade is lifted.

Both figures illustrate the rich feature in the I-V characteristics. The plateaux results from two sources: the discrete energy levels in the dot and the asymmetry of the tunnel junctions. The former can be varied by changing the size of the dot, while the latter is somewhat more difficult to control as explained previously.

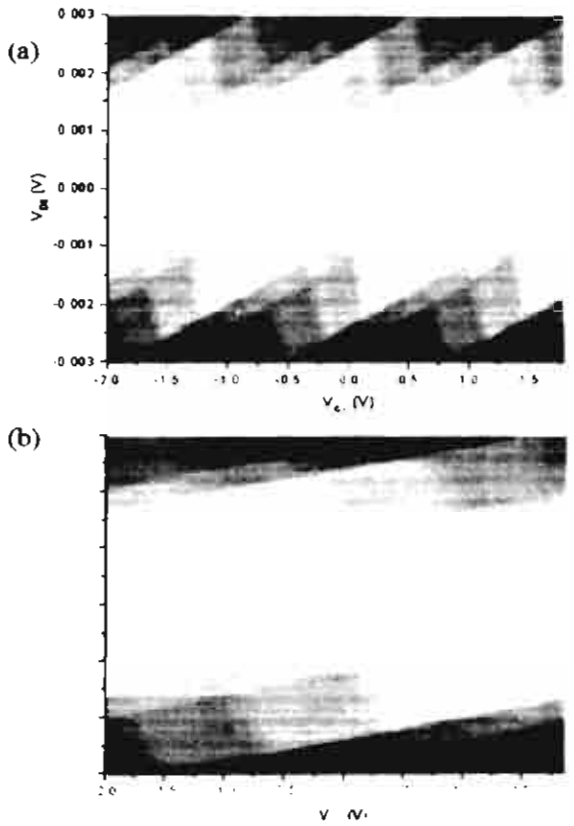

Fig. 5. Grayscale drain current plot for asymmetrical single-electron transistor as functions of V_{DS} and (a) V_{GX}, low coupling-capacitance gate voltage, and (b) V_{GY}, high coupling-capacitance gate voltage.

Corresponding results of Figs. 4(a) and 4(b) are plotted in the grayscale plots in Figs. 5(a) and 5(b) respectively. At a fixed V_{ds}, varying gate voltage results in an oscillatory change in the drain current. However, the drain-current oscillation obtained from the asymmetrical case differs strongly from the symmetrical case. In the latter case, the oscillation is almost sinusoidal in nature with a single peak in each cycle. In the former case, however, each cycle contains several peaks and troughs. In some cases, plateaux can be obtained. This may find