factor. To avoid the negative value of L_m and to guarantee a smooth change in L_m, V_{DS} in equation (19) is replaced by a smoothing function V_{DSX} [12]

$$V_{DSX} = V'_{DSAT}\left[1 + \frac{\ln\left(1+e^{A\left(V_{DS}/V_{DSAT}-1\right)}\right)}{\ln\left(1+e^{A}\right)}\right] \quad (14)$$

The expression V_{DSX} in equation (14) gives V_{DS} and V'_{DSAT} when $V_{DS} \cup V'_{DSAT}$ and $V_{DS} \subset V'_{DSAT}$ respectively. Parameter A in equation (20) is used to control the smoothness of the curve.

III. Results and Discussion

To verify the validity of the model, the model results have been compared with the experimental data[2]. The devices were fabricated with several gate lengths ranging from 0.07μm to 0.25μm with the oxide thickness of 4.5nm. Fig. 1 shows the electric field from (3)(dash line) and the electron temperature from (4)(solid line) of the 0.1 μm MOSFET for two different drain source voltages(V_{DS}=0.1V and 0.2V) respectively. As seen, higher drain source voltage results in higher electric field and thus higher electron temperature. It can be noticed that carriers take longer distance before they are in equilibrium with the lattice.

Figure 2 shows the comparison between the theoretical predictions of current voltage characteristic(solid line), the theoretical predictions without velocity overshoot[7](dash line) and the experimental data(dot)[2]. In the simulation, an effective channel doping concentration (N_A), low field mobility (μ_O), saturation velocity (v_{sat}), parasitic drain source resistance (R), smoothing factor (A) and χ are 7×10^{17} cm^{-3}, 480 cm^2/V•s, 9×10^6 V/cm, 55 Ω, 10 and 0.12 respectively. As seen, the predictions show increasing differences in the drain current with and without velocity overshoot especially for larger applied drain source voltages V_{DS}. This is attributed to the increasing electric field. For example, for the device biased at V_{GS}= 0.8V and V_{DS}= 0.6V, the drain current including velocity overshoot effect can be 29% larger than the current without velocity overshoot. The agreements between the theoretical predictions and the experimental data are well obtained over a wide range of applied gate and drain voltages.

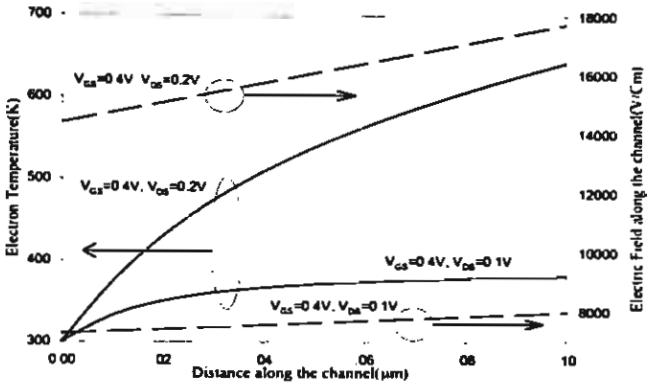

Fig. 1 Electric field and electron temperature along the channel

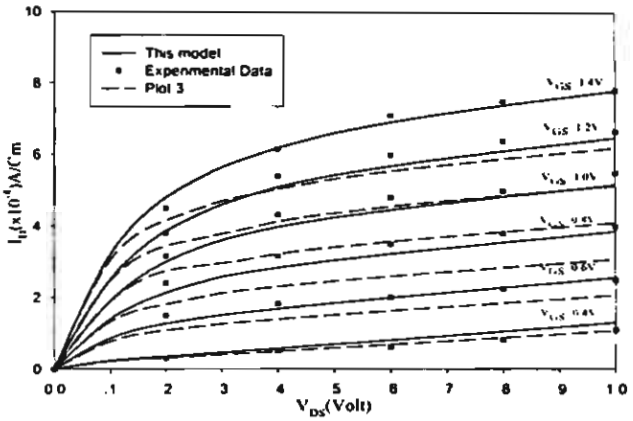

Fig. 2 I-V Characteristics

IV. Conclusion

A physics-based modeling of short channel MOSFET including velocity overshoot is presented. The model is developed based on the solution of energy balance equation. Electron temperature is analytically obtained along the channel and the thermoelectric and drift current are calculated. The model includes the effects of the mobility degradation, channel length modulation, drain induced barrier lowering and parasitic drain source resistance. The theoretical predictions of the model are compared with the experimental data and shown to be in good agreement over a wide range of biasing conditions.

ACKNOWLEDGEMENT

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A 3Volt High Frequency and Low Input Impedance CMOS Current-Mode Precision Full-Wave Rectifier

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Abstract **This paper presents a 3Volt high frequency and low input impedance CMOS current mode precision full-wave rectifier. The circuit is designed based on an improved Wilson current miller. All MOS transistors are biased at low current resulting in small power dissipation. Negative feedback has been employed to reduce the input impedance of the circuit(236Ω). HSPICE is used to perform the simulation and the result shows the frequency of operation as high as 100 MHz with a standard 0.5μm CMOS technology. The mismatch obtained from the input and rectifier's output is 0.21% for an input current of ±150μA. The DC transfer characteristic shows good linearity, very sharp corner at zero crossing point and good symmetry during positive and negative input cycle while power dissipation is 5.8μW.**

I. INTRODUCTION

PRECISION Full-Wave Rectifiers (PFWRs) are one among very important circuit building blocks for analog and digital signal processing, conditioning and instrumentation especially for low level signals. Applications include RMS to DC conversions and peak detectors. Several approaches have been proposed[1-5] to build precision rectifiers. Conventionally, precision rectifiers are based on diodes and opamps[1-2]. The rectifier however has a problem with a high distortion during the zero crossing of the input signal due to that the opamps have to recover during non-conduction/conduction transition with a finite small signal dV/dt(slew rate). The rectifiers are thus limited to a frequency performance well below the gain bandwidth product f_T of the amplifier. An improvement of the rectifier design was to use current conveyors and diodes[3-4]. The resulting circuits can operate at high frequency. However, the circuits are power hungry and quite large making them unsuitable for implementing in the large scale integrated circuit. Recently, a high performance precision rectifier has been proposed[5]. The circuit consists of only three transistors and are biased with low current resulting in low total power dissipation(4.8μW). The circuit can also operate at high frequency(100 MHz). However, the input impedance of the circuit is quite high(7.2kΩ-47kΩ) posing a problem in the current mode circuit design. In addition, the output signal is not symmetry during positive and negative input cycle.

In this paper, a high frequency low input impedance CMOS current mode precision full-wave rectifier is proposed. The circuit is designed based on an improved Wilson current miller. All MOS transistors are biased at low current resulting in small power dissipation. Negative feedback has been employed to reduce the input impedance of the circuit. The DC transfer characteristic shows good linearity, very sharp corner at zero crossing point and good symmetry during positive and negative input cycle.

II. PRECISION FULL-WAVE RECTIFIER (PFWR)

Fig. 1 shows the proposed precision rectifier. The circuit is designed based on two precision half wave rectifiers(M_{1a}-M_{5a} and M_{1b}-M_{5b}) operating alternatively during positive and negative input cycle. I_{in1} and I_{in2} are the input currents with the same magnitude but 180 degree out of phase. $M_{5a,b}$ are used to biased $M_{1a,b}$-$M_{4a,b}$ on the edge of conduction. When I_{in1} and I_{in2} flows into node a and out of node b respectively, M_{3a} cuts off while M_{3b}, which is connected as a common gate, allows the input current I_{in2} to flows through the load R_L. Same explanation is applied when I_{in1} and I_{in2} flows out of node a and into node b respectively. As a result, the circuit works as a full-wave rectifier. The input impedance of the circuit(node a and b) are very low due to the negative feedback(shunt input) with in the loop $M_{1a,b}$-$M_{4a,b}$. To demonstrate this

fact, when I_{in1} flows into node a, Voltage at node a, V_a, is pulled high. The signal V_a is amplified via M_{2a}(common source) causing voltage at the drain of M_{2a} and at the gate of M_{4a} to go low. As a result, the source voltage of M_{3a} is forced to be low. Straight forward circuit analysis shows the input impedance of the circuit given by

$$R_{in} \cong \frac{1}{g_{m1a,b} + g_{m3a,b} + g_{m2a,b}\, g_{m3a,b}(r_{o2a,b} // r_{o5a,b})} \quad (1)$$

while the output impedance is given as

$$R_{out} \cong r_{o3a,b}\left[1+g_{m2a,b}(r_{o2a,b} // r_{o5a,b})\right]. \quad (2)$$

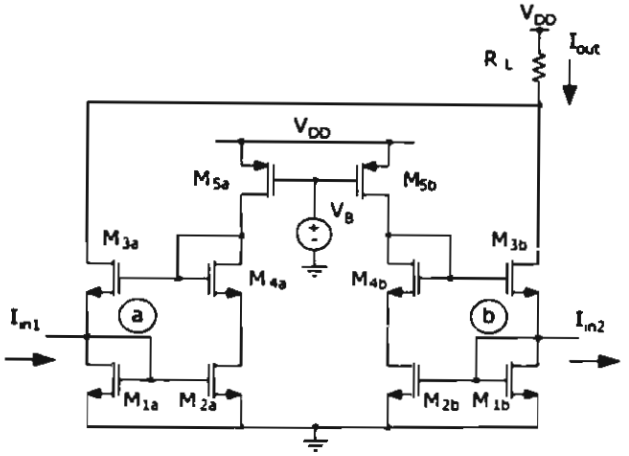

Fig. 1 Schematic diagram of the proposed precision full-wave rectifier(PFWR).

III. APPLICATION

There are many applications of the precision full-wave rectifier circuit such as RMS-to-DC converters and averaging circuits [6]. In this section, averaging current circuit is presented based on our proposed full-wave rectifier. This can be done by passing the output current after rectified to the first order low pass filter. Fig. 2 shows a simple first order low pass filter which consists of a current miller(M_6 and M_7) and a capacitor C_{AV} to control the ripple of the output current signal.

The averaging output current signal I_{AV} of the first order low-pass filter in Fig. 2 is given by

$$I_{AV} = \frac{|I_{in}|}{1 + s(C_{AV}/g_{m6})} \quad (3)$$

$$I_{AV} = \frac{|I_{in}|}{1 + s(C_{AV}/g_{m6})} \quad (4)$$

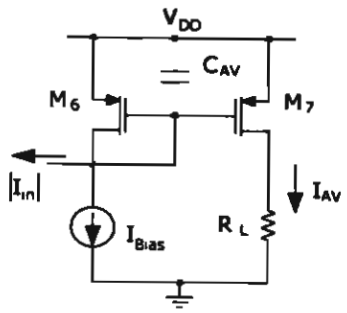

Fig 2. First order Low-pass filter

If $sC_{AV}/g_{m6} >> 1$, then I_{AV} in the s-domain and time-domain are

$$I_{AV} = |I_{in}| \frac{g_{m6}}{sC_{AV}} \quad (5)$$

$$I_{AV} = \frac{1}{T}\int_0^T |I_{in}|\,dt \quad (6)$$

respectively and T is the RC time constant equal to C_{AV}/g_{m6}.

The criterion for selecting the value of C_{AV} is that the capacitor has to be large enough to keep the residual output ripple within specified limits [6] or

$$C_{AV} >> \frac{g_{m6(\max)}}{4\pi f_{(\min)}} \quad (7)$$

where $f_{(\min)}$ is the low end of input frequency range of interest. Because g_{m6} varies as a function of the drain current I_D, $g_{m6(\max)}$ or $\sqrt{2\mu C_{ox}(W/L)_6 |I_{in(\max)}|}$ should be employed. C_{AV} should exceed the right-hand term by the inverse of the fractional ripple error that can be tolerated at the output current.

IV. PERFORMANCE OF THE PROPOSED PFWR

To verify the circuits performance, HSPICE is used to simulate the proposed circuit using a standard 0.5μm CMOS process. In this work, the bias voltage V_B is used to bias M_{5a} and M_{5b} to have the drain currents of 0.5μA. Table 1 shows all transistors' aspect ratio. Fig. 3 shows input impedance of the proposed PFWR(solid line) and that by[5](dash line). As seen, our proposed circuit has relatively much lower input impedance. To the best of authors' knowledge,

our circuit offers lowest input impedance(236Ω). Fig. 4 shows the comparison of the DC transfer characteristic of our circuit (solid line) and [5](dash line). As seen, the proposed circuit shows a sharp corner at zero crossing point and good symmetry during positive and negative input cycle while the circuit by [5] shows mismatch during positive input cycle as a result of channel length modulation of the transistor. The mismatch obtained from the input and rectifier's output in this PFWR are 0.21% for an input current of ±150μA. Fig. 5 shows transient simulation of input signal(dot), our circuit(solid line) and [5](dash line) for the input frequency of 100MHz. The results show that our circuit gives a good symmetry for both positive and negative input cycle at high frequency. The total power dissipation is 5.8μW. Fig. 6 shows averaging current as a function of time. As seen, at steady state, our output current shows 64.75μA while the theoretical output current should read 63.66μA or 1.7% error. This error is a direct result of the drain source voltage mismatch between M_6 and M_7 and can be solved by increasing the channel length of the transistors M_6 and M_7 or using cascode technique to enhance the output impedance at the output node.

Table 1 Transistor's geometrical dimensions

Device	W(μm)	L(μm)
$M_{1a,b}$ $M_{4a,b}$	0.5	0.5
$M_{5a,b}$	7	2
M_6, M_7	10	2

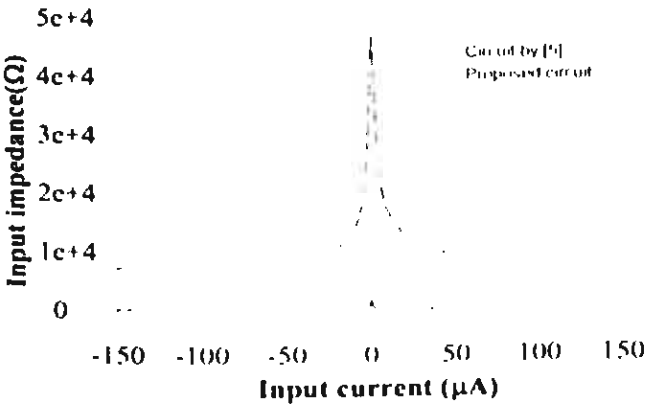

Fig. 3 Input Impedance.

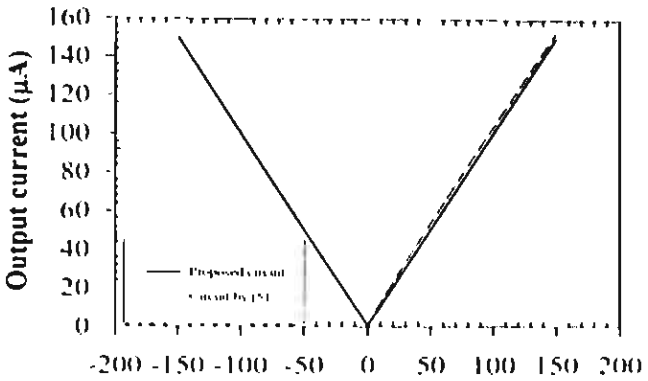

Fig. 4 DC Transfer Characteristics.

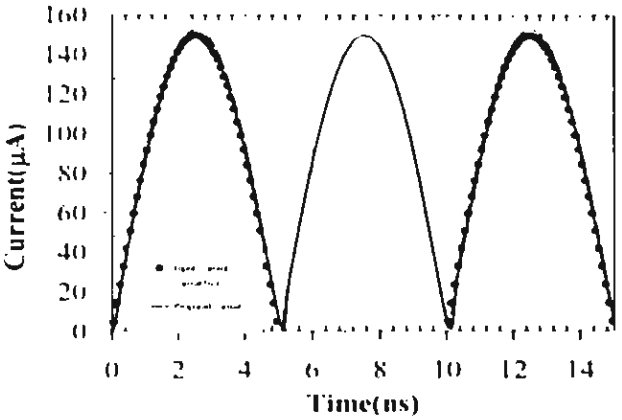

Fig. 5 Transient response (100 MHz)

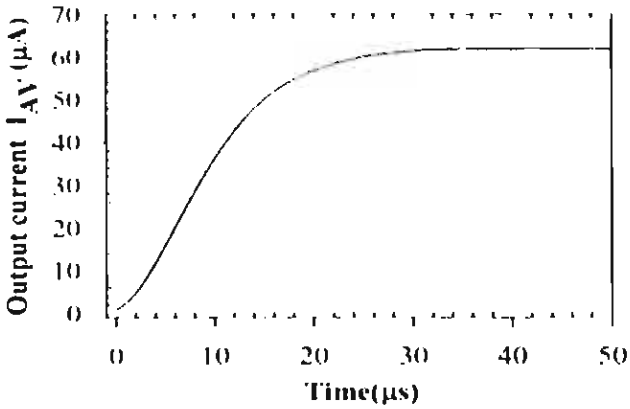

Fig. 6 Averaging current (input frequency of full-wave rectifier at 4 MHz with amplitude ±100μA, using C_{ll} 1nF)

V. CONCLUSION

A high performance current mode precision full-wave rectifier based on an improved Wilson current miller is proposed. All transistors are biased at low current resulting in small power

dissipation (5.8μW). The input impedance of the circuit is small(236Ω) and the circuit can operate at 100 MHz with only 0.21% mismatch between input and output signals for ±150μA input current.

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±1.5V HIGH PERFORMANCE CMOS RAIL TO RAIL VOLTAGE FOLLOWER

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ABSTRACT

±1.5V high performance CMOS rail to rail voltage follower is presented. The circuit is based on the symmetrical class AB voltage follower and can operate under supply voltages of ± 1.5 V. The proposed circuit has power dissipation of 5.2mW under quiescent condition and can drive ±1.25 V to 250 Ω load with a total harmonic distortion of less than 0.5 percent and cut off frequency of 237 MHz. Although simple, the proposed circuit enables the output transistors to drive load efficiently.

1. INTRODUCTION

An integrated voltage follower is one of the indispensable blocks in many analog VLSI systems. At present, most system requirements make it necessary for the follower to be able to drive low-resistance loads while, at the same time, handle large output voltage swing and maintain low harmonic distortion Several approaches have been proposed to achieve this goal [1-6] One among the most popular approaches for realizing such follower is to employ a pseudo source follower which has a pair of complementary common-source MOS transistors. A pseudo source follower has a key advantage in that it offers small output impedance. Moreover, the pseudo source follower offers a larger output voltage swing compared to a simple common drain type source follower. However, this approach suffers from the difficulty in the control of the quiescent current as a result of the random threshold voltage and high transconductance of pullup and pulldown parts. Therefore, any practical circuit using such approach needs to incorporate an additional mechanism to control the quiescent current. In addition, compensation capacitors are required to improve the stability and the transient response and thus requiring large chip area. Kadanka et al.[7] has proposed wild swing voltage follower without feedback. The circuit contains both BJTs and MOS transistors and is based on a double buffer implemented in the class AB emitter follower configuration. BJTs are employed as a core part and connected as an emitter follower due to two main reasons: 1) BJT has higher transconductance over MOS transistor, and 2) the mismatch in base-emitter voltage(ΔV_{BE}) of npn and pnp is much less than the mismatch in the gate-source voltage(ΔV_{GS}) of NMOS and PMOS. The circuit shows good dynamic performance, good stability and low power dissipation. The circuit implementation however requires BiCMOS process which has lower level of integration and higher power dissipation compared to the well known CMOS technology.

This paper presents ±1.5V high performance CMOS rail to rail voltage follower which is capable of handling large output voltage swing and maintaining low harmonic distortion. The circuit is based on the symmetrical voltage follower with additional circuit to enhance transconductance and, at the same time, reduce gate-source voltage mismatch. The circuit can operate under ±1.5V supplies and can drive ±1.25V to 250 Ω load with a total harmonic distortion of less than 0.5 percent and cut off frequency of 237 MHz. The power dissipation under quiescent condition is 5.2mW.

2. CIRCUIT DESCRIPTION

A conventional symmetrical voltage follower is shown in Fig. 1. The circuit consists of four transistors(M1-M4) connecting in the two stage common drain(double buffer) using class AB configuration. This configuration however has three main drawbacks: 1) a large offset voltage due to the mismatch between the gate-source voltage of NMOS and PMOS, 2) a high output impedance due to a reduced transconductance(g_m) of the MOS transistor compared to BJT's counterpart, and 3) a significant limitation in the linear output swing. All these problems can be alleviated using the proposed circuit shown in Fig. 2.

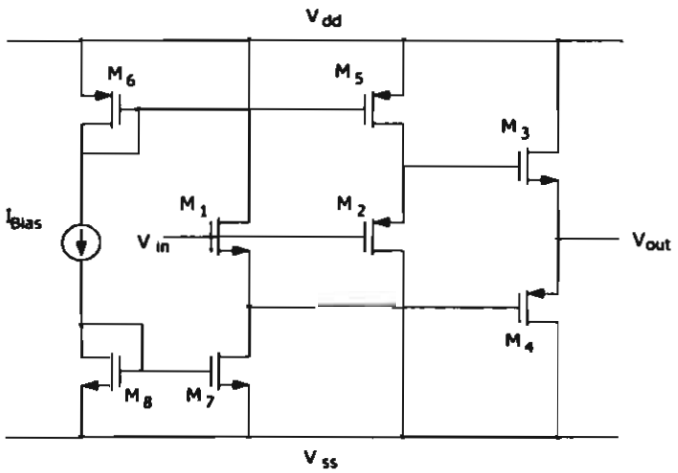

Figure 1. Conventional symmetrical voltage follower.

The proposed circuit in Fig. 2 is based on the symmetrical voltage follower described in Fig.1. The four

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transistors (M1, M3, M5 and M7) work as two stage common drain stage and are biased by current mirrors implemented by both NMOS and PMOS transistors (M2-M4 and M6-M8) with a transfer current ratio of α(see Fig.2). Since M1 has the same drain current as M2 and M3 has the same drain current as M4, the gate-source voltages of M1 and M3 are then nearly equal provided that all NMOS have the same dimensions and all PMOS have the same dimensions. This gate-source voltage matching approach is also applied to the upper follower (M5-M8). As a result, the offset voltage of the voltage follower has been minimized[8]

The transconductance of the output MOS transistors can be increased by using two compound transistors as suggested in [8] consisting of M1-M4 and M5-M8. The transconductance of the lower follower (M1-M4) and upper follower (M5-M8) are given by Eqs (1a) and (1b) as

$$g_{m(LOWER)} = \frac{g_{m1} \cdot g_{m3}}{g_{m1} - \alpha \cdot g_{m3}} \qquad (1a)$$

$$g_{m(UPPER)} = \frac{g_{m5} \cdot g_{m7}}{g_{m5} - \alpha \cdot g_{m7}} \qquad (1b)$$

respectively.

From Eqs.(1a) and (1b), the transconductance of output transistors can be adjusted through the transfer current ratio α. The simulation shows that proper value of α can result in very high transconductance

For the input voltage with the amplitude in between V_{LOW} and V_{HIGH}, the circuit will operate as a conventional voltage follower with an enhanced transconductance and the reduced gate-source voltage

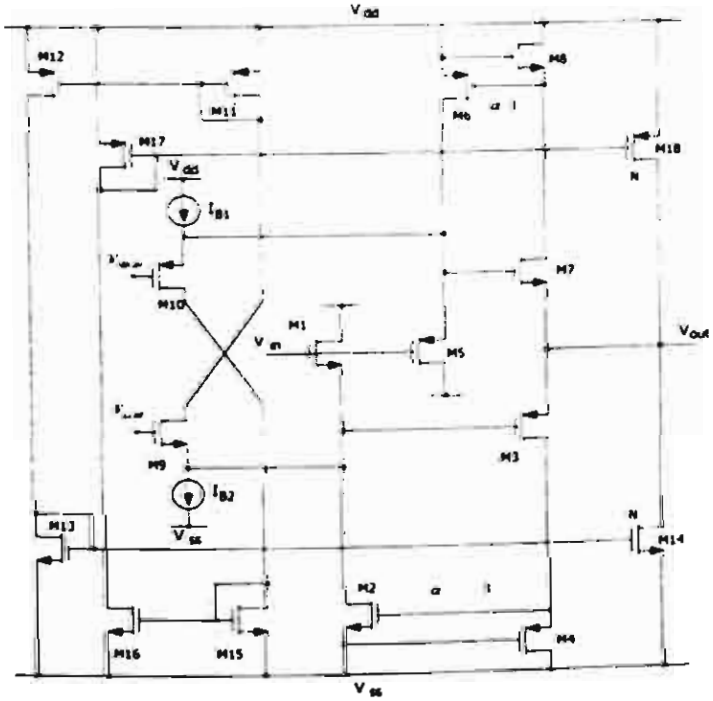

Figure 2. Proposed rail to rail voltage follower

mismatch. By using Eqs.(1a) and (1b), the output impedance of the circuit is given by

$$R_O = \left(\frac{1}{g_{m3}} - \frac{\alpha}{g_{m1}}\right) \Big\| \left(\frac{1}{g_{m7}} - \frac{\alpha}{g_{m5}}\right) \qquad (2)$$

If the input voltage is lower than V_{LOW}, the bias current I_{B2} for both transistors M1 and M9, which are connected as a differential amplifier, mostly becomes the drain current of M9 and is mirrored by two current mirrors M11-M12 and M13-M14. M14, which has its width N-times that of M13, now acts as bias current for the upper voltage follower(M5-M8). The output is capable to swing within one overdrive (V_{DSAT14}) of the negative supply with the output impedance $R_{O(LOW)}$ given by $1/g_{m7} - \alpha/g_{m5}$. Similarly, if the input voltage is higher than V_{HIGH}, the bias current I_{B1} for transistors M5 and M10, which are connected as a differential amplifier, mostly becomes the drain current of M10 and is mirrored by two current mirrors M15-M16 and M17-M18. M18, which has its width N-times that of M17, now acts as bias current for the lower voltage follower (M1-M4). The output in this case is capable to swing within one overdrive (V_{DSAT18}) of the positive supply with the output impedance $R_{O(HIGH)}$ given by $1/g_{m3} - \alpha/g_{m1}$.

A low quiescent current of the circuit are obtained by properly selecting biasing currents I_{B1} and I_{B2} and two bias voltages V_{HIGH} and V_{LOW}. We have chosen the V_{HIGH} and V_{LOW} to be 0.5 V and -0.5 V and I_{B1} and I_{B2} to be 10 μA respectively. The quiescent current as a result is found to be 550 μA.

3. EXPERIMENTAL RESULTS

To evaluate the performance of the proposed circuit, the simulation is performed using HSPICE with a standard twin well 0.6 μm CMOS technology. All W/L values of the transistors used in the circuit are summarized in Table I. It is noted that the mobility of the electron in this process is approximately four times that of hole and the transfer current ratio α used in this work is around 1/8. The simulations results show high performance characteristics, namely low output impedance, low harmonic distortion, large linear output voltage swing, wide bandwidth and low power dissipation. The proposed voltage follower is connected to drive ±1.25 V to 250 Ω load and the highest output impedance of the circuit is found to be less than 3.8 Ω while the harmonic distortion is less than 0.5 percent. ors Figure 3 shows DC transfer characteristics of the circuit with the same load. Dotted and solid lines represent input and output waveform respectively. As seen, the output can trace the input over a wide range linearly. Figure 4 show output waveform of the circuit with the input signal is 1kHz at $1.5V_{P-P}$. Figure 5 shows a frequency response of the circuit. The cut off frequency is found to be 237MHz. Figure 6 shows the output impedance of the proposed follower. It can be seen that low output impedance can be obtained. in the range of operation (±1.25V) with maximum value of 3.8Ω. Figure 7 show the THD versus the input voltage for 1kHz sinusoidal signal. The power dissipation is 5.2mW under quiescent condition.

4. CONCLUSIONS

±1.5V high performance CMOS rail to rail voltage follower is presented. The circuit is based on the symmetrical class AB voltage follower and can operate under supply voltages of ± 1.5 V. The proposed circuit has power dissipation of 5.2mW under quiescent condition and can drive ±1.25 V to 250 Ω load with a total harmonic distortion of less than 0.5 percent and cut off frequency of 237 MHz. The maximum output impedance is less than 3.8 Ω. Although simple, the proposed circuit enables the output transistors to drive load efficiently.

Table 1. Aspect ratio of transistors

Transistors	Aspect Ratios (*W/L*)
M1,M2,M9	55/1
M3,M4	750/0.6
M5,M6,M10	220/1
M7,M8	450/0.6
M11,M12,M17	4.6/1
M13,M15,M16	1.2/1
M14	380/0.6
M18	1305/0.6

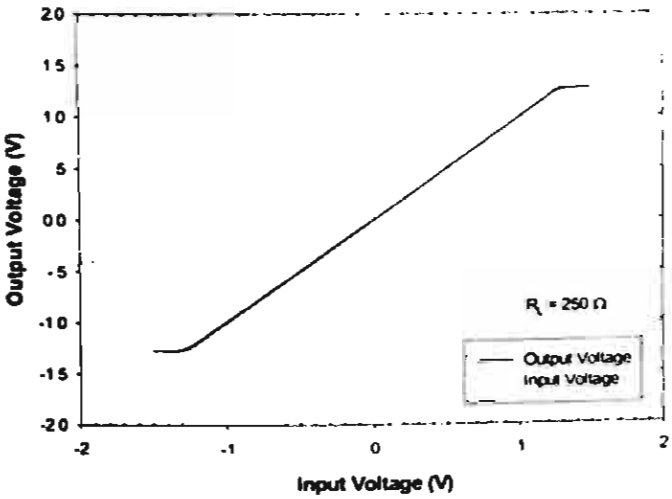

Figure 3. DC transfer characteristics

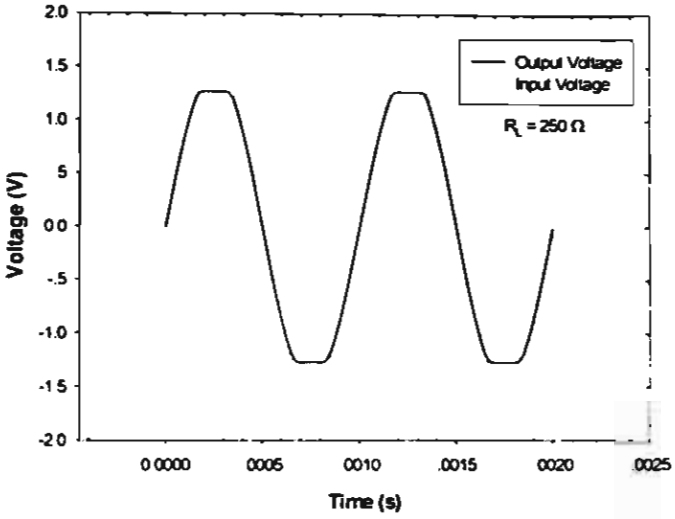

Figure 4. Output waveform

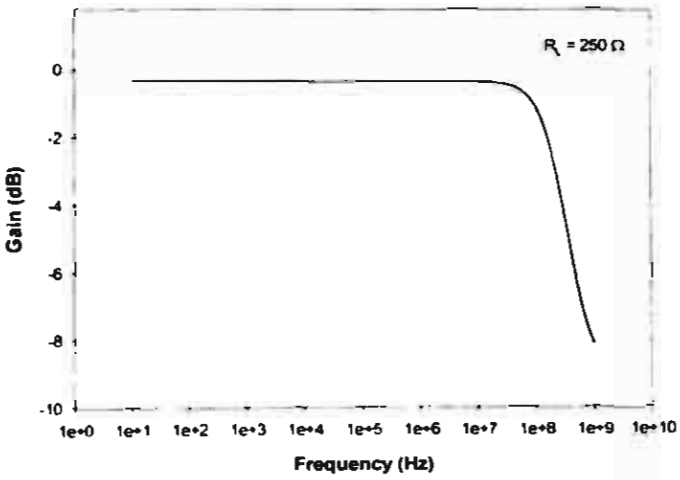

Figure 5. Frequency response of the proposed follower

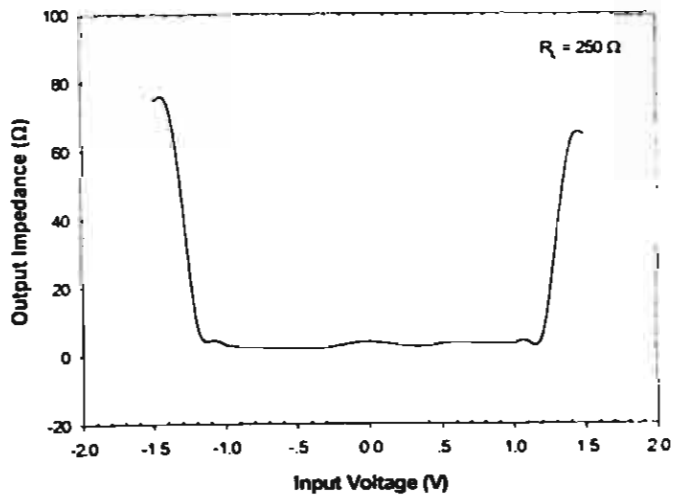

Figure 6. Output impedance

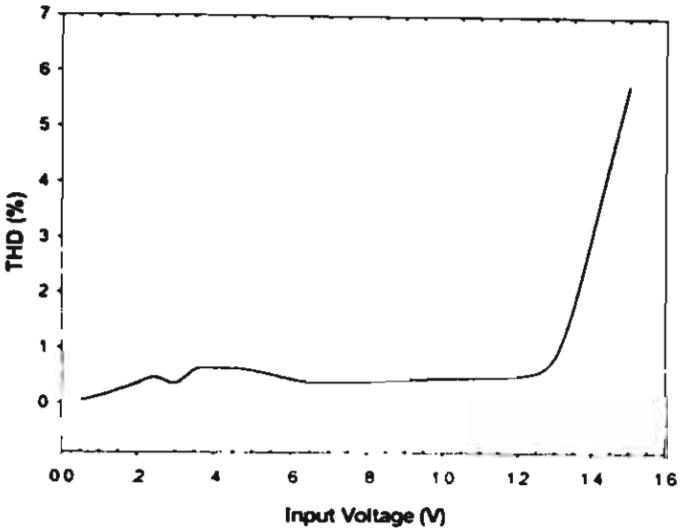

Figure 7. Total harmonic distortion (THD)

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A Physics-Based Bidirectional Model of Hot-Carrier-Induced nMOSFET Degradation Based on Exponential Interface State Profile

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***Abstract*— A bidirectional DC model of n-MOSFET using exponential interface state profile is proposed. The model employs single physically based exponential expression to describe localized distribution of the interface states along the channel. The saturation voltage as a function of a position along the channel due to localized interface states is taken into account. Several short-channel effects including vertical and lateral field degradations, saturation velocity, parasitic source-drain resistances, channel length modulation are included. The predictions of the model agree well with the experimental data.**

I. INTRODUCTION

At present, MOS device size has been scaled down without proportional reduction of supply voltages resulting in very high electric field especially near the drain end. Such high electric field creates hot carriers causing long term reliability concerns of the device operation. One of the main concerns is the injection of high energy electrons resulting in localized interface trap generation.

Several attempts [1-5] have been proposed to model the device degradation due to interface trapping N_{it}. Hsu et al.[2] employed uniform distribution of N_{it} throughout the channel while Chung et al [3] used uniform distribution of N_{it} only in the high field region(near the drain). The model accuracies are questionable as the interface trapping generation is a direct result of hot carriers which is caused by high electric field. It is well known that the electric field is not constant but increasing in the cosine hyperbolic trend [7] near the drain and thus uniform distribution is questionable. Chen et al. [1] and Leblebici et al.[4] proposed spatial dependent $N_{it}(y)$ in the linear form in damaged region and assumed zero elsewhere. In their model, such spatial dependent $N_{it}(y)$ has been however averaged to simplify the drain current expression and therefore the localized effects of $N_{it}(y)$ are not properly accounted for. In addition, two expressions are used to describe interface state profile causing a discontinuity in the model. Quader et al.[5] proposed the bidirectional model based on a uniform interface state in the high field regions. The uniform distribution is questionable as stated previously. The mobility as a function of $N_{it}(y)$ is again assumed average value. In addition, the current deviation from the pre-stressed device is calculated using superposition principle which is invalid since effects of the interface states from source and drain ends are not completely uncorrelated.

In this paper, a bidirectional DC model of n-MOSFET using exponential interface state profile is proposed. The model employs single exponential expression to describe localized distribution of $N_{it}(y)$ making the prediction results continuous. The model does not assume any average value and thus fully accounts for localized effects of $N_{it}(y)$. The saturation voltage as a function of a position in the channel due to localized $N_{it}(y)$ is taken into account. The resulting model provides physical explanation of the drain current degradation.

II. MODEL

In this work, single expression of the interface state profile is employed and given as

$$N_{it}(y) = N_{its0} \cdot e^{(-y/\gamma_s)} + N_{itd0} \cdot e^{(y-L)/\gamma_d} \qquad (1)$$

where y, L, N_{its0} and N_{itd0} are location along the channel, channel length, interface state densities at the source and drain ends respectively. γ_s and γ_d are fitting parameters used to determine the shape of the interface state profile as shown in Fig. 1. As seen, the interface state at drain and source ends are described using single physically based exponential expression and thus the problem of the discontinuity in the current voltage characteristic created by interface state profile has been avoided. Eq. (1) will be used in developing DC model instead of employing an average value as conventionally done in other research works[1-5] and therefore the localization of interface state is taken into account properly.

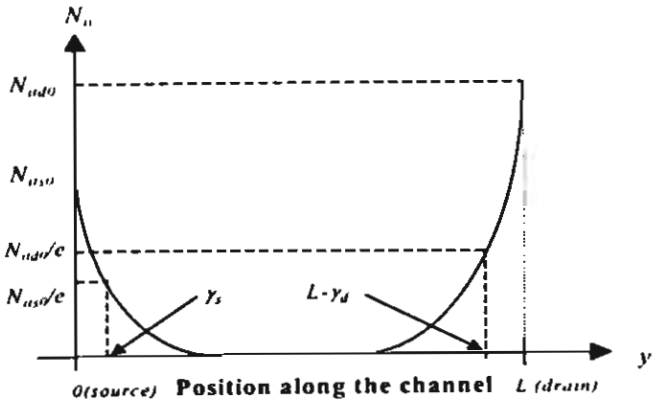

Fig. 1 Interface state distribution profile.

The drain current of the hot-carrier-induced MOSFET is

$$I_D = WQ_m(y)v(y) \qquad (2)$$

where W, $Q_m(y)$ and $v(y)$ are channel width, charge density and drift velocity given by

$$v(y) = \frac{\mu_{eff}}{(1 + KN_{it}(y))(1 + \frac{E_c}{E_c(y)})} \cdot E_c$$

and $$\mu_{eff} = \frac{\mu_0}{1 + \theta(V_{gs} - V_{TH})}$$

μ_0, E_c, θ and K are low field mobility, lateral electric field, vertical mobility degradation factor and fitting parameter accounting for the mobility degradation due to interface state. $E_c(y)$ is critical electric field given by $E_{c0}/1+KN_{it}(y))$ and E_{c0} is critical electric field of the pre-stressed devices[1].

The charge density $Q_m(y)$ is[1]

$$Q_m(y) = C_{ox}(V_{gs} - V_{TH} - 2a_0 V(y) - \Delta V_{FB}(y)) \qquad (3)$$

where C_{ox}, V_{TH}, a_0, $V(y)$ and $\Delta V_{FB}(y)$ are capacitance, threshold voltage, a Taylor's series correction factor, channel potential and localized flat band voltage variation as a result of interface state given by $q N_{it}(y) C_{ox}$ respectively

Substituting (1) into $q N_{it}(y) C_{ox}$ for $\Delta V_{FB}(y)$ and $Q_m(y)$ and $v(y)$ into (2) and integrating the result from the source to the drain ends yield the drain current in the linear region, I_{DL}, as

$$I_{DL} = \frac{W\mu_{eff}C_{ox}\left[(V_{gs} - V_{TH} - a_0 V_D - a_0 V_S - q A_1(L_{eff})/C_{ox})V_{DS} - a_0(V_D^2 - V_S^2) - q A_2(L_{eff})/C_{ox}\right]}{L + KA_1(L_{eff}) + V_{DS}/E_c} \qquad (4)$$

where

$$A_1(L_{eff}) = -\gamma_1 N_{it0}(k_1 - 1) + \gamma_2 N_{it} \left[k_2 \exp(L/\gamma_2) - \exp(-L/\gamma_2)\right]$$

$$A_2(L_{eff}) = \gamma_1^2 N_{it0}\left(1 - (\frac{L_{eff}}{\gamma_1} + 1)k_1\right) + \gamma_2^2 N_{it0}\left(1 + (\frac{L_{eff}}{\gamma_2} - 1)k_2\right)\exp(-L/\gamma_2)$$

$$A_3(L_{eff}) = \frac{\eta_1}{L_{eff}} A_1(L_{eff}) + 2\frac{(1-\eta_1)}{L_{eff}^2} A_2(L_{eff})$$

$$k_1 = \exp(-L_{eff}/\gamma_1), \quad k_2 = \exp(-L_{eff}/\gamma_2)$$

and L_{eff} is the channel length L. The value of L_{eff} (see Fig. 2) will be modified to L-l_d when device operates in the saturation region(discussed later). As seen, the current expression in (4) is a simple analytical expression and derived based local interface state in (1) without using an average value, $\bar{N}_{it}$.

The drain current in (4) assumes zero parasitic drain R_d and source resistances R_s. Such assumption is invalid especially for very short channel devices. To account for this effects, one can use the fact that $V_{gs} = V_{GS} - R_s I_{DL}$, $V_D = V_D - R_d I_{DL}$ and $V_s = V_S + R_s I_{DL}$ where V_{GS}, V_D and V_S are actual applied voltages.

The drain current in (4) including R_d and R_s is therefore given by

$$I_{DL} = \frac{-B_2 - \sqrt{B_2^2 - 4B_1B_3}}{2B_1} \qquad (5)$$

where

$$B_1 = (R_s + R_d)\left\{\frac{1}{E_{c0}} + W\mu_{eff}C_{ox}(R_s - a_0(R_d - R_s))\right\}$$

$$B_2 = W\mu_{eff}C_{ox}\left\{\frac{q}{C_{ox}}(R_s + R_d)A_2(L_{eff}) + 2a_0(R_s \cdot V_S + R_d \cdot V_D) - R_s(V_{DS}) + (V_{GS} - V_{TH})(R_s + R_d)\right\} - (L + K \cdot A_0(L_{eff}) + \frac{V_{DS}}{E_{c0}})$$

$$B_3 = W\mu_{eff}C_{ox}\left\{(V_{GS} - V_{TH})(V_{DS}) - a_0(V_D^2 - V_S^2) - \frac{q}{C_{ox}}(V_{DS})A_2(L_{eff})\right\}$$

When the drain voltage V_{ds} is increased upto the onset of saturaton voltage, V_{dsat0}, electron at the drain end moves with the saturation velocity, v_{sat}, and the device is known to operate at the onset of the saturation region. If V_{ds} is greater than V_{dsat0}, the point where electron moves with saturation velocity moves toward the source end and known as channel length modulation. In this case, device can be divided into two sections. The first section extends from the source end to the velocity saturation point, L_{eff}, which has channel potential of $V_{dsat}(L_{eff})$. The second section extends from the velocity saturation point to the drain end and is given by modulation length l_d.

One can find the drain current in the saturation region by substituting (3) into (2) with $v(y)$ replaced by v_{sat} as

$$I_{DS} = WC_{ox}(V_{gs} - V_{TH} - 2a_0 \cdot V_{dsat}(L_{eff}) - \Delta V_{FB}(L_{eff}))v_{sat} \qquad (6)$$

To compute $V_{dsat}(L_{eff})$, one has to replace V_{ds}, V_d, V_s in (4) by $V_{dsat}(L_{eff})$, $V_{dsat}+I_{DS}R_s+V_S$ and $V_S+I_{DS}R_s$ respectively and equating the result to (6) to yield

$$V_{dsat}(L_{eff}) = (-H_2 - \sqrt{H_2^2 - 4H_1H_3})/(2H_1) \qquad (7)$$

where

$$H_1 = -2a_0\rho\left(\frac{1}{E_{c0}} + W\mu_{eff}C_{ox}R_s(1 + 2a_0) + W\mu_{eff}C_{ox}a_0\right.$$

$$H_2 = \rho\left[V_{GS} - V_{TH} - q\frac{N_{it}(L_{eff})}{C_{ox}}\right]\left[\frac{1}{E_{c0}} + W\mu_{eff}C_{ox}R_s(1 + 2a_0)\right] - 2a_0\rho\left[L_{eff} + K \cdot A_0(L_{eff})\right] - W\mu_{eff}C_{ox}\left[V_{GS} - V_{TH} - 2a_0 V_S - \frac{q}{C_{ox}}A_2(L_{eff})\right],$$

$$H_3 = \rho\left[V_{GS} - V_{TH} - \frac{qN_{it}(L_{eff})}{C_{ox}}\right]\left[L_{eff} + K \cdot A_0(L_{eff})\right]$$

$$\rho = \frac{WV_{sat}C_{ox}}{1 + WV_{sat}C_{ox}R_s}.$$

To evaluate (6) and (7), one needs to know the value of L_{eff}. This L_{eff} can be obtained by applying a quasi two dimensional approximation (QTDA) to rectangular Gaussian box (shaded area in Fig. 2) in the second section including interface state given in (1) yields

$$\varepsilon_{ox}\int_0^W\int_0^{X_j - L_{eff}} E_c(L_{eff})dxdz - \varepsilon_{ox}\int_0^A\int_0^W E_{ox}(y')dy'dz \qquad (8)$$
$$-\varepsilon_{ox}\int_0^W\int_0^{X_j - L_{eff}} E_c(y')dxdz = \int_0^W\int_0^W\int_0^{X_j - L_{eff}} (Q'_m + Q'_d + Q'_{it})dxdy'dz$$

$$V_{ds} = V_{dsat}(L_{eff}) + \frac{q}{C_{ox}}\left(N_{it}(L_{eff}) + \left\{ \frac{\exp(l_d/l - l_d/\gamma_d)}{(\gamma_d - l)} - \frac{\exp(l_d/\gamma_d - l_d/l)}{(\gamma_d + l)} \right\} \cdot \frac{l \cdot N_{itd0}}{2} + N_{itd0} \cdot \gamma_d^2 / (l^2 - \gamma_d^2) \right.$$
$$\left. + (e^{-l_d/l} \cdot N_{itd0} \cdot \gamma_d^2)/(l^2 - \gamma_d^2) - \left\{ \frac{\exp(-l_d/l - L_{eff}/\gamma_s)}{(l - \gamma_s)} + \frac{\exp(l_d/l - L_{eff}/\gamma_s)}{(l + \gamma_s)} \right\} \cdot \frac{l \cdot N_{itso}}{2} \right)$$
$$+ E_c \cdot l \cdot \sinh(l_d/l) \quad \text{where} \quad l = \sqrt{\frac{\varepsilon_{ox} X_j}{\lambda C_{ox}}} \tag{9}$$

where X_j is junction depth and λ is a fitting parameter. Differentiating (8) with respect to y' and z gives a second order differential equation which can be solved subjected to proper boundary conditions, $E_y(y'=0) = E_c$ and $V(y'=l_d) = V_{ds}$, to give (9).

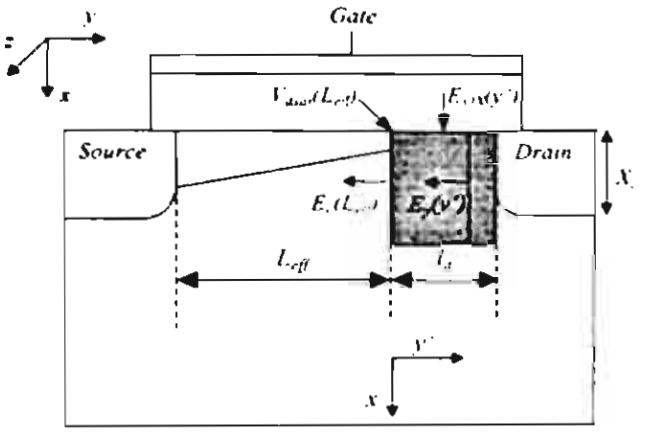

Fig. 2 Cross section of MOSFET and Gaussian box

As seen, (9) has one unknown, i.e. l_d, and can be found using Newton-Raphson method. We found that l_d is obtained after a few iterations (less than 12 iterations with initial guessed l_d computed without interface states). It is instructive to note that the potential at the point of saturation velocity, $V_{dsat}(L_{eff})$, is not a constant. This is partly due to the fact that the interface state is changing along the channel.

Fig. 3 shows $V_{dsat}(L_{eff})$ as a function of V_{DS} from the proposed model. The fitting parameters N_{itd0}, K and γ_d are 4.5×10^{11} cm^{-2}, 4.9×10^{12}cm and 5.1×10^{-6}cm respectively. As seen, our model gives continuous curve while it was shown discontinuous in Chen et al.[1]. Such discontinuity in $V_{dsat}(L_{eff})$ can cause discontinuity of the final drain current.

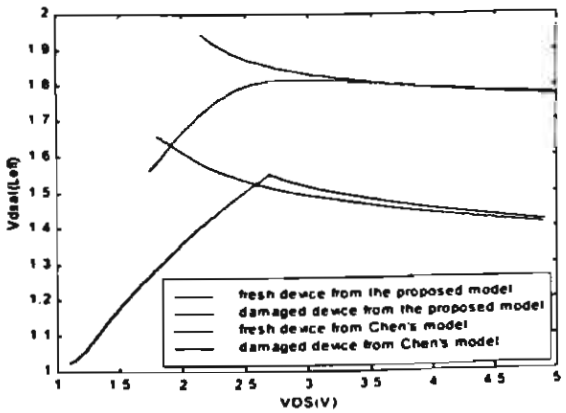

Fig. 3 Saturation voltages $V_{dsat}(L_{eff})$ as a function of V_{DS} from the proposed model compared to Chen et al.[1], at V_{GS} = 5 V.

III. Results and Discussion

The model results have been compared with the experimental data[4]. The device has the channel length L and width W of 1μm and 10μm. Gate oxide thickness t_{ox} is 20nm. Effective substrate doping concentration N_a is 5.0×10^{16}cm^{-3}. μ_0, v_{sat}, θ, a_0, λ, R_s and R_d are 633cm^2/Vs, 8.4×10^6cm/s, 0.11V^{-1}, 0.58, 3.35 and 35Ω respectively. Because the post-stress device is performed in one direction, N_{its0} is therefore zero while N_{itd0} is 4.5×10^{11} cm^{-2}. K and γ_d are 4.9×10^{12}cm and 5.1×10^{-6}cm. Fig. 4 shows a comparison of pre- and post-stress current-voltage characteristic. As seen, a good agreement between the predictions from this model and the experimental data [4] over a wide range of biasing conditions is obtained. It is noticed that the effect of the interface state is obvious in the linear region while it is negligible in the saturation region. This is because the modulation length l_d increases for an increasing V_{DS} making the effect of the interface state, mostly located near the drain, less pronounced.

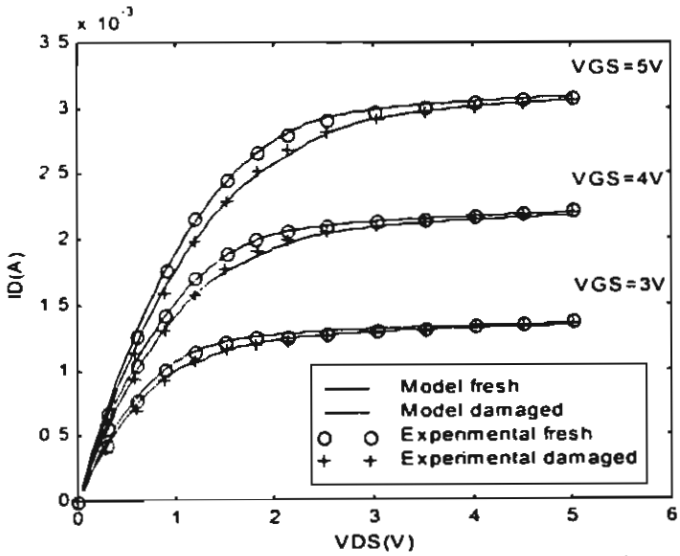

Fig. 4 Comparison of pre- and post- stress I_D-V_{DS} characteristic. Degraded device (W = 10 μm, L = 1 μm, t_{ox} = 20 nm) was stressed at V_{DS}=6.5V, V_{GS} = 2.6 V for 423 hours [4].

Our model can be extended to include the effect of time dependent degradation (age). To calculate generation of interface state, one can use ΔN_{it} generation expression [6]

$$\Delta N_{it} = C\left[t \frac{I_d}{W} e^{-\phi_{it}/qlE_m} \right]^n \tag{10}$$

where C and n are fitting parameters. λ, ϕ_{it} , E_m and t are electron mean free path, critical energy that electron possess to create interface state(3.7 eV), maximum lateral electric field in the channel and time for this stressing respectively. The generated ΔN_{it} is then used in the purposed model to predict the drain current for a given stressing time.

IV. Conclusions

A physics-based bidirectional model of n-MOSFET including interface state effects is proposed. The model does not use an average value of $N_{it}(y)$ and thus localized effects are accounted for properly. Single physically exponential interface state expression is used in developing model making model continuous over a wide range of biasing conditions. The predictions of the model agree well with the experimental data[4]

V. Acknowledgement

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ภาคผนวก ข

สำเนาบทความงานวิจัยที่ยังคงต้องรอผลการพิจารณาตอบรับ

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AN ANALYTICAL MODEL OF SHORT CHANNEL MOSFET INCLUDING VELOCITY OVERSHOOT

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Index Terms MOSFET devices, velocity overshoot.

Abstract In this paper, an analytical model for short channel MOSFET including velocity overshoot is proposed. The model is developed based on the solution of energy balance equation under the assumption of displaced Maxwellian distribution. The resulting mobility model is an augmented version of a conventional mobility model and all parameters involved are physical parameters. The model also includes the effects of the mobility degradation, channel length modulation, drain induced barrier lowering(DIBL) and parasitic drain source resistance. The theoretical predictions of the model are compared with the experimental data and shown to be in good agreement over a wide range of bias conditions.

I. INTRODUCTION

Velocity overshoot is becoming more prominent as MOSFET dimension reduced to the deep submicron regime(Ono et al. 1995, Sai-Halasz et al. 1988). This non local effect is a result of the carrier transit time that becomes comparable with the energy relaxation time. As a result, the field dependent mobility model assuming equilibrium with the lattice is not suitable for modeling the deep submicron devices. Several approaches(Kan et al. 1991, Tang et al. 1993, Sim 1995, Roldan et al. 1997, Kolhatkar and Dutta, 2000) have been proposed to take into account this nonlocal effects. The work by Kan et al. (1991) included the thermoelectric current to account for the velocity overshoot. The model is developed based on perturbation analysis on the carrier temperature using the energy balance equation. Tang et al. (1993) developed an improved hydrodynamic transport model. Both models however require numerical calculation making the models unsuitable for circuit simulator due to inefficient computation time. Sim (1995) has solved the energy balance equation incorporated with the drift-diffusion equation analytically. However the linear approximation is made on the integration of the thermoelectric current limiting the model validity. In addition, the current voltage characteristic has to be computed iteratively to include the effect of the parasitic drain and source resistance. Roldan et al. (1997) proposed the analytical model using augmented drift-diffusion velocity model. The model does not take into account parasitic drain source resistance. The transconductance has also been calculated but the model assumed no channel length modulation. Kolhatkar and Dutta et al. (2000) has proposed the analytical model including velocity overshoot effect using augmented drift-diffusion equation similar to that proposed by Roldan et al. (1997). The model however is valid for drain voltage less than the saturation voltage limiting the validity of the model. The derived transconductance is therefore limited to small drain voltages.

In this paper, an analytical model for short channel MOSFET including velocity overshoot is proposed. The model is developed based on the solution of energy balance equation under the assumption of displaced Maxwellian distribution. The resulting mobility model is an augmented version of a conventional mobility model and all parameters involved are physical parameters. The model also includes the effects of the mobility degradation, channel length modulation, drain induced barrier lowering and parasitic drain source resistance. The theoretical predictions of the model are compared with the experimental data with several gate lengths ranging from 0.07μm to 0.25μm and shown to be in good agreement over a wide range of bias conditions

II ANALYTICAL MODEL

The energy balance equation is written as(Lundstrom 1990)

$$J_n E = \nabla F_w + \frac{3}{2} nk \frac{T_e - T_O}{\tau_e} \tag{1}$$

where J_n and F_w are device current density and energy flux and given by

$$J_n = nq\mu E + qD_n \nabla n + \mu kn \nabla T_e \tag{2}$$

$$F_w = -\frac{5}{2}\frac{kT_e}{q}J - \frac{k^2}{q}n\mu T_e \nabla T_e, \tag{3}$$

k, T_e, T_O, τ_e, $\mu = (\mu_O T_O)/(\theta T_e)$, μ_O and θ are Boltzmann constant, electron temperature, lattice temperature, energy relaxation time, temperature dependent electron mobility, low field mobility, vertical mobility degradation coefficient given by $\theta = 1 + \theta_A (V_{GS} - V_T) + \theta_B V_{SB}$ where θ_A and θ_B account for degradation due to gate and body voltages respectively. Note that the first term on the right hand side(RHS) of equation (1) represents the gradient of energy flux while the second term represents the energy transferred from electrons to the lattice.

By substituting equations (2) and (3) into equation (1) and assuming that the gradients of energy flux and electron temperature are small (i.e., all the energy given to the electrons can transfer to the lattice simultaneously), one can solve for the electron temperature as

$$T_e^{Eq} = \frac{T_O}{2} + \left(\frac{T_O^2}{4} + \frac{2q\tau_e E^2 \mu_O T_O}{3k\theta} \right)^{1/2}. \tag{4}$$

However, if the gradient of the energy flux is taken into account, one can solve for the electron temperature as

$$T_e^{Non-Eq} = \frac{T_O}{2} + \left(\frac{T_O^2}{4} + \frac{2q\tau_e E^2 \mu_O T_O}{3k\theta} \right)^{1/2} - \frac{5}{6}\tau_e \frac{\mu_O}{\theta} T_O \frac{dE}{dy}. \tag{5}$$

It is instructive to note that T_e^{Eq} in equation (4) represents the electron temperature in equilibrium with the lattice while T_e^{Non-Eq} in equation (5) represents electron temperature in non-equilibrium with the lattice which is the case for submicron devices.

The temperature dependent electron temperature is related to electron and lattice temperatures(Baccarani and Wordeman 1985) as

$$\mu = \frac{\mu_O}{\theta}\frac{T_O}{T_e}. \tag{6}$$

If T_e in equation (6) is replaced with T_e in equations (4) and (5), the temperature dependent mobility in the equilibrium μ^{Eq} and non-equilibrium μ^{Non-Eq} become

$$\mu^{Eq} = \frac{\mu_O}{\theta}\frac{T_O}{\frac{T_O}{2} + \left(\frac{T_O^2}{4} + \frac{2q\tau_e E^2 \mu_O T_O}{3k\theta} \right)^{1/2}}, \tag{7}$$

$$\mu^{Non-Eq} = \frac{\mu_O}{\theta}\frac{T_O}{\frac{T_O}{2} + \left(\frac{T_O^2}{4} + \frac{2q\tau_e E^2 \mu_O T_O}{3k\theta} \right)^{1/2} - \frac{5}{6}\tau_e \frac{\mu_O}{\theta} T_O \frac{dE}{dy}} \tag{8}$$

Using the fact that $(2q\tau_e E^2 \mu_O T_O)/(3k\theta) \gg (T_O^2/4)$ and $1/(1-x) \cong 1+x$, μ^{Non-Eq} in equation (8) can be rearranged as

$$\mu^{Non-Eq} = \frac{\mu_O}{\theta}\left(1 + \frac{\alpha}{E}\frac{dE}{dy}\right)\frac{T_O}{\frac{T_O}{2} + \left(\frac{T_O^2}{4} + \frac{2q\tau_e E^2 \mu_O T_O}{3k\theta} \right)^{1/2}} \tag{9}$$

where $\alpha = \sqrt{\frac{25}{24}\frac{k\tau_e \mu_O T_O}{q\theta}}$.

From equations (7) and (8), it is obvious that the temperature dependent mobility in equilibrium can be modified to account for the case when electron and lattice are in non-

equilibrium by modifying the low field mobility term, μ_O, in equation (7) with the effective mobility, μ_O^{Eff}

$$\mu_O^{Eff} = \frac{\mu_O}{\theta}\left(1+\frac{\alpha}{E}\frac{dE}{dy}\right) \tag{10}$$

As seen, the effective mobility μ_O^{Eff} is augmented by the term which is responsible for the non-equilibrium condition and is a function of electric field. In this work, the electric field along the channel is given by[See (A-3) in the Appendix]

$$E = \frac{-m_2}{2\sqrt{m_1 - m_2 y}}. \tag{11}$$

where $m_1 = \left(\frac{1}{2a_o}\left[(V_{GS}' - V_T) - I_{DL}\left(\frac{1}{WC_{ox}\mu_O E_C} + R\right)\right] + I_{DL}R\right)^2$, $m_2 = \frac{I_{DL}'}{a_o W C_{OX}\mu_O}$ and I_{DL} is the drain current without velocity overshoot(to be derived shortly).

The electric field in equation (11) includes several second order effects such as parasitic drain sources resistance, vertical and horizontal mobility degradations but not velocity overshoot which is the main objective of this work. The electric field along the channel including velocity overshoot effect can be obtained but it requires numerical approach making the model inefficient in term of time computation. As will be shown next, the electric field in equation (11) results in a simple analytical expression of the drain current which can predict the results well over a wide range of biasing conditions.

Using a piecewise model(Hoefflinger et al. 1979), the drift velocity in a low field near the source region is given by

$$v_d^{Non-Eq} = \frac{\mu_O^{Eff} E}{1+(E/E_C)} \tag{12}$$

where E_C is the critical electric field for velocity saturation, v_{sat}.

By combining equations (10), (11) and (12), one obtains

$$v_d^{Non-Eq} = \mu_O\left(1+\frac{\alpha m_2}{2(m_1 - m_2 y)}\right)\frac{E}{1+(E/E_C)} \tag{13}$$

As seen, v_d^{Non-Eq} in equation (13) reduces to conventional field dependent velocity model if electron energy can be transferred to the lattice immediately (i.e., energy relaxation time and thus α is zero.). It is also instructive to note that the electric field expression given in equation (11) is valid only in the region where the gradual channel approximation is applied. For device operating in the saturation region, equations (11) and (13) are valid from the source terminal to the point where the channel potential is equal to saturation voltage.

The drain current including parasitic drain source resistance(R_S=R_D=R) is given by modifying the drain current in (Arora et al. 1994) as

$$I_D = WC_{ox}\left[V_{GS}' - V_T - 2a_o V(y)\right]v_d^{Non-Eq} \tag{14}$$

where W, C_{ox}, $V_{GS} = V_{GS} - I_D R$, $V_T = 2\psi_B + V_{FB} + \gamma_e\sqrt{2\psi_B + V_{SB}} - \sigma V_{DS}$, $V(y)$, σ and a_o are the width of the channel, gate oxide capacitance per unit area, gate source voltage, threshold voltage, channel potential, drain induced barrier lowing(DIBL) factor and Taylor series correction factor respectively.

By combining equations (13) and (14), the drain current is

$$I_D = \mu_O WC_{ox}\left[V_{GS}' - V_T - 2a_o V(y)\right]\left(1+\frac{\alpha m_2}{2(m_1 - m_2 y)}\right)\frac{E}{1+(E/E_C)} \tag{15}$$

Integrating equation (15) over the whole channel length yields the drain current as(Dwight 1961)

$$I_{DL}=\frac{-k_3+\sqrt{4k_1k_2+k_3^2}}{2k_1}+\frac{\alpha\eta_1 m_2}{4\eta_2}\left\{\begin{array}{l}2\left[V_{GS}-V_T-\frac{1}{2a_o}\left(V_{GS}-V_T-\frac{I'_{DL}}{WC_{ox}\mu_O E_C}-I'_{DL}R\right)\right]\times\\ \left(\frac{1}{\sqrt{m_1-m_2L}}-\frac{1}{\sqrt{m_1}}\right)-\ln\left(1-\frac{m_2L}{m_1}\right)\end{array}\right\} \tag{16}$$

where $\eta_1=WC_{ox}\mu_O$, $\eta_2=L+V_{DS}/E_C$, $k_1=(2/\eta_2)(\eta_1R^2(2a_o-1)-R/E_C)$, $k_2=(\eta_1/\eta_2)(V_{GS}-V_T-a_oV_{DS})V_{DS}$ and $k_3=(2k_2R/V_{DS})-(\eta_1/\eta_2)(2a_o-1)V_{DS}R+1$.

As seen, equation (16) consists of two current components: 1) the first term on the RHS which is the drain current contributed by the conventional mobility model or the drain current without velocity overshoot I'_{DL}, and 2) the second term on the RHS caused by the augmented portion of velocity overshoot model in equation (13).

As the drain voltage increases, the lateral electric field at the drain terminal reaches the critical field E_C. The drain voltage responsible for that critical electric field is saturation voltage V_{DSAT} and can be found using similar approach to Chaisirithavornkul and Kasemsuwan (2000) as

$$V_{DSAT}=V'_{DSAT}+2RI_{DSAT} \tag{17}$$

where $V'_{DSAT}=(-k_4+\sqrt{k_4^2+\eta_1k_5})/(2a_oRE_C\eta_1)$, $k_4=V_{GS}-V_T-2a_oLE_C$, $k_5=4a_oRE_C^2L(V_{GS}-V_T)$ and I_{DSAT} is the drain current at the onset of saturation given by equation (16) with V_{DS} replaced by V'_{DSAT}.

For device operating in the saturation region, the validity of the gradual channel approximation region is reduced from L to L-L_m where L_m is the channel shortening due to the channel length modulation. The drain current in this region can be found by integrating equation (15) from the source end to the point of the saturation(L-L_m) and is given by

$$I_{DS}=\frac{I_{DSAT}}{1-\frac{L_m}{\eta'_2+\eta_1RV'_{DSAT}}} \tag{18}$$

where η'_2 is $\eta_2|_{V_{DS}=V'_{DSAT}}$.

In this work, L_m is found by using quasi-two dimensional approximation and retaining the first three terms after the Taylor series expansion of L_m in Ko (1989) as

$$L_m=l\ln\left((1+\chi)+\frac{\gamma}{lE_C}+\frac{\gamma^2}{2(lE_C)^2}\right) \tag{19}$$

where $\gamma=V_{DS}-V'_{DSAT}$, $l=\sqrt{\varepsilon_{Si}t_{OX}X_J/\varepsilon_{OX}}$ and χ represents the Taylor series expansion correction factor. To avoid the negative value of L_m and to guarantee a smooth change in L_m, V_{DS} in equation (19) is replaced by a smoothing function V_{DSX}(Klos and Kostka 2000)

$$V_{DSX}=V'_{DSAT}\left[1+\frac{\ln\left(1+e^{A\left(V_{DS}/V_{DSAT}-1\right)}\right)}{\ln\left(1+e^{A}\right)}\right] \tag{20}$$

The expression V_{DSV} in equation (20) gives V_{DS} and V'_{DSAT} when $V_{DS} \square V'_{DSAT}$ and $V_{DS} \square V'_{DSAT}$ respectively. Parameter A in equation (20) is used to control the smoothness of the curve.

III. RESULTS AND DISCUSSION

To verify the validity of the model, the model results have been compared with the experimental data(Sai-Halasz et al. 1988). The devices were fabricated with several gate lengths ranging from 0.07μm to 0.25μm with the oxide thickness of 4.5nm. Figure 1 shows the comparison between the theoretical predictions of current voltage characteristic(solid line), the theoretical predictions without velocity overshoot i.e., equation (16) with τ_e=0ps(dash line) and the experimental data(dot)(Sai-Halasz et al. 1988). In the simulation, an effective doping concentration (N_A), low field mobility (μ_O), energy relaxation time (τ_e), saturation velocity (v_{sat}), parasitic drain source resistance (R), smoothing factor (A) and χ are $7\text{x}10^{17}$ cm^{-3}, 420 cm^2/V.s, 0.3 ps, $9\text{x}10^6$ V/cm, 32 Ω, 10 and 0.12 respectively. As seen, the predictions show increasing differences in the drain current for larger applied drain source voltage V_{DS} due to the larger channel electric field and its gradient. For the device biased at V_{GS}= 0.8V and V_{DS}= 0.6V, the drain current including velocity overshoot effect can be 29% larger than the current without velocity overshoot. The agreements between the theoretical predictions and the experimental data are well obtained over a wide range of applied gate and drain voltages. Figure 2 shows the comparison between the theoretical predictions of the device transconductance g_m(solid line), theoretical predictions without velocity overshoot(dash line) and the experimental data(dot)(Sai-Halasz et al. 1988) for different gate lengths(0.07μm-0.275μm) under 300K. The device transconductance in the linear and saturation regions can be calculated by taking derivative the drain currents in equation (16) and equation (18) with respect to V'_{GS} respectively. As seen, there is a sharp increase in the transconductrance as the channel length decreases. The difference in the transconductance from the theoretical predictions with and without velocity overshoot is 10% for channel length of 0.21μm and can go up to 20% when the channel length goes down to 0.08μm. Reasonable agreements between the experimental data and the predictions from this model are obtained.

V. CONCLUSION

In this paper, an analytical model for short channel MOSFET including velocity overshoot is presented. The model is developed based on the velocity overshoot model obtained from the solution of energy balance equation under the assumption of displaced Maxwellian distribution. The mobility model is found to be an augmented model and all parameters involved are physical parameters. The model also includes the effects of the mobility degradation, channel length modulation, drain induced barrier lowering(DIBL) and parasitic drain source resistance. The theoretical predictions of the model are verified by comparing its predictions with the experimental data and shown to be in good agreement over a wide range of bias conditions.

APPENDIX

ELECTRIC FIELD EXPRESSION

Combining equations (12) and (14) and taking into account parasitic drain source resistance i.e., $V'_{GS} = V_{GS} - I'_{DL}R$, yields the drain current in term of channel potential $V(y)$ after some algebraic manipulation as

$$I'_{DL} = WC_{ox}\mu_o\left[V_{GS} - V_T - 2a_o V(y) - I'_{DL}\left(R + \frac{1}{W\mu_{eff}C_{ox}E_C}\right)\frac{dV(y)}{dy}\right]. \quad \text{(A-1)}$$

The channel potential $V(y)$ can be obtained by integrating equation (A-1) from the source end to any position along the channel, y, subject to boundary condition $V(y)\big|_{y=0} = I'_{DL}R$ as

$$V(y) = \sqrt{m_1} + I'_{DL}R - \sqrt{m_1 - m_2 y} \quad \text{(A-2)}$$

where $m_1 = \left\{\frac{1}{2a_o}\left[(V_{GS} - V_T) - I'_{DL}\left(\frac{1}{WC_{ox}\mu_O E_C} + R\right)\right] - I'_{DL}R\right\}^2$ and $m_2 = \frac{I'_{DL}}{a_o WC_{ox}\mu_O}$.

Figure 3 shows channel potential along the channel of the MOS transistor with channel length of 0.1μm. The gate and drain voltages are 4.4V and 0.7V respectively. The potential at the source(y=0 in equation (A-2)) and the drain terminals(y=0.1μm in equation (A-2)) are 0.056V and 0.644V respectively. The voltage at the source and the drain terminals are not zero and V_{DS} due to the voltage drop across parasitic drain and source resistances respectively. The electric field along the channel is given by the negative of the gradient of channel potential in equation (A-2) as

$$E = \frac{-m_2}{2\sqrt{m_1 - m_2 y}}. \quad \text{(A-3)}$$

ACKNOWLEDGEMENT

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FIGURE CAPTIONS

Figure 1. I-V Characteristic. Measured data(dot)[2], this model with velocity overshoot(solid line) and without velocity overshoot(dash line)

Figure 2. Device Transconductance. Measured data(dot)[2], the model with velocity overshoot(solid line) and without velocity overshoot(dash line)

Figure 3. Channel potential(V_{GS}= 4.4V@V_{DS}=0.7V)

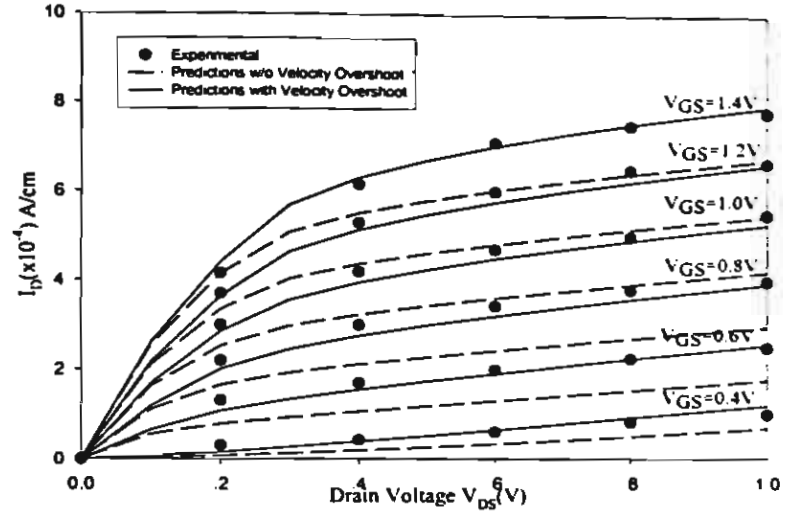

Figure 1

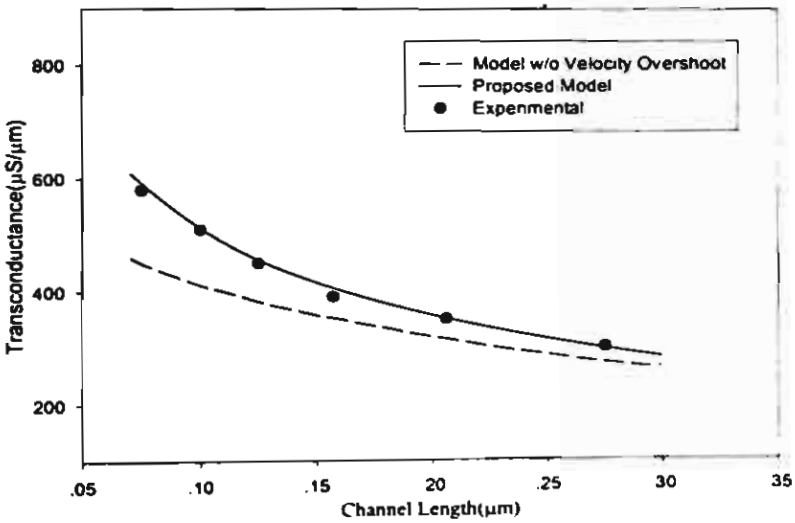

Figure 2

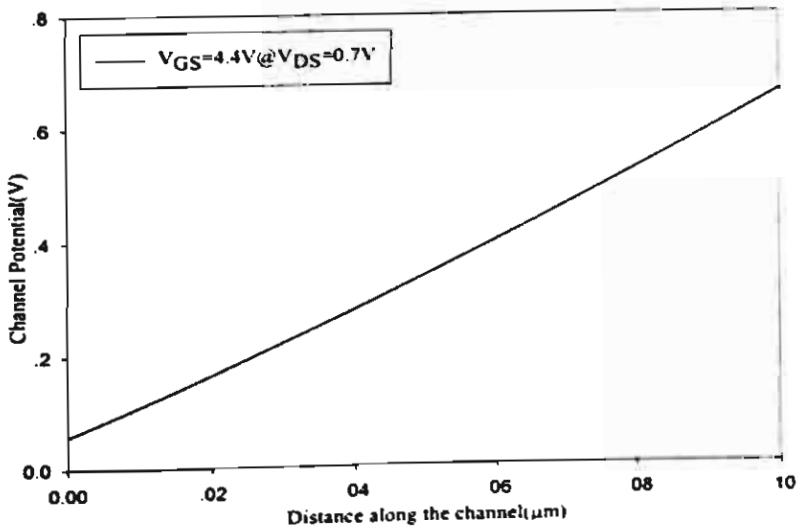

Figure 3

3Volt High Frequency and Low Input Impedance CMOS Current-Mode Precision Full-Wave Rectifier(PFWR)

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Subject categories: Analogue Electronics
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Keywords: Current-mode, Rectifier

3Volt High Frequency and Low Input Impedance CMOS Current-Mode Precision Full-Wave Rectifier(PFWR)

Varakorn Kasemsuwan and Surachet Khucharoensin

A high performance current-mode precision full-wave rectifier based on an improved Wilson current miller is proposed. All transistors are biased at low current resulting in small power dissipation(5.8μW). The input impedance of the circuit is very small(236Ω) and the circuit can operate at 100 MHz with only 0.21% mismatch between input and output signal currents for an input current of ±150μA.

Introduction: Precision rectifiers are one among very important circuit building blocks for analogue and digital signal processing, conditioning and instrumentation especially for low level signals. Applications include RMS to DC conversions and peak detectors. Several approaches have been proposed[1-5] to build precision rectifiers. Conventionally, precision rectifiers are based on diodes and opamps[1-2]. The rectifier however has a problem with a high distortion during the zero crossing of the input signal due to that the opamps have to recover during non-conduction/conduction transition with a finite small signal dV/dt(slew rate). The rectifiers are thus limited to a frequency performance well below the gain bandwidth product f_T of the amplifier. An improvement of the rectifier design was to use current conveyors and diodes[3-4]. The resulting circuits can operate at high frequency. However, the circuits are power hungry and quite large making them unsuitable for implementing in the large-scale integrated circuit. Recently, a high performance precision rectifier has been proposed[5]. The circuit consists of only three transistors and are biased with low current resulting in low total power dissipation(4.8μW). The circuit can also operate at high frequency(100MHz). However, the input impedance of the circuit is quite high(7.2kΩ-47kΩ) posing a problem in the current-mode circuit design. In addition, the output signal is not symmetry during positive and negative input cycle.

Proposed precision full-wave rectifier(PFWR): Fig. 1 shows the proposed precision rectifier. The circuit is designed based on two precision half-wave rectifiers(M_{1a}-M_{5a} and M_{1b}-M_{5b}) operating alternatively during positive and negative input cycle. I_{in1} and I_{in2} are the input currents with the same magnitude but 180 degree out of phase. $M_{5a,b}$ are used to biased $M_{1a,b}$-$M_{4a,b}$ on the edge of conduction. When I_{in1} and I_{in2} flows into node a and out of node b respectively, M_{3a} cuts off while M_{3b}, which is connected as a common gate, allows the input current I_{in2} to flows through the load R_L. Same explanation is applied when I_{in1} and I_{in2} flows out of node a and into node b respectively. As a result, the circuit works as a full-wave rectifier. The input impedance of the circuit(node a and b) are very low due to the negative feedback(shunt input) with in the loop $M_{1a,b}$-$M_{4a,b}$. To demonstrate this fact, when I_{in1} flows into node a, voltage at node a, V_a, is pulled high. The signal V_a is amplified via M_{2a}(common source) causing voltage at the drain of M_{2a} and at the gate of M_{4a} to go low. As a result, the source voltage of M_{3a} is forced to be low. Straightforward circuit analysis shows the input impedance of the circuit given by

$$R_{in} \equiv \frac{1}{g_{m1a,b} + g_{m3a,b} + g_{m2a,b} g_{m3a,b} (r_{o2a,b} \,//\, r_{o5a,b})}$$

Performance of proposed precision full-wave rectifier(PFWR): To verify the circuit performance, HSPICE is used to simulate the proposed circuit using a standard 0.5μm CMOS process. Fig. 2 shows input impedance of the proposed circuit(solid line) and that by[5](dash line). As seen, our proposed circuit has relatively much lower input impedance. To the best of authors' knowledge, our circuit offers lowest input impedance(236Ω). Fig. 3 shows the comparison of the DC transfer characteristic of proposed circuit(solid line), circuit in [5](dash line) and ideal output curve(triangle). A sharp corner at zero crossing point and good symmetry during positive and negative input cycle are well obtained. The mismatch obtained from the input and rectifier's output are 0.21% for an input current of ±150μA. Fig. 4 shows transient simulation of input signal(dot), our circuit(solid line) and [5](dash line) for the input frequency of 100MHz. The results show that our circuit gives a good symmetry for both positive and negative input cycle at high frequency. Lastly, the total power dissipation is 5.8μW

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Figure captions:

Fig. 1 Schematic diagram of the proposed precision full-wave rectifier(PFWR)

Fig. 2 Input impedance
—— proposed circuit
----- circuit by [5]

Fig. 3 DC Transfer Characteristic
∇ Ideal
—— proposed circuit
----- circuit by [5]

Fig. 4 Transient response (100MHz input current)
O input current
—— proposed circuit
----- circuit by [5]

Table caption:

Table 1. Transistor's geometrical dimensions

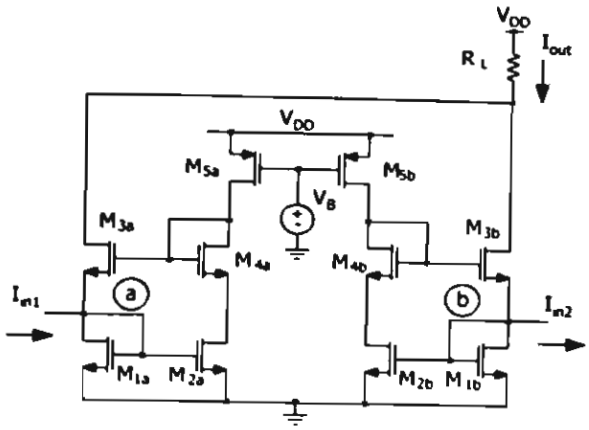

Figure 1

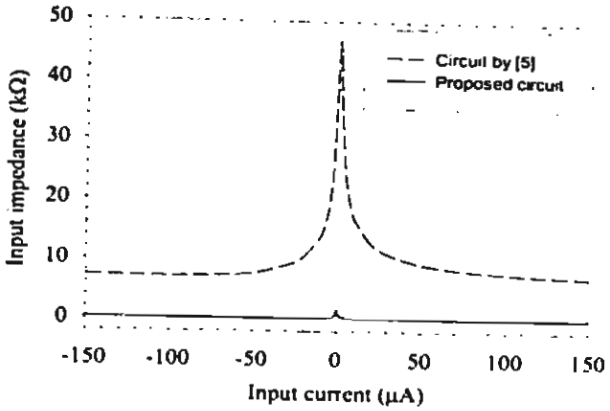

Figure 2

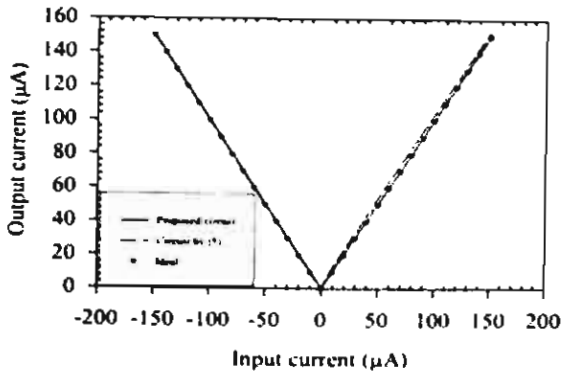

Figure 3

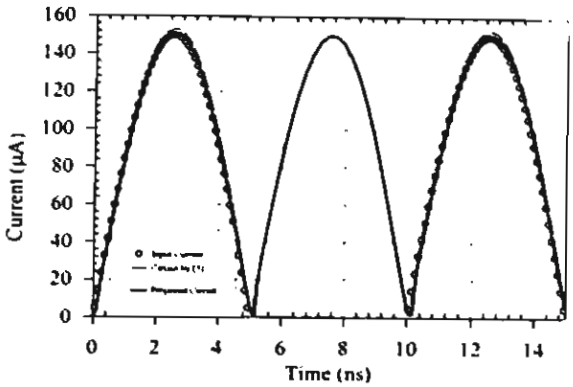

Figure 4

Table 1

Device	W(μm)	L(μm)
$M_{1a,b} - M_{4a,b}$	0.5	0.5
$M_{5a,b}$	7	2
M_6, M_7	10	2

High-Speed Low Input Impedance CMOS Current Comparator

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Subject categories: Analogue Electronics
Index Terms by subject categories: Analogue Processing Circuits
Keywords: Current mode, Comparator

High-Speed Low Input Impedance CMOS Current Comparator

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A simple high-speed low input impedance CMOS current comparator is proposed. The circuit uses improved Wilson current-mirror to perform a subtraction. Negative feedback is employed to reduce the input impedance of the circuit. HSPICE is used to verify the circuit performance with a standard 0.5μm CMOS technology. Simulation results demonstrate the propagation delay of 1.02 ns, average power consumption of 0.911 mW and input impedance of 137 Ω for ±0.1μA input current at the supply voltage of 3V.

Introduction: In recent years, current-mode circuits become increasingly popular among analog circuit designers. This is mainly attributed to higher speed, larger bandwidth and lower supply voltage requirement compared to the voltage mode circuit counterpart. Current comparator is widely used as a building block of analog systems including A/D converters, oscillator, VLSI neural network and other signal processing applications. Several approaches have been proposed to implement current comparator [1-5]. Current mirror current comparator has been firstly proposed by [1]. The circuit consists of two cascode current mirrors. The circuit can not operate at high frequency due to high impedance at the output node. To increase frequency of the operation and, at the same time, to reduce the input impedance of the circuit, source follower input stage current comparator as shown in Fig. 1a) is then proposed[2]. The input part of the circuit consists of two transistors(M_1 and M_3) connected as source follower to lower the input impedance while two transistors at the output(M_2 and M_4) are connected as complementary common source. The circuit however shows deadband region where the input impedance is quite high during input transition and thus limiting the speed of operation. A biasing method using current source[3] is proposed to alleviate this deadband problem. The circuit needs very well controlled current sources in addition to the requirement of a twin well process as the substrate of two diode connected transistors have to be tied to their sources. The input and output impedances of current comparator are further reduced by using a negative feedback approach[4-5]. The front end preamplifier circuit by[4] shown in Fig. 1b) is current source inverting amplifier with M_r operating as a resistive feedback element while the front end preamplifier circuit by[5] shown in Fig. 1c) is a cascode current source inverting amplifier with M_5 serving as a resistive feedback element. Their circuits exhibit low input and output impedances and the delay time is less than 1.5 ns for ±0.1μA input current.

Up to present, most proposed current comparators[2-5] assumed input current I_{in} as a subtraction(or difference) of the reference current(I_{REF}) and the actual input current(to be compared with I_{REF}). None of them shows the circuit that performs such subtraction. It is instructive to note that the subtraction circuit is also part of the current comparator and therefore previously reported simulation results, i.e., power dissipation, speed of operation and power delay product, are too optimistic as the subtraction circuit also consumes certain amount of power and exhibits certain delay time.

In this paper, a simple high speed and low input impedance CMOS current comparator is proposed. The circuit employs an improved Wilson current miller which serves two duties; 1) it is used to perform a current subtraction between the actual input current I_{in} and the reference current(I_{REF}) and 2) it is used to reduce an input impedance of the circuit via negative feedback within an improved Wilson current mirror itself. HSPICE is used to verify the circuit performance and the results show the propagation delay of 1.02 nsec with an average power dissipation of 0.911 mW using a standard

0.5μm CMOS technology for an input current of ±0.1μA at the supply voltage of 3V. The input impedance of the circuit is 137 Ω.

Circuit Description: Fig. 2 shows the proposed current comparator circuit. M_1-M_4 are connected as an improved Wilson current mirror and M_5 is a diode connected load. $M_{n1\text{-}n3}$ and $M_{p1\text{-}p3}$ are three resistive load amplifiers($M_{p1\text{-}p3}$ operating in the linear region) and are used to amplify the voltage signal at node c. $M_{n4\text{-}n5}$ and $M_{p4\text{-}p5}$ are two CMOS inverters and used to amplify the signal for rail to rail operation at the output. I_{REF} is referred to the reference current to be compared with the input current I_{in}. The operation of the circuit can be explained as follows: The reference current I_{REF} flows to M_3 making the drain current of M_1 and M_2 equal to I_{REF} provided that M_1 and M_2 have the same aspect ratio. The output current(drain current of M_4) is then the subtraction between the reference current I_{REF} and the input current I_{in}. If the input current I_{in} is increased and greater than the reference current I_{REF}, the output current I_O decreases pulling up the voltage at node c. The same situation is applied when input current I_{in} is decreased and less than the reference current I_{REF}, the voltage at node c is pulled down. The signal at node c is amplified by three resistive load common sources ($M_{n1\text{-}n3}$ and $M_{p1\text{-}p3}$) and two CMOS inverters($M_{n4\text{-}n5}$ and $M_{p4\text{-}p5}$) for rail to rail operation.

The input impedance of the circuit at node b is low due to the negative feedback(shunt input) within the loop on an improved Wilson current mirror consisting of M_1-M_4. To demonstrate this fact, when I_{in} flows into node b, voltage at node b(V_b) is pulled high. The signal V_b is amplified via M_1(common source) causing voltage at the drain of M_1 and at the gate of M_3 to go low. As a result, the source voltage of M_4 is forced to be low. Straightforward circuit analysis shows the input impedance of the circuit given by

$$R_{in} \cong \frac{1}{g_{m2} + g_{m4} + g_{m1}g_{m4}(r_{o1} /\!/ r_{oi})} \tag{1}$$

where g_m is the transconductance of MOS transistor, r_{o1} is drain-source resistance of transistor M_1 and r_{oi} is output impedance of the biasing current source I_{BIAS}. It can be easily shown that if g_m of M_1-M_4 are of the same value, Eq.(1) can be reduced to

$$R_{in} \cong \frac{1}{g_m^2(r_{o1} /\!/ r_{oi})} \tag{2}$$

Experimental Results: To verify the circuit performance, HSPICE is used to simulate the proposed circuit using a standard 0.5μm CMOS process with 3V supply voltage. Bias current I_{BIAS} is set to 20 μA while the reference current I_{REF} is 20 μA. The transistor dimensions of the proposed circuit are summarized in Table 1. It is instructive to note that the conventional input current used in [2], [4-5] is the difference between the actual input current and the reference current. This current is in fact equivalent to the drain current of transistor M_4 of our proposed circuit(see Fig. 2). To compare our circuit performance with others[2],[4-5], the input current, when referred to, means the drain current of M_4 and, in addition, transistor dimensions are chosen to be comparable with ours. Fig. 3 shows transient response of the input current signal (solid line) and output voltage signal (dash line) from our circuit. The input current is ±0.1μA square wave at the frequency of 25 MHz. The output signal shows rail to rail operation (0V-3V) with a propagation delay time of 1.02 ns. Fig. 4 shows a comparison of an average delay time as a function of the input current ranging from ±0.01μA to ±10μA for current comparator by [2](dot), [4](square), [5](triangle) and our proposed circuit(solid line). It is noted that we use the same standard 0.5μm CMOS technology during simulation for all

current comparators. From Fig. 4, it can be seen that for low input current, the delay time of the proposed comparator is much lower than that of [2] and is comparable with those of [4] and [5]. However, the delay time of all comparators become comparable when the input current increases up to 10μA. This is attributed to the fact that the delay time is mainly determined by the rail to rail amplifiers for high input current. Fig. 5 shows a comparison of power consumption as a function of the input current in the same range of Fig. 4 for current comparator by [2](dot), [4](square), [5](triangle) and our proposed circuit(solid line). Although the power consumption of our circuit is comparable with those in [5] but more than those in [2] and [4], it is instructive to note that the power consumption of the circuit by [2] and [4-5] exclude the power consumption taken by the subtraction circuit which is also part of the current comparator. In addition, the input impedance of our proposed circuit is much lower for the same input current. Fig. 6 shows a comparison of input impedance for current comparator by [2](dot), [4](square), [5](triangle) and our proposed circuit(solid line). As seen, the input impedance of our proposed circuit is smaller with an order of magnitude. For example, our circuit shows input impedance of 137 Ω at 0.1μA while the input impedance are found to be 36.8 kΩ in [2], 12 kΩ in [4] and 5 kΩ in[5]. To the best of authors' knowledge, our circuit gives lowest input impedance for the same biasing current. Fig. 7 shows a comparison of power delay product for current comparator by [2](dot), [4](square), [5](triangle) and our proposed circuit(solid line). As seen, our power delay product is superior to [2] and comparable to [4-5]. Again, the power consumption and the delay of [2] and [4-5] as shown in Fig. 6 assume zero power consumption and zero delay for the subtraction circuit which is not true. For a fair comparison, this additional power consumption and delay are to be included. We have implemented a simple current subtraction circuit and found the power consumption of 60 μW for biasing current of 10μA. By assuming the delay of the subtraction circuit is negligible, the power delay products of circuit by [2], [4], [5] and our circuit are 4.987pJ, 1.097pJ, 0.9307pJ and 0.9278pJ respectively.

Conclusions: A simple high-speed and low input impedance CMOS current comparator is proposed. The circuit employs an improved Wilson current miller to perform a current subtraction between the input current I_{in} and the reference current I_{REF}. Negative feedback has been employed to reduce the input impedance of the circuit. HSPICE is used to verify the circuit performance. The simulation results show the propagation delay of 1.02 ns, an average power dissipation of 0.911 mW and input impedance of 137 Ω using a standard 0.5μm CMOS technology for an input current of ±0.1μA at the supply voltage of 3V.

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Figure captions:

Fig. 1 Current Comparator by 1a) H. Träff [2], 1b) B.M. Min, et al.[4] and 1c) L. Chen, et al.[5]
Fig. 2 Schematic diagram of proposed circuit.
Fig. 3 Transient response of the proposed circuit.
Fig. 4 Delay time versus input current.
Fig. 5 Power consumption versus input current.
Fig. 6 Input impedance versus input current.
Fig. 7 Power delay product versus input current

Table caption:

Table 1 Transistor's geometrical dimensions

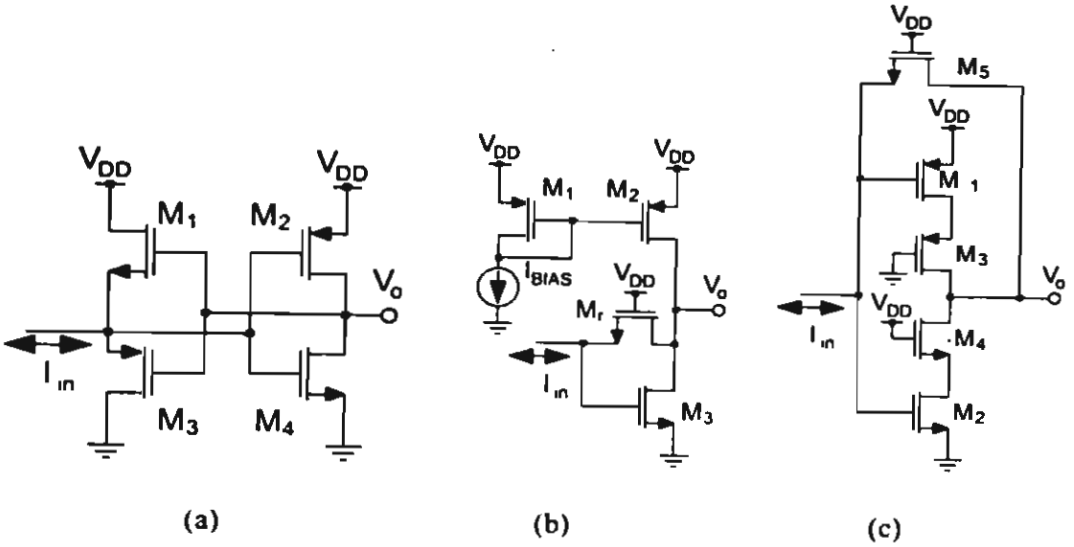

Figure 1

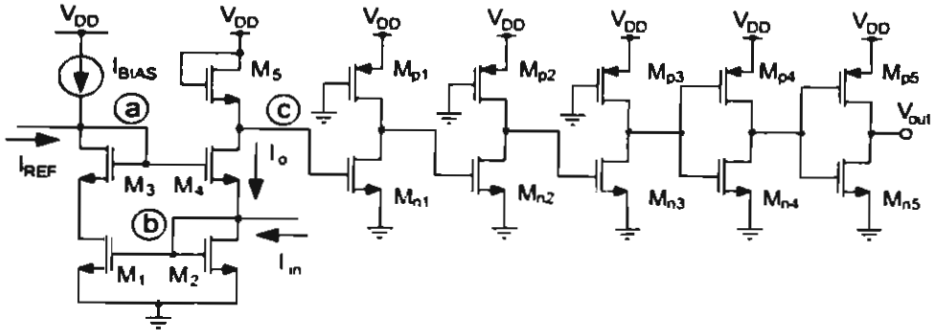

Figure 2

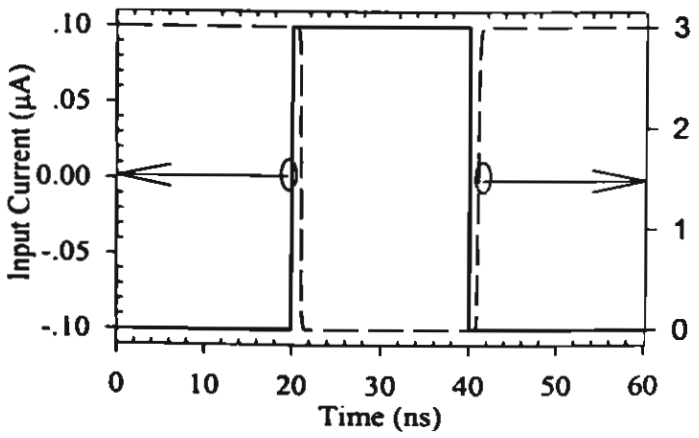

Figure 3

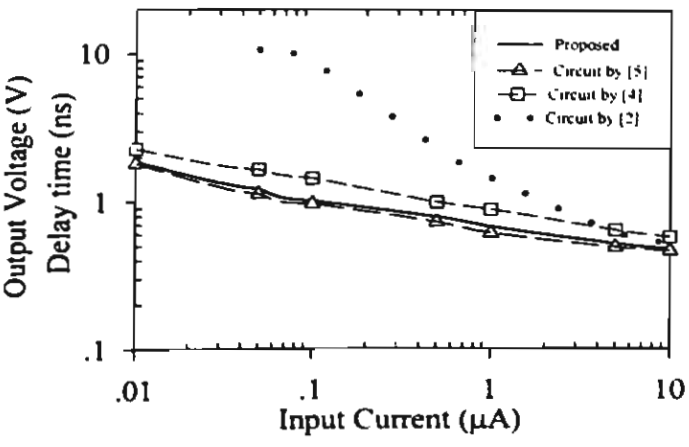

Figure 4

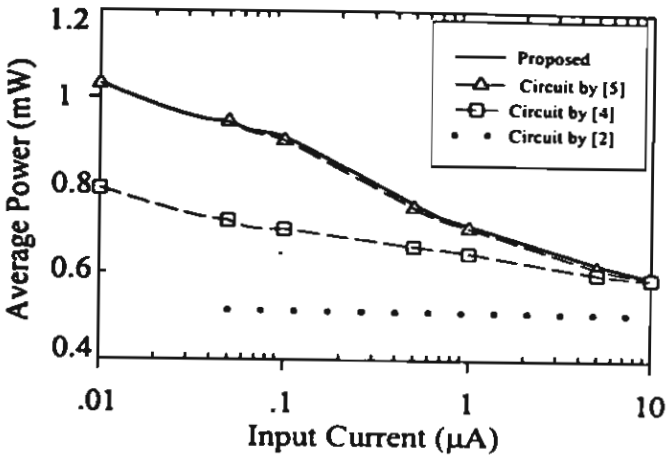

Figure 5

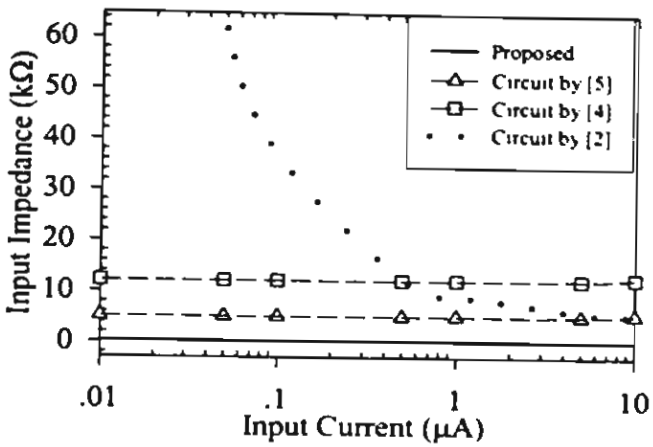

Figure 6

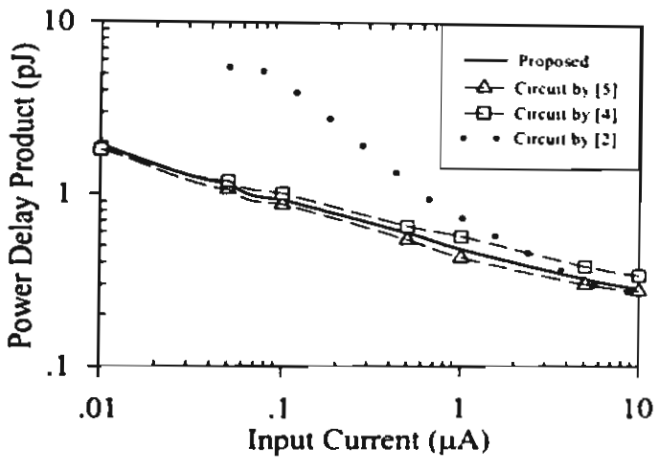

Figure 7

Table 1

Device	W (μm)	L (μm)
M_{BIAS}	8	2
M_1-M_4	2	0.5
M_5	0.5	0.6
Mn_1-Mn_5	0.5	0.5
Mp_1-Mp_3	0.5	0.6
Mp_4-Mp_5	2.4	0.5