รายงานวิจัยฉบับสมบูรณ์

โครงการ เทคนิควงจรแอนะลอกที่แรงดันไฟเลี้ยงและกำลังงานต่ำสำหรับการประมวลผลสัญญาณชีวภาพแบบพกพาและปลูกฝัง

โดย อภิศักดิ์ วรพิเชฐ

10 สิงหาคม 2554

สัญญาเลขที่ RMU5180033

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สนับสนุนโดยสำนักงานกองทุนสนับสนุนงานวิจัย
และสำนักงานคณะกรรมการอุดมศึกษา

Abstract

Project Code: **RMU5180033**

Project Title: **Very Low Voltage Low Power Analogue Techniques for Portable and Implantable Biomedical Signal Processing**

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Today's advancement of state-of-the-art fine-line CMOS processing has made feasible the implementation of portable and implantable bio-medical integrated circuits and systems for ubiquitous healthcare applications. Crucial parameters for such devices include low power consumption and low supply voltage with adequate dynamic range. In this research project, we have developed analogue CMOS techniques in sub-threshold inversion operation for very low voltage and low power circuits. In particular, a sampled-data switch-current analogue signal processing based on CMOS memory transistors operating in sub-threshold operation has been introduced and analyzed in details. Also developed are the sub-threshold R-MOSFET tunable resistors and mixers for continuous-time analogue signal processing. These techniques show good promise for future implementation of low voltage low power bio-medical integrated filters which are indispensible building elements for portable and implantable bio-medical signal processing.

Keywords: **Low voltage circuits, low power circuits, sub-threshold CMOS circuits, bio-medical CMOS circuits**

บทคัดย่อ

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ปัจจุบัน ความก้าวหน้าด้านเทคโนโลยีการผลิตวงจรรวมซีมอสที่มีขนาดเล็กมาก ได้ส่งผลให้เราสามารถสร้างระบบวงจรอิเล็กทรอนิกส์สำหรับอุปกรณ์พกพาและปลูกฝังได้ ทั้งนี้ สมรรถนะที่จำเป็นสำรับอุปกรณ์เหล่านี้ที่สำคัญอย่างยิ่งคือการกินกำลังงานที่ต่ำ รวมถึงระดับแรงดันไฟเลี้ยงที่ต่ำ โดยที่ยังต้องคงไว้ซึ่งระดับของพิสัยพลวัตที่เพียงพอ สำหรับโครงการวิจัยนี้ได้ทำการพัฒนาเทคนิควงจรแอนะลอกกำลังงานต่ำและแรงดันไฟเลี้ยงต่ำ ที่อาศัยมอสทรานซิสเตอร์ซึ่งทำงานในย่านใต้ขีดเริ่ม โดยเราได้ทำการพัฒนาและวิเคราะห์เทคนิคสวิทช์กระแสที่อาศัยหน่วยความจำมอสทรานซิสเตอร์ในย่านใต้ขีดเริ่มสำหรับการประมวลผลสัญญาณเชิงสุ่ม นอกจากนี้ ยังได้พัฒนาตัวต้านทานปรับค่าได้และวงจรผสมสัญญาณที่อาศัยโครงสร้างตัวต้านทานและมอสทรานซิสเตอร์ย่านใต้ขีดเริ่มสำหรับการประมวลผลสัญญาณเชิงต่อเนื่อง เทคนิคที่นำเสนอเหล่านี้ ได้มีการพิสูจน์ให้เห็นว่าเหมาะสมกับการสร้างระบบวงจรกรองที่มีการกินกำลังงานต่ำ และมีความต้องการระดับไฟเลี้ยงที่ต่ำ ซึ่งเป็นองค์ประกอบที่มีความสำคัญต่อการประมวลผลสัญญาณชีวแพทย์ในอุปกรณ์พกพาและปลูกฝังเป็นอย่างยิ่ง

คำหลัก: Low voltage circuits, low power circuits, sub-threshold CMOS circuits bio-medical CMOS circuits

Very Low Voltage Low Power Analogue Techniques for Portable and Implantable Biomedical Signal Processing

1. Introduction

Since its invention in 1958, integrated circuits technology has revolutionized electronic devices, which help transform the world into the so-called information age. This is made possible by its computing capability, inexpensive production, and tiny physical size. While the dominance of integrated circuits in data processing, communication and multi-media will continue into the foreseeable future, there has been considerable research effort in pushing the silicon technology into the realm of biology and medicine.

Today's advancement of state-of-the-art fine-line CMOS processing has made feasible the implementation of bio-medical integrated circuits and systems for ubiquitous healthcare applications, such as wearable heath and wellness monitoring, as well as portable and implantable molecular detection platform for disease diagnosis, DNA sequencing etc []. Crucial parameters for such devices include low power consumption and low supply voltage with adequate dynamic range.

In this research project, we have developed analogue CMOS techniques in sub-threshold inversion operation for very low voltage and low power circuits and systems. Particular emphasis is given on techniques for implementations of integrated filters – one of the indispensible building blocks for bio-medical signal processing. A list of the technical contributions resulting from this project, along with their summary is given as follows:

1) Circuit development and performance analysis of very low supply voltage, low power sampled-data switch-current analogue signal processing based on CMOS transistors in sub-threshold operation :
   The general performance of class AB switched currents (SI) is analysed using the general MOS equations, valid for all regions of operation. Using a figure-of-merit combining speed, dynamic range and power consumption, the overall performance is shown to improve progressively as the SI memory transistors' operating region is moved from strong inversion to moderate and then weak inversion. The analysis is validated firstly by experiment using transistor arrays and then by simulation using 0.35μm, 0.18μm and 90nm CMOS process data. After discussing non-ideal behaviour of the weak inversion memory cell, two practical designs are described: a cascoded class AB memory at 1.25V supply in the 3.3V, 0.35μm process and a two-step sampling class AB memory at 0.6V supply in the 1.8V, 0.18μm process, and each demonstrates good performance.

2) Circuit development and detailed analysis/design of sub-threshold R-MOSFET tunable resistors for very low supply voltage :

The sub-threshold R-MOSFET resistor structure which enables tuning range extension below the threshold voltage in the MOSFET with moderate to weak inversion operation is analyzed in detail. The principal operation of the sub-threshold resistor is briefly described. The analysis of its characteristic based on approximations of a general MOS equation valid for all regions is given along with discussion on design implication and consideration. Experiments and simulations are provided to validate the theoretical analysis and design, and to verify the feasibility at a supply voltage as low as 0.5V using a low-threshold devices in a
1.8-V 0.18 μm CMOS process.

3) Circuit development and detailed analysis/design of sub-threshold R-MOSFET mixers for very low supply voltage :
An enhanced mixer topology suitable for very low supply voltage applications is developed. The circuit introduces a linear resistor network to the conventional mixer based on cross-coupled triode MOS transistors to render extended transistors' operation and linearity improvement at a low supply. Detailed analysis that leads to a systematic design is outlined. The feasibility of the mixer for baseband wireless sensor applications is demonstrated through simulation of a 0.5-V demodulator for IEEE 802.15.4 radio using regular transistors in a 1.8V 0.18μm CMOS process with V_{T0} = 0.4V which is as large as 80% of the supply voltage. Also provided to verify its practicality is the experimental demodulator at a reduced data rate based upon a breadboard implementation using array transistors.

4) Analysis, design and silicon implementation of a very low voltage and low power R-MOSFET-C filters :
A 0.5-V fully-integrated R-MOSFET-C filter suitable for use in wearable and portable biomedical devices is demonstrated. Such a very low supply voltage and low power is made possible through the sub-threshold inversion operation of the MOS transistors in both the operational transconductance amplifiers (OTA) and the tunable resistors. A fully-integrated 5^{th}-order Chebychev low-pass filter in a 0.18-μm triple-well CMOS technology with V_T = 0.42 V is implemented for a 0.5 V supply voltage. The measured tuning frequency is from 91 kHz to 268 kHz which is more than one octave where the nominal cut-off frequency automatically set by the on-chip PLL circuit is at 130-kHz. The spurious-free dynamic range (SFDR) is better than 53.7 dB. The total current and power consumption (including the bias control circuits) are 1.2 mA and 600 μW respectively.

The details of each topic will be covered from Section 2 to 5 of this report.

2. Subthreshold SI Techniques for Low Power Biomedical Electronics

2.1 Introduction

Since its inception over a decade ago, the switched-current (SI) technique has claimed two main advantages over switched-capacitors (SC): because it operated in the current domain, it should be less impacted by lowering supply voltage, and because it did not use explicit capacitors, it should be better suited to "digital" CMOS. The SI technique has been found useful in many analogue applications where a compatibility with standard digital CMOS and low supply voltage, as well as a small chip area are of main concern [1-13]. However, despite numerous circuit developments, all using transistors operated in strong inversion (i.e. square law characteristics), performance never competed with that of SC. Theoretical comparisons of SI and SC [14-15] established that competitive performance could be achieved using class AB techniques but very low voltage operation was hindered by the use of strong inversion operation. As CMOS processes have headed towards smaller feature sizes and lower supply voltage, designs have been forced towards operating their transistors in moderate or even weak inversion, i.e. in the sub-threshold region, and the earlier theoretical comparison is no longer sufficiently general.

With this in mind, it has become necessary to extend the theoretical study by using the general saturated MOS model, valid for all regions of inversion. In Section II, the overall performance, expressed in terms of a figure-of-merit (FoM) embracing speed (F_C), dynamic range (DR) and power consumption (P), is derived. Section III discusses how SI performance is affected by the operating region of its transistors and Section IV provides a practical validation of the theory established in Section II. Section V describes some important non-ideal effects. Two practical sub-threshold designs are then demonstrated in Section VI and finally conclusions are given in Section VII.

2.2 Theoretical Performance Analysis

The general performance analysis presented in this section follows along similar lines to that presented earlier [14-15] for strong inversion**.** Thus, a cascade of the basic class AB memories shown in Fig. 2.1 is chosen since these form the basic configuration used by SI filters and ADCs. The SI memory has a sampling phase ϕ_1 during which an amplifier, made up from p- and n-MOS complementary transistors, is in a closed loop due to the closure of the switches ϕ_1. The voltage on its memory capacitors settles to a value determined by the input current i_{in} and the transconductance of the memory transistors. On the hold phase ϕ_2, the amplifier is open loop and the voltage held on the memory capacitors, together with the same transconductance, produces the output current i_o which is close to i_{in}. To promote analysis simplicity without loss of generality, it is assumed that the n- and p-MOS memory transistors are symmetrical, i.e. with identical transconductance parameter (β), threshold voltage (V_T) and memory capacitance ($C_{Gn} = C_{Gp} = C_G$) etc. All the parasitic capacitances are neglected leaving only the gate-to-source capacitance (C_{GS}) and gate-to-body capacitances (C_{GB}) to form the total memory capacitance

$C_{tot} = 2C_G = 2(C_{GS} + C_{GB})$. Note that C_{tot} is dominated by C_{GS} in strong inversion and by C_{GB} in weak inversion memory operation. Also, all the switches are assumed to have zero on-resistance and only thermal noise from transistors is included. Unless stated otherwise, saturation operation in the memory transistors is assumed throughout and signals are sinusoidal.

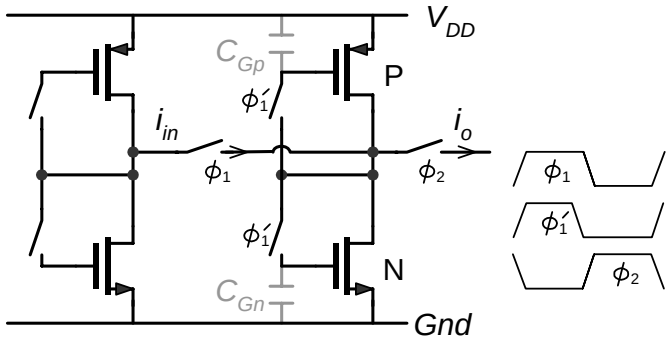


Fig. 2.1 Basic class AB SI memory configuration for FoM performance analysis

The following analysis is based on the approximate "single piece" saturation model equations for MOS transistors [16]**,** valid for all regions of inversion. It should be noted that although a compromise of the accuracy over the entire operating range is anticipated, the simple model can achieve a balanced compromise between simplicity and accuracy. In the model, the $I_D - V_{GS}$ characteristic, the small-signal transconductance g_m, the gate capacitance C_G, and the thermal noise power spectral density $S_n(f)$ of a MOS transistor are given by

$$I_D = I_S \cdot \left[\ln\left(1 + e^{\frac{V_{GS}-V_T}{2n\phi_t}} \right) \right]^2 \tag{1a}$$

$$g_m = \frac{I_D}{n\phi_t f(x)} \tag{1b}$$

$$S_n(f) = 4kT_j \left(\frac{1}{2} + \frac{1}{6} \cdot \frac{x}{f(x)^2} \right) n g_m \tag{1c}$$

$$C_G = WLC_{ox} \left[1 - \frac{1}{n} \cdot \left(1 - \left(\frac{3}{2} + \frac{f(x)}{x} \right)^{-1} \right) \right] \tag{1d},$$

with $I_S = 2\beta n\phi_t^2$, $x = I_D / I_S$ and $f(x) = \left(\sqrt{1+4x} + 1 \right) / 2$. In the equations, $\phi_t = kT/q$ is the thermal voltage, n is the slope factor ($1<n<2$), k is the Boltzmann's constant, T_j is the absolute temperature, C_{ox} is the oxide capacitance, W is the channel width, L is the channel length, and $\beta = \mu_{eff} C_{ox} W/L$ is the transconductance parameter where μ_{eff} is the effective mobility. The mobility reduction effect is modeled as $\mu_{eff} = \mu_0 / (1 + \theta \cdot V_{GT})$ where $V_{GT} = V_{GS} - V_T$, μ_0 is the low field mobility and θ is the mobility reduction parameter [16].

A. Figure-of-Merit Formulation

We now develop the figure-of-merit, FoM = $F_C \cdot DR / P$, from expressions for the memory clock frequency F_C, the power consumption P, and the dynamic range DR.

The memory's clock frequency, F_C, is related to the composite memory time-constant, $C_{tot}/(2g_m)$. Using (1a)-(1b), this gives

$$F_C = \frac{2g_m}{NC_{tot}} = \frac{2I_D}{NC_{tot} n\phi_t f(x)} \tag{2}$$

where N is a constant which depends on the desired settling accuracy (e.g. $N \approx 9$ for 0.1% settling accuracy [15]).

The average power consumption P for a maximum sinusoidal signal current is given by

$$P = \rho I_D V_{DD} \tag{3}$$

where I_D is the memory cell's quiescent current. The factor ρ needs further explanation. Under large signal conditions, the current flowing into the supply rail depends on both the circuit operation and the region of operation of its transistors. The factor ρ is the ratio of the average power supply current under maximum signal conditions to the cell's quiescent current I_D. For a class A SI memory, ρ is unity. In a class AB memory, since it can handle input signals larger than I_D, ρ >1 and is dependent on the inversion region of the memory transistors. The supply voltage V_{DD}, is determined by the threshold voltage V_T and also the operating region of the memory transistors.

Similar to continuous-time translinear MOS circuits with class AB operation where input currents can be much larger than the quiescent bias current, the output noise of class AB SI is dependent on the input current level, particularly at sub-threshold operation [17,18]. With such a noise characteristic, the signal-to-noise ratio (*SNR*) employed in [14-15] is not applicable and dynamic range (*DR*) is adopted as the performance measure to define the usable input range [18]. For the *DR* calculation, whereas the minimum input signal is limited by the total sampled noise current $\sqrt{\bar{i}_n^2}$ from the memory transistors, the maximum signal $\hat{i}_{in}$ is limited by the linearity performance. However, for the sake of simplicity it is assumed here that $\hat{i}_{in}$ is determined at a point where substantially all of the input current flows into one or other of the SI memory's composite transistors. This is in turn set by the quiescent bias current I_D and the region of inversion of the memory transistors. By using (1a) - (1c), the *DR* can be expressed as

$$DR = \frac{\hat{i}_{in}^2}{2\bar{i}_n^2} = \frac{(\alpha I_D)^2}{8 \cdot S_n(f) \cdot BW_n} = \frac{n(\alpha\phi_t f(x))^2}{\frac{8kT_j}{C_{tot}}\left(1 + \frac{1}{3} \cdot \frac{x}{f(x)^2}\right)} \tag{4}$$

where $BW_n = g_m/2C_{tot}$ is the equivalent noise bandwidth of the composite memory. The factor α is the ratio of the peak value of the maximum signal current to the quiescent current I_D. Similar to the factor ρ, α=1 for a class A memory and α>1 for a class AB memory and is dependent on the operating region of the memory transistors.

From the derived expressions (2)-(4), the general FoM of an SI memory is thus expressed as

$$\text{FoM} = \frac{F_C \cdot DR}{P} = \frac{\alpha^2}{\rho} \cdot \frac{\phi_t}{NV_{DD}} \cdot \frac{f(x)}{4kT_j\left(1+\frac{1}{3}\cdot\frac{x}{f(x)^2}\right)} \tag{5}$$

The analysis of the factors, ρ and α, is the subject of the next sub-section.

B. Calculation of Dependent Factors ρ and α

For SI memories using transistors operating in strong inversion, (1a) converges to the square-law relation, $I_D = (\beta/2n)\cdot V_{GT}^2$, and the function $f(x) \approx \sqrt{x} = \sqrt{I_D/I_S}$ since $I_D >> I_S$. For weak inversion, (1a) becomes the exponential relation, $I_D = I_S \cdot \exp(V_{GT}/n\phi_t)$, and $f(x) \approx 1$ as $I_D << I_S$. Note that, for the calculation of I_D and $f(x)$ in (1a)-(1d) in moderate inversion, one must resort to numerical computation.

For a class AB SI memory, the factor α is determined by considering how an input current i_{in} is shared between the memory transistors N and P in Fig. 2.1. The peak value of the maximum signal $\hat{i}_{in}$ is that which forces substantially all the current to flow in one transistor while substantially cutting-off the other. Following this, we have $\alpha = 4$ in the strong-inversion memory [11]. For the sub-threshold memory operation, it can be shown numerically using (1a) that, for the same quiescent current I_D, $\hat{i}_{in}$ increases further, i.e. $\alpha > 4$. This is primarily attributed to a heavier companding characteristic in a MOS transistor, i.e. from square-root companding [19] in strong inversion to natural log-exponential companding in weak inversion. For this, α can be determined analytically from the relation between the input current i_{in} and the variation in the gate overdrive voltage v_{GT} as follows

$$i_{in} = I_S e^{\frac{V_{GT}+v_{GT}}{n\phi_t}} - I_S e^{\frac{V_{GT}-v_{GT}}{n\phi_t}} = 2I_S \cdot \sinh\left(\frac{v_{GT}}{n\phi_t}\right) \tag{6}$$

Table I Summary of Analytical Performance Expressions

Performance	Strong Inversion SI	Weak Inversion SI
F_C	$\frac{4I_D}{NC_{tot}V_{GT}}$	$\frac{2I_D}{NC_{tot}n\phi_t}$
P	$\frac{3I_DV_{DD}}{2}$	$3.37\cdot I_DV_{DD}$
DR	$\frac{3C_{tot}V_{GT}^2}{8nkT_j}$	$\frac{49C_{tot}n\phi_t^2}{4kT_j}$
FoM	$\frac{1}{nNkT_j}\cdot\frac{V_{GT}}{V_{DD}}$	$\frac{7.28}{NkT_j}\cdot\frac{\phi_t}{V_{DD}}$

If the memory transistors' current ratio is assumed to be 100:1 for the maximum signal condition, it can be shown that we have the peak overdrive at $\hat{v}_{GT} \approx 2.3 \cdot n\phi_t$. From (6), this subsequently yields the peak current factor $\alpha = \hat{i}_{in} / I_D = 2\sinh(2.3) \approx 9.9$ in the class AB weak inversion memory.

Next, we consider the factor ρ. This is determined by calculating the average power supply current for the same maximum sinusoidal input current used in the determination of the factor α. For a class AB strong inversion memory with a balanced structure, ρ = 3/2 [15]. As the memory operation moves to moderate inversion, ρ gradually increases due to a larger peak input current handling capacity as described above. At weak inversion, the instantaneous supply current $I_{DD}(t)$ under a sinusoidal input current that gives an instantaneous memory transistor gate-overdrive $v_{GT}(t)$ is given by

$$I_{DD}(t) = I_S e^{\frac{(V_{GT}+v_{GT}(t))}{n\phi_t}} + I_S e^{\frac{(V_{GT}-v_{GT}(t))}{n\phi_t}} = 2I_D \cosh\left(arc\sinh\left(\frac{i_{in}}{2I_D} \right) \right) \tag{7}$$

With the peak gate-overdrive voltage at $\hat{v}_{GT} = 2.3 \cdot n\phi_t$ due to the peak input current $\hat{i}_{in} = 9.9 \cdot I_D$, the average supply current for half of the balanced memory can be computed and this yields ρ in the weak inversion class AB SI memory as

$$\rho = \frac{\frac{1}{2\pi}\int_0^{2\pi} \hat{I}_{DD}(t)\, d\omega t}{2I_D} = \frac{1}{2\pi}\int_0^{2\pi} \cosh\left(arc\sinh\left(\frac{9.9}{2} \cdot \sin(\omega t) \right) \right) d\omega t \approx 3.37 \tag{8}$$

Using the foregoing analysis, the analytical expressions for a class AB SI memory under strong and weak inversion operation were derived and these are summarized in Table I. The expressions will be particularly useful for performance discussion in the next section. In the table, due to inter-stage transmission constraints between two identical class AB SI memories, the maximum quiescent gate-overdrive for strong inversion is limited to $V_{GT} = V_T/2$ and hence we have $V_{DD} = 3 \cdot V_T$ [14]. At weak inversion, V_{DD} can be below $2 \cdot V_T$ when $I_D < I_S$. However, even though V_{DD} is inherently small, it must be made large enough to ensure saturated operation during inter-stage transmission. Since the peak gate-overdrive voltage is at $\hat{v}_{GT} \approx 2.3 \cdot n\phi_t$ and the weak inversion memory transistors require $V_{DS,min} \geq \sim 5\phi_t$ to keep saturated operation [16], the minimum supply voltage for the basic sub-threshold SI memory becomes

$$V_{DD,\min} \approx 2 \cdot (2.3 \cdot n + 5) \cdot \phi_t \tag{9}$$

For a typical value of the slope factor, n = 1.2 and ϕ_t = 26mV at 300K, we have $V_{DD,\min}$ = 0.38V.

As the improvement in sub-threshold class AB SI perfor-mance relies heavily on the ability to handle large input current, it is also instructive to discuss the effects that may influence the peak current handling. At strong inversion, mobility reduction results in less than square-law $I_D - V_{GS}$ characteristic in the memory transistors and this tends to increase the

voltage swing for the same drain current variation. Since there is a limit to the maximum voltage signal, a reduction in peak input current results. At weak inversion, a similar effect occurs due to the slope factor n, i.e. a larger n in the exponential $I_D - V_{GS}$ characteristic necessitates a larger voltage swing. In effect, the memory transistors' operation may be moved into moderate inversion over the intervals near the peak voltage swing and this results in a lower peak current handling. Another important effect can result from the asymmetry between the composite memory transistors. This makes one of the devices cut off more quickly than the other, unbalancing the drain current handling, and reducing the peak input current. In the general model equation in (1a), differences in any of the parameters except the threshold voltages contributes to a reduction in the peak input current handling but the most pronounced effect is the mismatch in the slope factors at weak inversion. The parameters α for the maximum input signal current and ρ for the average supply current including the aforementioned effects can be obtained numerically.

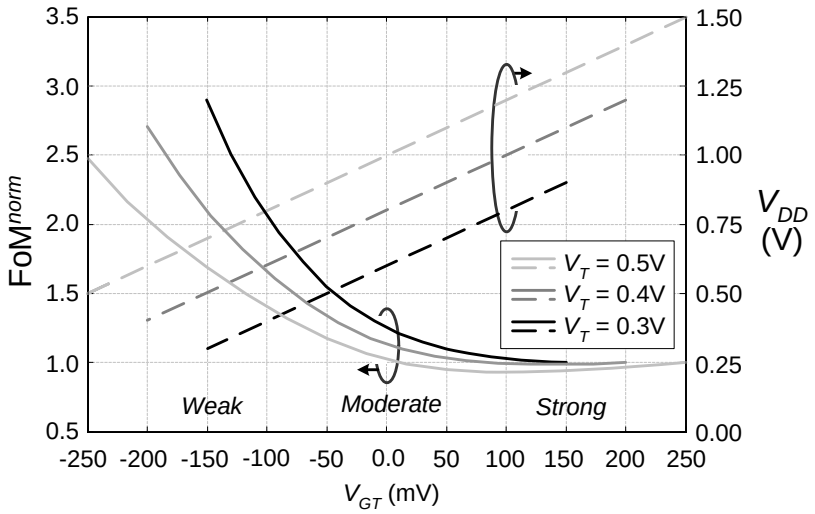


Fig. 2.2 Normalised basic class AB FoM performance and operating supply voltage V_{DD} versus V_{GT} at different memory transistor's threshold voltages.

2.3 Performance Discussions

The FoMs were calculated from (5), with α and ρ being nu-merically determined as outlined in Section II-B and with the transistor slope factor set to n=1 and mobility degradation set to θ = 0. Fig. 2.2 shows the FoMs versus V_{GT} for the class AB SI at different threshold voltages V_T = 0.5V, 0.4V and 0.3V. This corresponds to CMOS process generations spanning from 0.35μm down to 90nm according to the SIA roadmap. The range of V_{GT} is from $-V_T/2$ to $+V_T/2$ and all the plots are normalised to their corresponding strong inversion FoMs at the maximum $\hat{V}_{GT} = V_T / 2$. Also included in Fig. 2.2 is the variation of V_{DD} for the same range of V_{GT} and V_T.

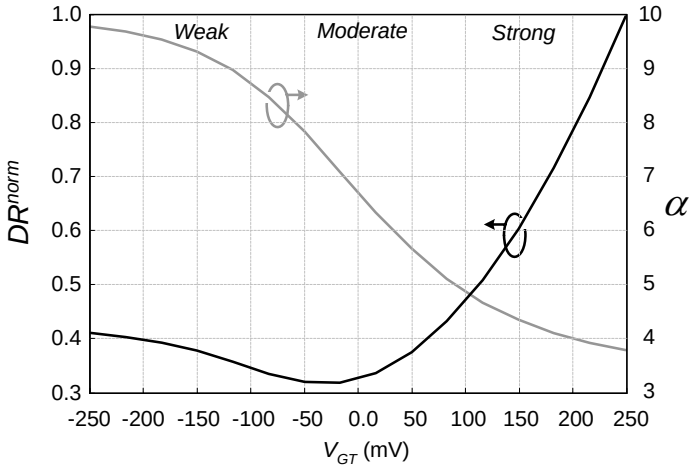
With the memory transistors in strong inversion, the FoM plots indicate that the performance of class AB SI remains almost constant with falling V_{GT}. This is also predicted by the analytical FoM expression for strong inversion operation in Table I (with $V_{GT} = V_T/2$ and $V_{DD} = 3 \cdot V_T$) and was already reported in detail in [16]. When entering moderate to weak

inversion, the FoM performance starts to rise and V_{DD} falls with falling V_{GT} and V_T indicating that class AB SI should offer better performance in modern CMOS processing. Interestingly, such a trend is in stark contrast to SC where performance is known to fall steadily with falling V_{DD}. Also note that the supply voltage level falls significantly when operating in weak inversion.

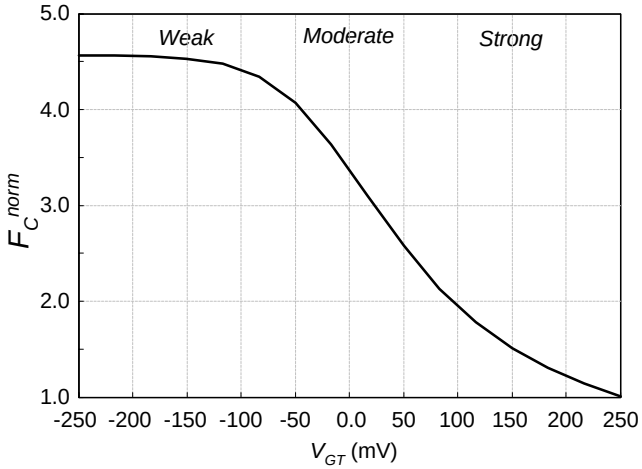
The FoM improvement at smaller gate overdrives can be explained by investigating how each of the performance vectors, *DR*, F_C and *P*, changes with V_{GT}. Consider, without loss of generality, a scenario in which V_{GT} falls but the quiescent drain current I_D in the memory transistors and the total capacitance C_{tot} remain *constant*. Based on the analysis in Section II, the plots of the performance vectors versus V_{GT}, *all normalised* to their corresponding values at $\hat{V}_{GT} = V_T / 2$ are given in Fig. 2.3(a)-(c) for V_T = 0.5V as a case example. It should be noted that, at strong and weak inversion operations, the performance dependencies in the figures follow the expressions summarized in Table I.

With strong inversion, the maximum signal current swings and signal power are almost constant [$\alpha \sim 4$ at strong inversion in Fig. 2.3(a)]. However, the reduced V_{GT} at a constant I_D necessitates the use of transistors with a proportionally higher transconductance g_m. It also produces a quadratically increased noise power since both the noise PSD and BW_{n} increase. This results in a quadratic reduction of the *DR* against V_{GT} ($DR \propto V_{GT}^2$ for strong inversion SI). Since we have kept C_{tot} constant, there is a proportional increase in memory speed F_C due to a higher g_m, $F_C \propto 1/V_{GT}$, [Fig. 2.3(b)]. The power consumption *P* falls with V_{GT} because of the reduced V_{DD} and almost constant average peak supply current [$\rho \sim 1.5$ at strong inversion in Fig. 2.3(c)]. Therefore, the net result is an almost constant FoM for SI with strong inversion, as evident in Fig. 2.2 and Table I, despite falling V_{GT}.

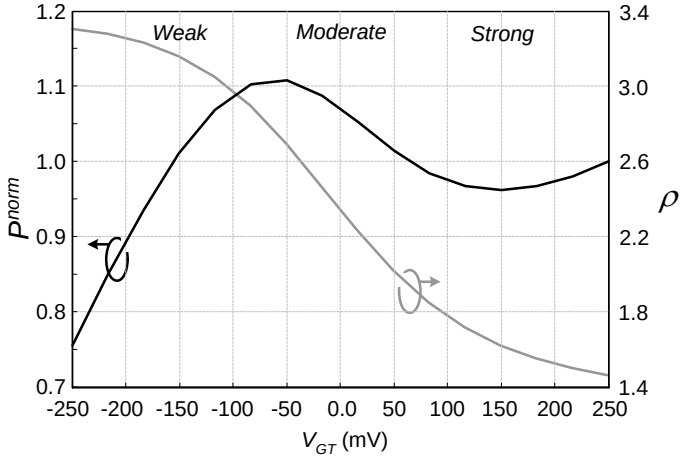
With moderate to weak inversion, as V_{GT} falls, the memory transistors' characteristics are gradually changed from a square-law to an exponential relationship. This yields an increasing maximum signal current swing and hence signal power, even though I_D is constant [see α rising to ~ 9.9 from the moderate to the weak inversion region in Fig. 2.3(a)]. Similarly, the transconductance g_m, and hence noise power, must increase to accommodate the reduced V_{GT}. However, the increases are slower than with strong inversion and so the *DR* drops more gradually and eventually stays almost constant [see DR^{norm} at moderate to weak region in Fig. 2.3(a)]. Similarly, the increase in the memory speed F_C is also less [see F_C at moderate to weak region in Fig. 2.3(b)]. The power consumption *P* rises slowly in moderate inversion because V_{DD} falls slowly while the average supply current falls more quickly due to the increased signal swing [see ρ rising to~3.37 from moderate to weak region in Fig. 2.3(c)]. Eventually in weak inversion, the



(a)



(b)



(c)

Fig. 2.3 Theoretical variations of basic class AB SI performances against V_{GT}.

Table II Extracted MOS Model Parameters for CD4007 Transistor Arrays

Parameter	pMOS	nMOS
I_S (A)	2.2 x 10^{-3}	7.2 x 10^{-3}
$\|V_T$ (V)$\|$	1.322	1.518
n	1.415	2.284
θ (V^{-1})	0.1839	0.1755

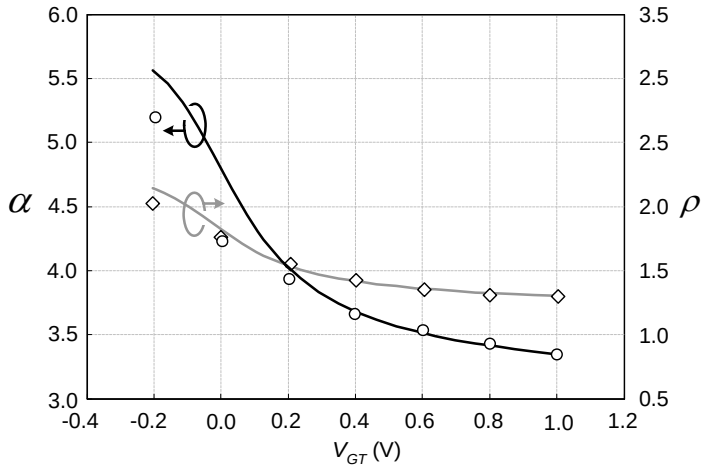


Fig. 2.4 Measured (markers) and simulated (solid) plots of α and ρ versus V_{GT}.

average supply current stays almost constant and thus P falls proportionally with V_{DD} [see P falling at weak inversion in Fig. 2.3(c)].

With these performance dependencies, the overall effect is that FoM is improved for class AB SI operating in moderate to weak inversion as depicted in Fig. 2.2. As V_{GT} falls in weak inversion V_{DD} falls proportionally and FoM rises inversely as indicated in Table I.

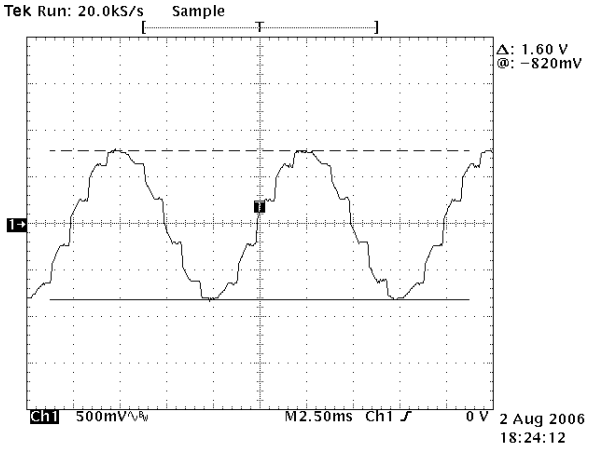
2.4 Analysis and Performance Verifications

A. Experimental Performance

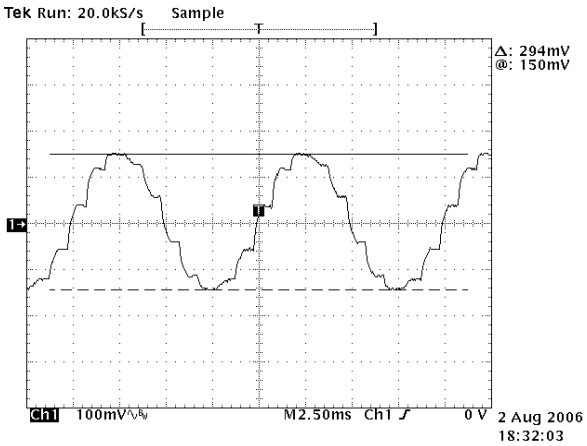
The analysis results obtained in Section II, particularly the input signal handling and signal-dependent supply current, are first verified by a breadboard implementation of the basic balanced class AB SI memory, using CD4007 transistor arrays as CMOS memory transistors and CD4016 as memory switches. Listed in Table II are the parameters of the MOS equation in (1a) for both the p- and n- MOS transistor arrays extracted to obtain best overall fit to their

measured characteristics in saturation over the operating range from strong to weak inversion with the help of MATLAB optimization tools. The maximum clock frequency F_C was set at 1kHz, and the sinusoidal input at 100Hz. The input *V*-to-*I* and output *I*-*V* converters were implemented by AD844 operational current amplifiers and linear resistors to facilitate voltage-domain measurement. For this measurement, the gate-overdrive voltages V_{GT} were adjusted via the supply voltage V_{DD} to set the operating region of the memory transistors. Since this also affected the transconductance, the memory bandwidth was maintained by adding external memory capacitors which could be tuned for memories operating in strong or weak inversion.

Fig. 2.4 shows both the measured peak signal current factor α and the measured peak average supply current factor ρ versus V_{GT}. Also given are the plots of α and ρ obtained from numerical calculation based on the theoretical analysis where the maximum errors as compared with the measured results are about 6.7% for α, and 4% for ρ. From the figures, it can be noticed that both α and ρ at V_{GT} = –0.2V, i.e. weak inversion memory operation, are somewhat smaller than the theoretical predictions in (6) and (7). This is because the slope factor *n* and the parameter I_S of the p- and n-MOS memory transistors are considerably different as evident in Table II. In order to illustrate the voltage *compression* characteristic in the weak inversion SI, the transient gate-source voltage waveforms of the class AB memories with strong inversion (V_{GT} = 0.8V) and weak inversion (V_{GT} = -0.2V) at their corresponding *peak* input currents were measured, and these are given in Fig. 2.5(a) and 5(b) respectively. Whereas the signal voltage swing in strong inversion is of the order of the threshold voltage V_{TP} or V_{TN} in Table II, that of the weak inversion memory is compressed to only a few hundred millivolts.



(a) [Continued]



(b)

Fig. 2.5 Voltage waveforms at the basic class AB SI memory's gate under maximum sinusoidal input (a) at strong inversion and b) at weak inversion operating conditions.

B. Simulated FoM Performance

Following the breadboard experimental verification, the theoretical performance of sub-threshold class AB SI in IC implementation is demonstrated via simulation using 3.3V, 0.35μm CMOS process data. The simulation models for MOS transistors are BSIM3v3. The extracted model parameters for the selected unit transistor dimensions, i.e. $(W/L)_p$ = 4.6μm/2.5μm and $(W/L)_n$ = 3.0μm/4.0μm, are summarised in Table III. Notice from the table that the p- and n-MOS transistors of the process exhibit good symmetrical characteristics (except V_T but this has no impact on the performance). Similar to the experimental test, the operating condition of the memory transistors was set by varying V_{GT} through V_{DD}. Although there was flexibility to simultaneously maintain the memory's transconductance and capacitance at different V_{GT}s by adjusting both W and L of the memory transistors, we chose to maintain the transconductance by only modifying the width W, which enabled us to use *multiples* of the unit transistor. This however did not maintain the memory speed (F_C = 1MHz*)* and so we compensated this by adding a sufficient number of unit capacitors. The total composite memory's transconductance and capacitance were held at $g_{mp} + g_{mn}$ = 50μS and C_{tot} = 3.5pF. In simulation, the cascade configuration of class AB memories in Fig. 2.1 was driven by an ideal input current source and was loaded by an identical 'diode-connected' memory cell.

Table III Extracted MOS Model Parameters for 0.35µ Unit Transistors

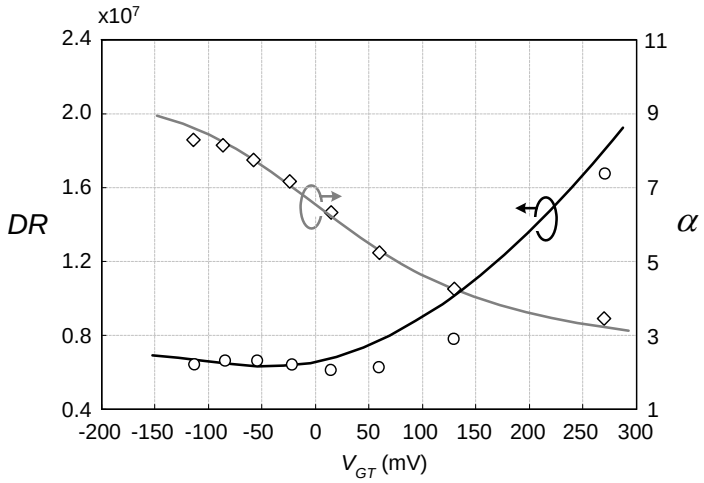
Parameter	pMOS	nMOS
I_S (A)	255 x 10^{-9}	231 x 10^{-9}
$\|V_T$ (V)$\|$	0.71	0.50
n	1.28	1.26
θ (V^{-1})	0.805	0.285
WLC_{ox} (F)	44.8 x 10^{-15}	56.4 x 10^{-15}

Table IV-A Extracted MOS Model Parameters for 0.18µ Unit Transistors

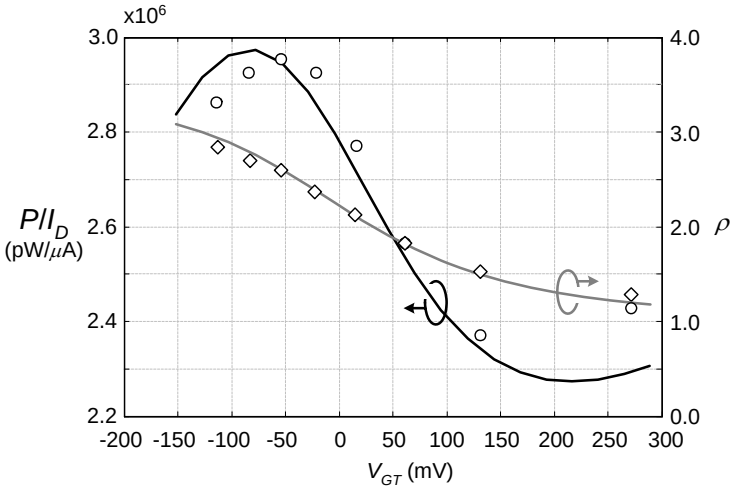
Parameter	pMOS	nMOS
I_S (A)	643 x 10^{-9}	585 x 10^{-9}
$\|V_T$ (V)$\|$	0.22	0.33
n	1.44	1.35
θ (V^{-1})	0.531	0.656
WLC_{ox} (F)	245.3 x 10^{-15}	205.6 x 10^{-15}

Table IV-B Extracted MOS Model Parameters for 90nm Unit Transistors

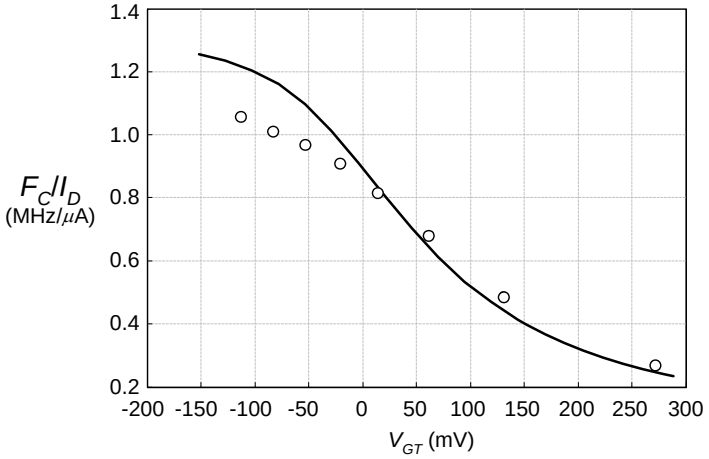
Parameter	pMOS	nMOS
I_S (A)	480 x 10^{-9}	487 x 10^{-9}
$\|V_T$ (V)$\|$	0.29	0.23
n	1.16	1.14
θ (V^{-1})	0.943	0.488
WLC_{ox} (F)	171.2 x 10^{-15}	184.5 x 10^{-15}



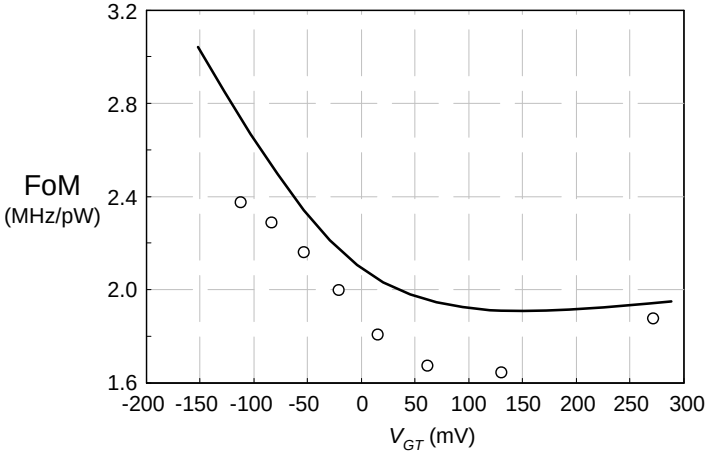
(a) [Continued]



(b)



(c)

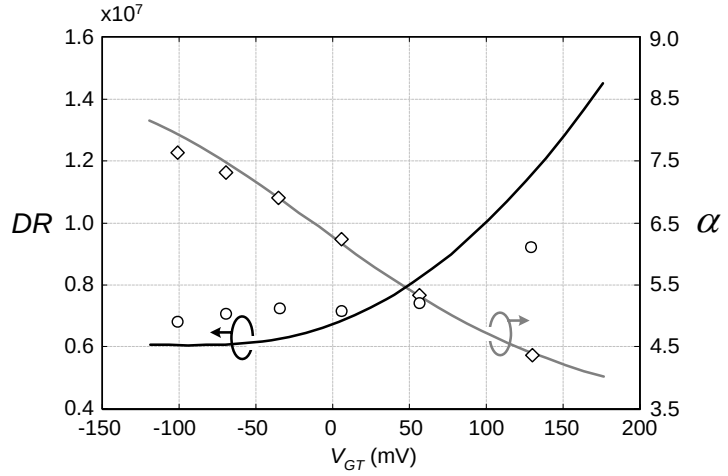


(d)

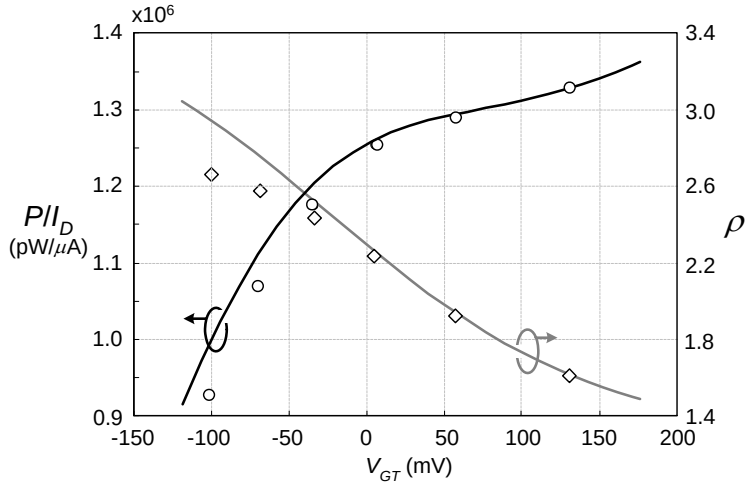
Fig. 2.6 Simulated (markers) and theoretical (solid) plots of basic class AB SI performances in 0.35μm CMOS process.

Fig. 2.6(a)-(d) show the simulated results of *DR*, P/I_D, F_C/I_D and FoM versus V_{GT} respectively, along with the plots of α in Fig. 2.6(a) and ρ in Fig. 2.6(b). Normalising the operating speed and power for I_D removes the variation of I_D with V_{GT} and this enables easier comparison with the theoretical plots of Fig. 2.2 and Fig. 2.3. The calculated performances are also included in the figures where the maximum error percentages for each plot is about 8.6% for α, 4.0% for ρ, 32.5% for *DR*, 5.1% for P/I_D, 15.7% for F_C/I_D and 17.3% for FoM. Some of the errors are quite significant due to an accuracy compromise of the extracted parameters needed to obtain good overall fit of the approximate model equation in (1a). However, a close relationship is observed in Fig. 2.6(a) to (d) between the calculated and simulated characteristics as the memory operation moves from strong to weak inversion. In this 0.35μm CMOS process with the average $V_T = (V_{TP} + V_{TN})/2 \approx 0.6$V (see Table III), the FoMs of weak inversion SI are better than those of the strong inversion counterpart by a factor of 1.27 from simulation and a factor of 1.5 from calculation [Fig. 2.6(d)]. Although the improvement factor is modest (because the process has large V_T), it should be noted that the strong inversion memory requires $V_{DD} = 1.75$V whereas the weak inversion SI operates at about $V_{DD} = 1.0$V which is a reduction by more than 40%.

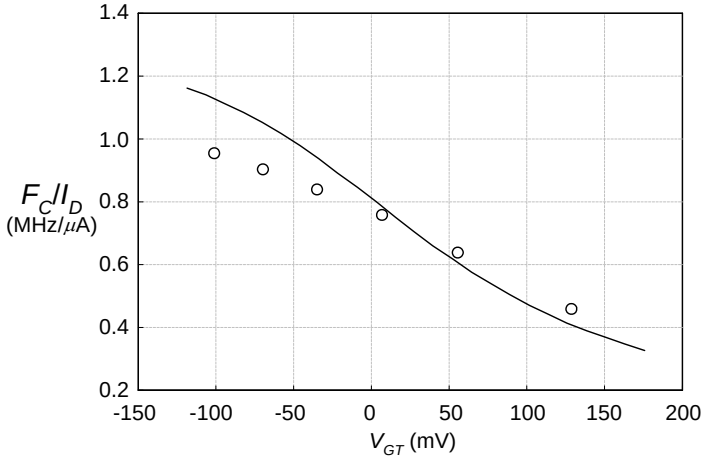
To show further the performance trend of the sub-threshold class AB SI memory, the same memory test as above was also conducted using low-threshold transistors of more advanced 1.8V 0.18μm and regular transistors of 1.2V 90nm CMOS processes with BSIM 3v3 MOS models. For the 0.18μm process, the unit transistor dimensions were chosen at $(W/L)_p$ = 9.5μm/3.0μm and $(W/L)_n$ = 6.5μm/6.0μm. For the 90nm process, the unit transistor dimensions were at $(W/L)_p$ = 5.0μm/2.5μm and $(W/L)_n$ = 3.0μm/5.5μm. From the simulated transistors' characteristics, the MOS parameters were extracted for theoretical computation and are summarized in Table IV-A for the 0.18μm process, and Table IV-B for the 90nm process. With similar total memory transconductance and capacitance to those of the 0.35μm CMOS design, the simulated performance vectors versus V_{GT} are plotted in Fig. 2.7(a)-(d) and Fig. 2.8(a)-(d), along with the calculated results. For the 0.18μm process, the maximum error percentages for each plot are about 4.9% for α, 9.8% for ρ, 25% for *DR*, 8.1% for P/I_D, 18% for F_C/I_D and 12.8% for FoM. For the 90nm process, the maximum error percentages for each plot are about 7.8% for α, 7.4% for ρ, 21.2% for *DR*, 2.6% for P/I_D, 12.1% for F_C/I_D and 12.9% for FoM. Despite these errors, similar dependencies between the calculated and simulated characteristics are observed in all the performance metrics and for both processes. For the 0.18μm process, it is noticed from the α and ρ plots at weak inversion that both the peak current handling and supply current are reduced compared to those obtained from 0.35μm and 90nm CMOS. This is primarily due to the effect of asymmetrical slope factors *n* between the employed CMOS devices [see Table IV-A]. With such low threshold voltage processes, it is shown in Fig. 2.7(d) and 8(d) that the weak inversion SI has a FoM improvement of more than two for both simulations and calculations. The required supply voltage of the weak inversion SI is at V_{DD} = 0.35V for the 0.18μm process, and $V_{DD} = 0.36$V for the 90nm process. These are less than half of the supply voltage used for the strong inversion memories in the 0.18μm and 90nm processes ($V_{DD} = 0.81$V and 0.74V respectively).


x10^7
1.6
1.4
1.2
1.0
0.8
0.6
0.4
DR
9.0
8.5
7.5
6.5
5.5
4.5
3.5
α
-150
-100
-50
0
50
100
150
200
V_GT (mV)

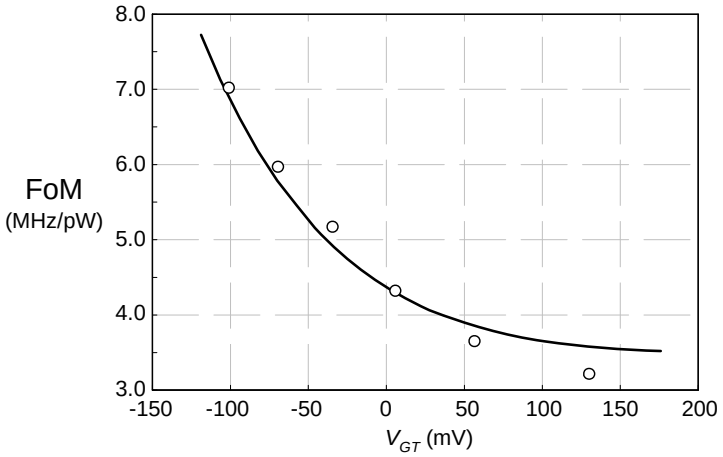
(a)


x10^6
1.4
1.3
1.2
1.1
1.0
0.9
P/I_D
(pW/μA)
3.4
3.0
2.6
2.2
1.8
1.4
ρ
-150
-100
-50
0
50
100
150
200
V_GT (mV)

(b)

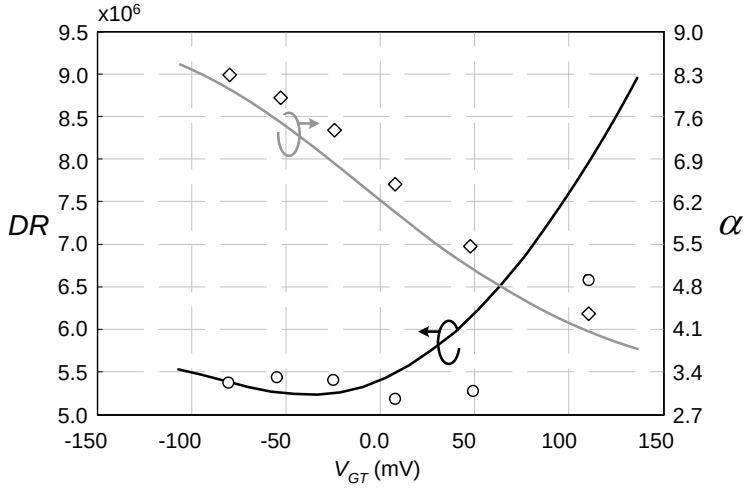

1.4
1.2
1.0
0.8
0.6
0.4
0.2
F_C/I_D
(MHz/μA)
-150
-100
-50
0
50
100
150
200
V_GT (mV)

(c)

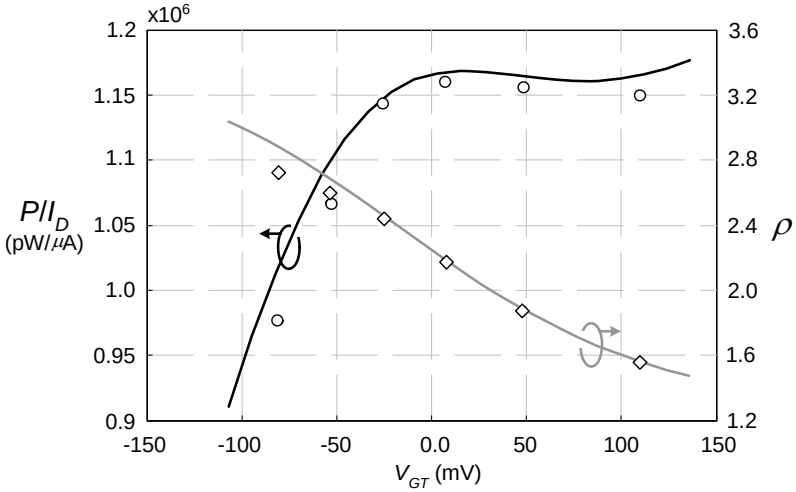


(d)

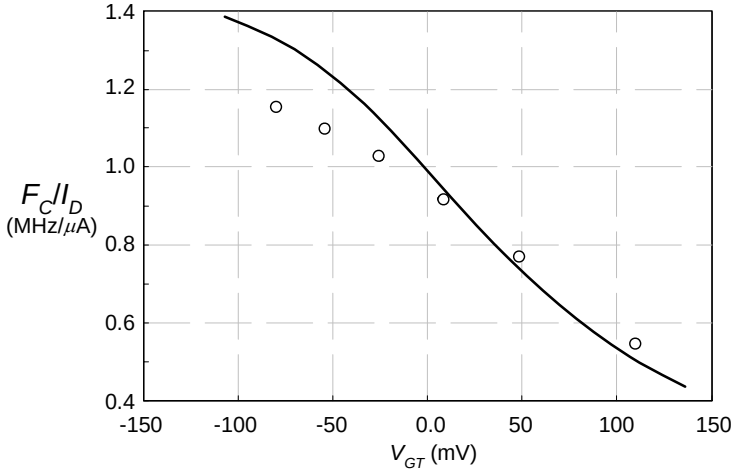
Fig. 2.7 Simulated (markers) and theoretical (solid) plots of basic class AB SI performances in 0.18μm CMOS process.



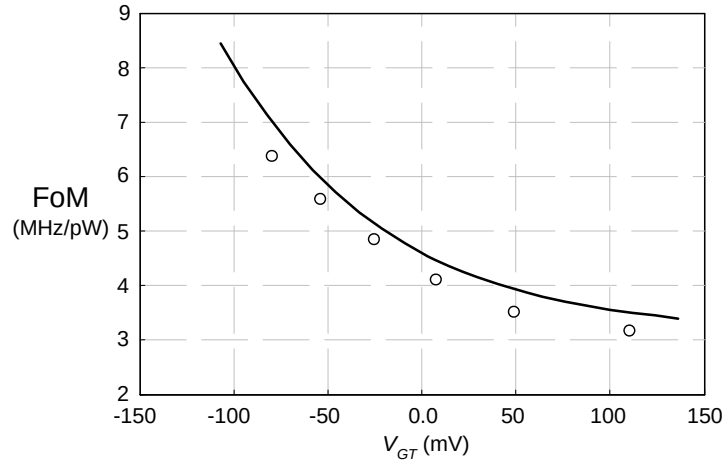
(a)



(b)



(c)



(d)

Fig. 2.8 Simulated (markers) and theoretical (solid) plots of basic class AB SI performances in 90nm CMOS process.

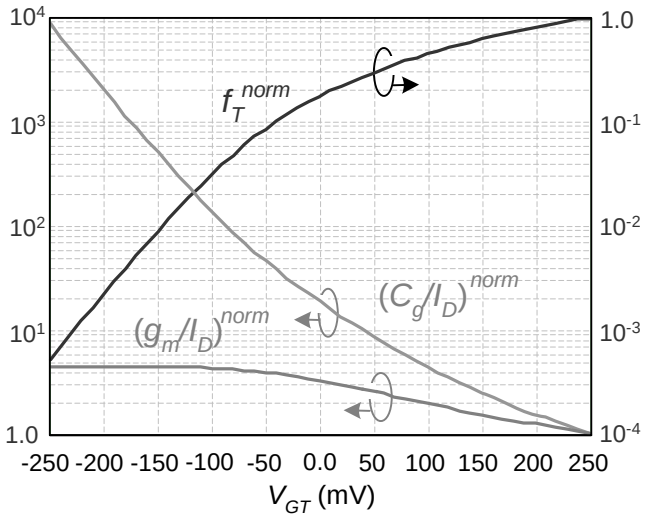


Fig. 2.9 Normalised g_m/I_D and C_g/I_D and f_T characteristics versus V_{GT}.

2.5 Non-ideal Behaviours

This section describes important second-order non-idealities that affect SI performances in the sub-threshold operating region, specifically in terms of speed and transmission accuracy. These considerations are useful in designing and optimising sub-threshold SI circuits in practice.

A. Speed Limitation

It is generally known that the transition frequency f_T, which indicates the intrinsic maximum usable frequency in a MOS transistor at a given channel length L, is reduced with decreasing gate-overdrive voltage V_{GT}. In particular, it has been shown in [16] that, at strong inversion, f_T is proportional to V_{GT}. Eventually at weak inversion, it becomes dependent on the drain current I_D which is now related to V_{GT} exponentially, making f_T fall faster with V_{GT} than with strong inversion operation.

To investigate how this impacts speed performance, we have plotted the transition frequency $f_T = g_m/2\pi C_G$ and the g_m/I_D and C_G/I_D ratios versus V_{GT} under a *constant* channel length L, by using (1a)-(1b) and (1c), and these are shown in Fig. 2.9. To facilitate the discussion, all the plots are normalized to their corresponding values in strong inversion operation with V_{GT} = 0.25V. From the normalised f_T characteristic in Fig. 2.9, when the transistor operation moves from the strong inversion to weak inversion, with V_{GT} = –0.1V as an example, f_T drops by more than thirty times. As indicated from the normalised g_m/I_D and C_G/I_D plots, such a significant f_T degradation is mainly attributed to a sharp increase in C_G/I_D, because a small V_{GT} in a sub-threshold MOS transistor requires a larger aspect ratio W/L for the same g_m and/or I_D when compared with strong inversion operation. At a constant channel length L, this results in a larger width W and hence a larger gate capacitance C_G ($\propto W{\cdot}L$).

While design for sub-threshold operation has dramatically worsened the transistor's f_T, this does not imply a worsening of the SI memory's operating speed. This is because the memory capacitance C_G of a particular design, whether in strong or weak inversion, is chosen to meet a noise specification. So a sub-threshold design having the same speed as a strong inversion design can be achieved simply by choosing transistors with a larger W and smaller L (but with the same area $W{\cdot}L$).

In SC, the situation is in absolute contrast. Unlike its SI counterpart, the gate capacitance C_G appears as a parasitic component. This creates non-dominant poles which may give rise to under-damped settling and even circuit instability. As a result, the considerably larger C_G, of a sub-threshold MOS transistor adversely affects the SC speed performance.

B. Transmission Accuracy

In SI, there are three major non-idealities that affect the memory's transmission accuracy: signal-dependent settling, charge injection of the memory's switches and finite output-input conductance ratio [1]. Since a class AB sub-threshold SI must handle input current which is much larger than its quiescent bias current, the transconductance g_m of the composite memory is heavily signal-dependent. This makes the memory's settling time considerably signal-dependent. However, since larger input current gives a larger g_m and hence a faster settling time, proper design of the memory's settling at a small input automatically

guarantees the required accuracy for the entire input range. As a result, the signal-dependent settling should not have a significant effect on the memory accuracy.

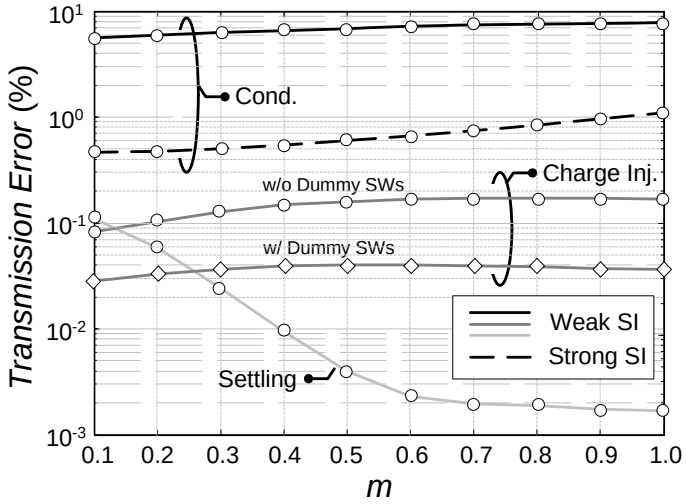


Fig. 2.10 Simulated error performances of basic class AB SI from individual error source under strong and weak operations.

Due to inherently small signal voltage swings in sub-threshold SI, the signal-dependent component from charge injection is also small. A more critical issue is the absolute charge of the memory switches as this can give rise to signal-dependent error through the signal-dependent g_m of the composite memory. Nevertheless, this can be effectively reduced by the use of a balanced SI structure and the dummy switch technique [20].

As explained earlier, the small V_{GT} associated with sub-threshold operation results in transistors with larger width W and smaller length L compared to their strong inversion counterpart. The transmission error resulting from finite output-input conductance ratio arises because of channel length modulation ($\propto 1/L$) and feedback to the gate capacitance C_G via the drain-gate overlap capacitance C_{DG} ($C_{DG}/C_G \propto 1/L$). So, output-input conductance ratio transmission errors are correspondingly higher in sub-threshold operation and must be accommodated by the chosen circuit technique.

The contribution of each non-ideal effect for each region of operation, including signal-dependent settling, charge injection and finite conductance ratio, was examined via simulation of the individual transmission errors. To enable the study, certain components or parameters were made ideal in the memory under test so that only the non-ideality under consideration became the major error source: to eliminate charge injection errors, ideal memory switches were employed; to suppress conductance errors, the memory was equipped with an ideal active feedback amplifier; to minimize the signal-dependent settling, considerable extension of the sampling period was allowed.

The resulting individual memory transmission error for the balanced weak inversion memory using 0.18μm CMOS process data with V_{GT} = –0.10V are depicted in Fig. 2.10. The errors are plotted versus the input current modulation index m, defined as the ratio of the signal current to its maximum value, $i_{in}/\hat{i}_{in}$. It is seen that the settling error is small and improves with larger m due to a higher g_m. The charge injection error is practically independent of the input

signal level due to the balanced structure and it is effectively reduced by using dummy switches. Contributing most to the memory's overall error is that resulting from the finite output-input conductance ratio. Compared with a similar strong inversion design (V_{GT} = –0.13V) the error is about ten times worse.

In summary, the basic class AB memory has higher transmission error when operated in weak inversion. To achieve good performance, these errors must be controlled by more sophisticated circuit techniques and two such examples are described in the next section.

2.6 Practical Designs

A. Cascode Design

To demonstrate the feasibility of the sub-threshold SI technique in practice, we have designed and simulated a balanced weak inversion class AB SI memory in 0.35μm CMOS. The design was based on the memory cell tested in Section IV-B at V_{DD} = 1.0V with the cascoded memory arrangement for accuracy enhancement [10]. For the test configuration, the memory cell was driven by a differential current source and the load was formed by an identical diode-connected memory. The operating clock frequency was at 1MHz and the total quiescent drain current was I_D = 2μA. The supply regulation scheme in [10] was also adopted to regulate the quiescent current and this increased the operating supply voltage to V_{DD} = 1.25V to accommodate the additional voltage headroom. The designed transistor dimensions are as follows: for memory transistors, $(W/L)_p$=588μm/2.5μm and $(W/L)_n$= 384μm/4.0μm, for cascoded transistors, $(W/L)_{Cp}$= 588μm/0.35μm and $(W/L)_{Cn}$ = 384μm/0.35μm.

The simulated accuracy performance of the weak inversion memory cell versus modulation index, m is summarised in Table V-A for extreme process and temperature conditions. The table indicates that a memory error of less than 0.8% can be achieved over the entire input range. Also, at m = 1, the simulated THD is less than –40dB even under extreme conditions. Table VI summarises the practical performances. It should be noted that as compared to the simulated plots of Fig. 2.6(a) to 6(c), due to the balanced structure, F_C/I_D is reduced by half whereas DR is increased by slightly less than twice (because of the additional noise from cascoded devices and switches). This yields the FoM of the balanced cascoded SI memory slightly less than the simulated plots at weak inversion of the basic class AB memory (Fig. 2.6(d)).

Table V-A Transmission Performance of Weak Inversion Cascoded Class AB SI

Modulation Index (m)	Transmission Error (%)		
	Slow 100°C	Typical 40 °C	Fast 0°C
0.2	0.14	0.15	0.25
0.4	0.15	0.11	0.28
0.6	0.18	0.15	0.25
0.8	0.19	0.19	0.54
1.0	0.35	0.25	0.78

Table V-B Transmission Performance of Weak Inversion Class AB S2I

Modulation Index (m)	Transmission Error (%)		
	Slow 100°C	Typical 40 °C	Fast 0°C
0.2	0.20	0.08	0.17
0.4	0.31	0.15	0.27
0.6	0.51	0.33	0.50
0.8	0.77	0.55	0.78
1.0	0.98	0.78	0.96

Table VI Typical Performance Summary of Practical Balanced SI Memories

Memory design	0.35μ Cascoded SI	0.18μ S^2I
pMOS memory size	588μ/2.5μ	304μ/3.0μ
nMOS memory size	384μ/4.0μ	208μ/6.0μ
Analog voltage	1.0V	0.35V
Total quiescent drain current	2μA	4μA
F_C	1MHz	1MHz
P	5.8μW	2.6μW
DR	$1.24\text{x}10^7$	$0.66\text{x}10^7$
FoM*	2.14MHz/pW	2.54MHz/pW
Transmission Error** (@ m =1)	0.78%	0.96%
THD** (@ m =1)	-40.9dB	-38.6dB
Supply voltage	1.25V	0.6V

* Calculated from analog voltages

** Worst case performances under fast processes and 0°C

B. Two-Step Design

Due to insufficient voltage headroom, the cascoded memory enhancement becomes ineffective for the weak inversion SI in the 0.18μm CMOS using low-voltage transistors. One of the existing techniques readily applicable at very low supply voltages is the class AB two-step sampling SI, S^2I [9]. Due to the use of a coarse and fine parallel memory configuration, some FoM degradation is expected in the weak inversion S^2I memory. Since the settling of input signal is continued from coarse to fine phases, the S^2I memory exhibits identical speed to its basic counterpart. In terms of power, as the fine memory only needs to handle the small residue input current left from the coarse phase, additional dynamic current close to the memory quiescent bias is required. Due to a high average drain current over the quiescent bias (ρ ~ 3.37) in the weak inversion memory cell, this only slightly increases the total power consumption. For the noise performance, the inclusion of the fine memory doubles the total noise power compared to that of the basic cell. By taking these considerations into the general FoM expression of the basic class AB SI in (5), the FoM of class AB S^2I in weak operation can be given as

$$\mathrm{FoM}_{S^2I}^{weak} = \frac{2.8}{NkT_j} \cdot \frac{\phi_t}{V_{DD}} \tag{10}$$

Comparing this with the FoM of the basic weak inversion SI in Table I, overall performance degradation by about a factor of 2.6 is expected from the use of the S^2I technique. For the 0.18μm process employed in Section V-B, this makes the FoM performance of the S^2I memory slightly less than its basic counterpart in strong inversion. Although the enhancement technique seems to undo the FoM benefit of weak inversion SI, such a drawback should be outweighed by the ability to operate at a very low supply voltage with good accuracy.

The balanced class AB weak inversion S^2I memory using low voltage transistors in the 1.8V 0.18μm process was designed at F_C = 1MHz where the transistor dimensions for both coarse and fine memories are given at $(W/L)_p$ = 304μm/3.0μm and $(W/L)_n$ = 208μm/6.0μm. The supply voltage was 0.35V and the total quiescent bias current was 4μA. With the regulation circuitry, the supply was increased to 0.6V. As summarized in Table V-B, simulation indicates an accuracy of better than 1.0% under extreme processing and temperature. Also from the performance summary in Table VI, the simulated THD at m = 1 is –38.6dB and the THD at m = 0.86 is –40dB. It should be noted that the simulated FoM of the balanced S^2I memory is about 20% less than the simulated FoM of the basic memory at strong inversion operation as indicated in Fig. 2.7(d).

2.7 Conclusions

The behaviour of the basic class AB SI memory with transistors operating in their sub-threshold region has been studied through the theoretical assessment of its overall performance using the general MOS equations valid for all regions of operation. Thanks to its ability to handle larger input signal current levels, basic sub-threshold SI operation has better performance with lower supply voltage than its strong inversion counterpart and this performance improves with the reducing threshold voltages which come with successive CMOS generations.

The theoretical performance analysis used a figure-of merit which embraced dynamic range, speed and power consumption and the results were extensively verified by both experiment and simulation using actual CMOS process data. It was found that while the theory was a little optimistic, it demonstrated similar behaviour and confirmed that sub-threshold operation gives worthwhile performance gains.

However, it was also found that sub-threshold design produced transistors with a large aspect ratio. This gave the basic class AB memory poor accuracy because the high output conductance produced large transmission errors. Enhanced circuit design was needed to overcome this shortcoming of the basic memory.

Two enhanced circuit styles were investigated: cascoding using a 0.35μm CMOS process, and two-step sampling using a 0.18 μm CMOS process. These designs were successful in restoring the accuracy but at some further cost to performance. Nevertheless, these designs demonstrated in a practical way that sub-threshold SI can produce much lower voltage operation without loss of performance when compared with strong inversion design. While the achievement of accurate low voltage operation and the realization of the full promise of performance improvement remain a challenging research goal, this work has nevertheless

demonstrated that sub-threshold SI is a viable analogue technique for the implementation of very low voltage CMOS circuits and systems, such as emerging implantable biomedical electronic devices.

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3. Very Low Voltage Mixer Techniques for 0.5-V Operation

3.1. Introduction

With potential applications in environmental moni-toring, surveillance, health-care, security etc, wireless sensor networks have been envisaged as holding promise for future ubiquitous wireless computing systems [1]. Among the essentials to a full scale deployment of such sensor networks are analogue techniques that can enable efficient operation at a very restricted supply voltage level. In response to this demand, various innovative circuits fully compatible with an ultra-low supply voltage in nanoscale CMOS have been demonstrated. These include an OTA for filter applications [2], passive analogue sampling circuits [3], [4], and an active track-and-hold circuit [5] for ADC applications — all operating at a 0.5-V supply voltage using *standard* transistors. Also developed were techniques for time-constant tuning based upon variable capacitors [2] and sub-threshold MOSFET operation [6,7]. To complement the ultra-low supply scenario, a circuit arrangement for a mixer with a commensurate supply voltage requirement is introduced in this letter, with the targeted application for baseband demodulators of wireless sensor transceivers.

3.2 Circuit Structure

Traditionally, a mixer topology for down-conversion and baseband applications makes use of four cross-coupled MOS transistors operated in *strong* inversion and triode region, with one of their drain/source terminals connected to a virtual ground [8], [9]. At a reduced supply voltage however, such a topology shares a similar difficulty to conventional tunable MOS resistors for integrated continuous-time filters [2]. Both require excessive headroom, particularly for the input voltages at the gate terminals, so as to keep the transistors in their strong triode operation at all times. Thus, without the use of a charge pump which may entail a reliability issue, the quad MOS transistors can be pushed into sub-threshold conduction, especially at the negative swing of the gate inputs. In effect, the mixer is turned to operate in a current commutation manner, where each of the transistor pairs takes turn to conduct during each half of the input cycle. This in turn degrades the linearity since the dependence of g_{DS} on V_{DS} is now highly nonlinear and can no longer be suppressed by virtue of the double-balanced structure [7]. Moreover, the conversion gain of the mixer is degraded due to a significant reduction of g_{DS} at sub-threshold conduction. With a continued supply reduction to a very low voltage, the mixer may cease to operate entirely.

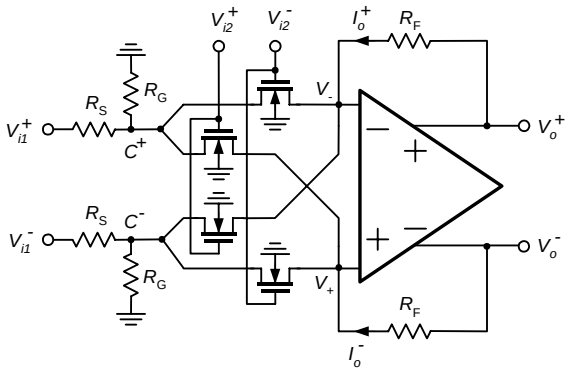


Fig. 3.1 Very low voltage mixer topology

Fig. 3.1 shows an enhanced low-voltage mixer topology where it resembles the conventional triode-biased mixer, but with the incorporation of the linear resistors R_S and R_G at the drain/source terminals of the quad transistors. In the circuit, one of the differential input signals is applied at the resistors' terminals, $V_{i1}^{+/-}$, and the other at the transistors' gates, $V_{i2}^{+/-}$. The mixing output current $I_o^{+/-}$ is converted to the differential voltage, $V_o^{+/-}$, by the feedback resistors R_F. The resistor network serves as a voltage division that essentially pulls down the drain/source terminals of the quad MOS transistors below the quiescent bias voltage of $V_{i1}^{+/-}$(typically at a mid-supply level), thereby enlarging the gate overdrives and pushing the devices' operation back towards strong inversion. In addition, R_S and R_G together form an equivalent linear resistor in series with the quad transistors, yielding a significant improvement in the linearity as it helps suppress the effect of the nonlinear g_{DS}-V_{DS} characteristics contributed by the transistors, especially when they are in sub-threshold conduction. It is worth noting that the grounded resistors R_G in Fig. 3.1 can be replaced by a current source to produce a similar extended operation in the transistors, but this is not the choice here due to the associated flicker noise.

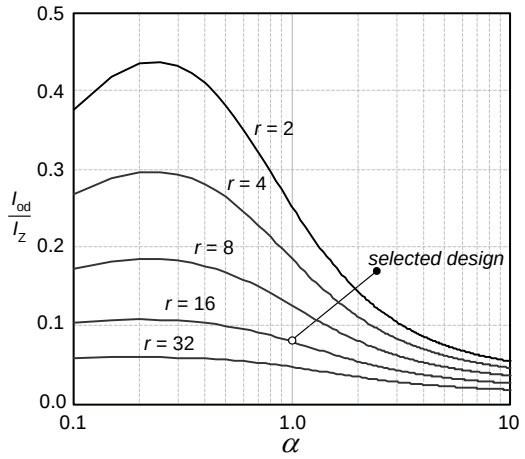


Fig. 3.2 Plot of the normalized differential peak output current versus the design parameters r and α

3.3 Mixer Design

Of prime importance is a careful design methodology of the very low voltage mixer, due to a limited available signal swing at a low supply voltage. Also, due to such a wide coverage of the MOSFET's operation, it is obliged to employ a general current-voltage MOS equation valid for all regions in the analysis. This may be given by [9]:

$$I_{DS} = 2m\varphi_t^2\beta\left(\ln^2\left[1+e^{\frac{V_{GB}-V_{T0}-mV_{SB}}{2m\varphi_t}}\right]-\ln^2\left[1+e^{\frac{V_{GB}-V_{T0}-mV_{DB}}{2m\varphi_t}}\right]\right) \tag{1}$$

with $$m=\left(1-\gamma/2\sqrt{V_{GB}-V_{T0}+\left(\gamma/2+\sqrt{\varphi_0}\right)^2}\right)^{-1}$$

where $\beta = \mu C_{ox}W/L$ is the transconductance parameter, $\varphi_t = kT/q$ is the thermal voltage, μ is the carrier effective mobility in the channel, C_{ox} is the gate-oxide per unit area, W and L are the channel width and length, V_{T0} is the threshold voltage at $V_{SB} = 0$, γ is the body effect coefficient, φ_0 is a characteristic potential, and m is the slope factor. It is noted that the short-channel effects and the dependence of the mobility on the transversal field are not included in (1). By using (1), and applying KCL at the common node C^+ or C^- ($C^{+/-}$) of the circuit in Fig. 3.1, the following normalized equation can be obtained:

$$\begin{aligned}\frac{v_{i1}^{+/-}-v_C^{+/-}}{r} &= \frac{v_C^{+/-}}{\alpha r}-\left(\ln^2\left[1+e^{v_{i2}^{+}-v_T-mv_C^{+/-}}\right]-\ln^2\left[1+e^{v_{i2}^{+}-v_T-mv_{+/-}}\right]\right)\\ &\quad -\left(\ln^2\left[1+e^{v_{i2}^{-}-v_T-mv_C^{+/-}}\right]-\ln^2\left[1+e^{v_{i2}^{-}-v_T-mv_{-/+}}\right]\right)\end{aligned} \tag{2}$$

where the input voltages $v_{i1,2}^{+/-}$, the common node's voltages $v_C^{+/-}$, the threshold voltage V_{T0}, and the opamp's input voltages $V_{+/-}$ [cf. Fig. 3.1] are all divided by $2m\varphi_t$ to form the normalized variables $v_{i1,2}^{+/-}$, $v_C^{+/-}$, v_T, and $v_{+/-}$ in (2), respectively. Also, $\alpha = R_G/R_S$ and $r = R_S\beta\varphi_t$. Note that the normalization yields the closed-form equation in (2) which facilitates a systematic design as will be shortly described.

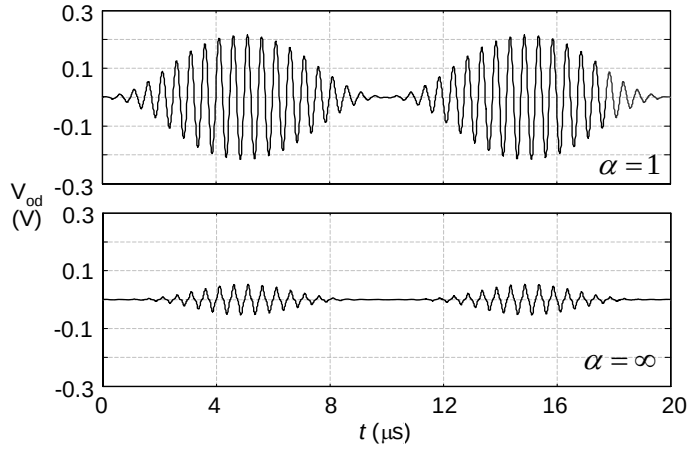
Given a set of dc bias and input signal levels, one can determine $v_C^{+/-}$ based on numerical computation of (2). Subsequently, the normalized mixer's output currents $I_o^{+/-}/I_Z$, where $I_Z = 2m\varphi_t^2\beta$, can be calculated as

$$\frac{I_O^{+/-}}{I_Z} = \left(\ln^2\left[1+e^{v_{i2}^{+}-v_T-mv_C^{-/+}}\right] - \ln^2\left[1+e^{v_{i2}^{+}-v_T-mv_{-/+}}\right] \right) + \left(\ln^2\left[1+e^{v_{i2}^{-}-v_T-mv_C^{+/-}}\right] - \ln^2\left[1+e^{v_{i2}^{-}-v_T-mv_{-/+}}\right] \right) \quad (3)$$

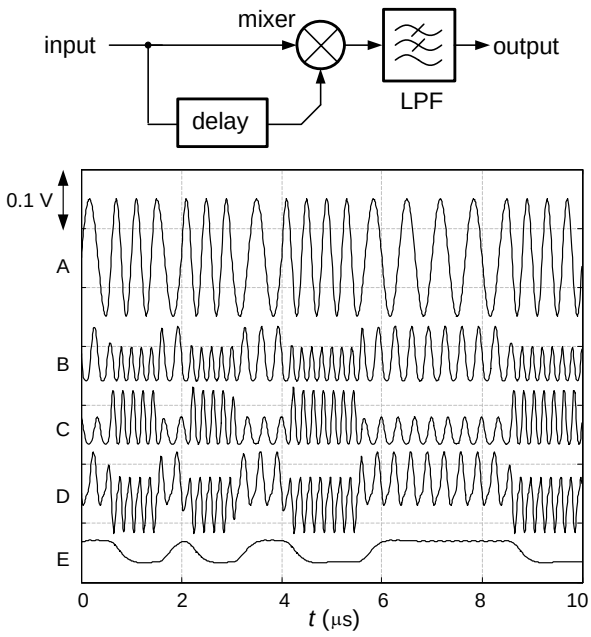
For a particular set of conditions compatible with values assigned in the subsequent simulation, the numerical plot of the normalized *differential peak* output current, $\hat{I}_{od}/I_Z = (\hat{I}_o^+ - \hat{I}_o^-)/I_Z$ can be determined using (3). This is given in Fig. 3.2 as a function of the design parameters r and α. The plot indicates that, at a constant r, the output peak current increases with a successive reduction of α. This trend holds until around α = 0.2 to 0.3 where only a marginal improvement or even a drop in the output is obtained. For a constant α, a smaller r results in a larger output but this can not be reduced indefinitely since a smaller r results in smaller R_S and R_G, and there exists a limit determined by the driving capability of the preceding stage.

3.4 Design and Performance Verification

The mixer in Fig. 3.1 has been designed and simulated using a 1.8V 0.18μm CMOS process. The supply voltage was set at 0.5V and the dc bias for $V_{i1,2}^{+/-}$ were both at 0.25V. The differential peak inputs were at $\hat{v}_{id1} = \hat{v}_{i1}^{+} - \hat{v}_{i1}^{-} = 0.2V_p$, and $\hat{v}_{id2} = \hat{v}_{i2}^{+} - \hat{v}_{i2}^{-} = 0.4V_p$. The dc bias of



(a) [Continued]



(b)

Fig. 3.3 Simulated waveforms of (a) mixer with 50kHz and 2.0MHz inputs and (b) FSK demodulator.

its input terminals was set at $V_+ = V_- = 0.4$V. In order to demonstrate a very low voltage capability, the standard n-channel devices were used with $W/L = 110\mu$m/1.1μm. As extracted from simulation, this yields $\beta = 25$mA/V^2 ($I_Z = 45.6\mu$A and $1/\beta\varphi_t = 1.55$kΩ) and $V_{T0} \approx 0.4$V. Based on Fig. 3.2, for the design case at $r = 16$ and $\alpha = 1.0$, $R_S = R_G = 16/\beta\varphi_t \approx 25k\Omega$ were determined. This also results in the normalized differential peak output current at $I_{od}/I_Z = 0.08$. With $R_F = 55$kΩ, the differential peak output voltage, $\hat{v}_{od} = \hat{v}_o^+ - \hat{v}_o^-$, is at $|\hat{v}_{od}| = |\hat{i}_{od} \cdot R_F| \approx 0.2V_p$. Since we have $V_{i1d} = 0.2$V$_p$, the conversion gain is $G = |\hat{v}_{od}/\hat{v}_{id1}| = \sim 1.0$V/V.

Fig. 3.3(a) shows the simulated waveform (solid line) at the mixer's differential output for a 2MHz high frequency input at $v_{i1}^{+/-}$ and a 50kHz low frequency input at $v_{i2}^{+/-}$. The resulting output differential peak voltage is at ~0.2V$_p$, yielding the down conversion gain at $G = \sim 1.0$V/V. Also given in the plot is the mixer's output with R_G in Fig. 3.1 removed (gray line), i.e. α approaches infinity, where it is seen that the amplitude and hence the gain drops significantly by more than five folds. It should be noted that simulations of the mixer with other sets of the parameters, i.e. r ranging from 2 to 32, and α from 0.5 to 2.0 [cf. Fig. 3.2], were also conducted and the resulting conversion gain exhibit good agreement with the theoretical analysis throughout.

The effectiveness of the designed mixer for use in a baseband application at a 0.5-V supply was also validated. It was employed as a mixer block in the differential delay demodulator for a low-IF IEEE 802.15.4 receiver (schematic as depicted in Fig. 3.3(b)), with the delay at $-\pi/2$ phase shift for the low-IF of 2.0MHz. A 2-FSK modulated signal (a combination of I- and Q- O-QPSK signals compliant with IEEE 802.15.4 standard) was applied. Fig. 3.3 shows the simulated waveforms of the demodulator for the 1.5/2.5MHz FSK input at 2Mchip/s (trace A), the single-ended and differential outputs of the mixer (traces B,

C and D), and the filtered output (trace E). The filtered output matches well to that obtained from the ideal demodulator where the mixer was replaced by an ideal multiplier with the same conversion gain.

3.5. Conclusion

A very low voltage opamp-based mixer incorporating a linear resistor network to extend the operation of the cross-coupled triode transistors has been presented. Detailed analysis, design and verification have been provided. Its viability has been demonstrated via simulation and experiment where it has made possible an FSK demodulator's operation at a very restricted supply of 0.5V using standard transistors in a 1.8V 0.18μm CMOS. It should be noted that the technique is also readily applicable to extend the operation of the sub-threshold MOS resistor technique in [6], [7].

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4. Sub-threshold Resistor-MOSFET Tunable Resistor Technique

4.1 Introduction

With the continued reduction of supply voltages due to aggressive downsizing of transistors in modern CMOS processes, the design of analog circuits that co-integrate with digital circuits on the same chip with sufficient performance promises to be increasingly challenging. For analog filtering applications, continuous-time (CT) MOSFET-C and linearity enhanced R-MOSFET-C techniques that employ no switches as well as no anti-aliasing and smoothing filters have been demonstrated as attractive alternatives to sampled-data switched-capacitor (SC) filters at low voltages [1-4]. One major issue however for the low-voltage CT filters is the limited range of the gate voltage available for tuning the corner frequency through the MOSFET resistance so as to cope with inevitable process and temperature variations. Although this may be circumvented either by using native transistors, low threshold transistors or thick oxide transistors, a control voltage larger than the supply is often necessary, thereby necessitating a clock boosting circuitry which invariably poses reliability concerns on the devices. Another means is to employ the variable MOS capacitors [1], but a switched array of parallel *linear* capacitors for coarse tuning must be included to achieve a good linearity and adequate overall tuning range.

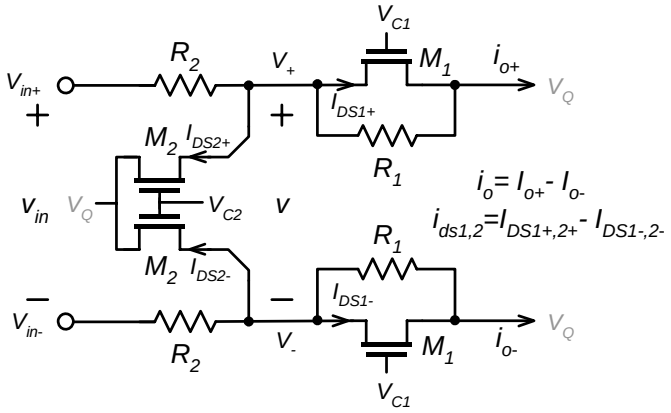


Fig. 4.1 Sub-threshold R-MOSFET tunable resistor structure

Recently, an enhanced structure that can extend the usability of the R-MOSFET approach by enabling MOSFET operation in moderate to weak (or sub-threshold) inversion, without significant impairment on linearity, was introduced [5]. The so-called sub-threshold R-MOSFET structure essentially relies upon a *cancellation* of the nonlinearity which can be *strongly* nonlinear such as that exhibited by a saturated sub-threshold MOSFET. This is in stark contrast to the existing R-MOSFET configurations that rely upon series and/or parallel linear resistor(s) to *suppress* the non-linearity and thus become ineffective at sub-threshold MOSFET operation. For the sub-threshold resistor to exhibit optimum linearity and tuning capability, it requires an appropriate design and this is the subject of this paper. In Section 2, the principal operation and detailed analysis, which leads to a perfect linearization in the sub-threshold resistor, are outlined. Also discussed in this section is a possible design guideline

for good linearity performance over the required tuning range. Section 3 provides extensive analysis and design verification through experiments and simulations. This is followed by conclusions in Section 4.

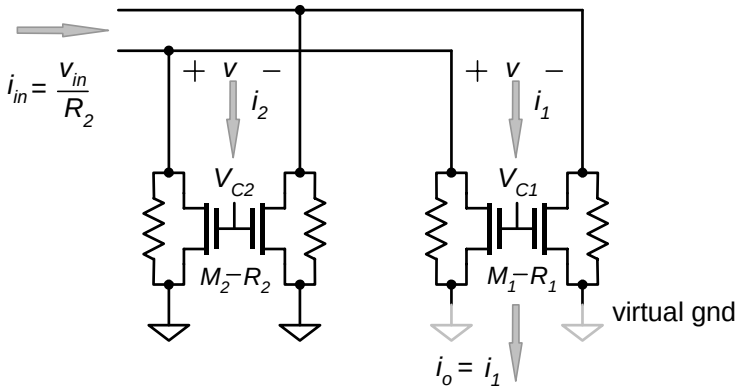


Fig. 4.2 Norton's equivalent circuit of sub-threshold R-MOSFET resistor

4.2 Sub-Threshold R-MOSFET analysis

A. Principal operation

Fig. 4.1 shows the sub-threshold R-MOSFET resistor where it consists of the linear resistors R_1-R_2 and the MOS transistors M_1-M_2. When compared to the simple series-parallel R-MOSFET resistor which comprises R_1, R_2 and M_1, the sub-threshold resistor of Fig. 4.1 employs the additional transistor pair, M_2. From another point of view, when compared to the dump configuration of the R-MOS-FET resistor in [3] which comprises R_2, M_1 and M_2, the sub-threshold resistor employs the additional resistor pair, R_1. Thus, the major differences lie in the fact that the sub-threshold resistor makes simultaneous use of both R_1 and M_2 and this offers linearity improvement, especially when the MOS transistors operate in the sub-threshold region.

An insight into its underlying principle can be gained by transforming the differential input voltage v_{in} and the series R_2 into its Norton's equivalent. The resultant circuit, after rearrangement for the sake of description, is as shown in Fig. 4.2, with all the voltage/current variables indicated being differential. The transformed circuit is essentially a parallel of two *nonlinear* resistance branches, each comprising a pair of linear resistors and MOSFETs. In operation, the equivalent input current $i_{in} = v_{in}/R_2$ is divided into two paths — one through the parallel combination of R_1 and M_1 to produce the output current $i_o = i_1$ with a nonlinear current-voltage relation $i_1 = G_1(v)$; the other through R_2 and M_2 to produce the current i_2 with a nonlinear relation, $i_2 = G_2(v)$, where v is the common differential voltage across the two branches. Note that the linear terms of $G_1(v)$ and $G_2(v)$ are mainly contributed by the linear resistors, while the nonlinear terms are mainly contributed by the MOSFETs. Thus, to achieve a perfectly linear relationship between $i_o = i_1$ and i_{in}, hence between i_o and v_{in}, it demands that the current division be linear. This can be accomplished when the two nonlinear branches are *linearly dependent*, i.e., $G_1(v) = \delta \cdot G_2(v)$ where δ is a constant, *regardless* of the nonlinear characteristic. It should be noted that such a linearization

condition emphasizes the critical role of including both R_1 and M_2 in the sub-threshold resistor structure.

One important consideration now is the fact that, under a low supply voltage and a large signal swing, the MOSFET operation in the sub-threshold resistor can span not only from strong to moderate and weak inversion, but also from non-saturation to saturation. Thus, it is of prime importance to conduct detailed analysis that could lead to design guidelines so as to ensure good linearity over the resistance tuning range.

B. Sub-Threshold R-MOSFET analysis

Due to such a wide coverage of the MOSFET's operation, it is necessary to employ a general current-voltage MOS equation valid for all regions. This can be given by [6]

$$I_{DS} = 2m\varphi_t^2 \mu C_{ox} \frac{W}{L}\left(\ln^2\left[1+e^{\frac{V_{GB}-V_{T0}-mV_{SB}}{2m\varphi_t}}\right] - \ln^2\left[1+e^{\frac{V_{GB}-V_{T0}-mV_{DB}}{2m\varphi_t}}\right]\right) \tag{1a}$$

with

$$m = \left(1-\gamma/2\sqrt{V_{GB}-V_{T0}+\left(\gamma/2+\sqrt{\varphi_0}\right)^2}\right)^{-1} \tag{1b}$$

where $\varphi_t = kT/q$ is the thermal voltage, μ is the carrier effective mobility in the channel, C_{ox} is the gate-oxide per unit area, W and L are the channel width and length, V_{T0} is the threshold voltage at $V_{SB} = 0$, γ is the body effect coefficient and φ_0 is a characteristic potential [6]. It is noted that the short-channel effects and the dependence of the mobility on the transversal field are not included in (1).

Consider the sub-threshold R-MOSFET resistor in Fig. 4.1. It is assumed that the input and output quiescent voltages are set at V_Q, the body voltage of all the MOSFETs at $V_B = 0$, the gate bias at V_{C1} for M_1, and at V_{C2} for M_2. For a balanced differential input, $\pm v_{in}/2$, the following equation

$$\frac{v_{in}-(V_+-V_-)}{R_2} = \overbrace{\overbrace{I_{Z1}\left(\ln^2\left[1+e^{\frac{V_{C1}-V_{T0}-mV_-}{2m\varphi_t}}\right]-\ln^2\left[1+e^{\frac{V_{C1}-V_{T0}-mV_+}{2m\varphi_t}}\right]\right)}^{i_{ds1}}+\frac{(V_+-V_-)}{R_1}+\overbrace{I_{Z2}\left(\ln^2\left[1+e^{\frac{V_{C2}-V_{T0}-mV_-}{2m\varphi_t}}\right]-\ln^2\left[1+e^{\frac{V_{C2}-V_{T0}-mV_+}{2m\varphi_t}}\right]\right)}^{i_{ds2}}}^{i_o} \tag{2}$$

is obtained by applying KCL at the intermediate nodes with the voltages V_+ and V_- in Fig. 4.1, and taking their difference. In (2), $I_{Z1,2} = 2m\varphi_t^2 \mu C_{ox} W_{1,2}/L_{1,2}$, and i_{ds1} and i_{ds2} are the differential drain/source currents of the MOSFET pairs, M_1 and M_2, respectively. $i_o = i_{o+} - i_{o-}$ denotes the differential output current. To obtain manageable results that enable insight into the circuit operation, and also help offer a design implication, the following approximations are applied to (2). Due to the presence of the *linear* resistors R_1 and R_2, it is possible to assume that V_+ and V_- are also balanced similar to the input v_{in}, i.e., $V_+ = V_Q + v/2$ and $V_- = V_Q - v/2$, and hence the definition of the differential voltage v is $v = V_+ - V_-$. To help simplify the analysis, each variable in (2) is normalized by the following definitions: $x =$

$v_{in}/2m\varphi_t$, $z = v/2m\varphi_t$, $a_{1,2} = (V_{C1,2} - V_{T0} - mV_Q)/2m\varphi_t$, and $g_{1,2} = 2m\varphi_t/I_{Z1}R_{1,2}$. Thus, it follows that (2) can be rewritten as

$$\begin{aligned} g_2(x-z) = & \underbrace{\left(\ln^2\left[1+e^{a_1+mz/2}\right]-\ln^2\left[1+e^{a_1-mz/2}\right]\right)}_{y} + g_1 z \\ & + r\left(\ln^2\left[1+e^{a_2+mz/2}\right]-\ln^2\left[1+e^{a_2-mz/2}\right]\right) \end{aligned} \tag{3}$$

with $r = I_{Z2}/I_{Z1}$ and $y = i_o/I_{Z1}$. With the use of Taylor series representation similar to [7] (for analysis of non-saturated strong inversion MOSFET resistors), the normalized differential current-voltage relation of the MOSFET pairs in (3) which involve a difference of square logarithmic operation can be expressed in a polynomial form with no even-order terms due to the balanced structure. Such an expansion with respect to z yields

$$\ln^2\left[1+e^{a+mz/2}\right]-\ln^2\left[1+e^{a-mz/2}\right] \approx c_1^n z + c_3^n z^3 + c_5^n z^5 \tag{4a}$$

with

$$c_1^n = \frac{2me^a}{1+e^a}\ln(1+e^a) \tag{4b}$$

$$c_3^n = \frac{m^3 e^a}{12(1-e^a)^3}\left(3e^a + \ln(1+e^a) - e^a\ln(1+e^a)\right) \tag{4c}$$

$$\begin{aligned} c_5^n = & \frac{m^5 e^{2a}}{960(1+e^a)^5}\cdot\Big[5\left(3-e^a\left(6-e^a\right)\right) \\ & +2\left(1-e^a\right)\left(\cosh(a)-5\right)\ln(1+e^a)\Big] \end{aligned} \tag{4d}$$

where c_1^n, c_2^n and c_5^n (with the superscript "n") are the *normalized* Taylor's coefficients. Note from (4b) that the first-order coefficient is reduced to $c_1^n = 2a$ for $a >> 0$ (strong inversion MOSFETs) and, after de-normalization, this yields the usual small-signal characteristic of a non-saturated MOSFET resistor [6]. To further simplify the analysis, the difference of square logarithmic operation is approximated by a third-order polynomial, i.e., the fifth-order coefficient c_5^n in (4d) is omitted. The validity of this simplification will be discussed soon. Following this, by substituting the third-order Taylor's series in (4) into (3), after some rearrangement, we obtain

$$g_2 x = \underbrace{(g_1 + c_{11}^n)z + c_{31}^n z^3}_{y} + \underbrace{\left(g_2 + rc_{12}^n\right)z + rc_{32}^n z^3}_{h} \tag{5}$$

where $c^n_{11,31}$ are the normalized coefficients for the MOSFET pair M_1 and $c^n_{12,32}$ are those for M_2. It is observed from (5) that, for a linear characteristic between x and y, h must be linearly dependent on y, i.e., $h = \delta y$ where δ is a constant. It is interesting to note that, with reference to the Norton's equivalent circuit of Fig. 4.2, the variable y corresponds to the normalized current $i_o/I_{Z1} = i_1/I_{Z1}$ in the M_1-R_1 branch, and h corresponds to the normalized current i_2/I_{Z1} in

the M_2-R_2 branch. By using (5), the linear dependence condition implies the following relation:

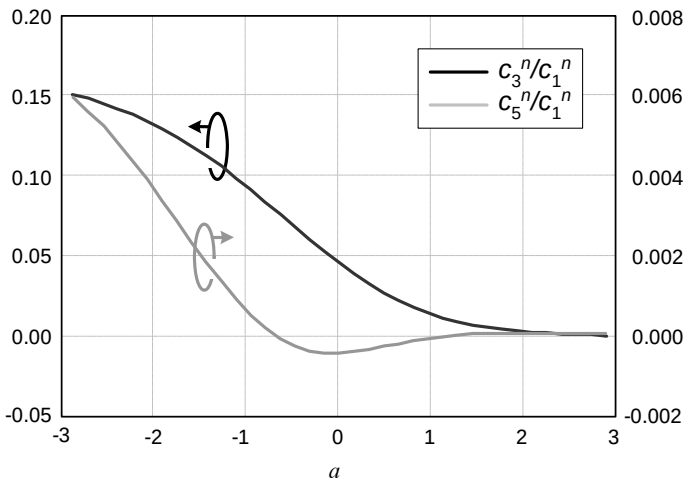


Fig. 4.3 Normalized Taylor's coefficients ratios c_3^n/c_1^n and c_5^n/c_1^n of MOSFET pair's normalized I-V characteristics

$$\frac{g_2 + rc_{12}^n}{g_1 + c_{11}^n} = r \cdot \frac{c_{32}^n}{c_{31}^n} = \delta \tag{6}.$$

Using (5) and (6), we obtain $y = g_2(1+\delta)^{-1}x$. After denormalizing the associated variables, the differential characteristic of the sub-threshold R-MOSFET resistor is thus given by

$$i_o = R_{eff}^{-1} v_{in} = \left[(1+\delta) R_2 \right]^{-1} v_{in} \tag{7}.$$

For ease of implementation and characterization, the transistor pairs M_1 and M_2 should be integer multiples of the same unit MOSFET. By assigning the number of unit transistors at n_1 for M_1 and at n_2 for M_2, the parameter relation for a perfect linearization can be obtained by de-normalizing (6), and this yields

$$\frac{R_2^{-1} + n_2 \cdot c_1(V_{C2})}{R_1^{-1} + n_1 \cdot c_1(V_{C1})} = \frac{n_2 \cdot c_3(V_{C2})}{n_1 \cdot c_3(V_{C1})} = \delta \tag{8}$$

where $c_{1,3}(V_C)$'s are the *normal* coefficients of the third-order polynomial describing the differential current-voltage characteristic of the unit MOSFET pair at the gate control voltage V_C. Note that these may be obtained by de-normalizing (4b) and (4c).

From the analysis outlined above, the equations (7), (8) are central to the analysis and design of the sub-threshold R-MOSFET resistor. Inspection of (8) also reveals that scaling of the effective resistance from R_{eff} to $k \cdot R_{eff}$ can be simply obtained, without upsetting the linearization condition, by modifying R_1, R_2 by the factor k and n_1, n_2 by the inverse $1/k$.

It is important to point out that the third-order polynomial approximation applied in the forgoing analysis is valid for MOSFET operation in strong to moderate inversion. This is

evident as shown in Fig. 4.3 which provides the plots versus a of the ratios of the third-order and the fifth-order to the first-order normalized coefficients, c_3^n/c_1^n and c_5^n/c_1^n, using (4). At weak inversion operation (approximately at $a < -1$ or $(V_{C1} - V_{T0} - mV_Q) < -2m\varphi_t$), the characteristic of the MOSFET pair becomes increasingly nonlinear and it can be seen from the ratio plots that the fifth-order term can no longer be omitted. Nevertheless, as will be evident in the experiments and simulations of Section 3, if the coefficients $c_{1,3}(V_C)$ in (8) are to be determined *empirically* from the unit MOSFET characteristic at various V_Cs, instead of being calculated from (4b)-(4c), it is possible to fit the characteristics with the third-order polynomial while still obtaining a reasonable accuracy. In this way, the use of the developed equations in (8) can be extended down to weak MOSFET operation. In fact, such empirical coefficient determination is valid for more general conditions [7]. That is, with proper fitting values of c_1 and c_3, all the second-order effects omitted in (1) are automatically incorporated. Since this approach is simple and yet provides good accuracy in practice, it will be employed in Section 3.

Table I Empirical coefficients for ALD array MOSFET pair

V_C	1.25	1.30	1.35	1.40	1.45	1.50
c_1/c_3 ($\cdot 10^{-4}$)	0.022 /1.35	0.098 /1.79	0.238 /1.89	0.454 /1.77	0.717 /1.62	1.033 /1.46

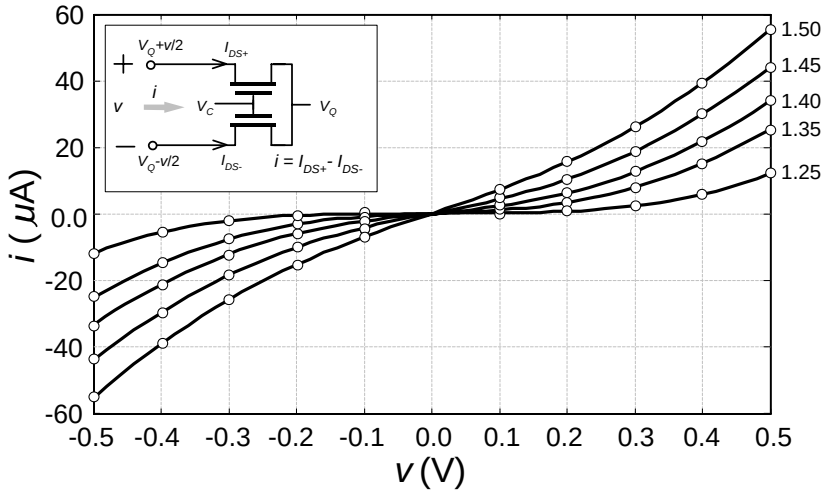


Fig. 4.4 Measured (solid) and calculated (marker) differential characteris-tics of ALD1106 unit MOSFET pair at different V_Cs

C. Design discussion

For an ideal operation of the sub-threshold R-MOSFET resistor, when the main control voltage V_{C1} of M_1 is changed, the auxiliary control voltage V_{C2} of M_2 should be adjusted accordingly in order to maintain good linearity over the entire resistance tuning range. For ease of implementation however, it should be more convenient to maintain V_{C2} at

a constant voltage. In such a case, the condition for a perfect non-linearity cancellation is satisfied at a *single* set of V_{C1} and V_{C2} through proper selection of R_1, R_2 and the dimensions of M_1 and M_2 according to (8). Only a partial cancellation is obtained at other set of control voltages. As will be demonstrated by both experiments and simulations, the constant V_{C2} scheme proves to be effective for moderate linearity applications, provided that particular attention is paid to satisfying the linearization condition at a set of V_{C1} and V_{C2} within the sub-threshold operation of the MOSFETs where the nonlinearity is most pronounced. With such a design consideration, adequate resistance tunability with good linearity over the entire range can be ensured.

4.3 Performance verification

A. Experimental results

The integrity of the analysis and design, and the functionality of the sub-threshold R-MOSFET resistor, were first verified via breadboard implementation using the n-channel MOSFET of an ALD1106 transistor array as the unit transistor. To facilitate the test, the R-MOSFET resistor was built around off-the-shelf opamps with negative feedback using linear resistors to form a different-tial inverting amplifier where the differential output current i_o in Fig. 4.1 can be measured indirectly via the amplifier's output voltage. For this breadboard design, the terminal input/output quiescent voltages were chosen at V_Q = 0.5V. Measurement indicates the extrapolated nominal threshold voltage of the MOSFET at $V_{T0} \approx 0.65$V and this is increased to $V_{TB} \approx 0.88$V for $V_D = V_S = V_Q = 0.5$V and $V_B = 0$. Therefore, the gate control voltage V_C below $V_Q + V_{TB} \approx 1.38$V covers the sub-threshold operation. For the selected V_C range from 1.25V to 1.50V, the measured differential characteristic of the ALD1106 nMOS pair at V_Q = 0.5V are depicted in Fig. 4.4. Also given are the calculated plots based on the extracted polynomial coefficients c_1s and c_3s (using MATLAB) in Table 1 for each corresponding V_C where close agreement with measurement is observed.

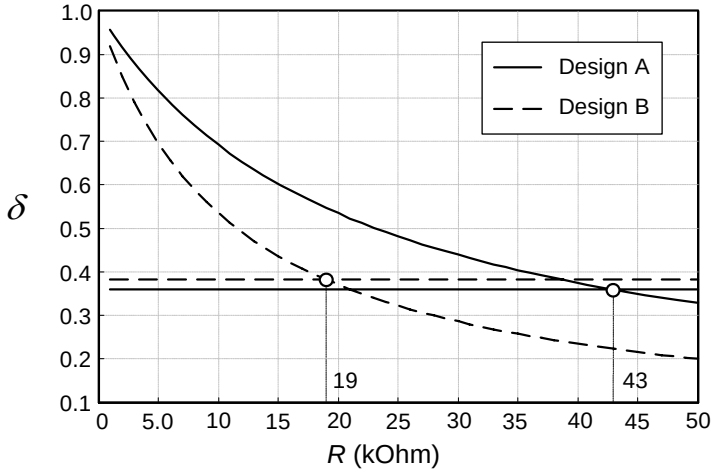


Fig. 4.5 Design curves for sub-threshold resistor using ALD1106.

For ease of tuning, the scheme with a fixed gate voltage for V_{C2} was adopted. In this design example, the numbers of the unit transistors at n_1 = 2 and n_2 = 1 and an identical

resistance $R_1 = R_2 = R$ were selected. To determine the linearization conditions, the ratios on the left- and right-hand sides of (8) are plotted against the resistance R, where the intersection between the two curves indicates the designed resistance value. Based on the extracted coefficients in Table 1, the plots for two example designs for linearization at different V_Cs are shown in Fig. 4.5. For design A with the linearization at V_{C1} = 1.35V and V_{C2} = 1.25V, the intersection yields R = 43kΩ. For design B with the linearization at V_{C1} = 1.40V and V_{C2} = 1.25V, we obtain R = 19kΩ. In the test, available resistor values were used, i.e., R = 50kΩ for design A, and R = 20kΩ for design B. It should be noted that the selected V_{C2} = 1.25V for both designs results in the operation of M_2 at ~130mV less than the threshold voltage.

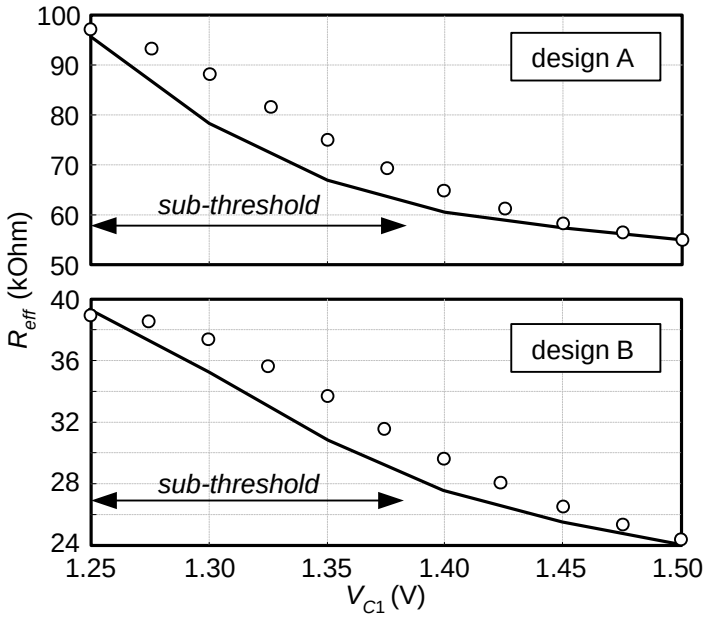
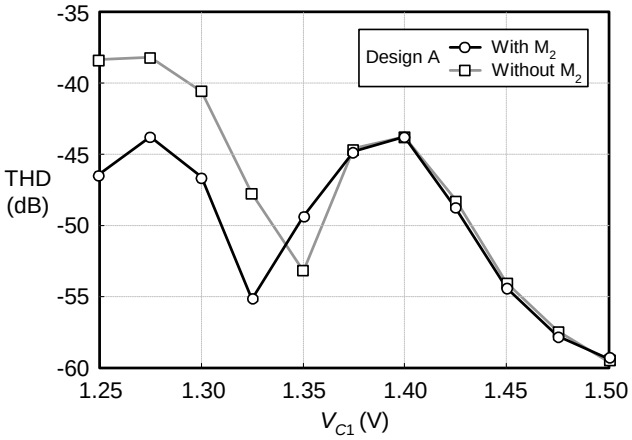


Fig. 4.6 Measured (marker) and calculated (solid) small-signal resistance versus V_{C1}.

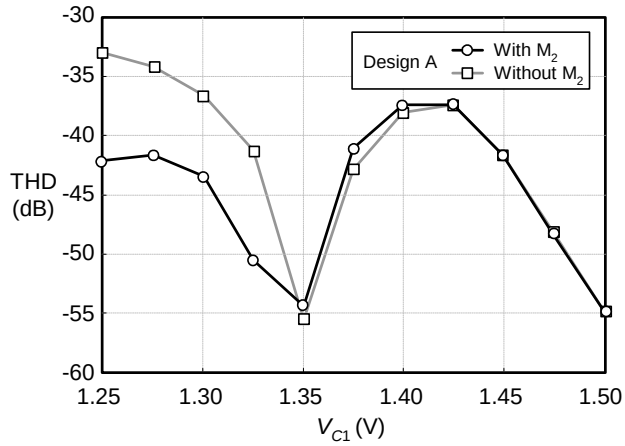
Fig. 4.6 shows the measured resistance characteristics, which were extracted from the measured small-signal voltage gain versus V_{C1} at an input v_{in} of $0.1V_p$ (differential peak voltage). Also given for comparison are the calculated resistances using (7) based on the coefficients in Table 1. It is seen that R_{eff} can be tuned from 55kΩ to 97kΩ, yielding the tuning ratio at ~1.76 for design A. For design B, R_{eff} can be tuned from 24.5kΩ to 38kΩ, giving the tuning ratio at ~1.55. Also, based on the measured values, the sub-threshold operation in the MOSFETs covers the resistance tuning range by more than 50% for both designs A and B.

Fig. 4.7 and 8 show the measured total harmonic distortion (THD) of the output voltage v_o versus V_{C1}, at v_{in} = $0.4V_p$ and $0.8V_p$ (differential peak voltage). For design A, the plots indicate the dips in the THD of the sub-threshold resistor at the intermediate control voltage V_{C1} = 1.325V at $0.4V_p$, and at V_{C1} = 1.35V for the test inputs at $0.8V_p$. For design B, the dips occur at V_{C1} = 1.375V for both of the test inputs. These voltage locations are in close agreement with the design specifications, i.e., at V_{C1} = 1.35V for design A, and at V_{C1} = 1.40V for design B. Some discrepancies are mainly due to the approximation of the MOSFET characteristics by the third-order polynomial.

Also included for comparison in Fig. 4.7 and 8 are the THD plots when the transistor pair M_2 in Fig. 4.1 was removed and the circuit was turned into the conventional series-parallel R-MOSFET resistor. As observed, the
proposed sub-threshold resistors can provide THD improvement, particularly over the V_{C1} range where M_1 operates in sub-threshold inversion. For the range of V_{C1} where M_1 is in strong operation, almost identical linearity is displayed between the two resistors as the effect of M_2 becomes negligible.



(a)



(b)

Fig. 4.7 Measured THD performances at 10kHz input frequency of design A at (a) $0.4V_p$ input and (b) $0.8V_p$ input.

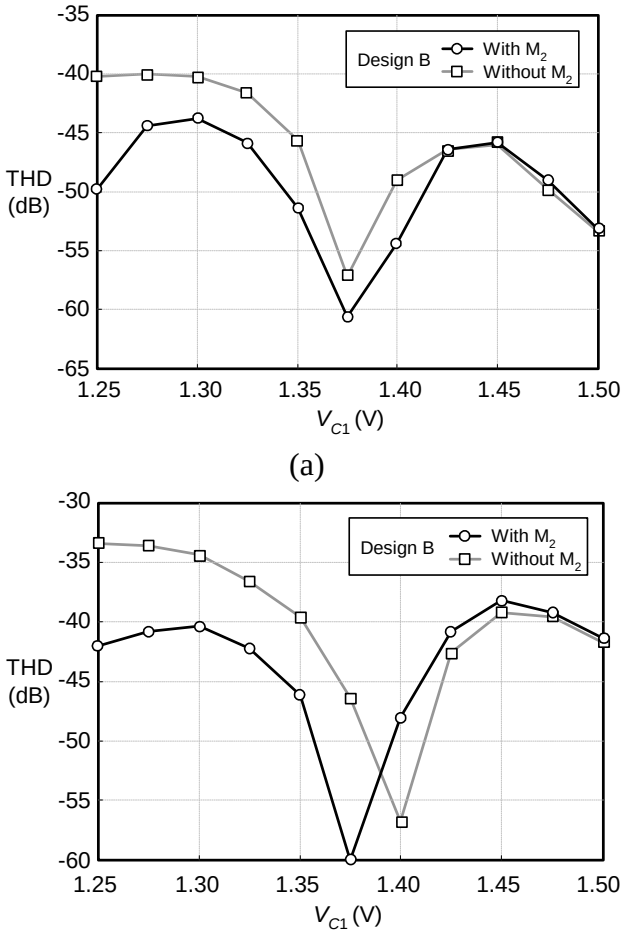


Fig. 4.8 Measured THD performances at 10kHz input frequency of design B at (a) $0.4V_p$ input and (b) $0.8V_p$ input.

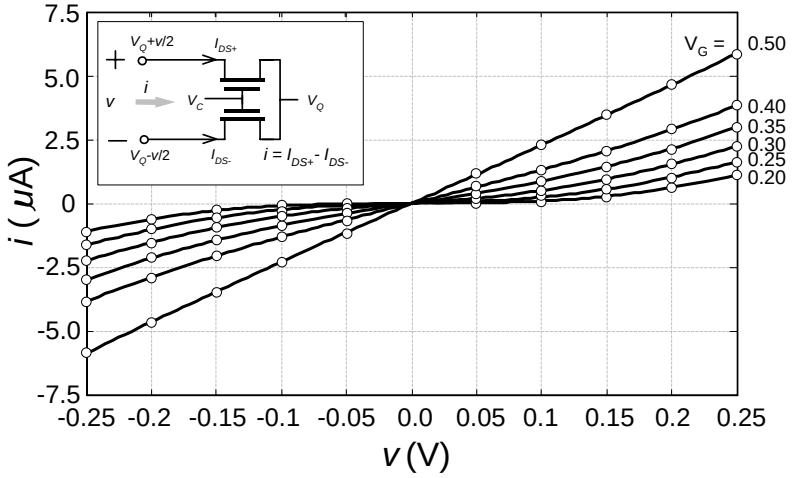


Fig. 4.9 Simulated (solid) and calculated (marker) differential characteris-tics of the low-threshold unit MOSFET pair at different V_Cs.

Table II Empirical coefficients for low threshold MOSFET pair

V_C	0.2	0.25	0.3	0.35	0.4	0.50
c_1/c_3 ($\cdot 10^{-4}$)	0.003 /0.677	0.019 /0.785	0.045 /0.766	0.082 /0.629	0.127 /0.427	0.228 /0.108

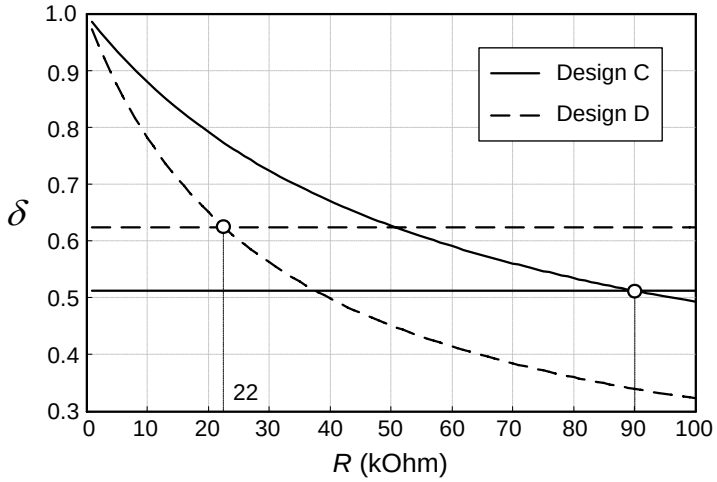
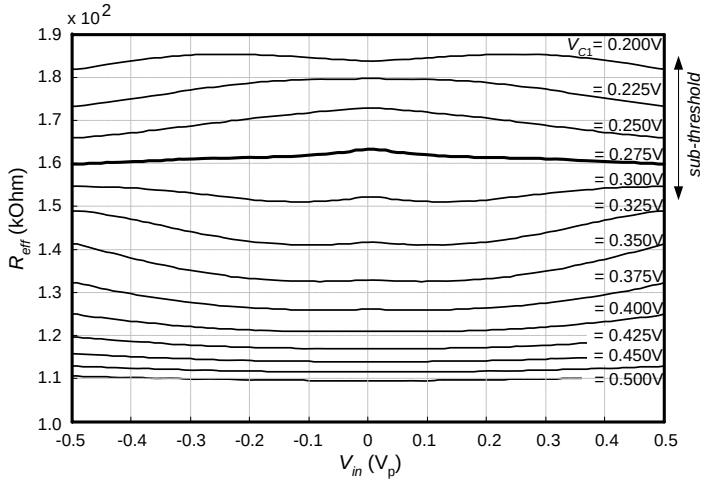


Fig. 4.10 Design curves for sub-threshold resistor using 0.18 μm CMOS.

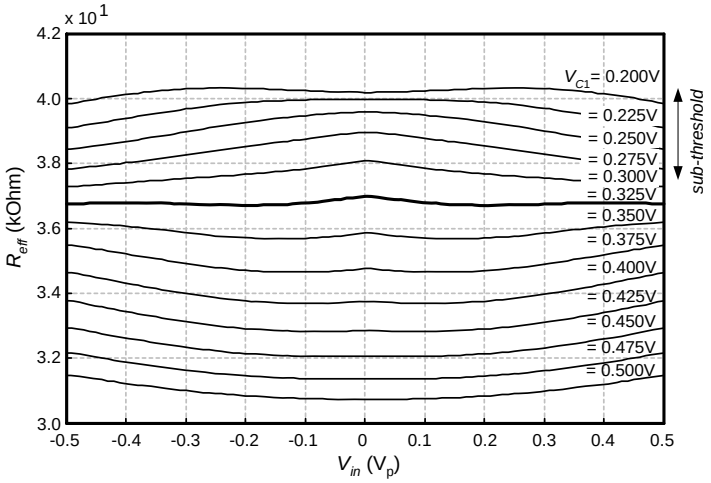
B. Simulation results

The performance of the sub-threshold R-MOSFET resistor in IC implementation was also demonstrated via simulation using the *low-threshold* n-channel MOSFET of the UMC 1.8-V 0.18 μm CMOS process with the gate tuning voltage below the supply at 0.5V. Unlike the transistor array implementation, the output current $i_o = i_{o+} - i_{o-}$ in Fig. 4.1 was measured directly in simulation. For this example application at a 0.5-V supply, the quiescent voltage V_Q was set at a half-supply level, V_Q = 0.25V. The unit transistor was selected at W/L=1.1μm/4.0μm. As extrapolated from simulation, the threshold voltage of the MOSFET is $V_{TB} \approx$ 0.05V at $V_D = V_S = V_Q$ = 0.25V and V_B = 0V whereas the nominal value is $V_{T0} \approx$ 0.01V. Thus, the transistor enters sub-threshold operation at V_C below $V_Q + V_{TB} \approx$ 0.30V. The simulated and calculated differential characteristics of the unit MOSFET pair at various V_Cs are shown in Fig. 4.9, and the extracted polynomial coefficients that fit the curves are given in Table 2.

Similar to the breadboard design, the fixed gate voltage scheme for V_{C2} was employed and $R_1 = R_2 = R$ was selected. In design C, the numbers of the unit transistors were given at n_1 = 4 and n_2 = 2 and the perfect linearization condition was set at V_{C1} = 0.30V and V_{C2} = 0.25V. By using (8) and the extracted coefficients in Table 2, Fig. 4.10 shows the design curves [cf. Fig. 4.5 for designs



(a)



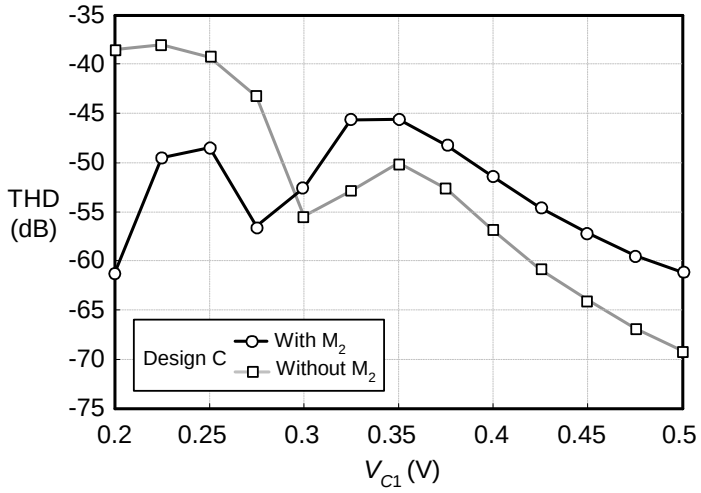
(b)

Fig. 4.11 Simulated resistance characteristics at different V_Cs for (a) Design C and (b) Design D.

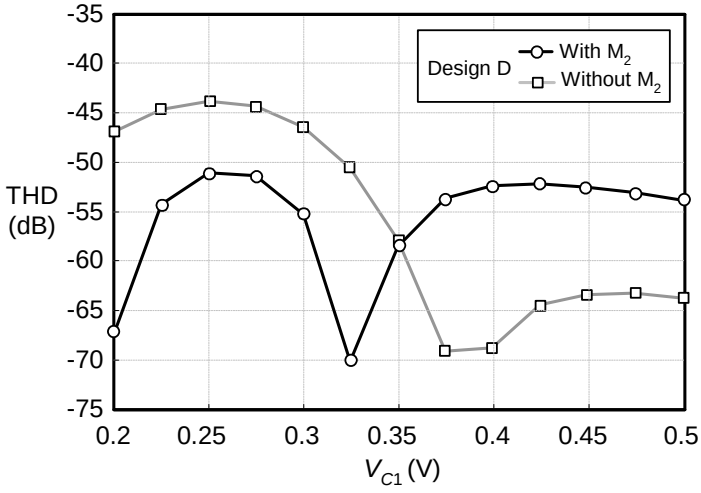
[A-B] where R = 90kΩ is obtained for design C. For design D, another linearization condition at V_{C1} = 0.35V and V_{C2} = 0.25V, was selected and this yields R = 22kΩ. Note that for both designs, the control voltage V_{C2} = 0.25V results in the operation of M_2 at ~50mV less than the threshold voltage.

Fig. 4.11(a)-(b) show the simulated resistance charac-teristics under typical process and temperature for designs C and D with V_{C1} ranging from 0.2V to 0.5V and the differential peak input v_{in} between $-0.5V_p$ and $0.5V_p$. It is noticed that the simulated characteristics are close to straight lines at V_{C1}= 0.275V for design C and V_{C1} = 0.325V for design D in close agreement with the specifications. For design C, R_{eff} can be tuned from 110kΩ to 184kΩ with the tuning ratio at ~1.67, and from 30.8kΩ to 40.6kΩ with the tuning ratio at ~1.32 for design D. Also note from the plots that the sub-threshold operation in the MOSFETs occupies about 40% of the resistance tuning range for design C, and about 30% for design D.

Fig. 4.12 shows the simulated THD performances versus V_{C1} at v_{in} = 0.5V_p. Compatible with the resistance plots of Fig. 4.11, the distortions of the sub-threshold resistors under typical process and temperature exhibit intermediate dips at V_{C1} = 0.275V for design C, and at V_{C1} = 0.325V for design D. Also included in the figure are the THD plots of the corresponding series-parallel R-MOSFET resistors. Similar to the measured results of Fig. 4.7 and 8, improvement in the THD for the range of V_{C1} which yields sub-threshold operation in M_1 is clearly observed. Unlike the measured results however, the series-parallel counterparts exhibit somewhat less distortion at strong operation in M_1. This is due to the fact that, for designs C and D, M_2 was selected to operate at ~50mV below the threshold voltage, as compared to ~130mV for the case of designs A and B. This results in over-compensation of the nonlinearity in M_1 by M_2 when M_1 enters a triode strong region of operation with a linear characteristic. Nonetheless, it can be seen from Fig. 4.12 that the sub-threshold resistors could offer better overall THD performance over the tuning voltage, extending down to weak inversion operation in the MOSFETs.



(a)



(b)

Fig. 4.12 Distortion performances of sub-threshold and series-parallel resistors at typical conditions and 10kHz input for (a) Design C and (b) Design D.

To demonstrate robustness of the sub-threshold R-MOSFET resistor, the simulated THD performances over extreme process and temperature conditions are given in Fig. 13(a)-(b) where the intermediate drops of the THDs at the same corresponding V_{C1}s under the typical conditions are noticed for both designs. Also, the plots indicate the THD better than –42dB in the sub-threshold resistor over the extreme conditions.

To investigate the impact of component mismatches on linearity, systematic mismatches at 10% were introduced to the resistor pairs R_1 and R_2, as well as the channel width W of the transistor pairs M_1 and M_2. For the threshold mismatch in the transistor pairs, it was set at 5% of the supply voltage, i.e., ΔV_{TB} = 25mV. The resulting simulated THDs versus inputs under the assigned mismatches are given in Fig. 4.14 alongside the plots with perfect matching, both at typical conditions of designs C and D. Note that the THD plots are given at V_{C1} = 0.25V since this yields the worst distortion performances in both designs under sub-threshold operation in M_1 and M_2 [cf. Fig. 4.12]. It is seen that such mismatches cause the distortion to increase at low inputs by as much as 9dB, and this is primarily due to considerable increase in the second harmonic distortion components. At larger inputs, the degradation in the THD is successively reduced. At the maximum input of $0.5V_p$, the distortion level is practically intact for design C, where it is increased by less than 1dB for design D, suggesting good robustness in linearity against mismatches at high input levels.

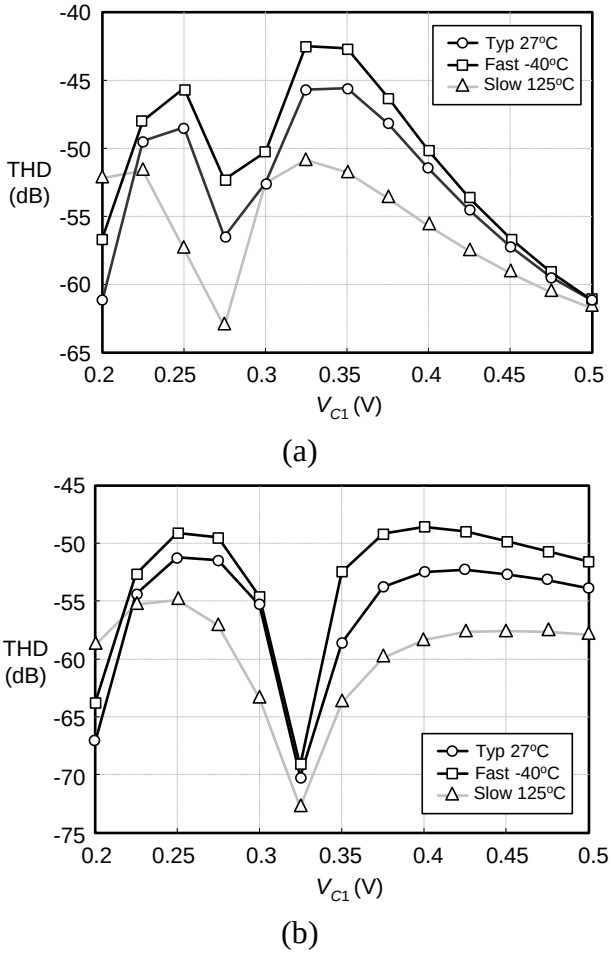


Fig. 4.13 Distortion performances at extreme conditions (a) Design C and (b) Design D.

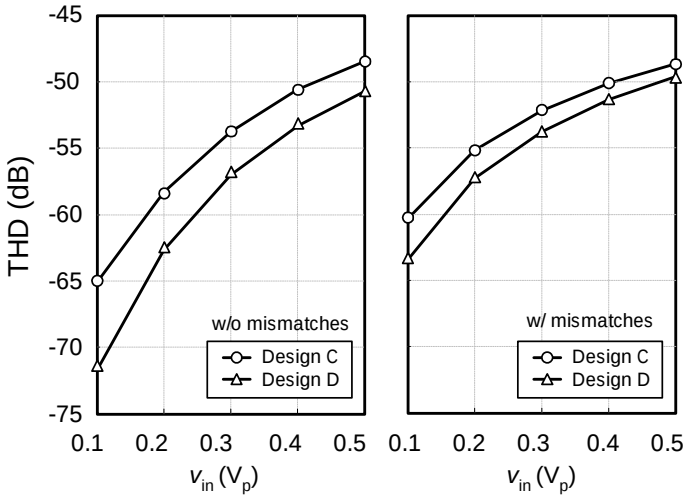


Fig. 4.14 Simulated THD performances versus input for design C and D under typical conditions at V_{C1} = 0.25V with and without systematic mismatches.

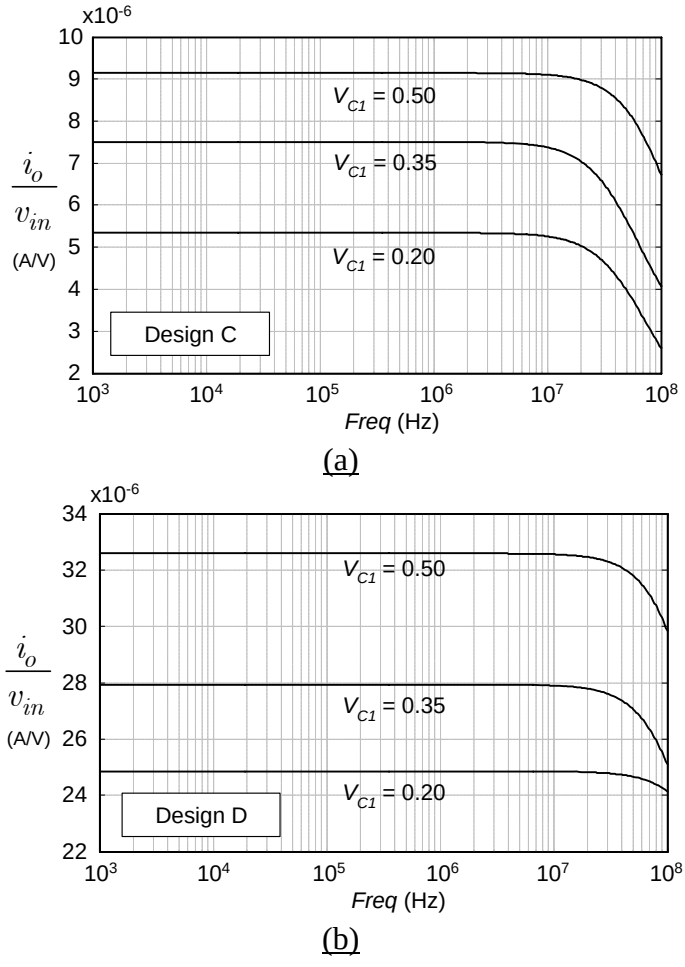


Fig. 4.15 Simulated frequency responses at V_{C1} = 0.2V, 0.35V and 0.5V for (a) Design C and (b) Design D.

Also simulated was the performance of the sub-threshold resistors in terms of the frequency response. These are as shown in Fig. 4.15(a) and 15(b) for the i_o/v_{in} characteristics at typical conditions and different V_{C1}s. It is evident that the operation up to several tens of MHz is feasible for the resistances of design C and D which are in the order of ten to hundred kilo-ohms [cf. Fig. 4.11]. Finally, to verify the scaling property, both the sub-threshold R-MOSFET resistors were scaled by a factor $k = 1/4$, i.e., with $R_1 = R_2 = 22.5\text{k}\Omega$, $n_1 = 16$ and $n_2 = 8$ for design C, and $R_1 = R_2 = 5.5\text{k}\Omega$, $n_1 = 16$ and $n_2 = 8$ for design D. Simulation indicates corresponding reduction of the effective resistances [cf. Fig. 4.11] by a factor of four whereas there is practically no change on the distortion performances [cf. Fig. 4.12-4.14].

4.4 Conclusions

The analysis, design and performance verification of the sub-threshold R-MOSFET tunable resistor with extended MOSFET operation from traditional non-saturated strong inversion to saturated sub-threshold inversion have been presented. The operation of the sub-threshold resistor was described to rely upon a parallel of two non-linear resistive branches with a linear dependency to achieve a linear input/output characteristic. The analysis was first outlined based on a general MOS equation valid for all regions of operation. Various approximations including the use of a third-order polynomial to represent the characteristic of a MOSFET pair were subsequently introduced and this led to operational insight and practical design conditions of the sub-threshold resistor to ensure a good linearity over the tuning range. Extensive verification of its functionality and performance was given via breadboard experiments, and its feasibility in IC realization via simulation. Based on the achievable distortion performances, the sub-threshold resistor technique should prove very useful for a very low supply continuous-time filter implementation with a moderate linearity requirement.

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5. Low-Power, Wide-Frequency-Tuning Filter Using Cross-Forward Common-Mode Cancellation and Sub-Threshold R-MOSFET Resistor Techniques

5.1 Introduction

The advancement of state-of-the-art fine-line CMOS processing has made feasible the implementation of biomedical integrated circuits and systems for ubiquitous healthcare applications, such as wearable health and wellness monitoring, portable molecular detection platform for disease diagnosis etc [1]. Crucial parameters for such wearable and portable devices include low power consumption and low supply voltage with adequate dynamic range [2],[3,],[4]. In this paper, we present analogue techniques to achieve very low voltage and low power filters – one of the indispensible building blocks for biomedical signal processing.

In particular, the circuit architectures for realizing the operational transconductance amplifier (OTA) and the linear tunable resistors based on low power, low supply CMOS transistors in moderate-to-weak or sub-threshold inversion operation are introduced. For the OTA, it makes use of the pseudodifferential structure for a low supply voltage, and the cross-forward (CF) common-mode cancellation technique which has a capability to maintain the transconductance /bias-current efficiency, thereby exhibiting a low power requirement. To enable simultaneous low supply and wide resistance tuning operation with good linearity, the sub-threshold R-MOSFET (SubRMOS) resistor technique [5] is utilized where its underlying operation relies upon a linear current division between two linearly-dependent nonlinear conductances. Validation of these techniques in practice is given via an implementation of a 0.5-V fully-integrated filter in a 0.18-μm CMOS technology.

5.2 Low Voltage Fully Differential Cross-Forward OTA

A. Circuit Architecture

Fig. 5.1 shows the schematic of the low voltage two-stage cross-forward operational transconductance amplifier (CFOTA). Its first stage makes use of a pseudo-differential common-source transistor pair $M_{1a} - M_{1b}$ biased in saturated moderate inversion operation [2]. The active loads are formed by the diode-connected transistor pair $M_{5a} - M_{5b}$ which set the DC bias level, and the cross-coupled transistor pair $M_{6a} - M_{6b}$. Under a differential-mode signal, the cross-coupled pair acts as a negative conductance reducing the overall load conductance [6], so that the differential-mode voltage gain of the first stage can be set at a sufficiently high value. Under a common-mode signal, the pair acts as a positive conductance and this helps reduce the common-mode voltage gain.

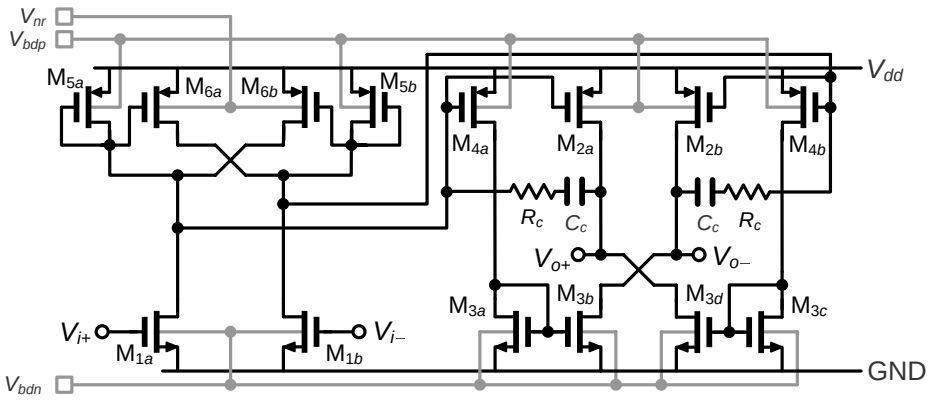


Fig. 5.1 Fully differential cross-forward OTA with frequency compensation

For the second stage, it contains two identical common-source transistor pairs M_{2a} – M_{2b} and M_{4a} – M_{4b}. The drains of M_{4a} and M_{4b} are fed to the current mirror loads M_{3a} – M_{3b} and M_{3c} – M_{3d}, respectively. The mirrors' outputs at the drains of M_{3b} and M_{3d} are then *cross* connected to the drains of M_{2b} and M_{2a}, respectively, and this forms the CFOTA's outputs. The cross-forward arrangement results in a summation of differential-mode signals and a subtraction of common-mode signals, yielding a common-mode rejection capability at practically no penalty on transconductance/bias-current efficiency [7]. This is in contrast to the technique employed in [2], [8], where the added common-mode feed-forward cancellation path provides no differential gain. The capacitors C_c across the second stage perform the pole-splitting compensation, and the series resistors R_c are included for right-half-plane (RHP) zero cancellation.

It should be noted that the second stage of the OTA in Fig. 5.1 also offers a *lateral* class AB operation. That is, under a large differential output signal, one side of the circuit can supply the load current while the opposite side is off [7]. When compared to the conventional class AB stage based on push-pull CMOS transistors of which the minimum supply voltage is limited by the gate-source stacking of the complementary devices, the lateral class AB stage has a potential for a lower supply voltage operation.

Similar to the OTA in [2], the CFOTA of Fig.1 employs a triple-well process so that it can make extensive use of the body terminals of the nMOS and pMOS transistors. To obtain minimum complexity and to guarantee no forward bias in the body terminals, the bodies of all the transistors, except $M_{6a,b}$, are biased at $V_{bdn} = V_{bdp} = V_{DD}/2 = 0.25$ V. This helps reduce the threshold voltages V_{Tn} and V_{Tp}, and thus facilitates moderate inversion operation in the transistors at a very low supply voltage. To obtain an adequate open-loop differential DC gain at $V_{DD} = 0.5$ V, the gate-source voltage for the input transistors, M_{1a} – M_{1b}, is set at $V_{i+/-} = 0.35$ V. For maximum output signal swing, the common-mode voltage level of the CFOTA's output terminals is set at $V_{o+/o-} = 0.25$ V. The bias circuits for setting up these voltage levels will be described in Section IV. For the body voltage V_{nr} of the cross-coupled pair M_{6a} – M_{6b} for gain enhancement in the first stage, it is set automatically via an on-chip auxiliary control loop as will be described in Section V.

B. Differential and Common-mode DC Gains

The small-signal differential DC voltage gains of the first- and second stage, A_{d01} and A_{d02}, are given by

$$A_{d01} = -\frac{g_{m1}}{g_{m5} - g_{m6} + g_{ds1} + g_{ds5} + g_{ds6}}, \tag{1}$$

$$A_{d02} = -\frac{g_{m2} + g_{m4} \cdot \overbrace{\frac{g_{m3b,d}}{g_{m3a,c} + g_{ds3} + g_{ds4}}}^{\gamma_g}}{g_{ds2} + g_{ds3}} = -\frac{g_{m2} + g_{m4}\gamma_g}{g_{ds2} + g_{ds3}} \tag{2}$$

where the overall gain is $A_{d0} = (V_{o+} - V_{o-}) / (V_{i+} - V_{i-}) = A_{d01} \cdot A_{d02}$. In the equations, g_{mj} and g_{dsj} are the transconductance and the drain-source conductance of the transistor pair $M_{ja,b,(c,d)}$, respectively, and each pair of the transistors are assumed identical. It is noted from (1) that A_{d01} can be made very high by selecting the relative value between the transconductances g_{m5} and g_{m6}. Typically however, g_{m5} is set identical to g_{m6} so as to provide an adequate first-stage gain while ensuring overall non-negative differential load conductance over process and temperature variation.

For the small-signal common-mode DC voltage gains, they can be given by

$$A_{c01} \approx -\frac{g_{m1}}{g_{m5} + g_{m6} + g_{ds1} + g_{ds5} + g_{ds6}} \tag{3}$$

$$A_{c02} \approx -\frac{g_{m2} - g_{m4} \cdot \gamma_g}{g_{ds2} + g_{ds3}} \tag{4}$$

where the overall common-mode gain is $A_{c0} = (V_{o+} + V_{o-}) / (V_{i+} + V_{i-}) = A_{c01} \cdot A_{c02}$. The first-stage gain A_{c01} is determined by the ratio of the transconductance of $M_{1a,b}$ to those of the loads $M_{5a,b}$ and $M_{6a,b}$, and thus the common-mode attenuation due to this stage is quite limited. On the other hand, the second stage gain A_{c02} can be made small by setting $g_{m2} \approx g_{m4} \cdot \gamma_g$.

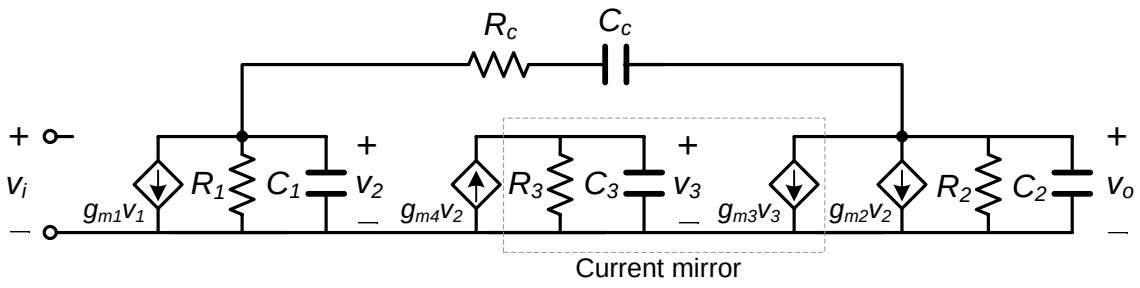


Fig. 5.2 Small-signal circuit model for CFOTA frequency analysis

C. Frequency Response and Compensation

- *Differential-Mode Characteristics*

The frequency response of the CFOTA in Fig. 5.1 and its compensation can be analytically examined using its small-signal differential half-circuit model in Fig. 5.2, where we have

$$R_1 = (g_{m5} - g_{m6} + g_{ds1} + g_{ds5} + g_{ds6})^{-1} \tag{5}$$

$$R_2 = (g_{ds2} + g_{ds3} + g_L)^{-1} \tag{6}$$

$$R_3 = (g_{m3} + g_{ds3} + g_{ds4})^{-1} \tag{7}$$

$$C_1 = C_{gs5} + C_{gs6} + C_{ds1} + C_{ds5} + C_{ds6} \tag{8}$$

$$C_2 = C_{ds2} + C_{ds3} + C_L \tag{9}$$

$$C_3 = 2C_{gs3} + C_{ds3} + C_{ds4} \tag{10}.$$

where C_{gsj} and C_{dsj} are the gate-source and drain-source capacitances of $M_{ja,b,(c,d)}$ respectively, R_L is load resistance, and C_L is the load capacitance. Also in the figure, $v_i = v_{id} = (V_{i+} - V_{i-})/2$, and $v_o = v_{od} = (V_{o+} - V_{o-})/2$. It is noted that the transistors' gate-drain capacitances and any other extrinsic capacitances that may introduce non-dominant poles/zeros at far beyond the CFOTA's unity-gain frequency ω_u are neglected.

The circuit model of Fig. 2 is quite similar to that of a conventional two-stage CMOS OTA [9], except that the second stage contains the additional components ($g_{m4}v_2$, $g'_{m3}v_3$, R_3 and C_3) that model the cross-forward path and the associated time constant R_3C_3 of the current mirrors [cf. Fig. 1]. As will be described shortly, it is this path that gives rise to important differences in the CFOTA's frequency response and compensation as compared to its conventional counterpart, particularly at frequencies near ω_u. Based on the small-signal model of Fig. 2, by omitting the second-order terms and assuming that $g_{m4}\gamma_g = g_{m2}$, it can be shown that the differential voltage gain $A_d(s)$ is given by

$$A_d(s) = \frac{V_{od}(s)}{V_{id}(s)} \approx \overbrace{g_{m1}R_1 \cdot 2g_{m2}R_2}^{A_{d0}} \cdot \frac{\left(\left(1-\frac{1}{g_{m2}R_c}\right)\frac{\tau_c\tau_3}{2}\right)s^2 + \left(\left(1-\frac{1}{2g_{m2}R_c}\right)\tau_c + \frac{\tau_3}{2}\right)s + 1}{\left(\frac{C_c}{C_{12c}}\tau_3 + \tau_c\right)\tau_1\tau_2 s^3 + \frac{C_c}{C_{12c}}\tau_1\tau_2 s^2 + 2g_{m2}R_2\frac{C_c}{C_1}\tau_1 s + 1} \tag{11}$$

where $C_{12c} = 1/(C_1^{-1} + C_2^{-1} + C_c^{-1})$ and $A_{d0} = g_{m1}R_1 \cdot 2g_{m2}R_2$ is the differential DC gain as given in (1) and (2). Also in (11), we have $\tau_1 = R_1C_1$, $\tau_2 = R_2C_2$, $\tau_3 = R_3C_3$, and $\tau_c = R_cC_c$.

Let us first consider the characteristic at low to mid-band frequencies where the non-dominant pole frequency $1/\tau_3$ of the cross-forward path, and the zero frequencies at near ω_u can be omitted. Following this, the differential gain in (11) can be simplified as

$$A_d(s) = A_{d0} \cdot \frac{1}{\frac{C_c}{C_{12c}}\tau_1\tau_2 s^2 + 2g_{m2}R_2\frac{C_c}{C_1}\tau_1 s + 1} \tag{12}.$$

By applying to (12) the assumption that the poles p_{d1} and p_{d2} of the transfer function in (12) are real and widely separate [9[, [10], the pole locations are approximated at

$$p_{d1} = -\frac{1}{2g_{m2}R_2R_1C_c}, \qquad p_{d2} = -2g_{m2}\cdot\frac{C_{12c}}{C_1C_2} \tag{13}.$$

Clearly, as the capacitor C_c and hence C_{12c} increase, the dominant pole p_{d1} is moved to a lower frequency whereas the non-dominant pole p_{d2} is pushed to a higher frequency, indicating the pole-splitting phenomenon as in a conventional two-stage OTA [9].

Let us now investigate the high-frequency characteristic. For the case that C_c is sufficiently large so that the dominant pole p_{d1} is shifted very close to DC, and that the pole p_{d2}, which is pushed toward ω_u, starts to interact with the finite pole frequency at $1/\tau_3$ of the cross-forward path, the differential gain in (11) can be re-written as

$$A_d(s) = A_{d0} \cdot \frac{\left(\left(1-\frac{1}{g_{m2}R_c}\right)\frac{\tau_c\tau_3}{2}\right)s^2 + \left(\left(1-\frac{1}{2g_{m2}R_c}\right)\tau_c + \frac{\tau_3}{2}\right)s + 1}{\left(\left(\frac{C_c}{C_{12c}}\tau_3 + \tau_c\right)\tau_1\tau_2 s^2 + \frac{C_c}{C_{12c}}\tau_1\tau_2 s + 2g_{m2}R_2\frac{C_c}{C_1}\tau_1\right)s} \tag{14}.$$

The transfer function in (14) has two non-dominant poles p_{d2} and p_{d3}, of which locations are given by

$$p_{d2,d3} = \frac{1}{2\left(R_c C_{12c} + \tau_3\right)}\left(-1 \pm \sqrt{1 - 4\frac{g_{m2} C_{12c}}{C_1 C_2}\left(R_c C_{12c} + \tau_3\right)}\right) \tag{15}.$$

The equation indicates that as C_c and hence C_{12c} increase, p_{d2} and p_{d3} are moved toward each other. This is because the term in the square root decreases with C_{12c}. Under the condition that

$$C_c = (C_1 + C_2) \cdot \frac{1 + \frac{2 g_{m2}\tau_3}{C_1 + C_2}\left(\sqrt{1 + \frac{R_c C_1 C_2}{g_{m2}\tau_3^2}} - 1\right)}{\left(4 g_{m2}\tau_3(\tau_3 + R_c C_{12}) - (C_1 + C_2)\right) \cdot \frac{1}{C_{12}}} \tag{16}$$

where $C_{12} = 1/(C_1^{-1} + C_2^{-1})$, p_{d2} and p_{d3} are identical. For C_c beyond this value, the poles become a complex conjugate pair. To summarize the locations of the poles p_{d1}, p_{d2} and p_{d3} of the CFOTA as described above, the diagram illustrating their movement against C_c is given in Fig. 5.3 based on (13) and (15).

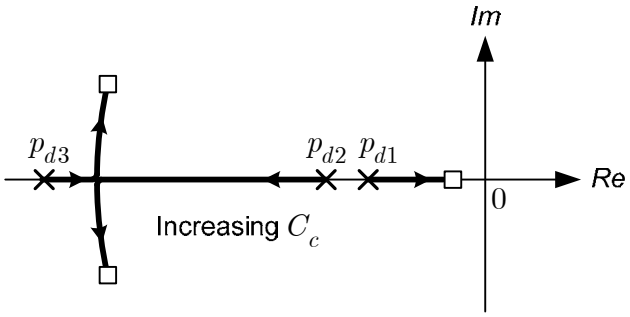


Fig. 5.3 Diagram showing movement of CFOTA's poles

As also indicated by (14), the CFOTA has two high-frequency finite zeros – one is attributed to the direct signal path provided by the compensation capacitor C_c, and the other is due to the finite pole frequency at $1/\tau_3$ associated with the cross-forward path. Under the condition of the compensation resistor $R_c < 1/g_{m2}$, the coefficients of the s^2 and s terms in the numerator of (14) are negative and positive, respectively. This result in one left-half-plane (LHP) zero z_{d1}, and one right-half-plane (RHP) zero z_{d2} which introduces phase lag, thereby shrinking the phase margin of the CFOTA. However, the RHP zero z_{d2} is entirely eliminated by setting $R_c = 1/g_{m2}$, and this yields the LHP zero z_{d1} at

$$z_{d1} = -\frac{2}{\tau_c + \tau_3} \tag{17}$$

When R_c is further increased, both of the coefficients in the numerator are positive, and the zero z_{d2} is thus moved into the left-half plane. This can be used to further improve the phase margin.

From the numerator of (14), the zero locations z_{d1} and z_{d2} are given by

$$z_{d1,d2} = -\frac{1}{\tau_3}\left(1 + \frac{\tau_{c2} + \tau_3}{2(R_c C_c - \tau_{c2})} \pm \sqrt{\left(1 + \frac{\tau_{c2} + \tau_3}{2(R_c C_c - \tau_{c2})}\right)^2 - 2\frac{\tau_3}{2(R_c C_c - \tau_{c2})}}\right) \tag{18}$$

where $\tau_{c2} = C_c / g_{m2}$. The diagram in Fig. 5.4 illustrates the movement of z_{d1} and z_{d2} against R_c based on (17) and (18).

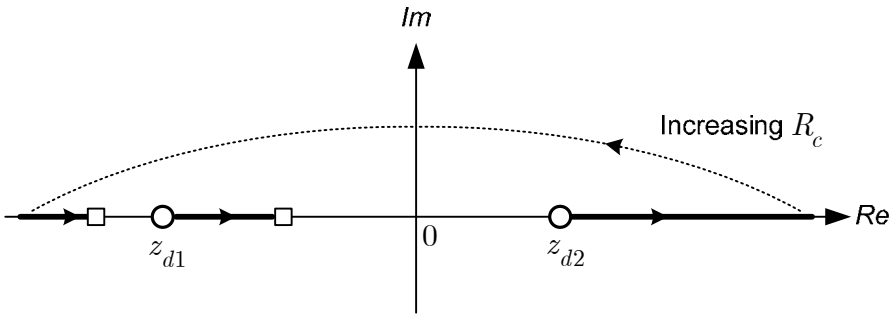


Fig. 5.4 Diagram showing movement of CFOTA's zeros

From the above discussion, it can be summarized that the differential-mode frequency characteristic of the CFOTA can be compensated in as much the same way as the conventional OTA, i.e., by virtue of the capacitor C_c for the pole splitting compensation and the resistor R_c for the RHP zero elimination. One major consideration is the effect of the complex conjugate poles p_{d2} and p_{d3} at high frequencies, particularly if C_c is beyond the value given in (16), which may degrade the phase margin. Nevertheless, the presence of the LHP zero z_{d1} effectively compensates this adverse effect. If required, z_{d2} can also be employed to further improve the phase margin, by setting $R_c > 1 / g_{m2}$.

- *Common-Mode Characteristics*

By reversing the direction of the controlled source $g_{m4}v_2$ in the cross-forward path, and setting

$$R_1 = g_{m5} + g_{m6} + g_{ds1} + g_{ds5} + g_{ds6} \tag{19}$$

, the half-circuit model of Fig. 2 can be used to investigate the common-mode frequency characteristic of the CFOTA. In this case, $v_i = v_{ic} = (V_{i+} + V_{i-})/2$, and $v_o = v_{oc} = (V_{o+} + V_{o-})/2$. Upon considering this modified model, it is seen that there is a subtraction between the direct signal path through the controlled source $g_{m2}v_2$ and the cross-forward path through the controlled source $g_{m4}v_2$ and the current mirror, yielding common-mode signal attenuation. In this way, the common-mode gain is determined at low frequencies by the signal mismatch between the direct and cross-forward paths. As frequencies increase, the pole-splitting capacitor C_c provides a feed-through signal path to the output because its impedance is reduced. When the impedance is sufficiently low, typically at mid-band frequencies, the common-mode gain becomes flat. It is noted that at high frequencies the finite pole frequency $1/\tau_3$ associated with the mirror also causes the direct and cross-forward path mismatch. However, this typically occurs beyond the frequencies where the common-mode gain has significantly dropped as a result of the parasitic capacitances.

With the use of the common-mode small-signal model, the common-mode voltage gain $A_c(s)$ can be derived and subsequently simplified as given by

$$A_c(s) = \frac{V_{oc}(s)}{V_{ic}(s)} \approx \overbrace{g_{m1}R_1 \cdot (g_{m2} - g_{m4}\gamma_g)R_2}^{A_{c0}} \cdot \frac{\dfrac{C_c - g_{m2}\tau_3}{g_{m2} - g_{m4}\gamma_g}s - 1}{\left(\tau_c + \dfrac{C_c}{C_{12c}}\tau_1\right)\tau_2 s^2 + (\tau_2 + R_2C_c)s + 1} \tag{20}$$

If real and widely separated poles are assumed, the poles of the common-mode transfer function in (20) can be approximated at

$$p_{c1} = -\frac{1}{(\tau_2 + R_2C_c)} = -\frac{1}{R_2(C_2 + C_c)}, \qquad p_{c2} = -\frac{1 + C_c/C_2}{\tau_c + \tau_1 C_c/C_{12c}} \tag{21}$$

For the finite zero in (20), it is located at

$$z_{c1} = \frac{g_{m2} - g_{m4}}{C_c - g_{m2}\tau_3} \tag{22}$$

Since it is typical that $C_c > g_{m2}\tau_3$, the zero in the common-mode characteristic is primarily due to the signal feed-through via C_c. Also from (22), $z_{c1} = 0$ if $g_{m2} = g_{m4}\gamma_g$.

D. Noise Analysis

The input-referred voltage noise spectral density in V^2/Hz of the CFOTA is expressed by

$$\frac{\overline{V_{neq,\mathrm{CFOTA}}{}^2}}{\Delta f} \approx 4kT \cdot \overbrace{\left\{\frac{K_n}{2kTC_{ox}W_1L_1}\cdot\frac{1}{f}+\frac{2}{g_{m1}}\left(n_n\sigma_{n1}+\frac{n_p}{g_{m1}}\left(\sigma_{p5}g_{m5}+\sigma_{p6}g_{m6}\right)\right)\right\}}^{R_{neq,\mathrm{OTA}}} \tag{23}$$

where $R_{neq,\mathrm{CFOTA}}$ is the equivalent input noise resistance of the CFOTA, k is the Boltzmann's constant, T is the absolute temperature, C_{ox} is the gate oxide capacitance per unit area, and K_n is the flicker noise (1/f) coefficient of the nMOS transistors which is bias dependent [11]. Also, $n_{n,p}$ are the slope factors of n- and p-MOS transistors, and $\sigma_{nj,pj}$ of $\mathrm{M}_{ja,b}$ are defined as [11].

$$\sigma_{nj,pj} = 1+\frac{4}{3}\cdot\left(\frac{I_{dj}/I_{znj,pj}}{\left(\sqrt{1+4I_{dj}/I_{znj,pj}}+1\right)^2}\right) \tag{24}$$

where $I_{znj,pj} = 2n_{n,p}(kT/q)^2(W_j/L_j)\mu_{n,p}C_{ox}$. The first term in (23) is the equivalent input 1/f noise due to the nMOS amplifiers $\mathrm{M}_{1a,b}$ of the first stage. The 1/f noise associated with the pMOS load transistors $\mathrm{M}_{5a,b}$ – $\mathrm{M}_{6a,b}$ is omitted due to the fact that it is typically much lower than that of the nMOS counterpart. For the second term in (23), it is the equivalent input thermal noise due mainly to the transistors in the first stage, which are operated in saturated moderate inversion. The noise contribution from the second-stage is omitted because it is significantly reduced by the first-stage gain.

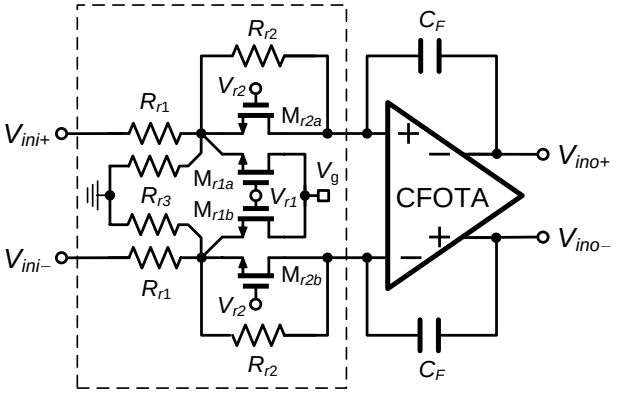
5.3 Low-Voltage Sub-threshold R-MOSFET Tunable Resistor

Shown in the dash box of Fig. 5.5(a) is the schematic of the balanced sub-threshold R-MOSFET or SubRMOS tunable resistor, utilized in conjunction with the CFOTA and feedback capacitors C_F to construct the 0.5-V SubRMOS-C integrator. The SubRMOS resistor consists of the linear resistors R_{r1} – R_{r3} and the nMOS transistor pairs $\mathrm{M}_{r1a,b}$ and $\mathrm{M}_{r2a,b}$ operated mainly in sub-threshold inversion. As compared to the structure presented in [5], additional grounded resistors R_{r3} are included. This essentially pulls down the source terminals of $\mathrm{M}_{r1a,b}$ and $\mathrm{M}_{r2a,b}$, to a DC voltage lower than the common-mode level at the inputs $V_{ini+/-}$ = 0.25 V (=$V_{ino+/-}$), and the transistors' drain terminals at $V_{i+/-} = V_g$ = 0.35 V. As a consequence, the available range of the gate tuning voltages $V_{r1,2}$ are expanded, thereby extending in the SubRMOS resistance tuning and hence the frequency tuning range of the SubRMOS-C integrator and filter. Note that the bodies of all the transistors are tied to V_{bdn} = 0.25 V to help reduce the threshold voltage.

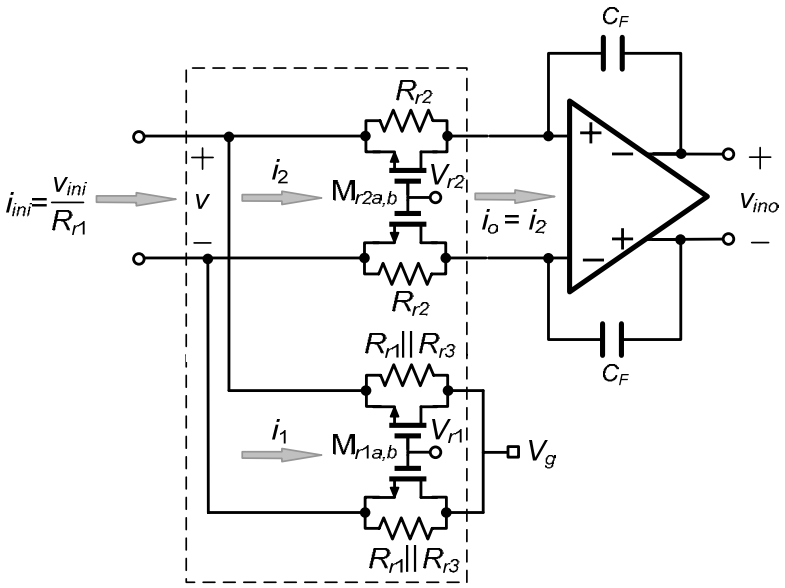
A. Operation of SubRMOS Resistor

The underlying operation of the SubRMOS resistor can be explained by its Norton's equivalent circuit, which is essentially a parallel of two nonlinear conductance branches as shown in Fig. 5.5(b), each comprising a pair of linear resistors and nonlinear sub-threshold

MOS transistors with the nonlinear characteristics $i_1 = G_1(v)$ and $i_2 = G_2(v)$. Note that all the voltage/current variables indicated (except the gate voltages $V_{r1,2}$) are of differential mode. If the characteristics of the two nonlinear conductances are *linearly* dependent, i.e. $G_1(v) = \delta \cdot G_2(v)$ where δ is a constant, the current division of $i_{ini} = v_{ini}/R_{r1}$ into i_1 and $i_2 = i_o$ is linear, and thus we achieve a linear relation between i_o and v_{ini}, regardless of the nonlinear characteristics $G_{1,2}(v)$ [5].



(a)



(b)

Fig. 5.5 Balanced SubRMOS resistor in SubRMOS-C integrator realization (a) circuit structure and (b) Norton's equivalent circuit

It is important to note that the SubRMOS technique is different from the R-MOSFET resistor in [12] which employs series linear resistors for good linearity and current-steering strong-inversion MOS transistors for tunability. The technique is also different from the

structure in [13] which makes use of a current division between two linear branches – one made from linear resistors and the other from linear quad-MOS transistors.

The SubRMOS resistor was extensively analyzed in [5], by virtue of a third-order truncated polynomial expansion of the differential source conductance characteristic of a MOS pair biased from moderate-to-weak inversion operation by the gate voltage V_r. By assuming that $M_{r1a,b}$ and $M_{r2a,b}$ are integer multiples of the unit MOS transistor at n_1 and n_2, respectively, it was derived that, based on the linear dependent condition, $G_1(v) = \delta \cdot G_2(v)$, a perfect linearization can be achieved under the parameters relation:

$$\delta(V_{r1,}V_{r2}) = \frac{(R_{r1} \,||\, R_{r3})^{-1} + n_1 \cdot g_{s,1}(V_{r1})}{R_{r2}^{-1} + n_2 \cdot g_{s,1}(V_{r2})} = \frac{n_1 \cdot g_{s,3}(V_{r1})}{n_2 \cdot g_{s,3}(V_{r2})} \tag{25}.$$

In the equation, $g_{s,1}(V_r)$ and $g_{s,3}(V_r)$ are, respectively, the first-order and third-order coefficients of the polynomial describing the nonlinear source conductance of the unit MOS transistor at the gate voltage V_r, where the drain and source bias voltages are the same as those in the SubRMOS-C integrator. Note that $g_{s,1}$ is the small-signal source conductance. Although these coefficients can be analytically computed as detailed in [5], they should be determined empirically for better accuracy since all the second-order effects are automatically incorporated. With the use of (25), the effective resistance R_{eff} of the SubRMOS resistor is given by

$$R_{eff}(V_{r1,}V_{r2}) = \frac{v_{ini}}{i_o} = \left(1 + \delta(V_{r1,}V_{r2})\right) \cdot R_{r1} \tag{26}.$$

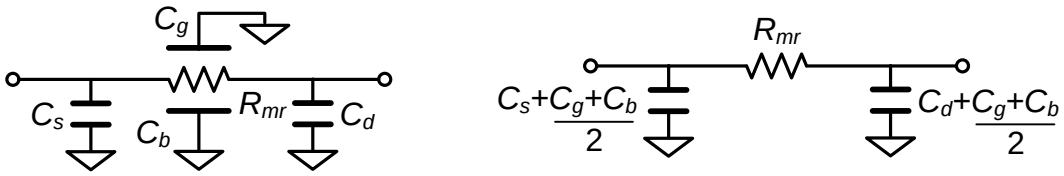
If an ideal CFOTA is assumed, the differential transfer function of the SubRMOS-C integrator in Fig. 5.5(a) is $H(s) = V_{ino}(s) / V_{ini}(s) = -1 / [R_{eff}(V_{r1}, V_{r2}) C_F s]$. As also indicated by (25) and (26), scaling of the effective resistance from R_{eff} to αR_{eff} can be simply obtained, without upsetting the parameters relation in (25) and hence the linearization condition, by modifying R_{r1} to R_{r3} by the factor α and n_1, n_2 by the inverse $1/\alpha$.

For ease of practical implementation, the gate voltage V_{r1} can be maintained at a constant voltage while V_{r2} is mainly employed for resistance tuning. Although this only satisfies the linearization condition at one level of V_{r2}, it was extensively demonstrated by experiment and simulation in [5] that wide resistance tuning ability with good linearity can be achieved, provided that a particular attention is paid to satisfying the condition in (25) at a set of V_{r1} and V_{r2} within the weak inversion MOS operation where the nonlinearity is most pronounced.

B. Effect of Parasitic Capacitance

Let us consider the capacitance of a single MOS transistor in triode operation from the small-signal equivalent circuit in Fig. 5.6(a). C_g is the distributed oxide capacitance between the channel and the gate, and C_b is the distributed depletion capacitance between the

channel and the body [14]. Note that both C_g and C_b increase with the gate area WL. C_s and C_d are the terminal capacitances due to the *p*-*n* junctions and the gate-diffusion overlaps. For the case that the channel length employed in the SubRMOS resistor is relatively short, and that the operating frequency is not too high, the distributed capacitances can be approximated by two half-split lumped capacitances $C_g/2$ and $C_b/2$ at the terminals as shown in Fig. 5.6(b). This yields a total terminal parasitic capacitance at $C_p = C_{s/d} + (C_g + C_b)/2$.



(a) (b)

Fig. 5.6 Small-signal circuits of a MOS resistor (a) distributed model [14] and (b) lumped equivalent model

The effect of the parasitic capacitances can be analyzed by substituting the simplified MOS resistor model of Fig. 5.6(b) into the SubRMOS-C integrator in Fig. 5.5(a). For those parasitic capacitors connected at the input terminals of the OTA, their influence can be omitted as long as the gain is sufficiently high, and the terminals' capacitances are reasonably matched [14]. By assuming that the parasitic capacitance due to the linear resistors is negligible, and that the CFOTA is ideal, the integrator's transfer function is given by

$$H(s) = \frac{1}{R_{eff} C_F s\left(1 + R_{rmr} C_{pmr} s\right)} \tag{27}.$$

In the equation, $C_{pmr} = C_{pmr1} + C_{pmr2}$ and $R_{rmr} = 1/[R_{r1}^{-1} + R_{r2}^{-1} + R_{r3}^{-1} + R_{mr1}^{-1} + R_{mr2}^{-1}]$. $R_{mr1} = (n_1 \cdot g_{s,1})^{-1}$ and $R_{mr2} = (n_2 \cdot g_{s,1})^{-1}$ are the small-signal source resistances of $M_{r1a,b}$ and $M_{r2a,b}$, respectively. Clearly, the transfer function exhibits a non-dominant pole frequency at $\omega_{pmr} = 1/(R_{rmr} C_{pmr})$, and this results in a phase error which in turn gives rise to a distorted frequency response in the filter. In order to ensure that the parasitic effect can be effectively compensated using a relatively simple technique, such as the use of a resistor in series with C_F to produce a compensating zero [15], ω_{pmr} should be located sufficiently far from the integrator's unity-gain frequency at $\omega_u = 1/(R_{eff} C_F)$. This can be achieved by appropriate sizing of the channel's width W and length L in the transistor pairs $M_{r1a,b}$ and $M_{r2a,b}$ [cf. Fig. 5.5(a)], so as to obtain small gate area and hence a small C_p while maintaining good matching characteristic.

C. Noise Analysis

By assuming that the thermal noise dominates, the equivalent input-referred voltage noise spectral density in V^2/Hz of the SubRMOS resistor in Fig. 5.5(a) can be derived as

$$\frac{\overline{V_{neq,\mathrm{SubRMOS}}^2}}{\Delta f} = 4kT \overbrace{\left\{ 2R_1 + 2\left(\frac{R_1}{R_3}\right)^2 R_3 + 2\left(\frac{R_1}{R_{mr1}}\right)^2 R_{mr1} + \frac{2}{\left(R_2 + R_{mr2}\right)^2}\left(1 + \frac{R_1}{R_3 \,||\, R_{mr1}}\right)^2 \left(R_{mr2}^2 R_2 + R_2^2 R_{mr2}\right) \right\}}^{R_{neq,\mathrm{SubRMOS}}} \quad (28).$$

where $R_{neq,\mathrm{SubRMOS}}$ is the equivalent input noise resistance of the SubRMOS resistor. It should be noted that (28) is based on the upper-bound thermal noise level of the transistors for a given R_{mr} under the condition $V_{ds} = 0$. Although the transistors' noise is smaller for the same R_{mr} when $V_{ds} > 0$, as in the case of the SubRMOS resistor, it is largely dependent on the terminals' voltages [16], [17]. When employed in the SubRMOS integrator and filter, the transistors' gate voltage can be varied over process and temperature, the upper bound noise employed in (28) is thus more suitable for a design in practice. Note that the transistors also exhibit 1/*f* noise since they conduct a non-zero bias current. However, this is not included in (28) because the 1/*f* noise associated with the CFOTA's input transistors $M_{1a,b}$ and the bias circuits, which will be discussed later, is significantly higher.

5.4 SubRMOS-C Integrator with On-Chip Biasing Circuits

Fig. 5.7 represents one typical filter section which utilizes the SubRMOS-C integrator. There are two SubRMOS resistors in each section, one connected to the CFOTA's inputs whereas the other connected at the outputs to provide a feedback to the preceding OTA in the filter loop. Note from the figure that the resistance is tuned via the voltage $V_{rf} = V_{r2}$, while the voltage V_{r1} is fixed at $V_g = 0.35$ V [cf. Fig. 5.5(a)]. Also shown in the figure is the gate bias circuit which consists of the resistors R_g in parallel with the cross-coupled current mirror transistors M_g to provide a differential negative conductance so that the differential gain loading effect can be avoided [2]. Note that the cross-coupled transistors also help further reduce common-mode signals.

The voltage difference between $V_{ini+/-}$ (= 0.25 V) and $V_{i+/-}$ (= 0.35 V) together with the presence of the grounded resistors R_{r3} create non-zero quiescent bias currents in the SubRMOS resistors. As shown in Fig. 5.7, for the resistors R_{r1} at the CFOTA's inputs and outputs, these are supplied by the bias transistors M_{c1} and M_{c3}, respectively. For R_{r2} and $M_{r2a,b}$, the currents are supplied by the transistors M_{c2}. Note that M_{c2} also provides the currents for the gate resistors R_g and the transistors M_g. By properly setting up the currents I_1, I_2 and I_3 of the transistors M_{c1}, M_{c2} and M_{c3}, respectively, the common-mode voltages $V_{ini+/-}$

and $V_{ino+/-}$ of the integrator, as well as $V_{i+/-}$ of the CFOTA can be set at the desired levels. This can be accomplished via the automatic generations of the gate bias voltages V_{c1}, V_{c2} and V_{c3} using negative feedback on-chip control loops, as will be described below. Note from Fig. 5.7 that the bias currents I_3 of M_{c3} are also adjusted to balance with the offset currents of the CFOTA in order to set up the output voltages $V_{ino+/-}$. The fixed bias transistors M_{c4} degenerated by the source resistors R_{c4} are added to ensure that the offset currents is unidirectional, thereby enabling a proper operation of the control loop over process and temperature variations.

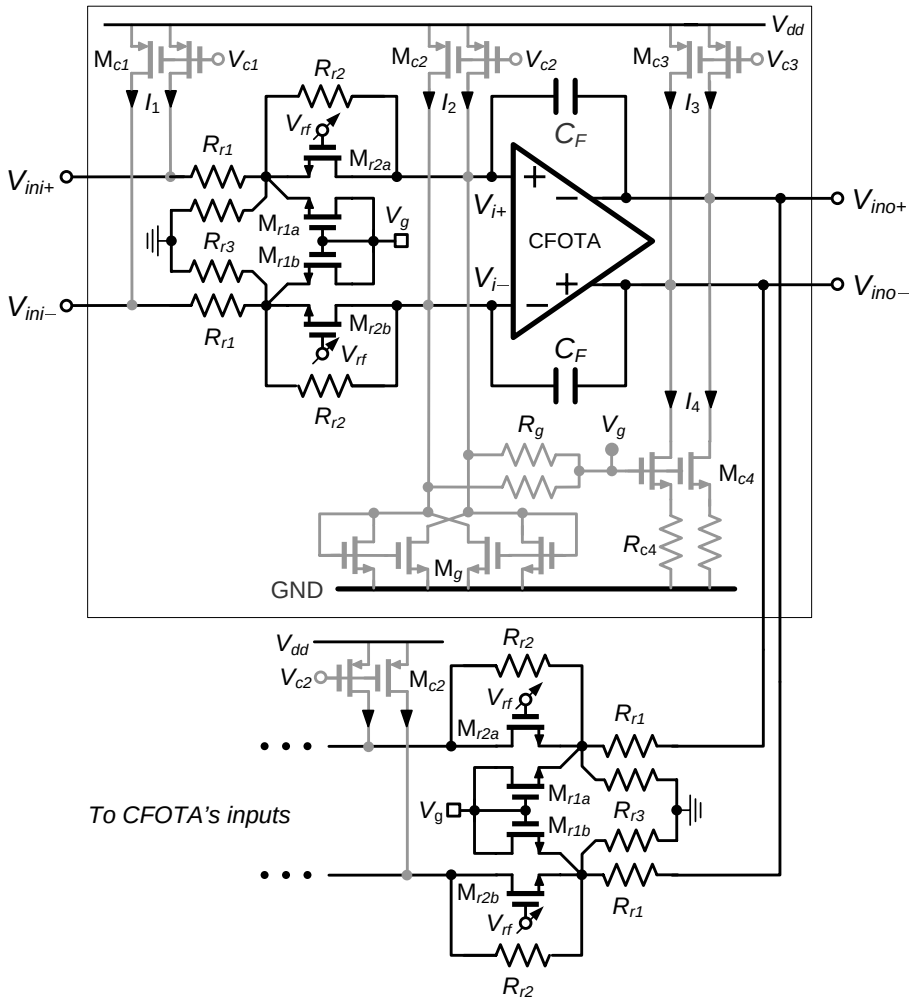
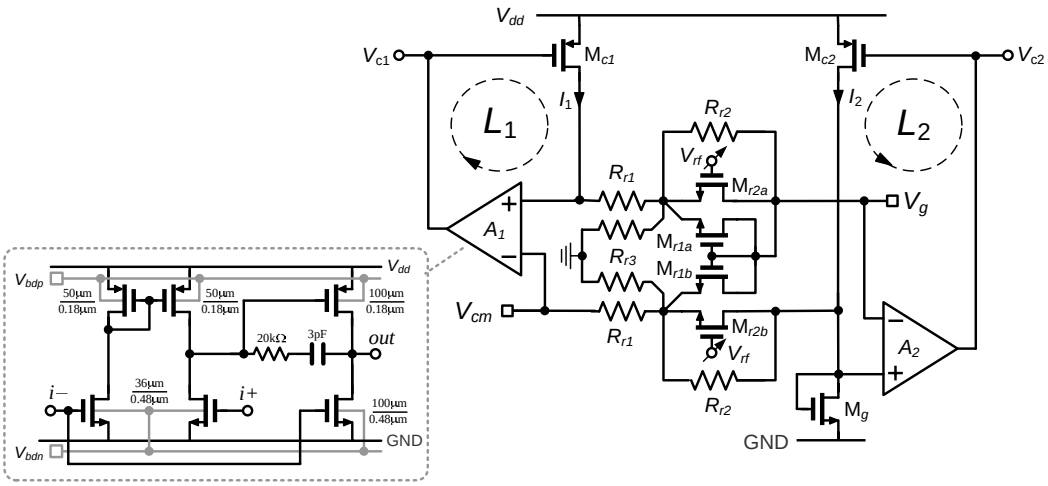


Fig. 5.7 SubRMOS-C Integrator implementation with bias circuits for setting up common-mode voltages.

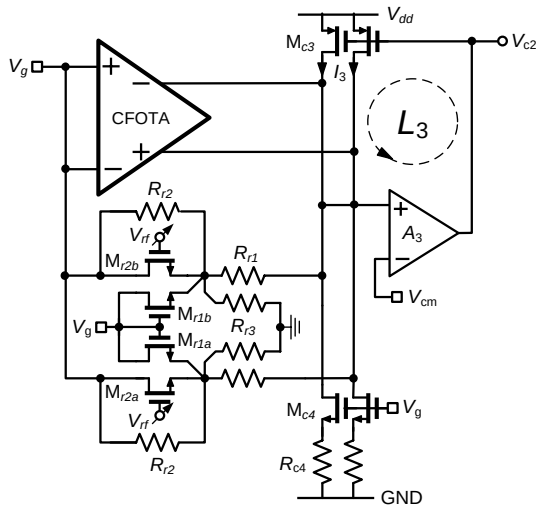
A. On-Chip Biasing Circuits

Fig. 5.8(a) shows the schematic of the control loops L_1 and L_2 for the generation of the bias voltages V_{c1} and V_{c2}, respectively, to set up the common-mode voltages $V_{ini+/-}$ and

$V_{i+/-}$. Both of the loops share a replica of the unit SubRMOS resistor employed in the main filter. The loop L_1 contains the upper part of the resistor, a replica of the bias transistor M_{c1} and a high gain amplifier A_1 (schematic in the dash box) which adjusts its output voltage V_{c1} via the negative feedback action to minimize its terminal voltages. This thereby generates V_{c1} for the common-mode voltage $V_{A1+} = V_{A1-} = V_{cm} = 0.25$ V. For the loop L_2, it contains the lower part of the unit resistor, replicas of M_{c2} and M_g and the amplifier A_2 which, via the negative feedback action, generates V_{c2} for the common-mode voltage $V_{A2+} = V_{A2-} = V_g = 0.35$ V. Note that, in the main filter, there are always two SubRMOS resistors connected to the CFOTA's input, each of which is equipped with the bias transistors M_{c2}, as shown in Fig. 5.7. Therefore, only one transistor M_g is required in the loop L_2. Fig. 5.8(b) shows the schematic of the loop L_3 for setting up the voltage $V_{ino+/-}$. It contains replicas of the CFOTA, the bias transistor M_{c3}, the unit SubRMOS resistor, the fixed bias current sources M_{c4} with R_{c4}, and the amplifier A_3. The inputs of the CFOTA and the outputs of the resistor are tied to $V_g = 0.35$ V. With a similar high-gain negative feedback action, the loop generates the voltage V_{c3} for $V_{A3+} = V_{A3-} = V_{cm} = 0.25$ V. When the generated voltages V_{c1}, V_{c2} and V_{c3} are used in the SubRMOS integrators of the main filter, by assuming perfect matches between the replica components of the loops and those of the filter, the common-mode voltages $V_{ini+/-} = V_{ino+/-} = 0.25$ V and $V_{i+/-} = 0.35$ V can be obtained.



(a)



(b)

Fig. 5.8 Biasing control loops for generation of (a) V_{c1} and V_{c2} and (b) V_{c3}. A two-stage unbuffered opamp shown in the dash box is employed as error amplifier.

B. Overall Noise Performance

By including the noise contribution from the biasing circuits, the overall noise performance of the SubRMOS-C integrator can be determined. Note that because the integrator is driven by a similar stage when employed in the filter, both the bias transistors M_{c1}, and M_{c3} are essentially connected to the outputs. Thus, their noise contributions are suppressed and can be neglected. Following this, the total equivalent input-referred voltage noise spectral density in V^2/Hz of the SubRMOS-C integrator can be given in terms of the equivalent noise resistances by

$$\frac{\overline{V^2_{eq,\text{Integrator}}}}{\Delta f} = 4kT\left\{R_{neq,\text{SubRMOS}} + \left(1+\frac{R_1}{R_3 \,||\, R_{mr1}}\right)^2\left(R_{neq,\text{CFOTA}} + R_{neq,\text{Bias}}\right)\right\} \qquad (29).$$

In the equation, $R_{neq,\text{CFOTA}}$ and $R_{neq,\text{SubRMOS}}$ are the equivalent noise resistances of the CFOTA and the SubRMOS resistors as defined in (23) and (28), respectively. For the equivalent noise resistance $R_{neq,\text{Bias}}$ of the bias circuits, it is given by

$$R_{neq,\text{Bias}} \approx R_{eff}^2\left\{\frac{1}{2kTC_{ox}}\left(\frac{2g_{mg}K_n}{W_gL_g}+\frac{g_{mc2}K_p}{W_{c2}L_{c2}}\right)\cdot\frac{1}{f}+2\left(\frac{1}{R_g}+2n_n\sigma_{ng}g_{mg}+n_p\sigma_{pc2}g_{mc2}\right)\right\} \qquad (30).$$

where $K_{n,p}$ is the bias-dependent flicker noise (1/*f*) coefficients of the n- and pMOS transistors, $n_{n,p}$ and $\sigma_{n,p}$ are as defined in (23and (24)), and R_{eff} is the effective resistance of the SubRMOS resistor as given in (26).

5.5 Practical Verification

A. Simulated Results of CFOTA

A 0.5-V CFOTA in a 0.18-μm 1.8V triple-well CMOS process for use in the experimental low-voltage prototype filter of Section V-B was designed and simulated. Table I summarizes the component parameters of the circuit. Fig. 5.9 shows the simulated differential-mode and common-mode magnitude and phase responses versus frequency with the load resistance of 75 kΩ to model the subsequent stage when operated in the filter loop.

Table I Components parameters of CFOTA [cf. Fig. 5.1]

Transistors	Sizes	Resistor and Capacitor	Values
M_{1a}, M_{1b}	240μm/0.50μm	R_c	5.0kΩ
M_{2a}, M_{2b}, M_{4a}, M_{4b}	140μm/0.36μm	C_c	4.8pF
M_{3a}, M_{3b}, M_{3c}, M_{3d}	120μm/0.36μm		
M_{5a}, M_{5b}, M_{6a}, M_{6b}	140μm/0.36μm		

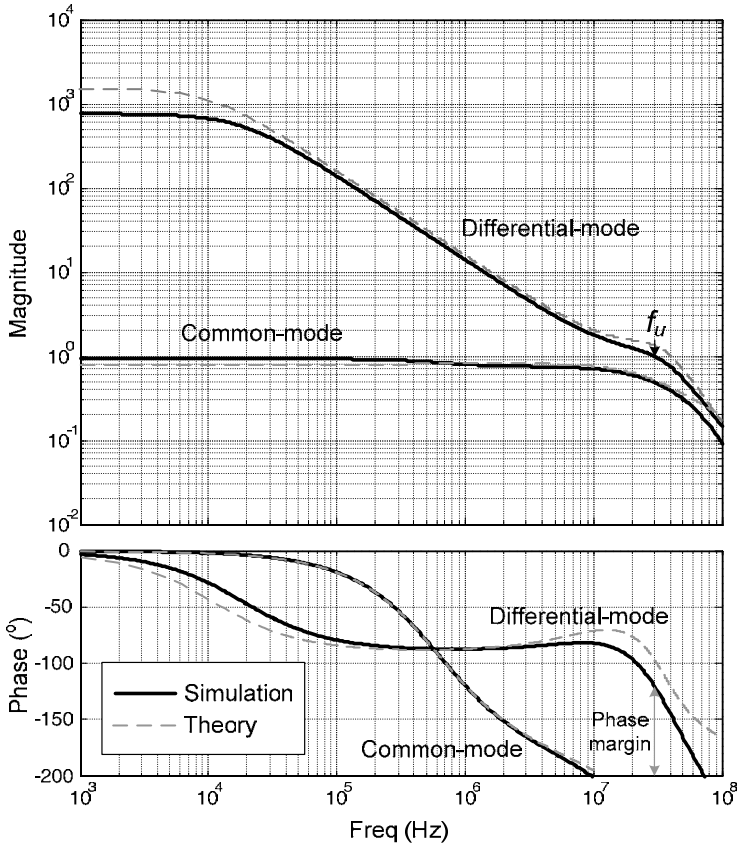


Fig. 5.9 Simulated and theoretical open-loop frequency responses under differential- and common- mode signals

From the differential-mode magnitude response, the simulated DC gain is around 58 dB at the bias voltages V_{nr} = 0.235 V. In the vicinity of the unity gain frequency at 30 MHz, the gain starts to roll off at less than –20 dB/dec, before approaching –40 dB/dec. This is due to the effect of the RHP zero z_{d1} and the non-dominant complex pole pair $p_{d2,3}$, as explained in Section II. The phase margin at more than 60° is obtained, thereby guaranteeing a good stability. For the common-mode responses, the simulated DC gain is at around unity or 0 dB. The gain drops and becomes flat at mid-band frequencies because of the feed-through signal via the compensation capacitor C_c. Subsequently, the common-mode gain rolls off at –40 dB/dec as it approaches the unity gain frequency.

Also included Fig. 9 are the theoretical plots of the frequency responses based on the derived equations in (11) and (20). Note that the circuit parameters of the small-signal CFOTA model in Fig. 2 were extracted from simulation. As evident from Fig. 9, close agreement between theory and simulation for both differential-mode and common-mode responses are obtained.

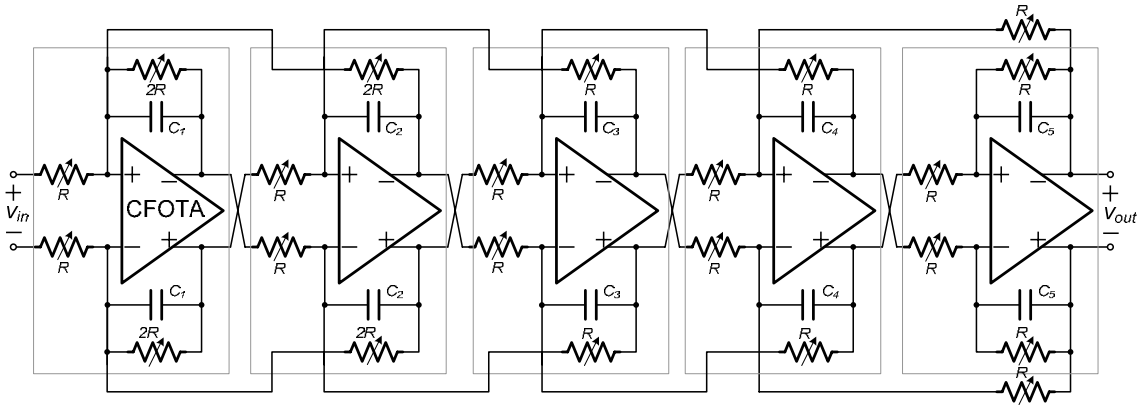


Fig. 5.10 5th-order Chebyshev filter prototype SubRMOS-C integrator techniques. Each circuit in the dash boxes is similar to Fig. 5.7.

Table II Filter design parameters

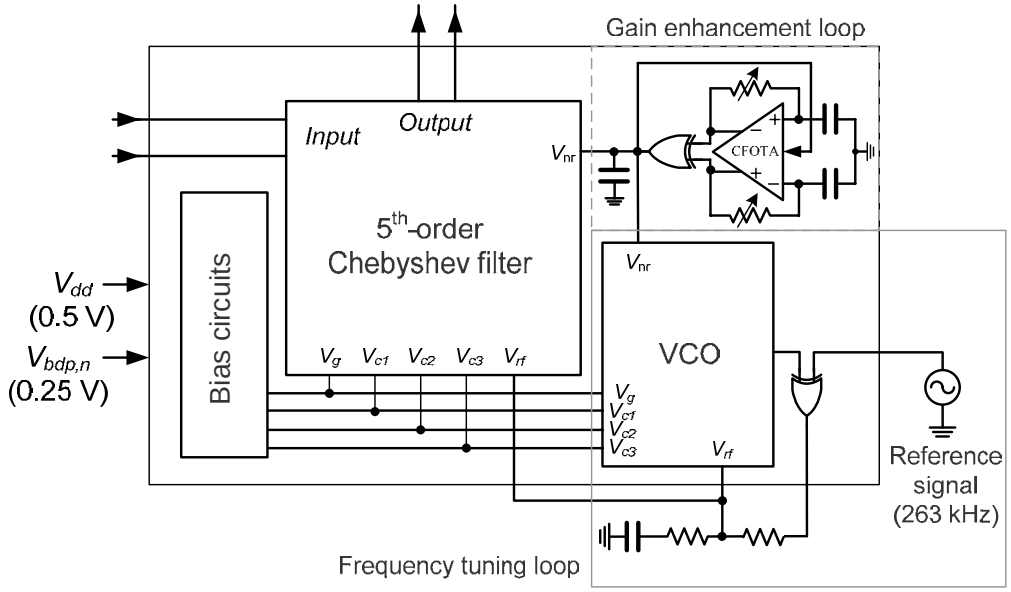
Capacitor	Value	Capacitor	Value
C_1	11.31pF	C_5	22.62pF
C_2	16.31pF	Resistor	Value
C_3	33.70pF	R	75kΩ
C_4	16.31pF		

Table III Components parameters of unit SubRMOS resistor and bias circuits [cf. Fig. 5.7] for a nominal resistance value of 150 kΩ

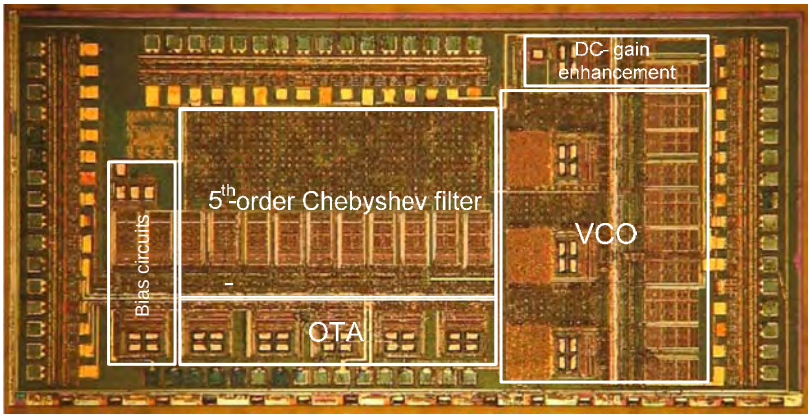
Transistors	Sizes	Resistors	Values
M_{r1a}, M_{r1b}, M_{r2a}, M_{r2b}	100μm/1.8μm	R_{r1}, R_{r2}, R_{r3}	75kΩ
M_{c1}, M_{c2}, M_{c3}	192μm/0.36μm	R_{c4}	10kΩ
M_{c4}	30μm/0.48μm		
M_g	48μm/0.48μm		

B. Experimental Results of 0.5-V SubRMOS-C filter

A 0.5-dB-ripple 5th-order Chebyshev fully-integrated filter based on the SubRMOS-C integrator techniques with the bias control loops was designed and fabricated in a 0.18-μm triple-well CMOS process. The filter prototype is shown in Fig. 5.10 and the design parameters, with no components scaling for equalization of peak signal amplitudes, are summarized in Table II. Table III summarizes the components parameters of the unit SubRMOS tunable resistor at a nominal effective resistance of 150 kΩ, which is the resistance 2R in the filter prototype. The resistance R in the filter was realized by a parallel of these two unit SubRMOS resistors. For the components parameters of the CFOTA, they are as summarized in Table I. All the linear resistors are of poly-silicon type within an n-well.



(a) [Continued]



(b)

Fig. 5.11 Prototype filter (a) block diagram and (b) chip microphotograph.

Also included on-chip is the automatic frequency tuning of the filter by means of the phase locked loop (PLL), as shown in the block diagram of Fig. 5.11(a). The voltage controlled oscillator (VCO) is of a three-stage type [2] where each of the SubRMOS-C integrator stages is matched to those employed in the main filter. The phase detector is a low-voltage XOR gate and the loop filter is an off-chip lead-lag RC network. The PLL is locked to a reference frequency by controlling the VCO's oscillation frequency through the tuning voltage V_{rf} of the SubRMOS resistors. The same voltage V_{rf} is then applied to the main filter to tune the bandwidth in a master-slave control fashion. To ensure a sufficiently high DC gain in the CFOTA, the gain enhancement loop similar to [2] is also included. As indicated in Fig. 5.11(a), the loop contains a Schmitt-trigger oscillator using the CFOTA and an XOR gate with a capacitive load to generate the bias voltage V_{nr} for the CFOTAs in the main filter. The chip microphotograph is shown in Fig. 5.11(b). Various filter performances including frequency responses, noise, and distortion were extensively measured using a Vector Analyzer HP89441A.

The measured frequency responses at different frequency tuning voltages V_{rf} = 0.25, 0.37, 0.43 and 0.50V, with the frequency control loop deactivated, are shown in Fig. 5.12. Note that our measurement system only permits measurement of differential inputs to single-ended output due to the unavailability of a differential probe. Thus, the actual differential-to-differential frequency responses are very similar to these plots but with an addition of +6 dB, yielding the differential DC gains close to 0 dB. The plot of the filter's –3 dB bandwidth versus the tuning voltage V_{rf} is given in Fig. 5.13, where the frequency tuning range from 91 kHz to 268 kHz, which is over 200% tuning ratio, are obtained. By means of the PLL-based frequency control loop, the bandwidth can be automatically tuned from 95 kHz to 260 kHz, by tracking the loop to an external reference frequency between 190 kHz to 410 kHz. Note that at the nominal bandwidth of 130 kHz, the reference frequency is at 263 kHz.

The frequency responses of the filter, with the automatic frequency tuning for 130-kHz bandwidth and gain enhancement loops activated, were measured at different power supply voltages as shown in Fig. 5.14. It can be seen from the resulting responses that V_{dd}

variation from 0.45 V to 0.6 V renders gain deviation in the passband by less than ± 0.5 dB from the nominal characteristic at V_{dd} = 0.5V where the DC gain is at –0.5 dB.

Fig. 5.15 shows the differential output noise of the filter at the nominal bandwidth and supply voltage. The measurement was taken with the help of a subtract function between the two channels of the Vector Analyzer, however with no average option for mathematical functions. Also given in the figure is the simulated output noise for comparison. The measured integrated output noise from 1 kHz to 1 MHz is 153 μV_{rms}, in close agreement to simulation at 164 μV_{rms}. The measured integrated output noise is referred to the input at 162 μV_{rms}.

Distortion measurement was carried out for single-tone and two-tone inputs to investigate the filter's harmonic and inter-modulation distortion performances, respectively. For in-band input tones at 30 kHz and 90 kHz, 1% total harmonic distortion (THD) were measured at the differential input voltages of 269 mV_{rms} and 219 mV_{rms}, respectively. This yields the in-band 1% THD dynamic ranges at 62.0 dB and 60.7dB, respectively. Measured in-band inter-modulation distortion for two-tone inputs at 50 and 55 kHz is shown in Fig. 5.16. From the plots, the 3rd-order input intercept point IIP3 was extrapolated at +4 dBV_{rms}, and the in-band spurious-free dynamic range (SFDR) is at 53.7 dB. For the two-tone inputs at 90 and 95 kHz, the SFDR was measured at 54.0 dB. Out-of-band inter-modulation test was also performed for two-tone inputs at 200 and 350 kHz, where the IIP3 was measured at +14.0 dBV_{rms} and the SFDR at 59.2 dB. The overall filter performances are summarized in Table IV.

As also evident from Table III, the filter based on the SubRMOS-C integrator techniques compare favorably with comparison to the 0.5-V filter implementation in [2]. In particular, a wider tuning range by a factor of 1.7 and a lower current consumption by almost a factor of two are achieved. In addition, although the input noise is larger by almost two folds because there is extra noise contribution from the bias transistors at the inputs of the CFOTAs as explained in Section IV, a significant improvement in the linearity still offers a higher dynamic range by more than +4 dB. It is important to note that such a good linearity performance was obtained without dynamic range optimization via filter parameters scaling, and individual sizing of the OTAs depending on the load requirement as employed in [2].

The chip area for each circuit block of the filter is also given in Table IV. As noticed, the overall area is larger when compared to the corresponding blocks of the implementation in [2]. This is primarily because of the fact that the nominal resistance of the unit SubRMOS resistor was selected at the resistance $2R$ of the filter prototype in Fig. 5.10, and that each of the linear resistor components in the SubRMOS network has a higher value than its effective resistance R_{eff}. Moreover, unlike [2], no high resistivity resistors, which can occupy smaller area by more than two folds, were employed. It is also noted that no attempt was made on area minimization, specifically the VCO section, during the filter layout.

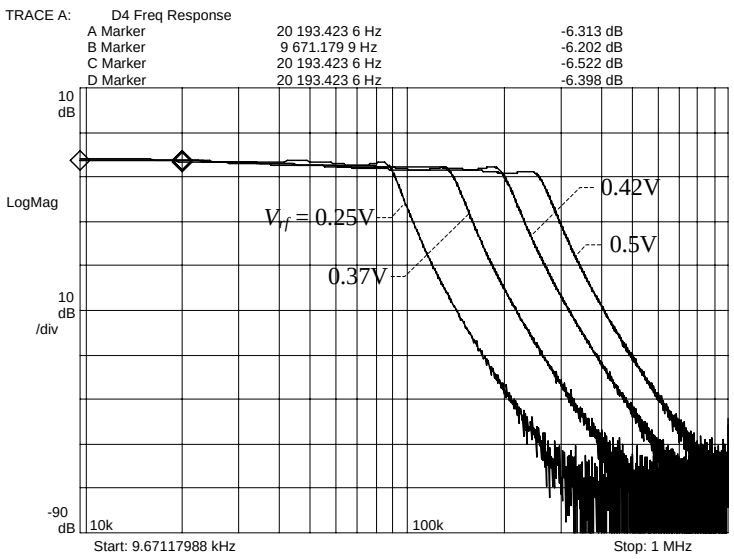


Fig. 5.12 Differential-to-single-ended frequency responses at different frequency tuning voltages V_{rf}.

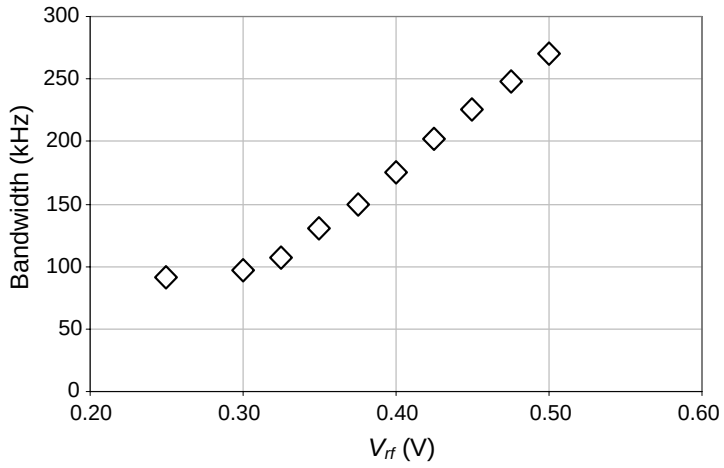
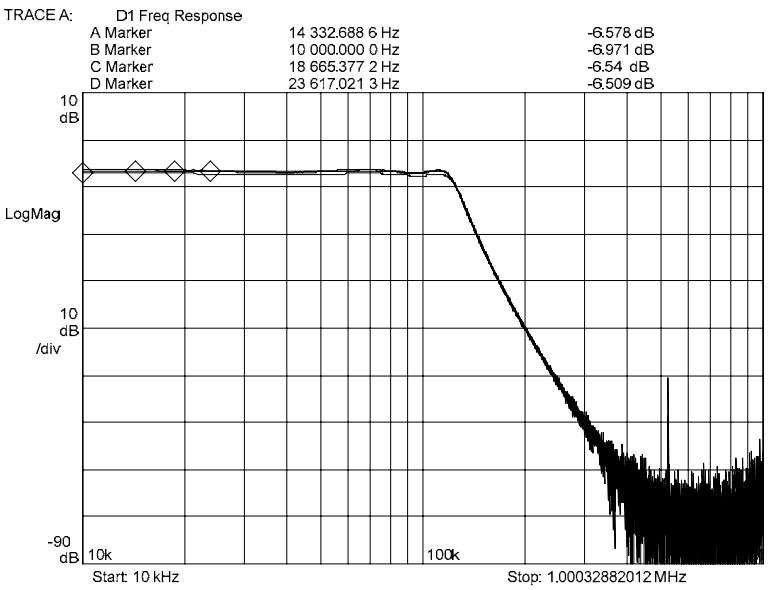
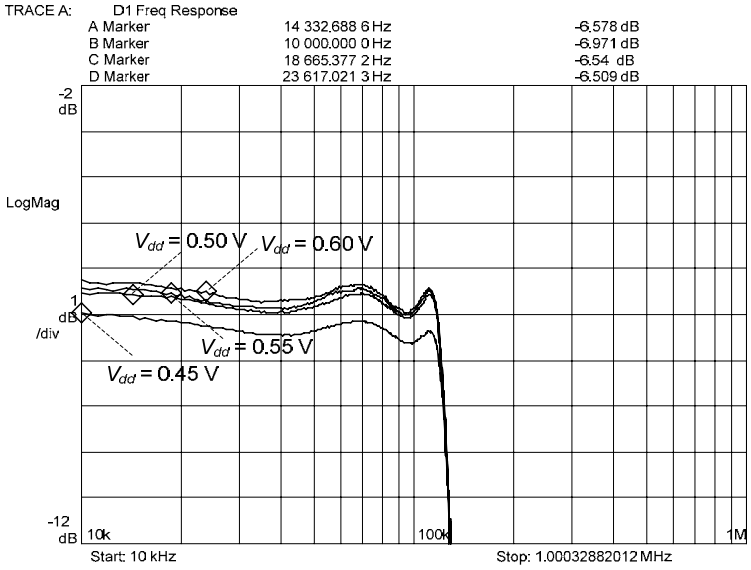


Fig. 5.13 Bandwidth versus frequency tuning voltages.



(a)



(b)

Fig. 5.14 (a) Frequency responses and (b) passband detail at V_{dd} = 0.45, 0.50, 0.55 and 0.60V (PLL is locked to a reference frequency at 263 kHz)

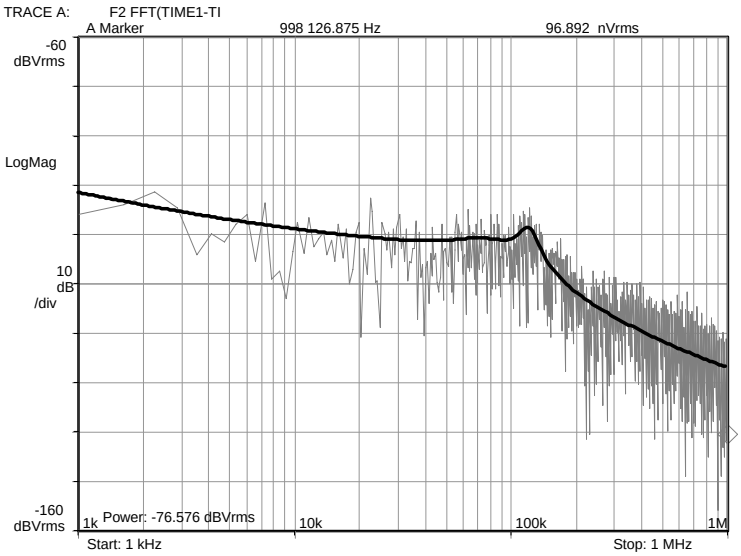


Fig. 5.15 Measured (gray line) versus simulated (dark line) differential output noise.

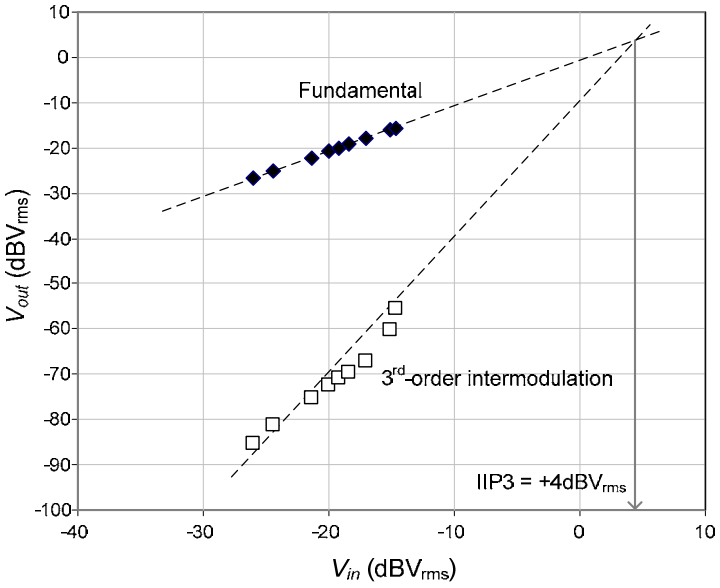


Fig. 5.16 Two-tone inter-modulation measurement with 50 and 55 kHz input frequencies.

Table IV Performance comparison with 0.5-V filter implementation in [2]

	[2]	This work
Supply voltage	0.5 V	0.5 V
Technology	0.18-μm	0.18-μm
Threshold voltage with $V_b = V_s$	0.5 V	0.42 V
Filter type	5th-order Elliptic	5th-order Chebyshev
Nominal –3dB bandwidth	135 kHz	130 kHz
DC gain (differential)	0 dB	–0.5 dB
Differential output noise†	NA	153 μV_{rms}
Input-referred noise	87 μV_{rms}	162 μV_{rms}
Dynamic range (1%-THD)	56.6 dB	60.7 dB
In-band IIP3 (f_{in} = 50kHz, 55kHz)	–3 dBV_{rms}	+4 dBV_{rms}
Out-of-band IIP3	+5 dBV_{rms}	+14 dBV_{rms}
In-band spurious-free dynamic range (SFDR)	NA	53.7 dB (f_{in} = 50, 55kHz) 54.0 dB (f_{in} = 90, 95kHz)
Total current consumption	2.2 mA	1.2 mA
Frequency tuning range	88 – 154 kHz	91 – 268 kHz
PLL lock range: - Capture range - Free-running frequency	 NA NA	190 – 400 kHz 190 – 220 kHz 203 kHz
PLL tone feed-through	85 μVrms @ 280kHz	9 μVrms @ **263kHz**‡
Chip area - OTAs - Filter resistors and capacitors - Bias circuits - VCO + DC Enhancement	 0.33×0.7 mm^2 (0.23 mm^2) 0.55×0.7 mm^2 (0.38 mm^2) 0.13×1.0 mm^2 (0.13 mm^2) 0.87×0.3 mm^2 (0.26 mm^2)	 0.25×1.17 mm^2 (0.29 mm^2) 0.7×1.17 mm^2 (0.82 mm^2) 0.75×0.25 mm^2 (0.19 mm^2) 1.07×0.77 mm^2 $+ 0.2 \times 0.67$ mm^2 (0.96 mm^2)

†: Integrated over 1 kHz to 1 MHz
‡: measured at single-ended output with no input signal applied

VI. Conclusions

The cross forward operational transconductance amplifiers (CFOTA) and the sub-threshold R-MOSFET (SubRMOS) resistors for a very low supply voltage application have been developed and extensively analyzed. Viability of the techniques has been demonstrated through the implementation of a 0.5-V fully-integrated SubRMOS-C filter. In exchange for a moderate increase in chip area, one obtains a lower current consumption due to an improved transconductace/bias-current efficiency of the CFOTA as compared to the two-stage weak inversion gate-input OTA in [2]. In addition, a wider frequency tuning range and a higher dynamic range are obtained due to extended tuning resistance and enhanced linearity in the SubRMOS resistors as compared to the filter tuning via the weak inversion MOS varactors [2]. This should make the CFOTA and SubRMOS techniques promising alternatives to very low-voltage, low-power, high-dynamic range filter implementation for future portable, wearable and implantable electronic devices.

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Output จากโครงการวิจัยที่ได้รับทุนจาก สกว.

1. ผลงานตีพิมพ์ในวารสารวิชาการนานาชาติ
   1.1 A. Worapishet, J. B. Hughes. “Performance enhancement of switched-current technique using sub-threshold MOS operation”, IEEE Transactions on Circuits and Systems – I: Regular Paper, Vol.55, No.11, pp. 3582-3592, December 2008 (Published).
   1.2 A. Worapishet, P. Khumsat, “Analysis and design of Sub-threshold R-MOSFET tunable resistor”, IEICE Transactions on Electronics, Vol.E92C, No.1, pp. 178-182, January 2009 (Published).
   1.3 P. Khumsat and A. Worapishet, “Very Low Voltage Mixer Techniques for 0.5-V Operation”, submitted to Microelectronics Journal.
   1.4 P. Khumsat and A. Worapishet, “0.5-V, low-power, wide frequency-tuning fully-integrated filter using cross-forward common-mode cancellation and sub-threshold R-MOSFET resistor techniques”, submitted to IEEE Transactions on Circuits and Systems – I: Regular Paper.

2. การนำผลงานวิจัยไปใช้ประโยชน์
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3. อื่นๆ คือผลงานตีพิมพ์ในที่ประชุมวิชาการในประเทศ ดังนี้
   3.1 P. Khumsat and A.Worapishet, “A 0.5-V 600-μW 125-kHz fully-integrated OTA-R-MOSFET-C filter using Cross-Forward common-mode cancellation and sub-threshold resistor techniques”, อยู่ระหว่างการพิจารณาเพื่อตีพิมพ์เผยแพร่ในการประชุมวิชาการทางวิศวกรรมไฟฟ้า ครั้งที่ 34 พฤศจิกายน 2554.

ภาคผนวก

บทความที่ได้รับการตีพิมพ์ในวารสารนานาชาติ

Performance Enhancement of Switched-Current Technique Using Subthreshold MOS Operation

Apisak Worapishet, *Member, IEEE,* and John B. Hughes

***Abstract*—The general performance of class AB switched currents (SI) is analyzed using the general MOS equations valid for all regions of operation. Using a figure-of-merit combining speed, dynamic range, and power consumption, the overall performance is shown to improve progressively as the SI memory transistors' operating region is moved from strong inversion to moderate and then weak inversion. The analysis is validated first by experiment using transistor arrays and then by simulation using 0.35-μm, 0.18-μm, and 90-nm CMOS process data. After discussing nonideal behavior of the weak inversion memory cell, the following two practical designs are described: a cascoded class AB memory at 1.25-V supply in the 3.3-V 0.35-μm process and a two-step sampling class AB memory at 0.6-V supply in the 1.8-V 0.18-μm process, and each demonstrates good performance.**

***Index Terms*—Class AB circuits, sampled-data circuits, subthreshold CMOS circuits, switched-current (SI) technique.**

I. Introduction

SINCE ITS inception over a decade ago, the switched-current (SI) technique has been claiming the following two main advantages over switched capacitors (SC): Because it operated in the current domain, it should be less impacted by lowering supply voltage, and because it did not use explicit capacitors, it should be better suited to "digital" CMOS. The SI technique has been found useful in many analog applications where a compatibility with standard digital CMOS and low supply voltage, as well as a small chip area, is of main concern [1]–[13]. However, despite numerous circuit developments, all using transistors operating in strong inversion (i.e., square-law characteristics), performance never competed with that of SC. Theoretical comparisons of SI and SC [14], [15] established that competitive performance could be achieved using class AB techniques, but very low voltage operation was hindered by the use of strong inversion operation. As CMOS processes have headed toward smaller feature sizes and lower supply voltage, designs have been forced toward operating their transistors in moderate or even weak inversion, i.e., in the subthreshold region, and the earlier theoretical comparison is no longer sufficiently general.

With this in mind, it has become necessary to extend the theoretical study by using the general saturated MOS model valid for all regions of inversion. In Section II, the overall performance, expressed in terms of a figure-of-merit (FoM) embracing speed (F_C), dynamic range (DR), and power consumption (P), is derived. Section III discusses how SI performance is affected by the operating region of its transistors, and Section IV provides a practical validation of the theory established in Section II. Section V describes some important nonideal effects. Two practical subthreshold designs are then demonstrated in Section VI, and finally, conclusions are given in Section VII.

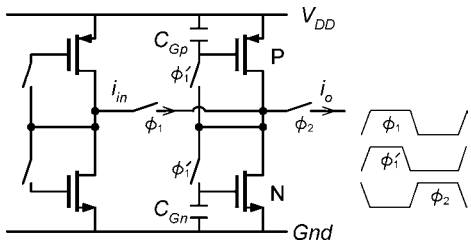

Fig. 1. Basic class AB SI memory configuration for FoM performance analysis.

II. Theoretical Performance Analysis

The general performance analysis presented in this section follows along similar lines to that presented earlier [14], [15] for strong inversion. Thus, a cascade of the basic class AB memories shown in Fig. 1 is chosen since these form the basic configuration used by SI filters and ADCs. The SI memory has a sampling phase ϕ_1, during which an amplifier, made up from p- and n-MOS complementary transistors, is in a closed loop due to the closure of the switches ϕ_1'. The voltage on its memory capacitors settles to a value determined by the input current $i_{\rm in}$ and the transconductance of the memory transistors. On the hold phase ϕ_2, the amplifier is open loop, and the voltage held on the memory capacitors, together with the same transconductance, produces the output current i_o which is close to $i_{\rm in}$. To promote analysis simplicity without loss of generality, it is assumed that the n- and p-MOS memory transistors are symmetrical, i.e., with identical transconductance parameter (β), threshold voltage (V_T), and memory capacitance $(C_{Gn} = C_{Gp} = C_G)$, among others. All the parasitic capacitances are neglected, leaving only the gate-to-source capacitance $(C_{\rm GS})$ and gate-to-body capacitances $(C_{\rm GB})$ to form the total memory capacitance $C_{\rm tot} = 2C_G = 2(C_{\rm GS} + C_{\rm GB})$. Note that $C_{\rm tot}$ is dominated by $C_{\rm GS}$ in strong inversion and by $C_{\rm GB}$ in weak inversion memory operation. Also, all the switches are assumed to have zero on-resistance, and only thermal noise from transistors is included. Unless stated otherwise, saturation operation in the memory transistors is assumed throughout, and signals are sinusoidal.

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The following analysis is based on the approximate "single-piece" saturation model equations for MOS transistors [16], valid for all regions of inversion. It should be noted that although a compromise of the accuracy over the entire operating range is anticipated, the simple model can achieve a balanced compromise between simplicity and accuracy. In the model, the I_D–$V_{\rm GS}$ characteristic, the small-signal transconductance g_m, the gate capacitance C_G, and the thermal-noise power spectral density $S_n(f)$ of a MOS transistor are given by

$$I_D = I_S \cdot \left[\ln\left(1 + e^{\frac{V_{\rm GS}-V_T}{2n\phi_t}}\right)\right]^2 \tag{1a}$$

$$g_m = \frac{I_D}{n\phi_t f(x)} \tag{1b}$$

$$S_n(f) = 4kT_j\left(\frac{1}{2} + \frac{1}{6}\cdot\frac{x}{f(x)^2}\right)ng_m \tag{1c}$$

$$C_G = WLC_{\rm ox}\left[1 - \frac{1}{n}\cdot\left(1 - \left(\frac{3}{2} + \frac{f(x)}{x}\right)^{-1}\right)\right] \tag{1d}$$

with $I_S = 2\beta n\phi_t^2$, $x = I_D/I_S$, and $f(x) = (\sqrt{1+4x}+1)/2$. In the equations, $\phi_t = kT/q$ is the thermal voltage, n is the slope factor ($1 < n < 2$), k is the Boltzmann constant, T_j is the absolute temperature, $C_{\rm ox}$ is the oxide capacitance, W is the channel width, L is the channel length, and $\beta = \mu_{\rm eff}C_{\rm ox}W/L$ is the transconductance parameter, where $\mu_{\rm eff}$ is the effective mobility. The mobility reduction effect is modeled as $\mu_{\rm eff} = \mu_0/(1+\theta\cdot V_{\rm GT})$, where $V_{\rm GT} = V_{\rm GS} - V_T$, μ_0 is the low-field mobility, and θ is the mobility reduction parameter [16].

A. FoM Formulation

We now develop the FoM, ${\rm FoM} = F_C\cdot{\rm DR}/P$, from expressions for the memory clock frequency F_C, the power consumption P, and the DR.

The memory's clock frequency F_C is related to the composite memory time constant, $C_{\rm tot}/(2g_m)$. Using (1a) and (1b), this gives

$$F_C = \frac{2g_m}{NC_{\rm tot}} = \frac{2I_D}{NC_{\rm tot}n\phi_t f(x)} \tag{2}$$

where N is a constant which depends on the desired settling accuracy (e.g., $N \approx 9$ for 0.1% settling accuracy [15]).

The average power consumption P for a maximum sinusoidal signal current is given by

$$P = \rho I_D V_{\rm DD} \tag{3}$$

where I_D is the memory cell's quiescent current. The factor ρ needs further explanation. Under large-signal conditions, the current flowing into the supply rail depends on both the circuit operation and the region of operation of its transistors. The factor ρ is the ratio of the average power supply current under maximum-signal conditions to the cell's quiescent current I_D. For a class A SI memory, ρ is unity. In a class AB memory, since it can handle input signals larger than I_D, $\rho > 1$ and is dependent on the inversion region of the memory transistors. The supply voltage $V_{\rm DD}$ is determined by the threshold voltage V_T and also the operating region of the memory transistors.

Similar to continuous-time translinear MOS circuits with class AB operation where input currents can be much larger than the quiescent bias current, the output noise of class AB SI is dependent on the input-current level, particularly at subthreshold operation [17], [18]. With such a noise characteristic, the signal-to-noise ratio employed in [14] and [15] is not applicable, and DR is adopted as the performance measure to define the usable input range [18]. For the DR calculation, whereas the minimum input signal is limited by the total sampled noise current $\sqrt{\bar{i}_n^2}$ from the memory transistors, the maximum signal $\hat{i}_{\rm in}$ is limited by the linearity performance. However, for the sake of simplicity, it is assumed here that $\hat{i}_{\rm in}$ is determined at a point where substantially all of the input current flows into one or other of the SI memory's composite transistors. This is, in turn, set by the quiescent bias current I_D and the region of inversion of the memory transistors. By using (1a)–(1c), the DR can be expressed as

$${\rm DR} = \frac{\hat{i}_{\rm in}^2}{2\bar{i}_n^2} = \frac{(\alpha I_D)^2}{8\cdot S_n(f)\cdot {\rm BW}_n} = \frac{n\left(\alpha\phi_t f(x)\right)^2}{\frac{8kT_j}{C_{\rm tot}}\left(1+\frac{1}{3}\cdot\frac{x}{f(x)^2}\right)} \tag{4}$$

where ${\rm BW}_n = g_m/2C_{\rm tot}$ is the equivalent noise bandwidth of the composite memory. The factor α is the ratio of the peak value of the maximum signal current to the quiescent current I_D. Similar to the factor ρ, $\alpha = 1$ for a class A memory and $\alpha > 1$ for a class AB memory and is dependent on the operating region of the memory transistors.

From the derived expressions (2)–(4), the general FoM of an SI memory is thus expressed as

$${\rm FoM} = \frac{F_C\cdot{\rm DR}}{P} = \frac{\alpha^2}{\rho}\cdot\frac{\phi_t}{NV_{\rm DD}}\cdot\frac{f(x)}{4kT_j\left(1+\frac{1}{3}\cdot\frac{x}{f(x)^2}\right)}. \tag{5}$$

The analysis of the factors ρ and α is the subject of the next section.

B. Calculation of Dependent Factors ρ and α

For SI memories using transistors operating in strong inversion, (1a) converges to the square-law relation, $I_D = (\beta/2n)\cdot V_{\rm GT}^2$, and the function $f(x) \approx \sqrt{x} = \sqrt{I_D/I_S}$ since $I_D \gg I_S$. For weak inversion, (1a) becomes the exponential relation, $I_D = I_S\cdot\exp(V_{\rm GT}/n\phi_t)$, and $f(x) \approx 1$ as $I_D \ll I_S$. Note that, for the calculation of I_D and $f(x)$ in (1a)–(1d) in moderate inversion, one must resort to numerical computation.

For a class AB SI memory, the factor α is determined by considering how an input current $i_{\rm in}$ is shared between the memory transistors N and P in Fig. 1. The peak value of the maximum signal $\hat{i}_{\rm in}$ is that which forces substantially all the current to flow in one transistor while substantially cutting off the other. Following this, we have $\alpha = 4$ in the strong inversion memory [11]. For the subthreshold memory operation, it can be shown numerically using (1a) that, for the same quiescent current I_D, $\hat{i}_{\rm in}$ increases further, i.e., $\alpha > 4$. This is primarily attributed to a heavier companding characteristic in a MOS transistor, i.e., from square-root companding [19] in strong inversion to natural log–exponential companding in weak inversion. For this, α can be determined analytically from the relation between the input

TABLE I
SUMMARY OF ANALYTICAL PERFORMANCE EXPRESSIONS

Performance	*Strong Inversion SI*	*Weak Inversion SI*
F_C	$\frac{4I_D}{NC_{tot}V_{GT}}$	$\frac{2I_D}{NC_{tot}n\phi_t}$
P	$\frac{3I_DV_{DD}}{2}$	$3.37 \cdot I_DV_{DD}$
DR	$\frac{3C_{tot}V_{GT}^2}{8nkT_j}$	$\frac{49C_{tot}n\phi_t^2}{4kT_j}$
FoM	$\frac{1}{nNkT_j} \cdot \frac{V_{GT}}{V_{DD}}$	$\frac{7.28}{NkT_j} \cdot \frac{\phi_t}{V_{DD}}$

current $i_{\rm in}$ and the variation in the gate-overdrive voltage $v_{\rm GT}$ as follows:

$$i_{\rm in} = I_S e^{\frac{V_{\rm GT}+v_{\rm GT}}{n\phi_t}} - I_S e^{\frac{V_{\rm GT}-v_{\rm GT}}{n\phi_t}} = 2I_S \cdot \sinh\left(\frac{v_{\rm GT}}{n\phi_t}\right). \quad (6)$$

If the memory transistors' current ratio is assumed to be 100:1 for the maximum-signal condition, it can be shown that we have the peak overdrive at $\hat{v}_{\rm GT} \approx 2.3 \cdot n\phi_t$. From (6), this subsequently yields the peak current factor $\alpha = \hat{i}_{\rm in}/I_D = 2\sinh(2.3) \approx 9.9$ in the class AB weak inversion memory.

Next, we consider the factor ρ. This is determined by calculating the average power supply current for the same maximum sinusoidal input current used in the determination of the factor α. For a class AB strong inversion memory with a balanced structure, $\rho = 3/2$ [15]. As the memory operation moves to moderate inversion, ρ gradually increases due to a larger peak input current handling capacity, as described earlier. At weak inversion, the instantaneous supply current $I_{\rm DD}(t)$ under a sinusoidal input current that gives an instantaneous memory transistor gate overdrive $v_{\rm GT}(t)$ is given by

$$\begin{aligned} I_{\rm DD}(t) &= I_S e^{\frac{(V_{\rm GT}+v_{\rm GT}(t))}{n\phi_t}} + I_S e^{\frac{(V_{\rm GT}-v_{\rm GT}(t))}{n\phi_t}} \\ &= 2I_D \cosh\left(\operatorname{arcsinh}\left(\frac{i_{\rm in}}{2I_D}\right)\right). \end{aligned} \quad (7)$$

With the peak gate-overdrive voltage at $\hat{v}_{\rm GT} = 2.3 \cdot n\phi_t$ due to the peak input current $\hat{i}_{\rm in} = 9.9 \cdot I_D$, the average supply current for half of the balanced memory can be computed, and this yields ρ in the weak inversion class AB SI memory as

$$\begin{aligned} \rho &= \frac{\frac{1}{2\pi}\int_0^{2\pi} \hat{I}_{\rm DD}(t)\, d\omega t}{2I_D} \\ &= \frac{1}{2\pi}\int_0^{2\pi} \cosh\left(\operatorname{arcsinh}\left(\frac{9.9}{2} \cdot \sin(\omega t)\right)\right) d\omega t \\ &\approx 3.37. \end{aligned} \quad (8)$$

Using the foregoing analysis, the analytical expressions for a class AB SI memory under strong and weak inversion operations were derived, and these are summarized in Table I. The expressions will be particularly useful for performance discussion in the next section. In the table, due to interstage transmission constraints between two identical class AB SI memories, the maximum quiescent gate overdrive for strong inversion is limited to $V_{\rm GT} = V_T/2$, and hence, we have $V_{\rm DD} = 3 \cdot V_T$[14]. At weak inversion, $V_{\rm DD}$ can be below $2 \cdot V_T$ when $I_D < I_S$. However, even though $V_{\rm DD}$ is inherently small, it must be made large enough to ensure saturated operation during interstage transmission. Since the peak gate-overdrive voltage is at $\hat{v}_{\rm GT} = 2.3 \cdot n\phi_t$ and the weak inversion memory transistors require $V_{\rm DS,min} \geq\sim 5\phi_t$ to keep saturated operation [16], the minimum supply voltage for the basic subthreshold SI memory becomes

$$V_{\rm DD,\,min} \approx 2 \cdot (2.3 \cdot n + 5) \cdot \phi_t. \quad (9)$$

For a typical value of the slope factor, i.e., $n = 1.2$, and $\phi_t = 26$ mV at 300 K, we have $V_{\rm DD,\,min} = 0.38$ V.

As the improvement in subthreshold class AB SI performance relies heavily on the ability to handle large input current, it is also instructive to discuss the effects that may influence the peak current handling. At strong inversion, mobility reduction results in less than square-law I_D–$V_{\rm GS}$ characteristic in the memory transistors, and this tends to increase the voltage swing for the same drain current variation. Since there is a limit to the maximum voltage signal, a reduction in peak input current results. At weak inversion, a similar effect occurs due to the slope factor n, i.e., a larger n in the exponential I_D–$V_{\rm GS}$ characteristic necessitates a larger voltage swing. In effect, the memory transistors' operation may be moved into moderate inversion over the intervals near the peak voltage swing, and this results in a lower peak current handling. Another important effect can result from the asymmetry between the composite memory transistors. This makes one of the devices cut off more quickly than the other, unbalancing the drain current handling and reducing the peak input current. In the general model equation in (1a), differences in any of the parameters, except the threshold voltages, contribute to a reduction in the peak input current handling, but the most pronounced effect is the mismatch in the slope factors at weak inversion. The parameters α for the maximum input signal current and ρ for the average supply current, including the aforementioned effects, can be obtained numerically.

III. PERFORMANCE DISCUSSION

The FoMs were calculated from (5), with α and ρ being numerically determined, as outlined in Section II-B, and with the transistor slope factor set to $n = 1$ and mobility degradation set to $\theta = 0$. Fig. 2 shows the FoMs versus $V_{\rm GT}$ for the class AB SI at different threshold voltages $V_T = 0.5$, 0.4, and 0.3 V. This corresponds to CMOS process generations spanning from 0.35 μm to 90 nm according to the SIA roadmap. The range of $V_{\rm GT}$ is from $-V_T/2$ to $+V_T/2$, and all the plots are normalized to their corresponding strong inversion FoMs at the maximum $\hat{V}_{\rm GT} = V_T/2$. Also, included in Fig. 2 is the variation of $V_{\rm DD}$ for the same range of $V_{\rm GT}$ and V_T.

With the memory transistors in strong inversion, the FoM plots indicate that the performance of class AB SI remains almost constant with falling $V_{\rm GT}$. This is also predicted by the analytical FoM expression for strong inversion operation in Table I

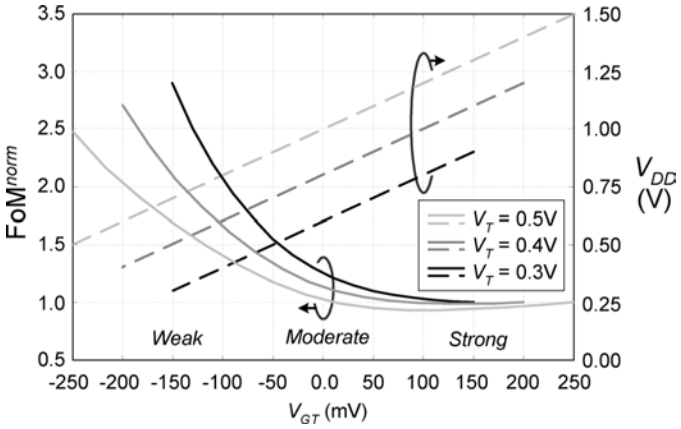

Fig. 2. Normalized basic class AB FoM performance and operating supply voltage $V_{\rm DD}$ versus $V_{\rm GT}$ at different memory transistor's threshold voltages.

(with $V_{\rm GT} = V_T/2$ and $V_{\rm DD} = 3{\cdot}V_T$) and was already reported in detail in [16]. When entering moderate to weak inversion, the FoM performance starts to rise, and $V_{\rm DD}$ falls with falling $V_{\rm GT}$ and V_T, indicating that class AB SI should offer better performance in modern CMOS processing. Interestingly, such a trend is in stark contrast to SC where performance is known to fall steadily with falling $V_{\rm DD}$. Also, note that the supply voltage level falls significantly when operating in weak inversion.

The FoM improvement at smaller gate overdrives can be explained by investigating how each of the performance vectors, namely, DR, F_C, and P, changes with $V_{\rm GT}$. Consider, without loss of generality, a scenario in which $V_{\rm GT}$ falls but the quiescent drain current I_D in the memory transistors and the total capacitance $C_{\rm tot}$ remain *constant*. Based on the analysis in Section II, the plots of the performance vectors versus $V_{\rm GT}$, *all normalized* to their corresponding values at $\hat{V}_{\rm GT} = V_T/2$, are shown in Fig. 3(a)–(c) for $V_T = 0.5$ V as a case example. It should be noted that, at strong and weak inversion operations, the performance dependences in the figures follow the expressions summarized in Table I.

With strong inversion, the maximum signal current swings and signal power are almost constant [$\alpha \sim 4$ at strong inversion in Fig. 3(a)]. However, the reduced $V_{\rm GT}$ at a constant I_D necessitates the use of transistors with a proportionally higher transconductance g_m. It also produces a quadratically increased noise power since both the noise PSD and $\rm BW_{\it n}$ increase. This results in a quadratic reduction of the DR against $V_{\rm GT}$ ($\rm DR \propto V_{GT}^2$ for strong inversion SI). Since we have kept $C_{\rm tot}$ constant, there is a proportional increase in memory speed F_C due to a higher g_m [$F_C \propto 1/V_{\rm GT}$; see Fig. 3(b)]. The power consumption P falls with $V_{\rm GT}$ because of the reduced $V_{\rm DD}$ and almost constant average peak supply current [$\rho \sim 1.5$ at strong inversion in Fig. 3(c)]. Therefore, the net result is an almost constant FoM for SI with strong inversion, as evident in Fig. 2 and Table I, despite falling $V_{\rm GT}$.

With moderate to weak inversion, as $V_{\rm GT}$ falls, the memory transistors' characteristics are gradually changed from a square-law to an exponential relationship. This yields an increasing maximum signal current swing and, hence, signal power, even though I_D is constant [see α rising to ~9.9 from the moderate to the weak inversion region in Fig. 3(a)].

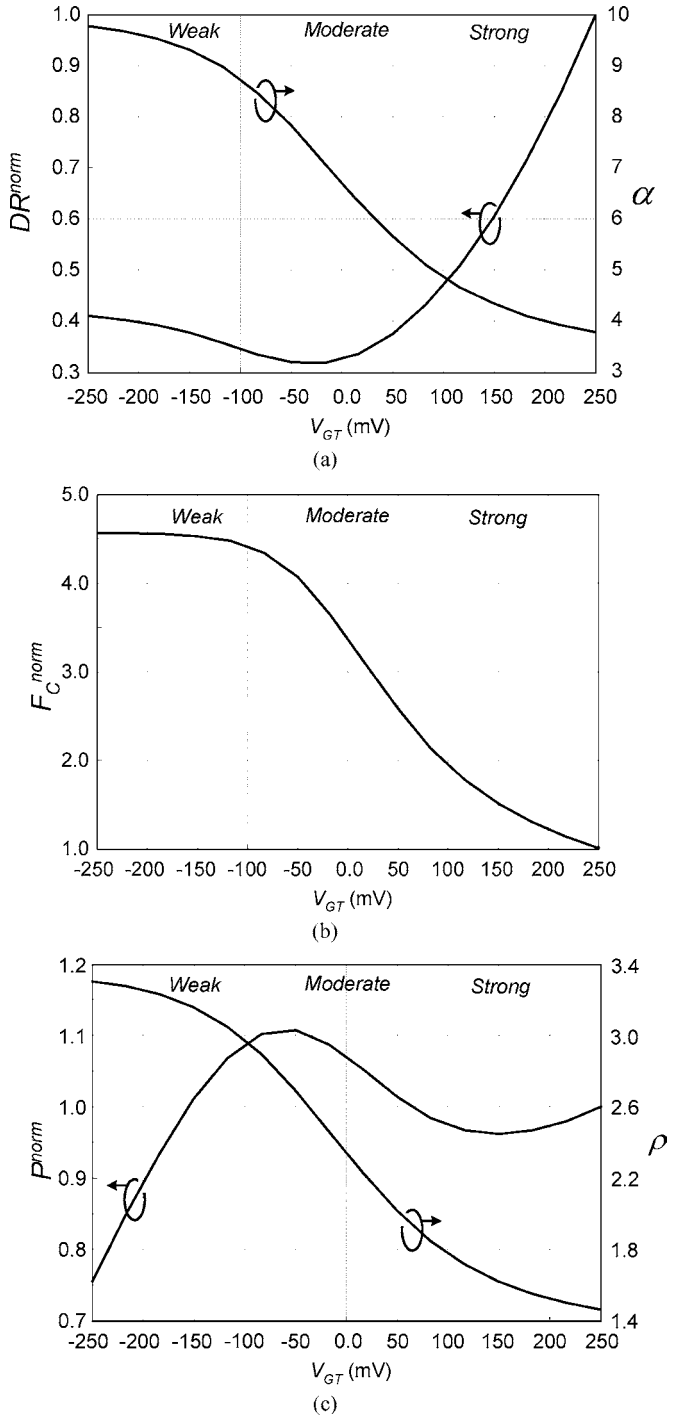

Fig. 3. Theoretical variations of basic class AB SI performances against $V_{\rm GT}$.

Similarly, the transconductance g_m, and hence noise power, must increase to accommodate the reduced $V_{\rm GT}$. However, the increases are slower than with strong inversion, and so, the DR drops more gradually and eventually stays almost constant [see $\rm DR^{norm}$ at the moderate to the weak inversion region in Fig. 3(a)]. Similarly, the increase in the memory speed F_C is also less [see F_C at the moderate to the weak inversion region in Fig. 3(b)]. The power consumption P rises slowly in moderate inversion because $V_{\rm DD}$ falls slowly, while the average supply current falls more quickly due to the increased signal

TABLE II
EXTRACTED MOS MODEL PARAMETERS FOR CD4007 TRANSISTOR ARRAYS.

Parameter	*pMOS*	*nMOS*
I_S (A)	2.2 x 10^{-3}	7.2 x 10^{-3}
$\lvert V_T \rvert$ (V)	1.322	1.518
n	1.415	2.284
θ (V^{-1})	0.1839	0.1755

swing [see ρ rising to ~3.37 from the moderate to the weak inversion region in Fig. 3(c)]. Eventually, in weak inversion, the average supply current stays almost constant, and thus, P falls proportionally with $V_{\rm DD}$ [see P falling at weak inversion in Fig. 3(c)].

With these performance dependences, the overall effect is that the FoM is improved for class AB SI operating in moderate to weak inversion, as shown in Fig. 2. As $V_{\rm GT}$ falls in weak inversion, $V_{\rm DD}$ falls proportionally, and the FoM rises inversely, as indicated in Table I.

IV. ANALYSIS AND PERFORMANCE VERIFICATIONS

A. Experimental Performance

The analysis results obtained in Section II, particularly the input signal handling and signal-dependent supply current, are first verified by a breadboard implementation of the basic balanced class AB SI memory, using CD4007 transistor arrays as CMOS memory transistors and CD4016 as memory switches. Listed in Table II are the parameters of the MOS equation in (1a) for both the p- and n-MOS transistor arrays extracted to obtain the best overall fit to their measured characteristics in saturation over the operating range from strong to weak inversion with the help of MATLAB optimization tools. The maximum clock frequency F_C and sinusoidal input were set at 1 kHz and 100 Hz, respectively. The input V–I and output I–V converters were implemented by AD844 operational current amplifiers and linear resistors to facilitate voltage-domain measurement. For this measurement, the gate-overdrive voltages $V_{\rm GT}$ were adjusted via the supply voltage $V_{\rm DD}$ to set the operating region of the memory transistors. Since this also affected the transconductance, the memory bandwidth was maintained by adding external memory capacitors which could be tuned for memories operating in strong or weak inversion.

Fig. 4 shows both the measured peak signal current factor α and the measured peak average supply current factor ρ versus $V_{\rm GT}$. Also shown are the plots of α and ρ obtained from numerical calculation based on the theoretical analysis where the maximum errors as compared with the measured results are about 6.7% for α and 4% for ρ. From the figures, it can be noticed that both α and ρ at $V_{\rm GT} = -0.2$ V, i.e., weak inversion memory operation, are somewhat smaller than the theoretical predictions in (6) and (7). This is because the slope factor n and the parameter I_S of the p- and n-MOS memory transistors are considerably different, as evident in Table II. In order to illustrate the voltage *compression* characteristic in the weak inversion SI, the transient gate–source voltage waveforms of the class AB memories with strong inversion ($V_{\rm GT} = 0.8$ V) and weak inversion

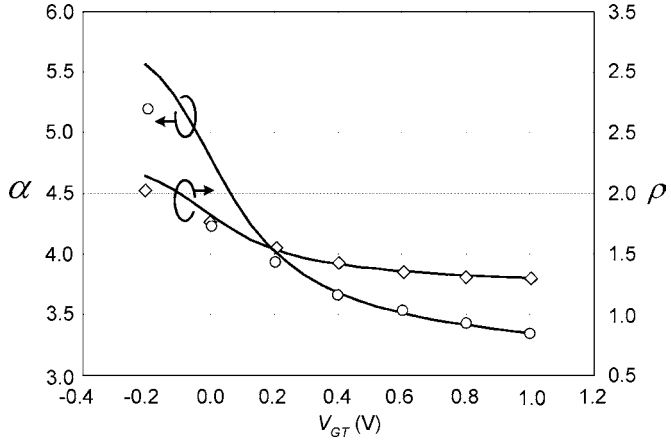

Fig. 4. (Markers) Measured and (solid) simulated plots of α and ρ versus $V_{\rm GT}$.

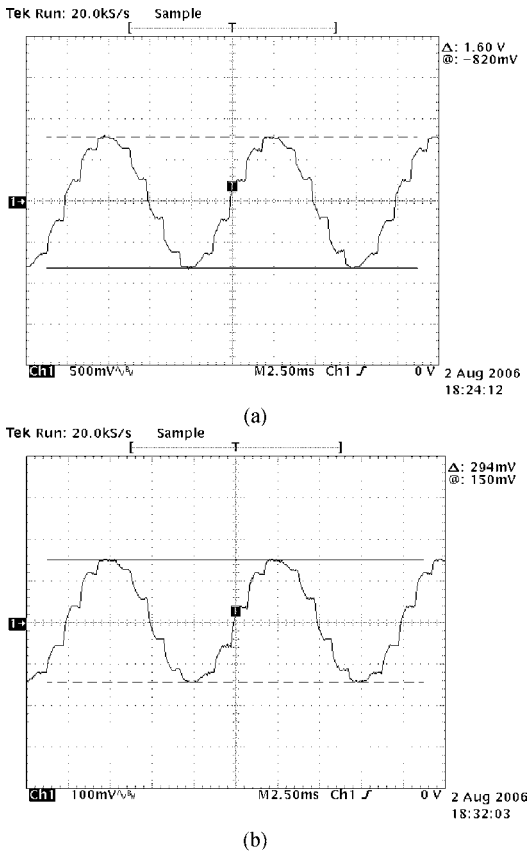

Fig. 5. Voltage waveforms at the basic class AB SI memory's gate under maximum sinusoidal input at (a) strong inversion and (b) weak inversion operating conditions.

($V_{\rm GT} = -0.2$ V) at their corresponding *peak* input currents were measured, and these are shown in Fig. 5(a) and (b), respectively. Whereas the signal voltage swing in strong inversion is on the order of the threshold voltage $V_{\rm TP}$ or $V_{\rm TN}$ in Table II, that of the weak inversion memory is compressed to only a few hundred millivolts.

B. Simulated FoM Performance

Following the breadboard experimental verification, the theoretical performance of subthreshold class AB SI in IC imple-

TABLE III
EXTRACTED MOS MODEL PARAMETERS FOR 0.35-μ UNIT TRANSISTORS

Parameter	*pMOS*	*nMOS*
I_S (A)	255 x 10^{-9}	231 x 10^{-9}
$\lvert V_T \rvert$ (V)	0.71	0.50
n	1.28	1.26
θ (V^{-1})	0.805	0.285
WLC_{ox} (F)	44.8 x 10^{-15}	56.4 x 10^{-15}

mentation is demonstrated via simulation using 3.3-V 0.35-μm CMOS process data. The simulation models for MOS transistors are BSIM3v3. The extracted model parameters for the selected unit transistor dimensions, i.e., $(W/L)_p = 4.6\ \mu\text{m}/2.5\ \mu\text{m}$ and $(W/L)_n = 3.0\ \mu\text{m}/4.0\ \mu\text{m}$, are summarized in Table III. Notice from the table that the p- and n-MOS transistors of the process exhibit good symmetrical characteristics (except V_T, but this has no impact on the performance). Similar to the experimental test, the operating condition of the memory transistors was set by varying V_{GT} through V_{DD}. Although there was flexibility to simultaneously maintain the memory's transconductance and capacitance at different V_{GT}'s by adjusting both W and L of the memory transistors, we chose to maintain the transconductance by only modifying the width W, which enabled us to use *multiples* of the unit transistor. This, however, did not maintain the memory speed ($F_C = 1$ MHz), and so, we compensated this by adding a sufficient number of unit capacitors. The total composite memory's transconductance and capacitance were held at $g_{mp} + g_{mn} = 50\ \mu\text{S}$ and $C_{\text{tot}} = 3.5$ pF, respectively. In simulation, the cascade configuration of class AB memories in Fig. 1 was driven by an ideal input current source and was loaded by an identical "diode-connected" memory cell.

Fig. 6(a)–(d) shows the simulated results of DR, P/I_D, F_C/I_D, and FoM versus V_{GT}, respectively, along with the plots of α in Fig. 6(a) and ρ in Fig. 6(b). Normalizing the operating speed and power for I_D removes the variation of I_D with V_{GT}, and this enables easier comparison with the theoretical plots of Figs. 2 and 3. The calculated performances are also included in the figures where the maximum error percentages for each plot are about 8.6% for α, 4.0% for ρ, 32.5% for DR, 5.1% for P/I_D, 15.7% for F_C/I_D, and 17.3% for FoM. Some of the errors are quite significant due to an accuracy compromise of the extracted parameters needed to obtain the good overall fit of the approximate model equation in (1a). However, a close relationship is observed in Fig. 6(a)–(b) between the calculated and simulated characteristics, as the memory operation moves from strong to weak inversion. In this 0.35-μm CMOS process with the average $V_T = (V_{TP} + V_{TN})/2 \approx 0.6\ V$ (see Table III), the FoMs of the weak inversion SI are better than those of the strong inversion counterpart by a factor of 1.27 from simulation and a factor of 1.5 from calculation [Fig. 6(d)]. Although the improvement factor is modest (because the process has large V_T), it should be noted that the strong inversion memory requires $V_{\text{DD}} = 1.75$ V, whereas the weak inversion SI operates at about $V_{\text{DD}} = 1.0$ V, which is a reduction by more than 40%.

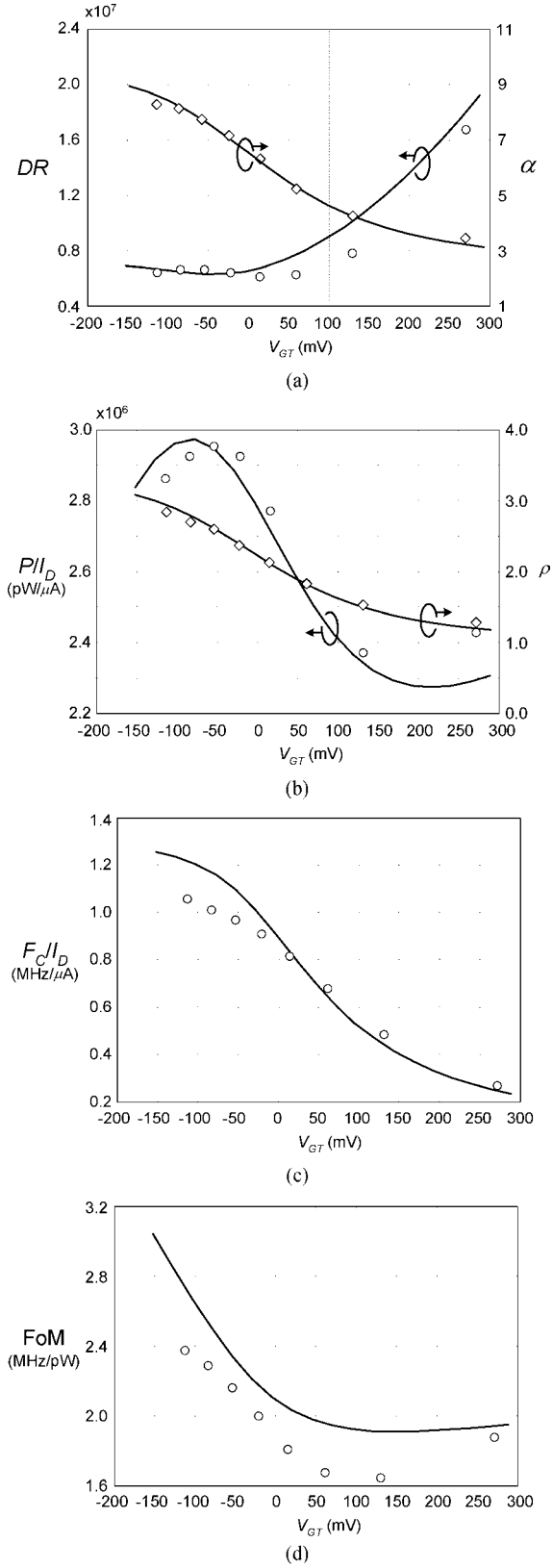

Fig. 6. (Markers) Simulated and (solid) theoretical plots of basic class AB SI performances in the 0.35-μm CMOS process.

To show further the performance trend of the subthreshold class AB SI memory, the same memory test as that previously used was also conducted using low-threshold transistors

TABLE IV
(A) EXTRACTED MOS MODEL PARAMETERS FOR 0.18-μ UNIT TRANSISTORS.
(B) EXTRACTED MOS MODEL PARAMETERS FOR 90-nm UNIT TRANSISTORS

Parameter	*pMOS*	*nMOS*
I_S (A)	643 x 10^{-9}	585 x 10^{-9}
$\lvert V_T \rvert$ (V)	0.22	0.33
n	1.44	1.35
θ (V^{-1})	0.531	0.656
WLC_{ox} (F)	245.3 x 10^{-15}	205.6 x 10^{-15}

Parameter	*pMOS*	*nMOS*
I_S (A)	480 x 10^{-9}	487 x 10^{-9}
$\lvert V_T \rvert$ (V)	0.29	0.23
n	1.16	1.14
θ (V^{-1})	0.943	0.488
WLC_{ox} (F)	171.2 x 10^{-15}	184.5 x 10^{-15}

of more advanced 1.8-V 0.18-μm and regular transistors of 1.2-V 90-nm CMOS processes with BSIM3v3 MOS models. For the 0.18-μm process, the unit transistor dimensions were chosen at $(W/L)_p = 9.5\ \mu\text{m}/3.0\ \mu\text{m}$ and $(W/L)_n = 6.5\ \mu\text{m}/6.0\ \mu\text{m}$. For the 90-nm process, the unit transistor dimensions were chosen at $(W/L)_p = 5.0\ \mu\text{m}/2.5\ \mu\text{m}$ and $(W/L)_n = 3.0\ \mu\text{m}/5.5\ \mu\text{m}$. From the simulated transistors' characteristics, the MOS parameters were extracted for theoretical computation and are summarized in Table IV(A) for the 0.18-μm process and in Table IV(B) for the 90-nm process. With similar total memory transconductance and capacitance to those of the 0.35-μm CMOS design, the simulated performance vectors versus V_{GT} are shown in Figs. 7(a)–(d) and 8(a)–(d), along with the calculated results. For the 0.18-μm process, the maximum error percentages for each plot are about 4.9% for α, 9.8% for ρ, 25% for DR, 8.1% for P/I_D, 18% for F_C/I_D, and 12.8% for FoM. For the 90-nm process, the maximum error percentages for each plot are about 7.8% for α, 7.4% for ρ, 21.2% for DR, 2.6% for P/I_D, 12.1% for F_C/I_D, and 12.9% for FoM. Despite these errors, similar dependences between the calculated and simulated characteristics are observed in all the performance metrics and for both processes. For the 0.18-μm process, it is noticed from the α and ρ plots at weak inversion that both the peak current handling and supply current are reduced compared to those obtained from 0.35-μm and 90-nm CMOS processes. This is primarily due to the effect of asymmetrical slope factors n between the employed CMOS devices [see Table IV(A)]. With such low threshold voltage processes, it is shown in Figs. 7(d) and 8(d) that the weak inversion SI has a FoM improvement of more than two for both simulations and calculations. The required supply voltage of the weak inversion SI is at $V_{\text{DD}} = 0.35$ V for the 0.18-μm process and at $V_{\text{DD}} = 0.36$ V for the 90-nm process. These are less than half of the supply voltage used for the strong inversion memories in 0.18-μm and 90-nm processes ($V_{\text{DD}} = 0.81$ and 0.74 V, respectively).

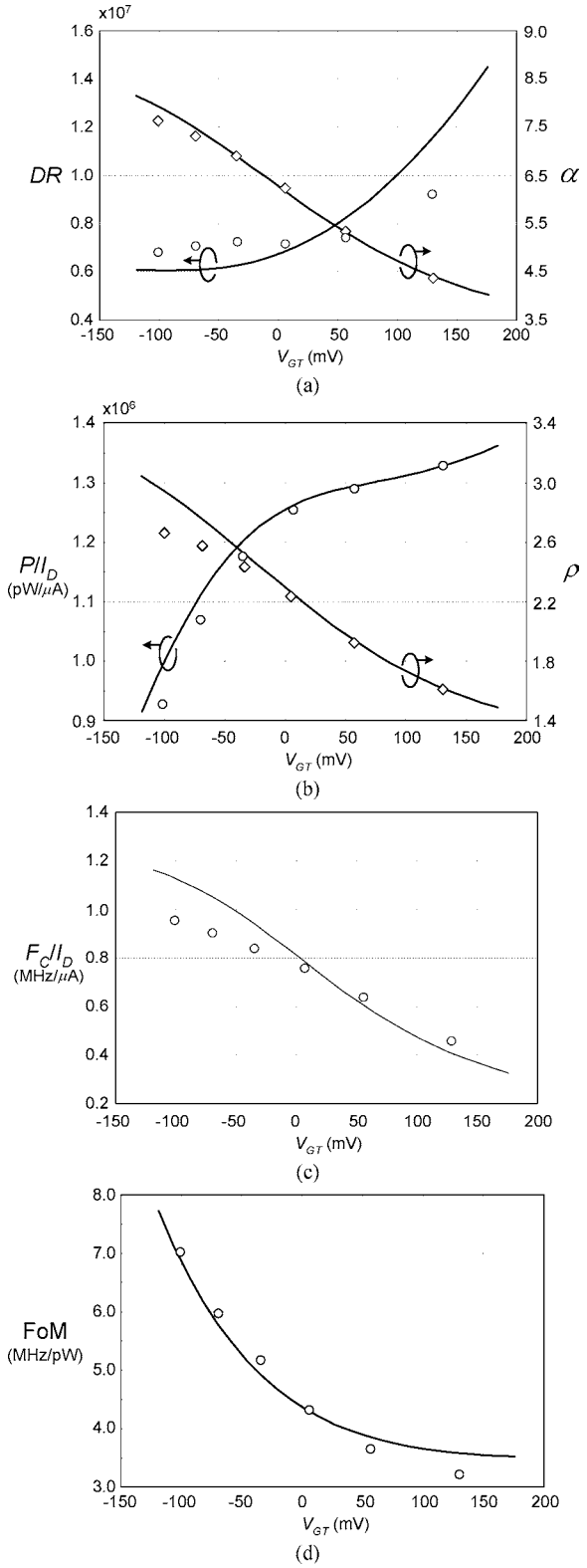

Fig. 7. (Markers) Simulated and (solid) theoretical plots of basic class AB SI performances in the 0.18-μm CMOS process.

V. NONIDEAL BEHAVIOR

This section describes important second-order nonidealities that affect SI performances in the subthreshold operating region, specifically in terms of speed and transmission accuracy. These considerations are useful in designing and optimizing subthreshold SI circuits in practice.

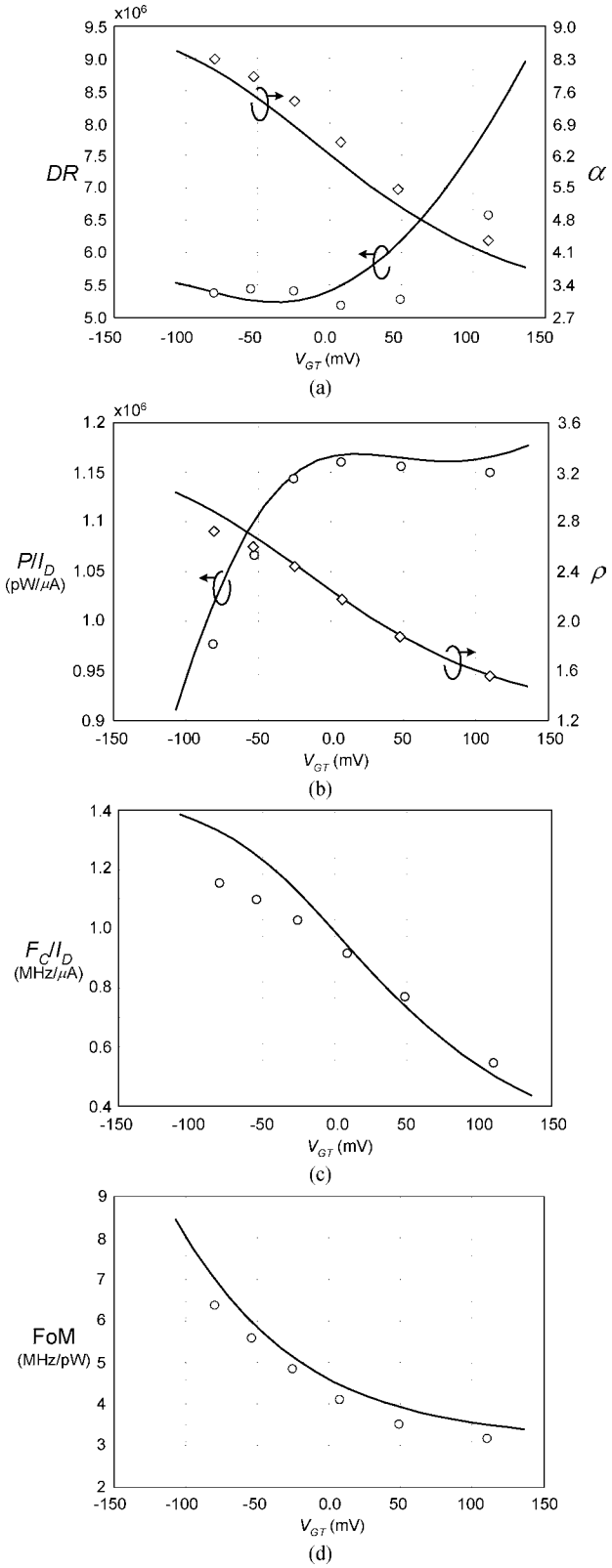

Fig. 8. (Markers) Simulated and (solid) theoretical plots of basic class AB SI performances in the 90-nm CMOS process.

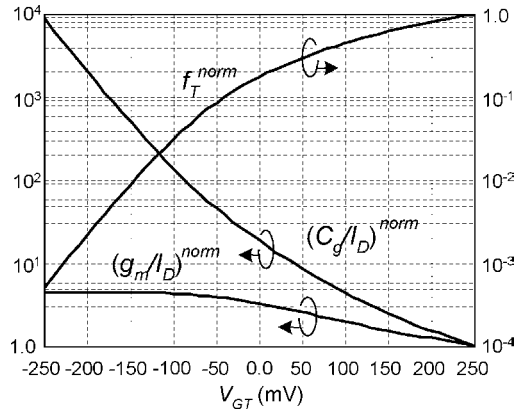

Fig. 9. Normalized g_m/I_D and C_g/I_D and f_T characteristics versus $V_{\rm GT}$.

A. Speed Limitation

It is generally known that the transition frequency f_T, which indicates the intrinsic maximum usable frequency in a MOS transistor at a given channel length L, is reduced with decreasing gate-overdrive voltage $V_{\rm GT}$. In particular, it has been shown in [16] that, at strong inversion, f_T is proportional to $V_{\rm GT}$. Eventually, at weak inversion, it becomes dependent on the drain current I_D which is now related to $V_{\rm GT}$ exponentially, making f_T fall faster with $V_{\rm GT}$ than with strong inversion operation.

To investigate how this impacts speed performance, we have plotted the transition frequency $f_T = g_m/2\pi C_G$ and the g_m/I_D and C_G/I_D ratios versus $V_{\rm GT}$ under a *constant* channel length L by using (1a)–(1c), and these are shown in Fig. 9. To facilitate the discussion, all the plots are normalized to their corresponding values in strong inversion operation with $V_{\rm GT} = 0.25$ V. From the normalized f_T characteristic in Fig. 9, when the transistor operation moves from the strong to weak inversion, with $V_{\rm GT} = -0.1$ V as an example, f_T drops by more than 30 times. As indicated from the normalized g_m/I_D and C_G/I_D plots, such a significant f_T degradation is mainly attributed to a sharp increase in C_G/I_D, because a small $V_{\rm GT}$ in a subthreshold MOS transistor requires a larger aspect ratio W/L for the same g_m and/or I_D when compared with strong inversion operation. At a constant channel length L, this results in a larger width W and, hence, a larger gate capacitance $C_G(\propto W \cdot L)$.

While the design for subthreshold operation has dramatically worsened the transistor's f_T, this does not imply a worsening of the SI memory's operating speed. This is because the memory capacitance C_G of a particular design, whether in strong or weak inversion, is chosen to meet a noise specification. Thus, a subthreshold design having the same speed as that of a strong inversion design can be achieved simply by choosing transistors with larger W and smaller L (but with the same area $W \cdot L$).

In SC, the situation is in absolute contrast. Unlike its SI counterpart, the gate capacitance C_G appears as a parasitic component. This creates nondominant poles which may give rise to underdamped settling and even circuit instability. As a result, the considerably larger C_G of a subthreshold MOS transistor adversely affects the SC speed performance.

B. Transmission Accuracy

In SI, the following are the three major nonidealities that affect the memory's transmission accuracy: signal-dependent settling, charge injection of the memory's switches, and finite output–input conductance ratio [1]. Since a class AB subthreshold SI must handle input current which is much larger

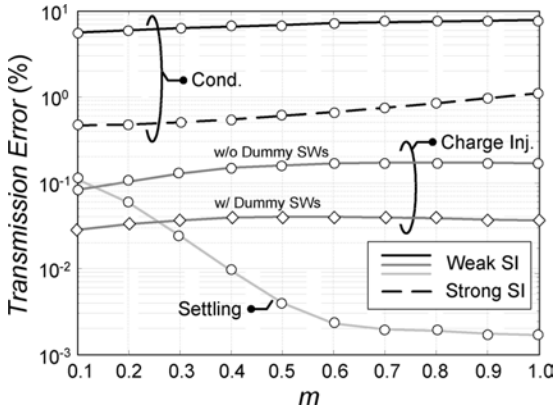

Fig. 10. Simulated error performances of basic class AB SI from individual error source under strong and weak operations.

than its quiescent bias current, the transconductance g_m of the composite memory is heavily signal dependent. This makes the memory's settling time considerably signal dependent. However, since larger input current gives a larger g_m and, hence, a faster settling time, proper design of the memory's settling at a small input automatically guarantees the required accuracy for the entire input range. As a result, the signal-dependent settling should not have a significant effect on the memory accuracy.

Due to inherently small signal voltage swings in subthreshold SI, the signal-dependent component from charge injection is also small. A more critical issue is the absolute charge of the memory switches, as this can give rise to signal-dependent error through the signal-dependent g_m of the composite memory. Nevertheless, this can be effectively reduced by the use of a balanced SI structure and the dummy switch technique [20].

As explained earlier, the small $V_{\rm GT}$ associated with subthreshold operation results in transistors with larger width W and smaller length L compared to their strong inversion counterpart. The transmission error resulting from finite output–input conductance ratio arises because of channel length modulation ($\propto 1/L$) and feedback to the gate capacitance C_G via the drain–gate overlap capacitance $C_{\rm DG}$ ($C_{\rm DG}/C_G \propto 1/L$). Therefore, output–input conductance ratio transmission errors are correspondingly higher in subthreshold operation and must be accommodated by the chosen circuit technique.

The contribution of each nonideal effect for each region of operation, including signal-dependent settling, charge injection, and finite conductance ratio, was examined via simulation of the individual transmission errors. To enable the study, certain components or parameters were made ideal in the memory under test so that only the nonideality under consideration became the major error source: To eliminate charge injection errors, ideal memory switches were employed; to suppress conductance errors, the memory was equipped with an ideal active feedback amplifier; and to minimize the signal-dependent settling, considerable extension of the sampling period was allowed.

The resulting individual memory transmission errors for the balanced weak inversion memory using 0.18-μm CMOS process data with $V_{\rm GT} = -0.10$ V are shown in Fig. 10. The errors are plotted versus the input current modulation index m, defined as the ratio of the signal current to its maximum value, $i_{\rm in}/\hat{i}_{\rm in}$. It is seen that the settling error is small and improves with larger m due to a higher g_m. The charge injection error is practically independent of the input signal level due to the balanced structure, and it is effectively reduced by using dummy switches. Contributing most to the memory's overall error is that resulting from the finite output–input conductance ratio. Compared with a similar strong inversion design ($V_{\rm GT} = +0.13$ V), the error is about ten times worse.

In summary, the basic class AB memory has higher transmission error when operated in weak inversion. To achieve good performance, these errors must be controlled by more sophisticated circuit techniques, and two such examples are described in the next section.

VI. Practical Designs

A. Cascode Design

To demonstrate the feasibility of the subthreshold SI technique in practice, we have designed and simulated a balanced weak inversion class AB SI memory in the 0.35-μm CMOS process. The design was based on the memory cell tested in Section IV-B at $V_{\rm DD} = 1.0$ V with the cascoded memory arrangement for accuracy enhancement [10]. For the test configuration, the memory cell was driven by a differential current source, and the load was formed by an identical diode-connected memory. The operating clock frequency was at 1 MHz, and the total quiescent drain current was $I_D = 2$ μA. The supply regulation scheme in [10] was also adopted to regulate the quiescent current, and this increased the operating supply voltage to $V_{\rm DD} = 1.25$ V to accommodate the additional voltage headroom. The designed transistor dimensions are as follows: For memory transistors, $(W/L)_p = 588$ μm/2.5 μm and $(W/L)_n = 384$ μm/4.0 μm, and for cascoded transistors, $(W/L)_{Cp} = 588$ μm/0.35 μm and $(W/L)_{Cn} = 384$ μm/0.35 μm.

The simulated accuracy performance of the weak inversion memory cell versus modulation index m is summarized in Table V(A) for extreme process and temperature conditions. The table indicates that a memory error of less than 0.8% can be achieved over the entire input range. Also, at $m = 1$, the simulated THD is less than -40 dB, even under extreme conditions. Table VI summarizes the practical performances. It should be noted that as compared to the simulated plots of Fig. 6(a)–(c), due to the balanced structure, F_C/I_D is reduced by half, whereas DR is increased by slightly less than twice (because of the additional noise from cascoded devices and switches). This yields the FoM of the balanced cascoded SI memory slightly less than the simulated plots at weak inversion of the basic class AB memory [Fig. 6(d)].

B. Two-Step Design

Due to insufficient voltage headroom, the cascoded memory enhancement becomes ineffective for the weak inversion SI in the 0.18-μm CMOS using low-voltage transistors. One of the existing techniques readily applicable at very low supply voltages is the class AB two-step sampling SI, S^2I[9]. Due to the use of a coarse and fine parallel memory configuration, some FoM degradation is expected in the weak inversion S^2I memory.

TABLE V
(A) TRANSMISSION PERFORMANCE OF WEAK INVERSION CASCODED CLASS AB SI. (B) TRANSMISSION PERFORMANCE OF WEAK INVERSION CLASS AB S^2I

Modulation Index (m)	Transmission Error (%)		
	Slow 100°C	Typical 40 °C	Fast 0°C
0.2	0.14	0.15	0.25
0.4	0.15	0.11	0.28
0.6	0.18	0.15	0.25
0.8	0.19	0.19	0.54
1.0	0.35	0.25	0.78

Modulation Index (m)	Transmission Error (%)		
	Slow 100°C	Typical 40 °C	Fast 0°C
0.2	0.20	0.08	0.17
0.4	0.31	0.15	0.27
0.6	0.51	0.33	0.50
0.8	0.77	0.55	0.78
1.0	0.98	0.78	0.96

TABLE VI
TYPICAL PERFORMANCE SUMMARY OF PRACTICAL BALANCED SI MEMORIES.

Memory design	0.35μ Cascoded SI	0.18μ S^2I
pMOS memory size	588μ/2.5μ	304μ/3.0μ
nMOS memory size	384μ/4.0μ	208μ/6.0μ
Analog voltage	1.0V	0.35V
Total quiescent drain current	2μA	4μA
F_C	1MHz	1MHz
P	5.8μW	2.6μW
DR	1.24x10^7	0.66x10^7
FoM*	2.14MHz/pW	2.54MHz/pW
Transmission Error** (@ m =1)	0.78%	0.96%
THD** (@ m =1)	-40.9dB	-38.6dB
Supply voltage	1.25V	0.6V

* Calculated from analog voltages
** Worst case performances under fast processes and 0°C

Since the settling of input signal is continued from coarse to fine phases, the S^2I memory exhibits identical speed to its basic counterpart. In terms of power, as the fine memory only needs to handle the small residue input current left from the coarse phase, additional dynamic current close to the memory quiescent bias is required. Due to a high average drain current over the quiescent bias ($\rho \sim 3.37$) in the weak inversion memory cell, this only slightly increases the total power consumption. For the noise performance, the inclusion of the fine memory doubles the total noise power compared to that of the basic cell. By taking these considerations into the general FoM expression of the basic class AB SI in (5), the FoM of class AB S^2I in weak inversion operation can be given as

$$\mathrm{FoM}_{\mathrm{S^2I}}^{\mathrm{weak}} = \frac{2.8}{NkT_j} \cdot \frac{\phi_t}{V_{\mathrm{DD}}}. \tag{10}$$

Comparing this with the FoM of the basic weak inversion SI in Table I, overall performance degradation by about a factor of 2.6 is expected from the use of the S^2I technique. For the 0.18-μm process employed in Section V-B, this makes the FoM performance of the S^2I memory slightly less than its basic counterpart in strong inversion. Although the enhancement technique seems to undo the FoM benefit of the weak inversion SI, such a drawback should be outweighed by the ability to operate at a very low supply voltage with good accuracy.

The balanced class AB weak inversion S^2I memory using low-voltage transistors in the 1.8-V 0.18-μm process was designed at $F_C = 1$ MHz where the transistor dimensions for both coarse and fine memories are given at $(W/L)_p = 304\ \mu\mathrm{m}/3.0\ \mu\mathrm{m}$ and $(W/L)_n = 208\ \mu\mathrm{m}/6.0\ \mu\mathrm{m}$. The supply voltage was 0.35 V, and the total quiescent bias current was 4 μA. With the regulation circuitry, the supply was increased to 0.6 V. As summarized in Table V(B), simulation indicates an accuracy of better than 1.0% under extreme processing and temperature. Also, from the performance summary in Table VI, the simulated THD at $m = 1$ is -38.6 dB, and the THD at $m = 0.86$ is -40 dB. It should be noted that the simulated FoM of the balanced S^2I memory is about 20% less than the simulated FoM of the basic memory at strong inversion operation, as shown in Fig. 7(d).

VII. CONCLUSION

The behavior of the basic class AB SI memory with transistors operating in their subthreshold region has been studied through the theoretical assessment of its overall performance using the general MOS equations valid for all regions of operation. Thanks to its ability to handle larger input signal current levels, basic subthreshold SI operation has better performance with lower supply voltage than its strong inversion counterpart, and this performance improves with the reducing threshold voltages which come with successive CMOS generations.

The theoretical performance analysis used an FoM which embraced DR, speed, and power consumption, and the results were extensively verified by both experiment and simulation using actual CMOS process data. It was found that while the theory was a little optimistic, it demonstrated similar behavior and confirmed that subthreshold operation gives worthwhile performance gains.

However, it was also found that the subthreshold design produced transistors with a large aspect ratio. This gave the basic class AB memory poor accuracy because the high output conductance produced large transmission errors. Enhanced circuit design was needed to overcome this shortcoming of the basic memory.

The following two enhanced circuit styles were investigated: cascoding using a 0.35-μm CMOS process, and two-step sampling using a 0.18 μm CMOS process. These designs were successful in restoring the accuracy but at some further cost to performance. Nevertheless, these designs demonstrated in a practical way that subthreshold SI can produce much lower voltage operation without loss of performance when compared with the strong inversion design. While the achievement of accurate low-voltage operation and the realization of the full promise of performance improvement remain a challenging research goal, this paper has nevertheless demonstrated that subthreshold SI is a viable analog technique for the implementation of very low voltage CMOS circuits and systems, such as emerging implantable biomedical electronic devices.

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PAPER

Analysis and Design of Sub-Threshold R-MOSFET Tunable Resistor

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SUMMARY The sub-threshold R-MOSFET resistor structure which enables tuning range extension below the threshold voltage in the MOSFET with moderate to weak inversion operation is analyzed in detail. The principal operation of the sub-threshold resistor is briefly described. The analysis of its characteristic based on approximations of a general MOS equation valid for all regions is given along with discussion on design implication and consideration. Experiments and simulations are provided to validate the theoretical analysis and design, and to verify the feasibility at a supply voltage as low as 0.5 V using a low-threshold devices in a 1.8-V 0.18 μm CMOS process.

key words: *MOSFET resistor, R-MOSFET resistor, sub-threshold techniques, low voltage techniques*

1. Introduction

With the continued reduction of supply voltages due to aggressive downsizing of transistors in modern CMOS processes, the design of analog circuits that co-integrate with digital circuits on the same chip with sufficient performance promises to be increasingly challenging. For analog filtering applications, continuous-time (CT) MOSFET-C and linearity enhanced R-MOSFET-C techniques that employ no switches as well as no anti-aliasing and smoothing filters have been demonstrated as attractive alternatives to sampled-data switched-capacitor (SC) filters at low voltages [1]–[4]. One major issue however for the low-voltage CT filters is the limited range of the gate voltage available for tuning the corner frequency through the MOSFET resistance so as to cope with inevitable process and temperature variations. Although this may be circumvented either by using native transistors, low threshold transistors or thick oxide transistors, a control voltage larger than the supply is often necessary, thereby necessitating a clock boosting circuitry which invariably poses reliability concerns on the devices. Another means is to employ the variable MOS capacitors [1], but a switched array of parallel *linear* capacitors for coarse tuning must be included to achieve a good linearity and adequate overall tuning range.

Recently, an enhanced structure that can extend the usability of the R-MOSFET approach by enabling MOSFET operation in moderate to weak (or sub-threshold) inversion, without significant impairment on linearity, was introduced [5]. The so-called sub-threshold R-MOSFET structure essentially relies upon a *cancellation* of the nonlinearity which can be *strongly* nonlinear such as that exhibited by a saturated sub-threshold MOSFET. This is in stark contrast to the existing R-MOSFET configurations that rely upon series and/or parallel linear resistor(s) to *suppress* the non-linearity and thus become ineffective at sub-threshold MOSFET operation. For the sub-threshold resistor to exhibit optimum linearity and tuning capability, it requires an appropriate design and this is the subject of this paper. In Sect. 2, the principal operation and detailed analysis, which leads to a perfect linearization in the sub-threshold resistor, are outlined. Also discussed in this section is a possible design guideline for good linearity performance over the required tuning range. Section 3 provides extensive analysis and design verification through experiments and simulations. This is followed by conclusions in Sect. 4.

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2. Sub-Threshold R-MOSFET Analysis

2.1 Principal Operation

Figure 1 shows the sub-threshold R-MOSFET resistor where it consists of the linear resistors $R_1 - R_2$ and the MOS transistors $M_1 - M_2$. When compared to the simple series-parallel R-MOSFET resistor which comprises R_1, R_2 and M_1, the sub-threshold resistor of Fig. 1 employs the additional transistor pair, M_2. From another point of view, when compared to the dump configuration of the R-MOSFET resistor in [3] which comprises R_2, M_1 and M_2, the

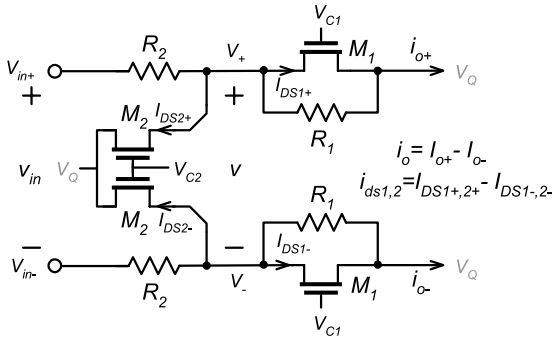

Fig. 1 Sub-threshold R-MOSFET tunable resistor structure.

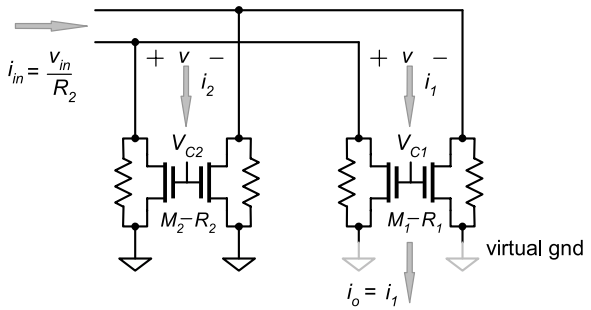

Fig. 2 Norton's equivalent circuit of sub-threshold R-MOSFET resistor.

sub-threshold resistor employs the additional resistor pair, R_1. Thus, the major differences lie in the fact that the sub-threshold resistor makes simultaneous use of both R_1 and M_2 and this offers linearity improvement, especially when the MOS transistors operate in the sub-threshold region.

An insight into its underlying principle can be gained by transforming the differential input voltage v_{in} and the series R_2 into its Norton's equivalent. The resultant circuit, after rearrangement for the sake of description, is as shown in Fig. 2, with all the voltage/current variables indicated being differential. The transformed circuit is essentially a parallel of two *nonlinear* resistance branches, each comprising a pair of linear resistors and MOSFETs. In operation, the equivalent input current $i_{in} = v_{in}/R_2$ is divided into two paths — one through the parallel combination of R_1 and M_1 to produce the output current $i_o = i_1$ with a nonlinear current-voltage relation $i_1 = G_1(v)$; the other through R_2 and M_2 to produce the current i_2 with a nonlinear relation, $i_2 = G_2(v)$, where v is the common differential voltage across the two branches. Note that the linear terms of $G_1(v)$ and $G_2(v)$ are mainly contributed by the linear resistors, while the nonlinear terms are mainly contributed by the MOSFETs. Thus, to achieve a perfectly linear relationship between $i_o = i_1$ and i_{in}, hence between i_o and v_{in}, it demands that the current division be linear. This can be accomplished when the two nonlinear branches are *linearly dependent*, i.e., $G_1(v) = \delta \cdot G_2(v)$ where δ is a constant, *regardless* of the nonlinear characteristic. It should be noted that such a linearization condition emphasizes the critical role of including both R_1 and M_2 in the sub-threshold resistor structure.

One important consideration now is the fact that, under a low supply voltage and a large signal swing, the MOSFET operation in the sub-threshold resistor can span not only from strong to moderate and weak inversion, but also from non-saturation to saturation. Thus, it is of prime importance to conduct detailed analysis that could lead to design guidelines so as to ensure good linearity over the resistance tuning range.

2.2 Sub-Threshold R-MOSFET Analysis

Due to such a wide coverage of the MOSFET's operation, it is necessary to employ a general current-voltage MOS equation valid for all regions. This can be given by [6]

$$I_{DS} = 2m\varphi_t^2\mu C_{ox}\frac{W}{L}\left(\ln^2\left[1+e^{\frac{V_{GB}-V_{T0}-mV_{SB}}{2m\varphi_t}}\right] - \ln^2\left[1+e^{\frac{V_{GB}-V_{T0}-mV_{DB}}{2m\varphi_t}}\right]\right) \quad (1a)$$

with

$$m = \left(1-\gamma/2\sqrt{V_{GB}-V_{T0}+(\gamma/2+\sqrt{\varphi_0})^2}\right)^{-1} \quad (1b)$$

where $\phi_t = kT/q$ is the thermal voltage, μ is the carrier effective mobility in the channel, C_{ox} is the gate-oxide per unit area, W and L are the channel width and length, V_{T0} is the threshold voltage at $V_{SB} = 0$, γ is the body effect coefficient and ϕ_0 is a characteristic potential [6]. It is noted that the short-channel effects and the dependence of the mobility on the transversal field are not included in (1).

Consider the sub-threshold R-MOSFET resistor in Fig. 1. It is assumed that the input and output quiescent voltages are set at V_Q, the body voltage of all the MOSFETs at $V_B = 0$, the gate bias at V_{C1} for M_1, and at V_{C2} for M_2. For a balanced differential input, $\pm v_{in}/2$, Eq. (2) at the bottom of the page is obtained by applying KCL at the intermediate nodes with the voltages V_+ and V_- in Fig. 1, and taking their difference. In (2), $I_{Z1,2} = 2m\phi_t^2\mu C_{ox}W_{1,2}/L_{1,2}$, and i_{ds1} and i_{ds2} are the differential drain/source currents of the MOSFET pairs, M_1 and M_2, respectively. $i_o = i_{o+} - i_{o-}$ denotes the differential output current. To obtain manageable results that enable insight into the circuit operation, and also help offer a design implication, the following approximations are applied to (2). Due to the presence of the *linear* resistors R_1 and R_2, it is possible to assume that V_+ and V_- are also balanced similar to the input v_{in}, i.e., $V_+ = V_Q + v/2$ and $V_- = V_Q - v/2$, and hence the definition of the differential voltage v is $v = V_+ - V_-$. To help simplify the analysis, each variable in (2) is normalized by the following definitions: $x = v_{in}/2m\phi_t$, $z = v/2m\phi_t$, $a_{1,2} = (V_{C1,2} - V_{T0} - mV_Q)/2m\phi_t$, and $g_{1,2} = 2m\phi_t/I_{Z1}R_{1,2}$. Thus, it follows that (2) can be rewritten as

$$g_2(x-z) = \underbrace{\left(\ln^2\left[1+e^{a_1+mz/2}\right]-\ln^2\left[1+e^{a_1-mz/2}\right]\right)+g_1 z}_{y} + r\left(\ln^2\left[1+e^{a_2+mz/2}\right]-\ln^2\left[1+e^{a_2-mz/2}\right]\right) \quad (3)$$

with $r = I_{Z2}/I_{Z1}$ and $y = i_o/I_{Z1}$. With the use of Taylor series representation similar to [7] (for analysis of non-saturated strong inversion MOSFET resistors), the normalized differential current-voltage relation of the MOSFET pairs in (3) which involve a difference of square logarithmic operation can be expressed in a polynomial form with no even-order terms due to the balanced structure. Such an expansion with respect to z yields

$$\ln^2\left[1+e^{a+mz/2}\right]-\ln^2\left[1+e^{a-mz/2}\right] \approx c_1^n z + c_3^n z^3 + c_5^n z^5 \quad (4a)$$

with

$$\frac{v_{in}-(V_+-V_-)}{R_2}=\underbrace{\overbrace{I_{Z1}\left(\ln^2\left[1+e^{\frac{V_{C1}-V_{T0}-mV_-}{2m\varphi_t}}\right]-\ln^2\left[1+e^{\frac{V_{C1}-V_{T0}-mV_+}{2m\varphi_t}}\right]\right)}^{i_{ds1}}+\frac{(V_+-V_-)}{R_1}}_{i_o}+\overbrace{I_{Z2}\left(\ln^2\left[1+e^{\frac{V_{C2}-V_{T0}-mV_-}{2m\varphi_t}}\right]-\ln^2\left[1+e^{\frac{V_{C2}-V_{T0}-mV_+}{2m\varphi_t}}\right]\right)}^{i_{ds2}} \quad (2)$$

$$c_1^n=\frac{2me^a}{1+e^a}\ln(1+e^a) \quad (4b)$$

$$c_3^n=\frac{m^3e^a}{12(1-e^a)^3}\left(3e^a+\ln(1+e^a)-e^a\ln(1+e^a)\right) \quad (4c)$$

$$c_5^n=\frac{m^5e^{2a}}{960(1+e^a)^5}\cdot\left[5\left(3-e^a\left(6-e^a\right)\right)+2\left(1-e^a\right)\left(\cosh(a)-5\right)\ln(1+e^a)\right] \quad (4d)$$

where c_1^n, c_2^n and c_5^n (with the superscript "n") are the *normalized* Taylor's coefficients. Note from (4b) that the first-order coefficient is reduced to $c_1^n = 2a$ for $a \gg 0$ (strong inversion MOSFETs) and, after de-normalization, this yields the usual small-signal characteristic of a non-saturated MOSFET resistor [6]. To further simplify the analysis, the difference of square logarithmic operation is approximated by a third-order polynomial, i.e., the fifth-order coefficient c_5^n in (4d) is omitted. The validity of this simplification will be discussed soon. Following this, by substituting the third-order Taylor's series in (4) into (3), after some rearrangement, we obtain

$$g_2x=\underbrace{(g_1+c_{11}^n)z+c_{31}^nz^3}_{y}+\underbrace{\left(g_2+rc_{12}^n\right)z+rc_{32}^nz^3}_{h} \quad (5)$$

where $c_{11,31}^n$ are the normalized coefficients for the MOSFET pair M_1 and $c_{12,32}^n$ are those for M_2. It is observed from (5) that, for a linear characteristic between x and y, h must be linearly dependent on y, i.e., $h = \delta y$ where δ is a constant. It is interesting to note that, with reference to the Norton's equivalent circuit of Fig. 2, the variable y corresponds to the normalized current $i_o/I_{Z1} = i_1/I_{Z1}$ in the M_1-R_1 branch, and h corresponds to the normalized current i_2/I_{Z1} in the M_2-R_2 branch. By using (5), the linear dependence condition implies the following relation:

$$\frac{g_2+rc_{12}^n}{g_1+c_{11}^n}=r\cdot\frac{c_{32}^n}{c_{31}^n}=\delta. \quad (6)$$

Using (5) and (6), we obtain $y = g_2(1+\delta)^{-1}x$. After denormalizing the associated variables, the differential characteristic of the sub-threshold R-MOSFET resistor is thus given by

$$i_o=R_{eff}^{-1}v_{in}=\left[(1+\delta)R_2\right]^{-1}v_{in}. \quad (7)$$

For ease of implementation and characterization, the transistor pairs M_1 and M_2 should be integer multiples of the same unit MOSFET. By assigning the number of unit transistors at n_1 for M_1 and at n_2 for M_2, the parameter relation for a perfect linearization can be obtained by de-normalizing (6), and this yields

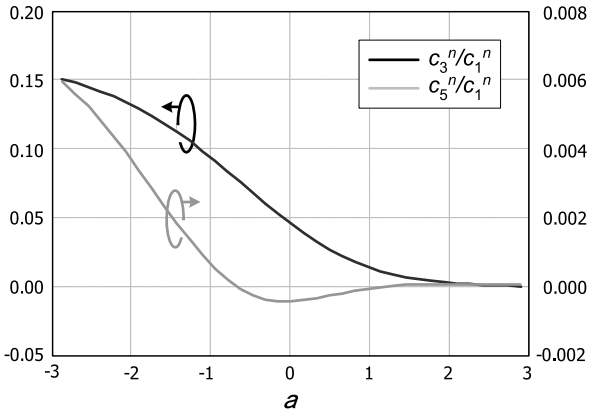

Fig. 3 Normalized Taylor's coefficients ratios c_3^n/c_1^n and c_5^n/c_1^n of MOSFET pair's normalized I-V characteristics.

$$\frac{R_2^{-1}+n_2\cdot c_1(V_{C2})}{R_1^{-1}+n_1\cdot c_1(V_{C1})}=\frac{n_2\cdot c_3(V_{C2})}{n_1\cdot c_3(V_{C1})}=\delta \quad (8)$$

where $c_{1,3}(V_C)$'s are the *normal* coefficients of the third-order polynomial describing the differential current-voltage characteristic of the unit MOSFET pair at the gate control voltage V_C. Note that these may be obtained by de-normalizing (4b) and (4c).

From the analysis outlined above, Eqs. (7), (8) are central to the analysis and design of the sub-threshold R-MOSFET resistor. Inspection of (8) also reveals that scaling of the effective resistance from R_{eff} to $k \cdot R_{eff}$ can be simply obtained, without upsetting the linearization condition, by modifying R_1, R_2 by the factor k and n_1, n_2 by the inverse $1/k$.

It is important to point out that the third-order polynomial approximation applied in the forgoing analysis is valid for MOSFET operation in strong to moderate inversion. This is evident as shown in Fig. 3 which provides the plots versus a of the ratios of the third-order and the fifth-order to the first-order normalized coefficients, c_3^n/c_1^n and c_5^n/c_1^n, using (4). At weak inversion operation (approximately at $a < -1$ or $(V_{C1} - V_{T0} - mV_Q) < -2m\phi_t$), the characteristic of the MOSFET pair becomes increasingly nonlinear and it can be seen from the ratio plots that the fifth-order term can no longer be omitted. Nevertheless, as will be evident in the experiments and simulations of Sect. 3, if the coefficients $c_{1,3}(V_C)$ in (8) are to be determined *empirically* from the unit MOSFET characteristic at various V_Cs, instead of being calculated from (4b), (4c), it is possible to fit the characteristics with the third-order polynomial while still obtaining a reasonable accuracy. In this way, the use of the developed equations in (8) can be extended down to weak

MOSFET operation. In fact, such empirical coefficient determination is valid for more general conditions [7]. That is, with proper fitting values of c_1 and c_3, all the second-order effects omitted in (1) are automatically incorporated. Since this approach is simple and yet provides good accuracy in practice, it will be employed in Sect. 3.

2.3 Design Discussion

For an ideal operation of the sub-threshold R-MOSFET resistor, when the main control voltage V_{C1} of M_1 is changed, the auxiliary control voltage V_{C2} of M_2 should be adjusted accordingly in order to maintain good linearity over the entire resistance tuning range. For ease of implementation however, it should be more convenient to maintain V_{C2} at a constant voltage. In such a case, the condition for a perfect non-linearity cancellation is satisfied at a *single* set of V_{C1} and V_{C2} through proper selection of R_1, R_2 and the dimensions of M_1 and M_2 according to (8). Only a partial cancellation is obtained at other set of control voltages. As will be demonstrated by both experiments and simulations, the constant V_{C2} scheme proves to be effective for moderate linearity applications, provided that particular attention is paid to satisfying the linearization condition at a set of V_{C1} and V_{C2} within the sub-threshold operation of the MOSFETs where the nonlinearity is most pronounced. With such a design consideration, adequate resistance tunability with good linearity over the entire range can be ensured.

3. Performance Verification

3.1 Experimental Results

The integrity of the analysis and design, and the functionality of the sub-threshold R-MOSFET resistor, were first verified via breadboard implementation using the n-channel MOSFET of an ALD1106 transistor array as the unit transistor. To facilitate the test, the R-MOSFET resistor was built around off-the-shelf opamps with negative feedback using linear resistors to form a differential inverting amplifier where the differential output current i_o in Fig. 1 can be measured indirectly via the amplifier's output voltage. For this breadboard design, the terminal input/output quiescent voltages were chosen at $V_Q = 0.5$ V. Measurement indicates the extrapolated nominal threshold voltage of the MOSFET at $V_{T0} \approx 0.65$ V and this is increased to $V_{TB} \approx 0.88$ V for $V_D = V_S = V_Q = 0.5$ V and $V_B = 0$. Therefore, the gate control voltage V_C below $V_Q + V_{TB} \approx 1.38$ V covers the sub-threshold operation. For the selected V_C range from 1.25 V to 1.50 V, the measured differential characteristic of the ALD1106 nMOS pair at $V_Q = 0.5$ V are depicted in Fig. 4. Also given are the calculated plots based on the extracted polynomial coefficients c_1s and c_3s (using MATLAB) in Table 1 for each corresponding V_C where close agreement with measurement is observed.

For ease of tuning, the scheme with a fixed gate voltage for V_{C2} was adopted. In this design example, the numbers

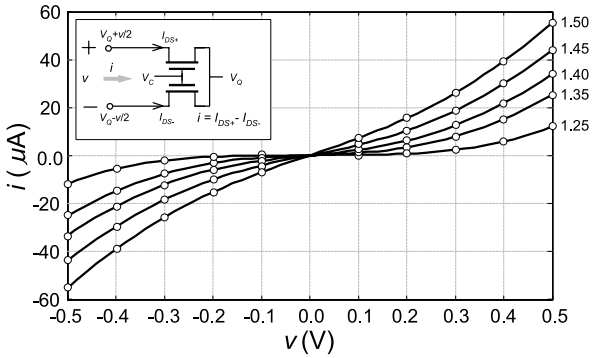

Fig. 4 Measured (solid) and calculated (marker) differential characteristics of ALD1106 unit MOSFET pair at different V_Cs.

Table 1 Empirical coefficients for ALD array MOSFET pair.

V_C	1.25	1.30	1.35	1.40	1.45	1.50
c_1/c_3 ($\cdot 10^{-4}$)	0.022 /1.35	0.098 /1.79	0.238 /1.89	0.454 /1.77	0.717 /1.62	1.033 /1.46

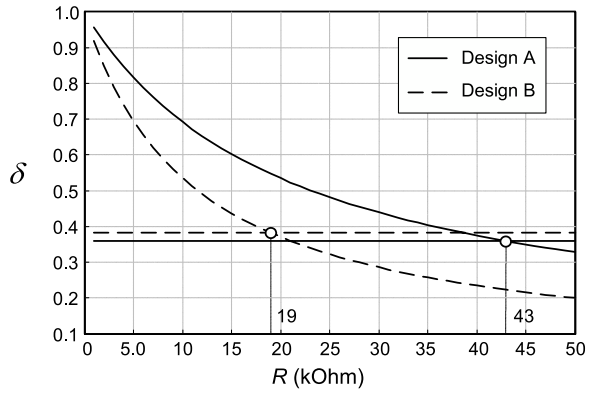

Fig. 5 Design curves for sub-threshold resistor using ALD1106.

of the unit transistors at $n_1 = 2$ and $n_2 = 1$ and an identical resistance $R_1 = R_2 = R$ were selected. To determine the linearization conditions, the ratios on the left- and right-hand sides of (8) are plotted against the resistance R, where the intersection between the two curves indicates the designed resistance value. Based on the extracted coefficients in Table 1, the plots for two example designs for linearization at different V_Cs are shown in Fig. 5. For design A with the linearization at $V_{C1} = 1.35$ V and $V_{C2} = 1.25$ V, the intersection yields $R = 43$ kΩ. For design B with the linearization at $V_{C1} = 1.40$ V and $V_{C2} = 1.25$ V, we obtain $R = 19$ kΩ. In the test, available resistor values were used, i.e., $R = 50$ kΩ for design A, and $R = 20$ kΩ for design B. It should be noted that the selected $V_{C2} = 1.25$ V for both designs results in the operation of M_2 at ∼130 mV less than the threshold voltage.

Figure 6 shows the measured resistance characteristics, which were extracted from the measured small-signal voltage gain versus V_{C1} at an input v_{in} of 0.1 V_p (differential peak voltage). Also given for comparison are the calculated resistances using (7) based on the coefficients in Table 1. It is seen that R_{eff} can be tuned from 55 kΩ to 97 kΩ, yield-

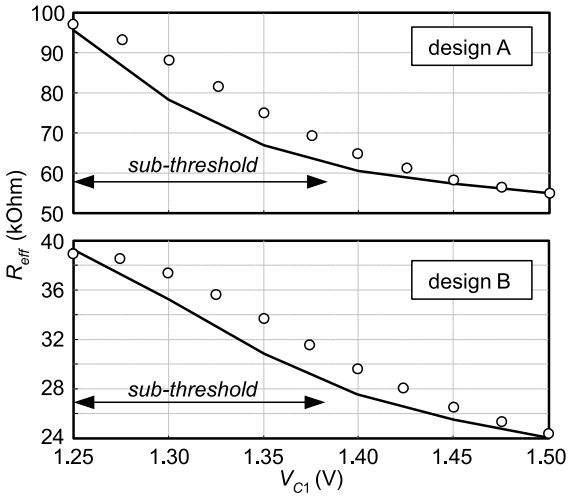

Fig. 6 Measured (marker) and calculated (solid) small-signal resistance versus V_{C1}.

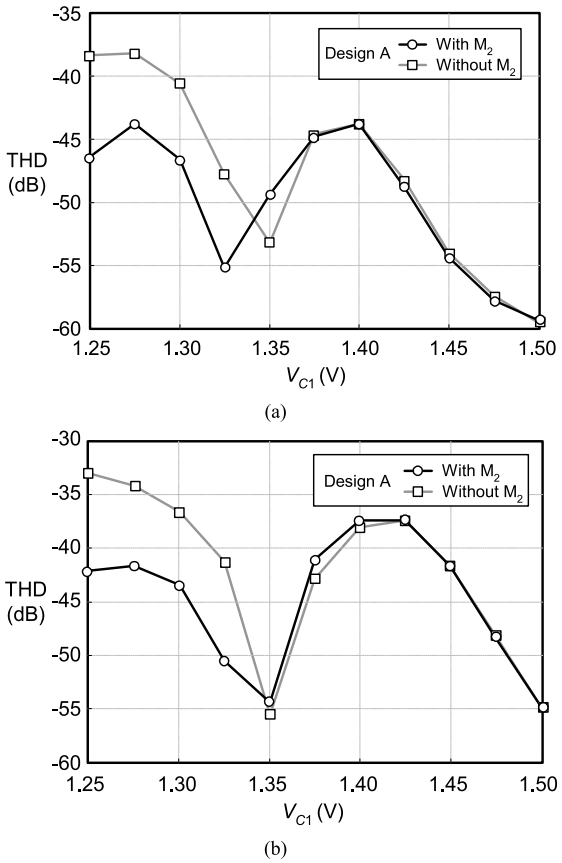

Fig. 7 Measured THD performances at 10 kHz input frequency of design A at (a) 0.4 V_p input and (b) 0.8 V_p input.

ing the tuning ratio at ~1.76 for design A. For design B, R_{eff} can be tuned from 24.5 kΩ to 38 kΩ, giving the tuning ratio at ~1.55. Also, based on the measured values, the sub-threshold operation in the MOSFETs covers the resistance tuning range by more than 50% for both designs A and B.

Figures 7 and 8 show the measured total harmonic distortion (THD) of the output voltage v_o versus V_{C1}, at v_{in} = 0.4 V_p and 0.8 V_p (differential peak voltage). For design A, the plots indicate the dips in the THD of the sub-threshold resistor at the intermediate control voltage V_{C1} = 1.325 V at 0.4 V_p, and at V_{C1} = 1.35 V for the test inputs at 0.8 V_p. For design B, the dips occur at V_{C1} = 1.375 V for both of the test inputs. These voltage locations are in close agreement with the design specifications, i.e., at V_{C1} = 1.35 V for design A, and at V_{C1} = 1.40 V for design B. Some discrepancies are mainly due to the approximation of the MOSFET characteristics by the third-order polynomial.

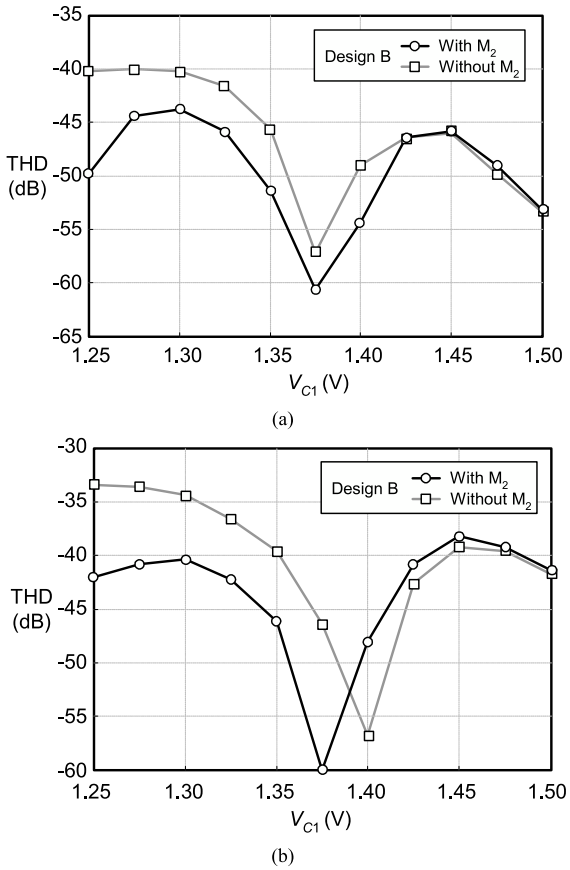

Fig. 8 Measured THD performances at 10 kHz input frequency of design B at (a) 0.4 V_p input and (b) 0.8 V_p input.

Also included for comparison in Figs. 7 and 8 are the THD plots when the transistor pair M_2 in Fig. 1 was removed and the circuit was turned into the conventional series-parallel R-MOSFET resistor. As observed, the proposed sub-threshold resistors can provide THD improvement, particularly over the V_{C1} range where M_1 operates in sub-threshold inversion. For the range of V_{C1} where M_1 is in strong operation, almost identical linearity is displayed between the two resistors as the effect of M_2 becomes negligible.

3.2 Simulation Results

The performance of the sub-threshold R-MOSFET resistor

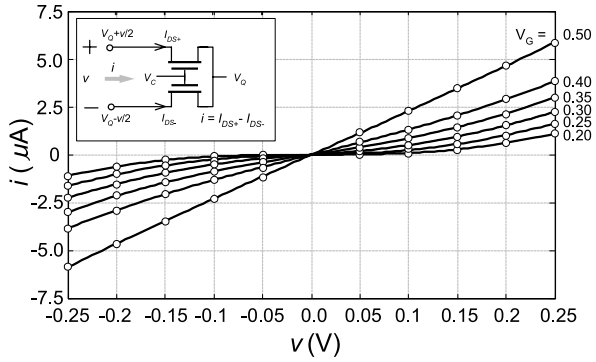

Fig. 9 Simulated (solid) and calculated (marker) differential characteristics of the low-threshold unit MOSFET pair at different V_Cs.

Table 2 Empirical coefficients for low threshold MOSFET pair.

V_C	0.2	0.25	0.3	0.35	0.4	0.50
c_1/c_3	0.003	0.019	0.045	0.082	0.127	0.228
$(\cdot 10^{-4})$	/0.677	/0.785	/0.766	/0.629	/0.427	/0.108

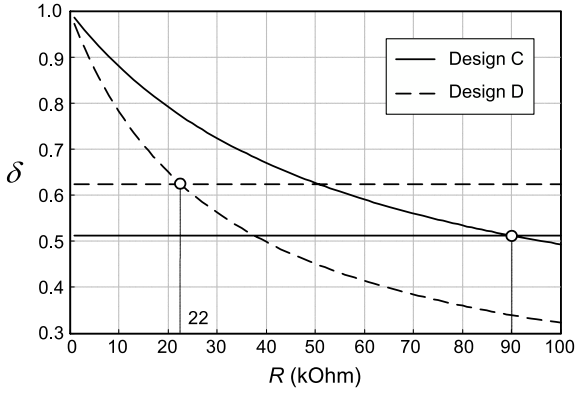

Fig. 10 Design curves for sub-threshold resistor using 0.18 μm CMOS.

in IC implementation was also demonstrated via simulation using the *low-threshold* n-channel MOSFET of the UMC 1.8-V 0.18 μm CMOS process with the gate tuning voltage below the supply at 0.5 V. Unlike the transistor array implementation, the output current $i_o = i_{o+} - i_{o-}$ in Fig. 1 was measured directly in simulation. For this example application at a 0.5-V supply, the quiescent voltage V_Q was set at a half-supply level, $V_Q = 0.25$ V. The unit transistor was selected at $W/L = 1.1\,\mu$m/4.0 μm. As extrapolated from simulation, the threshold voltage of the MOSFET is $V_{TB} \approx 0.05$ V at $V_D = V_S = V_Q = 0.25$ V and $V_B = 0$ V whereas the nominal value is $V_{T0} \approx 0.01$ V. Thus, the transistor enters sub-threshold operation at V_C below $V_Q + V_{TB} \approx 0.30$ V. The simulated and calculated differential characteristics of the unit MOSFET pair at various V_Cs are shown in Fig. 9, and the extracted polynomial coefficients that fit the curves are given in Table 2.

Similar to the breadboard design, the fixed gate voltage scheme for V_{C2} was employed and $R_1 = R_2 = R$ was selected. In design C, the numbers of the unit transistors were given at $n_1 = 4$ and $n_2 = 2$ and the perfect linearization condition was set at $V_{C1} = 0.30$ V and $V_{C2} = 0.25$ V. By using (8) and the extracted coefficients in Table 2, Fig. 10 shows the design curves [cf. Fig. 5 for designs A-B] where $R = 90\,\mathrm{k}\Omega$ is obtained for design C. For design D, another linearization condition at $V_{C1} = 0.35$ V and $V_{C2} = 0.25$ V, was selected and this yields $R = 22\,\mathrm{k}\Omega$. Note that for both designs, the control voltage $V_{C2} = 0.25$ V results in the operation of M_2 at ~50 mV less than the threshold voltage.

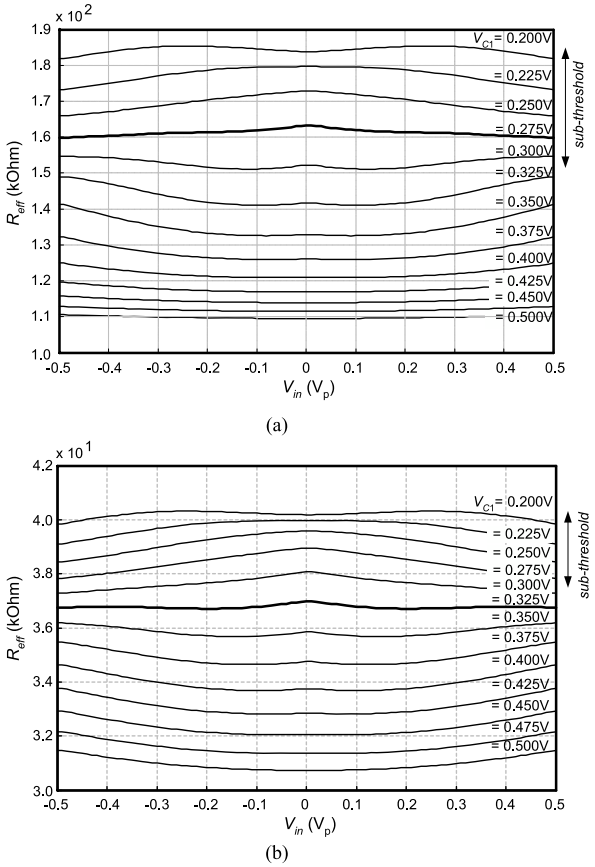

Fig. 11 Simulated resistance characteristics at different V_Cs for (a) Design C and (b) Design D.

Figures 11(a), (b) show the simulated resistance characteristic under typical process and temperature for designs C and D with V_{C1} ranging from 0.2 V to 0.5 V and the differential peak input v_{in} between $-0.5\,\mathrm{V_p}$ and $0.5\,\mathrm{V_p}$. It is noticed that the simulated characteristics are close to straight lines at V_{C1}= 0.275 V for design C and V_{C1} = 0.325 V for design D in close agreement with the specifications. For design C, R_{eff} can be tuned from 110 kΩ to 184 kΩ with the tuning ratio at ~1.67, and from 30.8 kΩ to 40.6 kΩ with the tuning ratio at ~1.32 for design D. Also note from the plots that the sub-threshold operation in the MOSFETs occupies about 40% of the resistance tuning range for design C, and about 30% for design D.

Figure 12 shows the simulated THD performances versus V_{C1} at $v_{in} = 0.5\,\mathrm{V_p}$. Compatible with the resistance plots of Fig. 11, the distortions of the sub-threshold resistors under typical process and temperature exhibit interme-

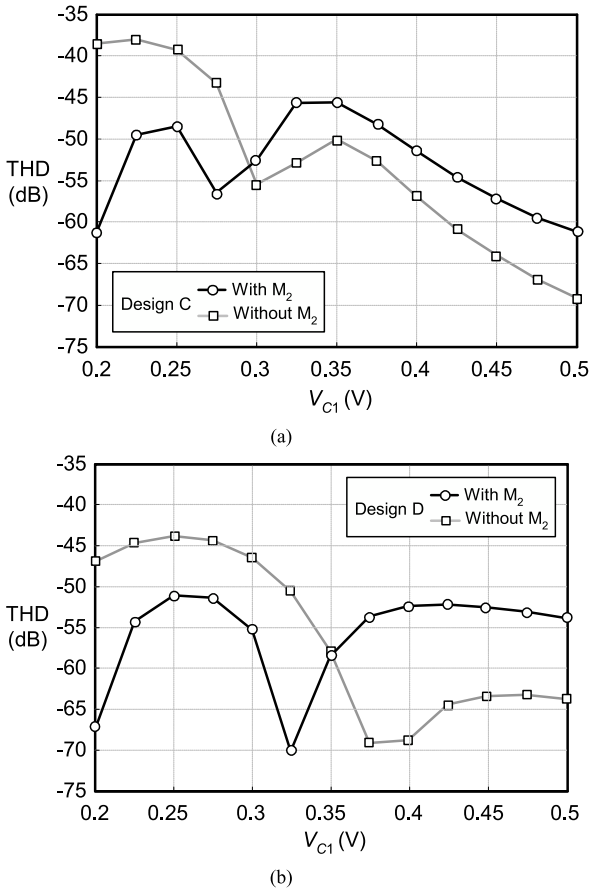

Fig. 12 Distortion performances of sub-threshold and series-parallel resistors at typical conditions and 10 kHz input for (a) Design C and (b) Design D.

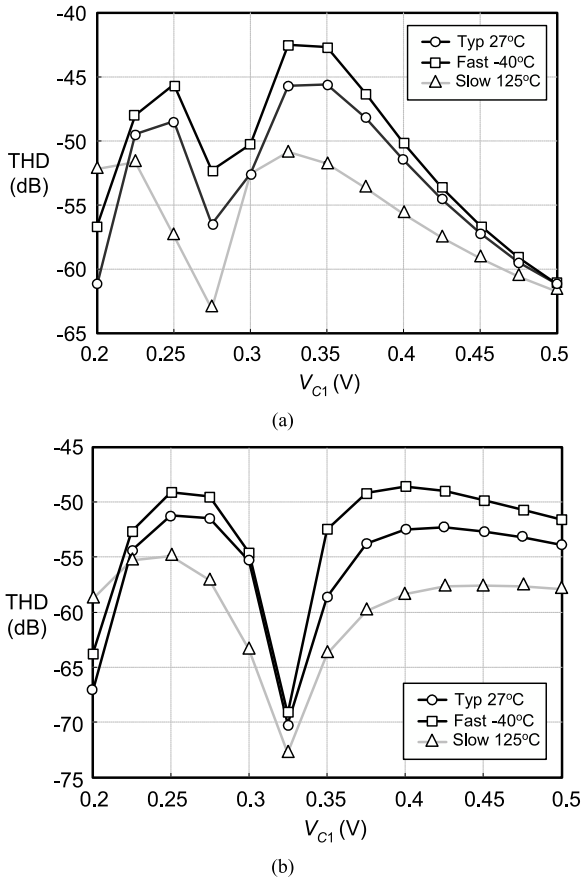

Fig. 13 Distortion performances at extreme conditions (a) Design C and (b) Design D.

diate dips at V_{C1} = 0.275 V for design C, and at V_{C1} = 0.325 V for design D. Also included in the figure are the THD plots of the corresponding series-parallel R-MOSFET resistors. Similar to the measured results of Figs. 7 and 8, improvement in the THD for the range of V_{C1} which yields sub-threshold operation in M_1 is clearly observed. Unlike the measured results however, the series-parallel counterparts exhibit somewhat less distortion at strong operation in M_1. This is due to the fact that, for designs C and D, M_2 was selected to operate at ~50 mV below the threshold voltage, as compared to ~130 mV for the case of designs A and B. This results in over-compensation of the nonlinearity in M_1 by M_2 when M_1 enters a triode strong region of operation with a linear characteristic. Nonetheless, it can be seen from Fig. 12 that the sub-threshold resistors could offer better overall THD performance over the tuning voltage, extending down to weak inversion operation in the MOSFETs.

To demonstrate robustness of the sub-threshold R-MOSFET resistor, the simulated THD performances over extreme process and temperature conditions are given in Figs. 13(a), (b) where the intermediate drops of the THDs at the same corresponding V_{C1}s under the typical conditions are noticed for both designs. Also, the plots indicate the THD better than −42 dB in the sub-threshold resistor over the extreme conditions.

To investigate the impact of component mismatches on linearity, systematic mismatches at 10% were introduced to the resistor pairs R_1 and R_2, as well as the channel width W of the transistor pairs M_1 and M_2. For the threshold mismatch in the transistor pairs, it was set at 5% of the supply voltage, i.e., ΔV_{TB} = 25 mV. The resulting simulated THDs versus inputs under the assigned mismatches are given in Fig. 14 alongside the plots with perfect matching, both at typical conditions of designs C and D. Note that the THD plots are given at V_{C1} = 0.25 V since this yields the worst distortion performances in both designs under sub-threshold operation in M_1 and M_2 [cf. Fig. 12]. It is seen that such mismatches cause the distortion to increase at low inputs by as much as 9 dB, and this is primarily due to considerable increase in the second harmonic distortion components. At larger inputs, the degradation in the THD is successively reduced. At the maximum input of 0.5 V_p, the distortion level is practically intact for design C, where it is increased by less than 1 dB for design D, suggesting good robustness in linearity against mismatches at high input levels.

Also simulated was the performance of the sub-threshold resistors in terms of the frequency response. These are as shown in Figs. 15(a) and 15(b) for the i_o/v_{in} characteristics at typical conditions and different V_{C1}s. It is evident

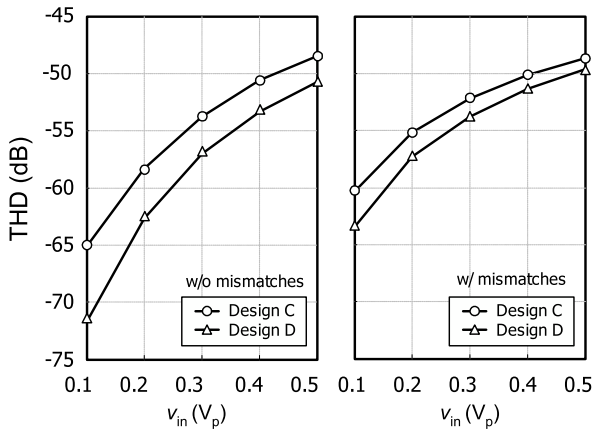

Fig. 14 Simulated THD performances versus input for design C and D under typical conditions at V_{C1} = 0.25 V with and without systematic mismatches.

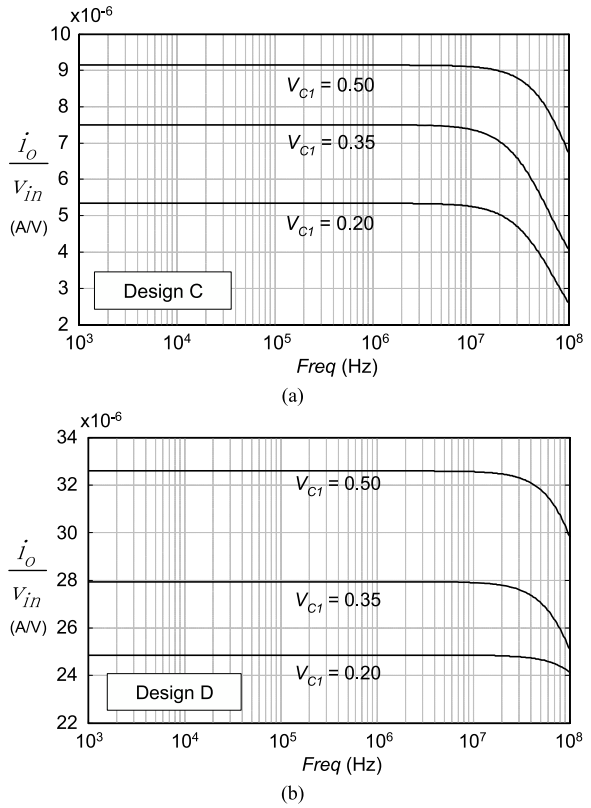

Fig. 15 Simulated frequency responses at V_{C1} = 0.2 V, 0.35 V and 0.5 V for (a) Design C and (b) Design D.

that the operation up to several tens of MHz is feasible for the resistances of design C and D which are in the order of ten to hundred kilo-ohms [cf. Fig. 11]. Finally, to verify the scaling property, both the sub-threshold R-MOSFET resistors were scaled by a factor k = 1/4, i.e., with R_1 = R_2 = 22.5 kΩ, n_1 = 16 and n_2 = 8 for design C, and R_1 = R_2 = 5.5 kΩ, n_1 = 16 and n_2 = 8 for design D. Simulation indicates corresponding reduction of the effective resistances [cf. Fig. 11] by a factor of four whereas there is practically no change on the distortion performances [cf. Figs. 12–14].

4. Conclusions

The analysis, design and performance verification of the sub-threshold R-MOSFET tunable resistor with extended MOSFET operation from traditional non-saturated strong inversion to saturated sub-threshold inversion have been presented. The operation of the sub-threshold resistor was described to rely upon a parallel of two non-linear resistive branches with a linear dependency to achieve a linear input/output characteristic. The analysis was first outlined based on a general MOS equation valid for all regions of operation. Various approximations including the use of a third-order polynomial to represent the characteristic of a MOSFET pair were subsequently introduced and this led to operational insight and practical design conditions of the sub-threshold resistor to ensure a good linearity over the tuning range. Extensive verification of its functionality and performance was given via breadboard experiments, and its feasibility in IC realization via simulation. Based on the achievable distortion performances, the sub-threshold resistor technique should prove very useful for a very low supply continuous-time filter implementation with a moderate linearity requirement.

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