รายงานวิจัยฉบับสมบูรณ์

โครงการ: การออกแบบวงจรรวมสำหรับปรับสัญญาณคลื่นไฟฟ้าหัวใจแบบพลังงานต่ำที่มีช่วงพลวัตรของสัญญาณขาเข้าที่กว้างสำหรับเครื่องวัดคลื่นไฟฟ้าหัวใจแบบสวมใส่

โดย ผศ. ดร. วรดร วัฒนพานิช

พฤษภาคม/2563

สัญญาเลขที่: RSA6080053

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ภาควิชาวิศวกรรมไฟฟ้า คณะวิศวกรรมศาสตร์

มหาวิทยาลัยเกษตรศาสตร์

สนับสนุนโดยสำนักงานกองทุนสนับสนุนการวิจัยและ

มหาวิทยาลัยเกษตรศาสตร์

(ความเห็นในรายงานนี้เป็นของผู้วิจัย สกว และมหาวิทยาลัยเกษตรศาสตร์ไม่จำเป็นต้องเห็นด้วยเสมอไป)

กิตติกรรมประกาศ

โครงการวิจัยนี้จะไม่สามารถสำเร็จลุล่วงไปได้หากขาดความร่วมมือร่วมใจจากสมาชิกห้องปฏิบัติการวิจัยด้านการออกแบบวงจรรวมและระบบบูรณาการพลังงานต่ำแห่งมหาวิทยาลัยเกษตรศาสตร์ทั้งที่ได้จบการศึกษาไปแล้วและกำลังทำการศึกษาอยู่ ที่ได้ร่วมแรงร่วมใจในการออกแบบ พัฒนาและทดสอบวงจรต่างๆ และระบบที่ได้อธิบายในรายงานฉบับสมบูรณ์ฉบับนี้ นอกจากนี้ ผู้วิจัยยังขอขอบคุณภาควิชาวิศวกรรมไฟฟ้า และคณะวิศวกรรมศาสตร์ มหาวิทยาลัยเกษตรศาสตร์ ที่ได้สนับสนุนสาธารณูปโภคต่างๆ ด้านการวิจัย ครุภัณฑ์ รวมทั้งเงินทุนสำหรับลูกศิษย์ที่ได้ช่วยในการทำงานวิจัยนี้

สุดท้ายนี้ ผู้วิจัยขอขอบคุณมหาวิทยาลัยเกษตรศาสตร์และสำนักงานกองทุนสนับสนุนการวิจัย ผู้สนับสนุนงบประมาณหลักสำหรับงานวิจัยนี้ จนผู้วิจัยสามารถทำงานจนสำเร็จลุล่วงไปได้

วรดร วัฒนพานิช

Final Report

Project Code: RSA6080053

Project Title: Design of A Wide-Dynamic-Range Ultra-Low-Power ECG Signal-Conditioning Integrated Circuit (IC) for Next-Generation Wearable ECG Acquisition Systems

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Abstract

In recent years, cardiovascular diseases have become, by far, the leading cause of death among the Thai population. Despite the enormous national budget spent on the diagnoses and treatments of cardiovascular diseases in hospital settings, many fellow Thai citizens still succumb to the diseases daily. The death rate due to heart diseases may be reduced if the majority of the Thai population has easy access to state-of-the-art wearable cardiac monitoring systems. To be useful in clinical applications and be widely adopted by the general public, such wearable cardiac monitoring system must be able to provide high-quality recorded electrocardiograms (ECG) for diagnostic and treatment purposes, be low-power, small in size, and be very convenient to use. These aspects put stringent requirements on the design of the ECG signal-conditioning circuits. In this research, we have designed, built, and tested a low-power wide-dynamic-range ECG signal-conditioning integrated circuit (IC), suitable for use in the next-generation cardiac monitoring systems. The IC, fabricated in a standard 0.18-μm CMOS technology, consumes a total current of less than 10 μA from a 1.2-V supply voltage, making it one of the lowest-power ECG readout IC in the literature. Due to its high input impedance, the IC is suitable for recording from dry electrodes, thus paving the way for the development of battery-powered wireless active-electrode ECG readout systems that are comfortable to wear on the body. As part of this research, we have also developed novel architectures for some of the IC's building blocks, which result in high-impact journal publications. We believe that the results from this study are useful not only in ECG recording applications, but also in implantable biomedical devices, other wearable electronics for health monitoring, and low-power sensor nodes in wireless sensor networks.

Keywords: bioelectronics, cardiac monitoring system, mixed-signal integrated circuit design, motion artifact, low-power, instrumentation amplifier, signal-folding amplifier,

Research area/ sub area of this project: Electrical Engineering, Analog/Mixed-Signal Integrated Circuit, Biomedical Circuits and Systems

ชื่อโครงการ: การออกแบบวงจรรวมสำหรับปรับสัญญาณคลื่นไฟฟ้าหัวใจแบบพลังงานต่ำที่มีช่วงพลวัตรของสัญญาณขาเข้าที่กว้างสำหรับเครื่องวัดคลื่นไฟฟ้าหัวใจแบบสวมใส่

บทคัดย่อ

ในไม่กี่ปีที่ผ่านมา โรคหัวใจและหลอดเลือดนับเป็นสาเหตุการตายอันดับหนึ่งของประชากรไทย ถึงแม้ว่ารัฐบาลจะได้ทุ่มเทงบประมาณในการตรวจวินิจฉัยและการรักษาโรคหัวใจและหลอดเลือดในโรงพยาบาล ก็ยังมีประชากรไทยจำนวนหลายคนที่ต้องเสียชีวิตจากโรคหัวใจและหลอดเลือดในแต่ละวัน อย่างไรก็ตาม เราสามารถลดอัตราการเสียชีวิตจากโรคหัวใจได้ถ้าประชากรส่วนใหญ่สามารถเข้าถึงระบบตรวจวัดคลื่นไฟฟ้าหัวใจแบบสวมใส่ที่ทันสมัย ในการจะเข้าถึงและได้รับการยอมรับโดยประชากรส่วนใหญ่ได้ เครื่องตรวจวัดคลื่นไฟฟ้าหัวใจแบบสวมใส่นี้ต้องสามารถตรวจวัดคลื่นไฟฟ้าหัวใจได้อย่างแม่นยำ อีกทั้งต้องมีขนาดเล็ก มีอัตราการกินพลังงานที่ต่ำ และต้องมีการใช้งานที่ง่ายอีกด้วย ข้อกำหนดเหล่านี้ทำให้การออกแบบวงจรสำหรับวัดและปรับสัญญาณคลื่นไฟฟ้าหัวใจมีความท้าทายอย่างยิ่ง ดังนั้นในงานวิจัยนี้ ผู้วิจัยจึงได้ทำการออกแบบ ผลิต และทำการทดสอบวงจรรวมสำหรับปรับสัญญาณคลื่นไฟฟ้าหัวใจแบบพลังงานต่ำที่มีช่วงพลวัตรของสัญญาณขาเข้าที่กว้าง สำหรับการใช้ในเครื่องตรวจวัดคลื่นไฟฟ้าหัวใจแบบสวมใส่แห่งอนาคต วงจรรวมนี้ได้ถูกผลิตในเทคโนโลยีซีมอสแบบมาตรฐานขนาด 0.18 ไมโครเมตร โดยมีอัตราการกินกระแสน้อยกว่า 10 ไมโครแอมป์จากไฟเลี้ยงขนาด 1.2 โวลต์ นอกจากนี้วงจรยังมีความต้านทานขาเข้าที่สูง ซึ่งเหมาะสมสำหรับการใช้วัดคลื่นไฟฟ้าหัวใจจากอิเล็กโทรดแบบแห้ง อันจะส่งผลให้การสวมใส่เครื่องดังกล่าวมีความสะดวกสบายกว่าการใช้อิเล็กโทรดแบบเปียกเป็นอย่างมาก และในงานวิจัยนี้ ผู้วิจัยยังได้พัฒนาสถาปัตยกรรมวงจรรูปแบบใหม่สำหรับวงจรส่วนประกอบต่างๆ ซึ่งได้ถูกรายงานในวารสารทางวิชาการระดับนานาชาติชั้นนำในสาขาวิชานี้ด้วย ผู้วิจัยจึงหวังเป็นอย่างยิ่งว่าความรู้ที่ได้จากงานวิจัยนี้จะเป็นประโยชน์ไม่ใช้เฉพาะในการออกแบบวงจรสำหรับการวัดคลื่นไฟฟ้าหัวใจเพียงอย่างเดียว แต่ยังมีประโยชน์สำหรับการใช้งานแบบอื่นๆ เช่น การออกแบบอุปกรณ์ชีวการแพทย์แบบฝังในร่างกาย และอุปกรณ์วัดสัญญาณชีพแบบสวมใส่อื่นๆ

Introduction to the research problem and its significance

Cardiovascular diseases and heart failure have become the leading causes of death throughout the world in the last few decades. Recently, due to lifestyle changes such as consuming diets high in saturated fat, exercising less, and smoking and drinking heavily, the Thai population is acquiring cardiovascular diseases at an alarming rate. Besides, Thailand is becoming an aging society, with a growing number of older people that outpaces the national birthrate. These aging people possess higher risks of acquiring cardiovascular diseases and heart failure. Such non-communicable diseases have become an epidemic in modern Thai society and have claimed the lives of a large number of our fellow citizens yearly. From the WHO's 2014 statistics, cardiovascular diseases account for 29 percent of all deaths in the Thai population — by far the leading cause of death in our country. There is no better cure for cardiovascular diseases other than changing to healthier lifestyles. Nevertheless, for a country with a large population already suffering from cardiovascular diseases, focusing on the diagnoses and treatments of the diseases should also be an immediate national agenda. Even though Thailand is spending a large amount of money dealing with such diagnoses and treatments, many people still lost their lives to cardiovascular diseases, especially those without easy means to access state-of-the-art medical facilities.

In a fully-equipped health center, medical personnel may observe a patient's electrocardiogram (ECG), the heart's electrical patterns projected onto the patient's body, to determine abnormalities of the heart — abnormalities in the ECG waveforms are usually called arrhythmias. This diagnosis is generally performed at a bulky ECG station at which the patient must lie still to minimize interferences induced by the patient's motions and muscle activities. Long wires are then connected between the ECG acquisition machine and the electrodes attached to various points on the patient's body to acquire the ECG. This cumbersomeness may have shunned even well-to-do patients from having frequent ECG diagnoses. Such frequent diagnoses may help prevent many severe symptoms from going unnoticed, thus helping reduce the number of deaths from cardiovascular diseases and heart failure. For abnormalities that are hard to identify in a limited time at a medical facility, doctors may prescribe the use of a Holter monitoring system, an ambulatory ECG recording device that can continuously record ECG for 24-48 hours. However, most Holter monitors in the market today offer only primitive functionalities while consuming too much power for long-term chronic use; they only store data in the devices' memories to be downloaded and analyzed later by the physicians. With their current power consumption level, most Holter monitors require at least two AAA batteries for 24-48 hours of operation, thus making them relatively large and increasing component and packaging cost. The

cost of a commercially-available mid-range Holter monitor in the market today is approximately 2,000-3,000 US dollars, still too expensive for the Thai general public. As a result, most Holter monitors today are only for diagnostic purposes, in which hospitals lease them to patients with some fees.

Now imagine if we have an ambulatory ECG acquisition system that is an order of magnitude smaller than current Holter monitors, and requires only button batteries to operate for months of operation. Also, imagine that such device can wirelessly transmit the recorded data in real-time to a remote computer on the physician's desk and can issue warnings when cardiac arrhythmias occur while being robust, low-cost, and comfortable to wear on the body. These devices may change the face of the Thai healthcare system regarding the diagnoses and treatments of cardiovascular diseases; with such devices, advanced cardiac monitoring can be accessible by patients with limited means. The full adoption of such technology may help in the early diagnoses and warnings of heart problems, which can save many lives that might otherwise be lost to cardiovascular diseases. The technology can also help reduce the overall healthcare cost since early diagnoses can prevent symptoms from getting worse, thus obviating expensive medical procedures needed for treating severe patients.

The small form factor and low power consumption of the devices require that such ECG acquisition systems be as integrated as possible. Figure 1 shows a high-level view of a low-power small-form ECG acquisition system mentioned above. The system consists of three main parts, which can be implemented as low-power integrated circuits (ICs): i) an ECG signal-conditioning IC ii) a wireless transceiver IC and iii) a power management IC. The ECG signal-conditioning IC interfaces directly with electrodes and performs simple signal-conditioning tasks on the input signal. The wireless transceiver IC transmits the conditioned signal to a nearby computing platform, such as a smartphone, for further processing and also receives commands to configure the system. The power management IC supervises all the power-related tasks of the system. While all the ICs are indispensable for the complete functionality of the system, the ECG signal-conditioning IC is the bottleneck for the performance of the overall acquisition system as it determines the quality of the acquired signal. Whether the acquisition system can be used in clinical applications depends mainly on the ECG signal-conditioning IC. There are many technical challenges regarding the signal conditioning that need to be addressed before such ambulatory ECG acquisition systems come into widespread use. These challenges can be categorized as follow:

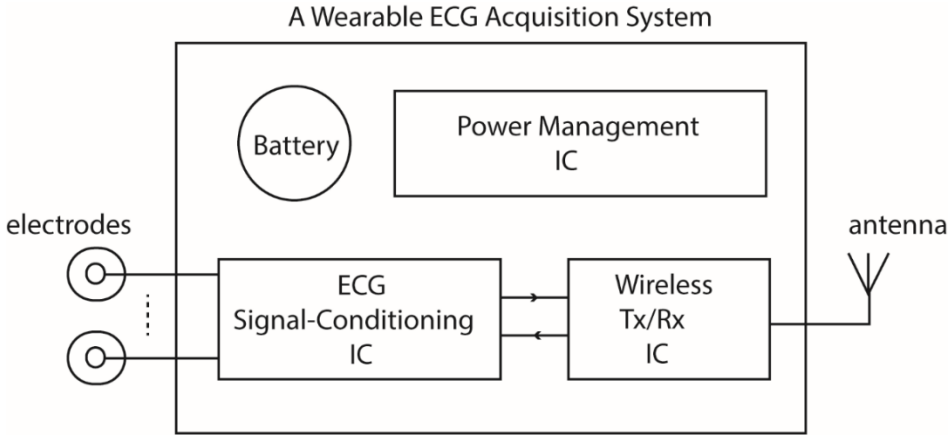


Figure 1: A low-power small-form ECG acquisition system.

Comfortability: Current Holter monitors use low-impedance wet Ag-AgCl electrodes to record ECG from the body's surface. This kind of electrode gives the highest signal quality due to its secure contact with the body through the adhesive gel. Though suitable for the diagnoses at an ECG station in a hospital setting, the gel electrode is not very suitable for the chronic monitoring application. After the electrodes are used for a long time, their adhesive gel becomes dry, causing discomfort to the user and significantly degrading the signal's quality. Thus, the majority of users may not be willing to use the device unless necessary, such as when prescribed by a physician. For less degree of discomfort, the device can use non-contact electrodes [1]. These electrodes are like clothes, which can be made as parts of the user's clothing, thus causing much less discomfort to the skin.

Quality of the Input Signal: Non-contact electrodes have a much higher impedance ($G\Omega$ range) compared to that of the Ag-AgCl electrode (tens of $k\Omega$s range). Due to their high impedances and less secure attachment to the body, non-contact electrodes yield inferior signal qualities compared to those obtained from the Ag-AgCl electrode. If the input impedance of the front-end amplifier is not high enough, the input signal will be attenuated due to the high electrode impedance. Also, non-contact electrodes are very susceptible to motion artifacts, the baseline variations in the recorded signals induced by the movements of electrodes relative to the skin. Motion artifact is a primary concern for most wearable devices intended for use in daily activities, in which the users are not restrained to a sedentary position. Apart from the motion artifact, non-contact electrodes are also susceptible to powerline interference (50/60 Hz interference from the mains). Even with differential recording and infinite common-mode rejection, the ECG recording system may have impedance mismatches in their electrodes, thus converting the common-mode powerline interference on the body into a differential-mode signal. As a result, the output of the front-end amplifier may contain powerline interference that is much larger than the desired ECG

waveform; the large interference significantly increases the dynamic range of the input signal, which complicates the design of the signal-conditioning IC.

Power Consumption: Due to its susceptibility to powerline interference and motion artifact, the ECG acquisition system employing non-contact electrodes must accommodate a large input dynamic range, which can be several times of the desired signal's amplitude. The combined powerline interferences and motion artifact can have amplitudes on the order of tens of millivolts. In contrast, the ECG typically has an amplitude of 1 mV_{pp} or less. The large overall input requires that the front-end amplifier of the ECG acquisition system have low gain. As a result, the analog-to-digital converter (ADC) that follows must have a high resolution to resolve the tiny ECG's features buried in the input signal—using a high-resolution ADC in the ECG acquisition system results in high overall power consumption. As a result, the acquisition system may need a larger battery, thus increasing the size and cost of the system; a large device is also less comfortable to wear on the body. As a first step to minimize the overall power consumption and, in turn, the size of the overall system, we need to minimize the required resolution of the ADC.

Output Signal Quality To record ECG waveform with diagnostic level quality, the ECG acquisition system must preserve the fidelity of the output signal even though the ADC's resolution is lowered to reduce the overall power consumption. Since reducing the ADC's resolution requires the front-end amplifier to have a high gain such that the ADC's quantization noise becomes negligible, the acquisition system must reject interferences and motion artifact within the front-end amplifier itself to prevent signal saturation at its output. Due to the limited power and area, we can only incorporate simple interference rejection algorithms on-chip; these algorithms can help reject some degrees of interferences but may distort the desired features of the ECG. Employing high-performance digital algorithms such as the Principle Component Analysis (PCA) or the wavelet transform to reject interferences may help lessen the distortion, but they are power-hungry, and their realization occupies a large chip area, thus are not suitable for low-power on-chip implementation. Our main question is how to use only these simple algorithms to reject interferences while preserving all the important features of the ECG signal.

In this research, we have designed, built, and tested a low-power ECG signal-conditioning IC suitable for acquiring ECG signals from high-impedance (dry/non-contact) electrodes. Circuit techniques and architectures are developed to preserve the important features of the ECG waveform, even when recording amidst large powerline interferences and motion artifacts. Based on the proposed IC, we have also built a prototype of a wireless ECG readout system that can

continuously record ECG from patients and send the recorded data wirelessly to a remote computer. We hope that the knowledge gained from this research will be instrumental in the design of miniaturized, low-cost wireless ECG recording systems, which, one day, can help save thousands of lives that might have been lost from cardiovascular diseases and heart failure.

Literature Review

To understand the challenges high-impedance electrodes pose for the design of a low-power ECG signal-conditioning IC, we first need to understand different types of high-impedance electrodes commonly employed in biosignal acquisition applications. The review paper [1] gives a good overview of the types of high-impedance electrodes and also discusses important issues for designing front-end amplifiers to interface to them. In a broad sense, high-impedance electrodes can be categorized into two types: 1) dry electrodes 2) non-contact or capacitive electrodes. The principle of dry electrodes is somewhat similar to that of the wet Ag-AgCl electrodes. Instead of employing explicit electrolytes, dry electrodes use moisture on the skin to act as an electrolyte. There are several dry electrodes reported in the literature [2-5]. These electrodes are based on rubber and fabric, which should provide enough flexibility for comfortable use in wearable ECG acquisition systems. However, unlike wet Ag-AgCl electrodes, which are fixed on the skin via adhesive gel, dry electrodes are more prone to movement relative to the skin. Such movement usually elicits motion artifact in the acquired ECG; large motion artifact increases the required input dynamic range of the system, thus increasing the design complexity and the overall power consumption. Besides, dry electrodes exhibit higher impedance than the wet Ag-AgCl electrodes, even though the impedance can become lower after a period of use as sweat builds up on the skin. As a result, most successful interfacing circuits employ the active electrode technique — i.e., placing a front-end amplifier right next to every dry electrode to minimize coupling from powerline interference and also minimize the front-end amplifier's input impedance — to buffer the signal and drive the cable [6]. However, this design technique may increase the overall power consumption of the system since all the front-end amplifiers must provide low enough input impedance to drive the cables; biasing the front-end amplifiers for low output impedance requires power. To obtain the best signal quality from dry electrodes, it is best to minimize the electrode impedance through some kinds of skin preparation.

In many cases, the high-resistance layer of the skin, called Stratum Corneum, can be abraded or hydrated to lower the contact resistance. To minimize the movement of electrodes relative to the skin, some electrode designs employ a layer of microfabricated needles [7, 8] to pierce through the Stratum Corneum to achieve a secure grip on the skin. It is not difficult to reason that lowering contact resistance through skin abrasion can cause discomfort to the body. As for the needle electrodes, the authors in [1] reported that such electrodes can cause skin irritation or even pain. In summary, dry electrode, requiring no adhesive gel for operation, may be a little more convenient for long-term use compared to conventional wet Ag-AgCl electrodes. However, due to the higher impedance and less secure contact to the skin, dry electrodes pose

other challenges for the design of interfacing circuits, especially when we want to avoid skin abrasion or the use of needle electrodes to maximize the usability of the ECG acquisition system. Without these techniques, our ECG signal-conditioning IC must exhibit high input impedance and must be able to handle higher levels of powerline interference and motion artifact, while consuming low power.

The other type of high-impedance electrodes, i.e., the non-contact or capacitive electrode, is even of higher interest to the PI than the dry electrode discussed earlier. This kind of electrode can sense signal through an insulating gap, such as clothing or air, between the sensor and the body; this type of electrode should offer maximum comfort when worn on the body and, thus, is a natural candidate for use in our system. Also, there are reports on the systems that use non-contact electrodes to sense biopotentials from sensors mounted on beds, chairs, or even toilet seats [9-11]. However, employing non-contact electrodes in wearable ECG acquisition systems poses even more challenges than does employing dry electrodes. The main reason is that non-contact electrodes exhibit very high source impedance, which can be thought of as consisting of small coupling capacitances (on the order of 10 pFs) and very large resistive elements (> 100 $\mathrm{M}\Omega$) [12, 13]. Such high source impedance poses a major challenge for the design of the front-end amplifier that interfaces with non-contact electrodes. The challenge arises because we must design the front-end amplifier to have much higher input impedance than that of the non-contact electrode to not cause strong attenuation due to the voltage division between the front-end amplifier's input impedance and the electrode's impedance. Also, even though we can design a front-end amplifier with a very high input impedance, the electrode-front-end-amplifier interface is a very high impedance node, which is highly susceptible to powerline interference. Therefore, successful systems frequently employ proper shielding and subject grounding techniques to minimize common-mode noise due to powerline [14]. We may envision that these techniques may not be so easily employed in next-generation wearable ECG acquisition systems as they may limit the use of the acquisition systems to only some constrained applications such as in a proper laboratory setting. What if the users wear the ECG acquisition systems in a noisy environment where proper shielding of the mains is not applicable? In this case, the ECG acquisition system should employ a combination of the driven-right-leg active ground technique [15], to minimize the common-mode noise, and other powerline interference cancellation techniques such as [16, 17]. It has been shown in [14] that the driven-right-leg active grounding scheme is effective in suppressing the common-mode noise even through the use of capacitive electrodes.

The major challenge posed by the use of non-contact electrodes is their susceptibility to motion artifact. Even though there are reports on successful systems employing non-contact electrodes in moving subjects [18, 19], these systems use a tight vest and chest band to minimize electrode movement with respect to the body. Without a means to secure the non-contact electrodes in place, the problem of how to cleanly remove motion artifact from the desired signal is still unresolved. In general, there are three main sources of motion artifact due to the use of non-contact electrodes: 1) large time constant of the high-impedance input node 2) electrode-to-skin displacement 3) friction between the electrode and insulation. Among these sources, friction is the most serious one since it can cause large voltage excursion at the high-impedance input node. Besides, there is no known solution to correlate the frictional action to its induced motion artifact in the acquired signal. Coupled with the large time constant of the high-impedance input node, the friction-induced motion artifact may cause prolonged signal saturation at the output of the front-end amplifier if its gain is too high. Therefore, the use of one high-gain front-end amplifier, though most efficient in terms of the power-noise tradeoff, may not be the best solution for ECG acquisition systems that employ non-contact electrodes. In this case, the use of distributed-gain front-end amplifier with some forms of motion artifact suppression should prove a more viable candidate. For the motion artifact induced by electrode-to-skin displacement, the authors of [20] proposed a simple method to suppress this type of motion artifact. However, the method relies on the precise knowledge of the electrode-to-skin coupling capacitance. We can thus argue that such a method is effective only in simulations and prepared experimental settings. In this research, we investigate an effective way to prevent signal saturation due to motion artifact, without relying on the precise knowledge of the motion-artifact-causing mechanisms.

Most of the reported ECG signal-conditioning circuits are designed for use with conventional wet Ag-AgCl electrodes, thus are not designed for a large enough input dynamic range necessary for high impedance electrodes. Here we consider a few notable systems, with an emphasis on the recording of the raw ECG since it is most relevant to clinical applications. In [21], the authors present quite a complete analog signal processor chip, consisting of one ECG readout channel for streaming out the raw ECG data, one band-power extraction channel for detecting heartbeats, one continuous-time impedance monitoring channel to detect whether the electrodes make proper contact with the body. The impedance monitoring channel can also be used for the suppression of motion artifact, as will be discussed later. The system contains one 11-bit successive-approximation-register (SAR) ADC, which is shared by all the three channels. The overall system, implemented in a 0.5-μm CMOS process, consumes only 30 μW from a supply voltage of 2 V. The ECG readout channel, which we are most interested in, provides four

gain settings ranging from 300 to 1300. This method of gain programmability is employed to increase the dynamic range of the input. The system can use the highest-gain setting if the input is clean (containing only ECG waveform whose amplitude is lower than 1 mV_{pp}), while it can switch to the lower-gain settings if the input contains large motion artifact and powerline interference. There are two drawbacks to this approach. First, notice that the system employs quite a high-resolution ADC (11-bit), which consumes a large chip area and a high power. The main reason for utilizing such a high-resolution ADC is the low gain of the signal path. As a rule of thumb, the ADC's quantization noise referred to the input of the system should be less than the input-referred noise of the front-end amplifier. In most systems, the front-end amplifiers are designed to provide input-referred noise lower than 1 μV_{rms}; this is to provide around 60 dB signal-to-noise ratio (SNR) for the ECG signal with 1-mV_{pp} amplitude). For the signal path's gain of only 300, we require an ADC with at least 11 bits to keep the input-referred ADC's quantization noise below that of the front-end amplifier. In this system, the ADC's resolution is chosen based on the worst-case input, which requires a gain of 300 in the signal path. The overall system should be more power-efficient if we can use an ADC with a much lower resolution, regardless of the amplitude of the input. The second drawback of this variable gain approach is that the system requires supervision by the user, which can be very inconvenient in practice. Otherwise, some forms of automatic gain control must be incorporated into the system, which increases the design complexity. In fact, the system in [21] does not include any form of automatic gain control, suggesting that gain calibration is performed manually by the user.

There are other works that employ the variable gain approach with a relatively high-resolution ADC. The work in [22], the follow up of the work in [21], utilizes even lower gains in the signal path (75-300), but compensate for the lower gain with a higher resolution ADC (12-bit SAR ADC). The system consumes 17 μW per channel from a 1.2 V supply for the raw data recording mode; such power consumption is quite impressive among systems that employ such a high-resolution ADC. The reason for such power efficiency is the use of the SAR topology. However, their ADC achieves an integral nonlinearity (INL) of almost 4 LSB, suggesting that the chosen SAR topology is practically not suitable for the 12-bit resolution. In this case, the $\Sigma\Delta$ topology is a more suitable choice. Another system [23] utilizes the variable gain approach with the gain ranging from 22-46 dB. It incorporates a 12-bit $\Sigma\Delta$ ADC to compensate for the low gain of the signal path. The system consumes 100 μW per channel, while the ADC alone consumes 46 μW, emphasizing the disadvantage of $\Sigma\Delta$ ADCs to SAR ADCs in terms of power efficiency. However, given such a high resolution requirement, the $\Sigma\Delta$ topology is a more natural choice since it is difficult to implement SAR ADC with a resolution of higher than 10 bits due to the

stringent component matching requirement. We thus emphasize that, to avoid the use of a high resolution ADC, we should maximize the overall gain of the signal path. Another low-power ECG signal-conditioning system that is worth mentioning is the work in [24]. This system, with 2 channels of ECG recording, consumes a total power of 74.8 μW from a 0.7-V supply. It is interesting to see that the system utilizes the signal path's gain that ranges from only 36-44 dB, but employs a SAR ADC with only 8 bits of resolution. As reported in [24], using such low-resolution ADC with a low signal path's gain comes at a price of almost 6.9 μV_{rms} noise referred to the input of the system — most systems are designed for input-referred noise of around 1 μV_{rms}.

Even with standard wet Ag-AgCl electrodes, the ECG acquisition systems mentioned thus far employ relatively low gains in their amplification stages followed by relatively high-resolution ADCs to achieve appropriate input dynamic range, but at the cost of the overall higher power consumption. With high-impedance electrodes, motion artifact and powerline interference will increase the input dynamic range even further. Does this mean that we have to use even a lower gain in the amplification stage and a higher-resolution ADC? This approach would, of course, incur even higher power consumption in the overall system. To reduce the input dynamic range, we should suppress the motion artifact and powerline interferences at the front-end amplifier. Here, let's review some systems that incorporate schemes to suppress motion artifact right at the front-end amplifier. Though these systems are not designed for use with high-impedance electrodes, the ideas presented apply to our proposed system as well. It has been shown in [25] that motion artifact has some correlation with variation in the electrode impedances caused by the user's movement. Thus, we can use an adaptive filtering scheme to find the correlation between the variation in the electrode impedances and the motion artifact in the recorded signal. Such correlation can be used to derive a nulling signal from the variation in the electrode impedances; we can then subtract this nulling signal at the input of the front-end amplifier such that its output is virtually free of motion artifact. There are some works [25, 26] that use adaptive filters with simple least-mean-square algorithms to perform motion artifact removal. But these algorithms are employed in the digital backend; thus, they would not help reduce the input dynamic range of the front-end amplifier. To take the adaptive filtering idea a step further, [27-29] propose a topology that can remove the motion artifact right at the front-end amplifier. The topology performs adaptive filtering on the digitized data using a low-power microcontroller (MSP430 from Texas Instrument) to obtain the nulling signal, then feeds the nulling signal back to cancel with the motion artifact at the input of the front-end amplifier through an on-chip digital-to-analog converter. These methods were shown to be effective, thus helping reduce the required

input dynamic range of the system. However, the main drawback of this method is that it requires a strong correlation between the variation in the electrode impedances and the motion artifact in the acquired signal. From what we have experienced in our research, such strong correlation is quite rare in normal usage of the system — such as while running or walking. The only case that we obtain a strong correlation is when we intentionally push and release electrodes in a pulsatile manner. Therefore, adaptive filtering might not be a viable choice for suppressing motion artifact at the front-end amplifier. In this research, we seek another more effective strategy.

Powerline interference is a major concern in most biosignal acquisition systems. Most of the time, we can view powerline interference as the common-mode noise into the input of the system. To minimize powerline interference, most ECG acquisition systems use differential-input topologies for their front-end amplifiers to achieve a high common-mode rejection ratio (CMRR). The works in [30-32] achieve a CMRR on the order of 120 dB at 50 Hz. Another method that is normally employed to minimize powerline interference is to suppress the common-mode noise on the user's body directly. To achieve this, we can use a technique called the driven-right-leg (DRL) that uses negative feedback to set the common-mode voltage on the body and suppress the common-mode noise [15, 33]. In practice, a combination of high-CMRR front-end amplifier and the DRL technique should be applied to suppress this common-mode noise. However, in practice, there exist numerous coupling paths between the mains and the electrodes, creating differential-mode noise at the input of the front-end amplifier. We should thus assume that there always exists differential-mode noise at the input, which cannot be suppressed by a high-CMRR front-end amplifier. A promising approach to suppress the differential-mode interference is to apply a nulling signal to the input of the front-end amplifier to suppress the interference in a feedback manner [16, 34]. This approach effectively creates a notch, at the interference's frequency, in the transfer function of the signal path. However, the current implementation of this approach requires power-hungry circuits such as a phase lock loop and analog multipliers [16] or require an off-chip digital processor to implement full-blown digital filters [34], thus making them unsuitable for ultra-low-power implementation in our system. Toward this aim, we have designed a low-power mixed-signal architecture for powerline interference cancellation [17]. This architecture consumes less than 1 μW of total power. We will use the knowledge gained from designing this architecture for suppressing the powerline interference in our proposed ECG signal-conditioning IC.

Objectives

1. To develop a new architecture of a low-power ECG signal-conditioning IC for use in wearable ECG acquisition systems.
2. To develop new knowledge and architectures on the integrated-circuit building blocks for acquiring ECG signals.
3. To demonstrate a high-performance, fully-functional ECG signal-conditioning IC that can record ECG signals from high-impedance electrodes while consuming less than 10 microwatts of power.

Methodology

General Considerations

Powerline interferences and motion artifact makes the design of an ultra-low-power ECG signal-conditioning IC for high-impedance electrodes difficult. At the electrodes, these interferences can have amplitudes on the order of tens of millivolts while the ECG waveform itself has an amplitude on the order of 1 mV or less. Thus, the signal-conditioning IC must have a high dynamic range to accommodate those large interferences while being able to resolve tiny features of the ECG waveform. In advanced IC processes, the supply voltage is on the order of 1 V. The conventional approach to acquiring ECG at the presence of large interferences is to employ a front-end amplifier with a relatively low gain (40 dB or less) to ensure no signal saturation at the front-end amplifier's output and then use a high-resolution ADC to resolve the tiny ECG features in the amplified signal.

Let's suppose that the input into the signal-conditioning IC, which operates from a 1.2-V supply voltage, has an amplitude of around 10 mV_{pp} due to powerline interferences and motion artifact. Let's also assume that the ECG waveform has an amplitude of 1 mV_{pp}, resulting in the combined input into the signal-conditioning IC with an amplitude of around 10 mV_{pp}. Also, let's suppose that, to prevent signal saturation at the output of the front-end amplifier operating from a 1.2-V supply voltage, the front-end amplifier can have a gain of at most 40 dB which results in the output's amplitude of 1 V_{pp}, almost the rail-to-rail level of the front-end amplifier. Suppose that the front-end amplifier has an input-referred noise of 1 μV_{rms}, i.e, 100 μV_{rms} at the front-end amplifier's output and, in turn, at the ADC's input. As a rule of thumb in choosing the ADC's resolution, the ADC's quantization noise should be negligible compared to the noise introduced by the front-end amplifier. For the ADC's full-scale voltage (V_{FS}) of 1.2 V whose quantization noise (V_Q) can be approximated as $V_Q = V_{FS} / \left(2^N \sqrt{12}\right)$ where N is the effective number of bits, we require $N > 11.8$ for V_Q to be less than the noise due to the front-end amplifier. In practice, we should use $N > 13$ for the quantization noise of the ADC to be negligible compared to the front-end amplifier's noise. The most commonly-used ADC in a low-power biosignal acquisition system is the SAR type due to its excellent power efficiency at low-to-moderate speed. This type of ADC employs a capacitive digital-to-analog converter (DAC) in feedback to help determine the output bits in the successive approximation fashion. The accuracy of SAR ADCs is normally limited by the matching accuracy of capacitances in the capacitive DAC. The matching accuracy of passive components in an IC process is rarely better than 0.1 % even with a careful layout. Thus, the SAR ADC's resolution is normally limited to 10 bits, without digital calibration. To achieve a

resolution of better than 13 bits, we normally employ the $\Sigma\Delta$ topology to implement the ADC. Since the $\Sigma\Delta$ ADC utilizes oversampling and noise shaping — these are power hungry digital techniques — to achieve a high resolution, its energy consumption per quantization level is significantly higher than that of a SAR ADC. Therefore, incorporating a 13-bit $\Sigma\Delta$ ADC in the signal-conditioning IC will prove prohibitive in terms of power. In this research, we will seek a better alternative.

The most energy-efficient way to minimize the required ADC's resolution is to use a high gain in the amplification stage. For example, if the amplifications stage provides a gain of 2000 (66 dB) and an input-referred noise of 1 μV_{rms}, the noise level due to the amplification stage will be 2 mV_{rms} at the ADC's input. An ADC with a full-scale voltage of 1.2 V and a resolution of 8 bits has a quantization noise of 1.35 mV_{rms}, which is already less than the 2 mV_{rms} noise from the amplification stage. Thus, with the amplification stage's gain of 66 dB, an 8-bit ADC is sufficient for use in the system. Ultra-low-power 8-bit SAR ADCs are very common in the literature. During his Ph.D. work, the PI designed a low-power 8-bit SAR ADC using custom digital logics for use in a neural recording system [35]; this ADC consumes energy per quantization level of 80 fJ. If this ADC were to be used in the system to digitize the ECG waveform at a sampling rate of 300 samples/second, it would consume a total power of only 6.14 nW; this power proves negligible in the signal-conditioning IC and further reduction of this power is no longer necessary.

The Proposed Architecture of The ECG Signal-Conditioning IC

Nevertheless, how can we amplify a 10-mV_{pp} input signal by a gain of 2000 in a system with the supply voltage of only 1.2 V. Our proposed solution is to cancel large interferences at a node within the front-end amplifier and use a signal-folding technique in the wide-output-range to keep the output signal within its output range. Even with perfect interference cancellation, effectively, the input signal's amplitude will be attenuated from 10 mV_{pp} down to 1 mV_{pp}, the amplitude of the ECG waveform, which still saturates the amplifier chain with a gain of 66 dB (1 mV_{pp} input signal results in an effective output swing of 2 V_{pp}). To prevent such output saturation, we will use a signal-folding scheme [36, 37] in which we place a circuit in the feedback path to monitor the output level of the wide-output-range amplifier and add appropriate correction voltages to a node within it such that the output level of the wide-output-range amplifier stays within the supply rails.

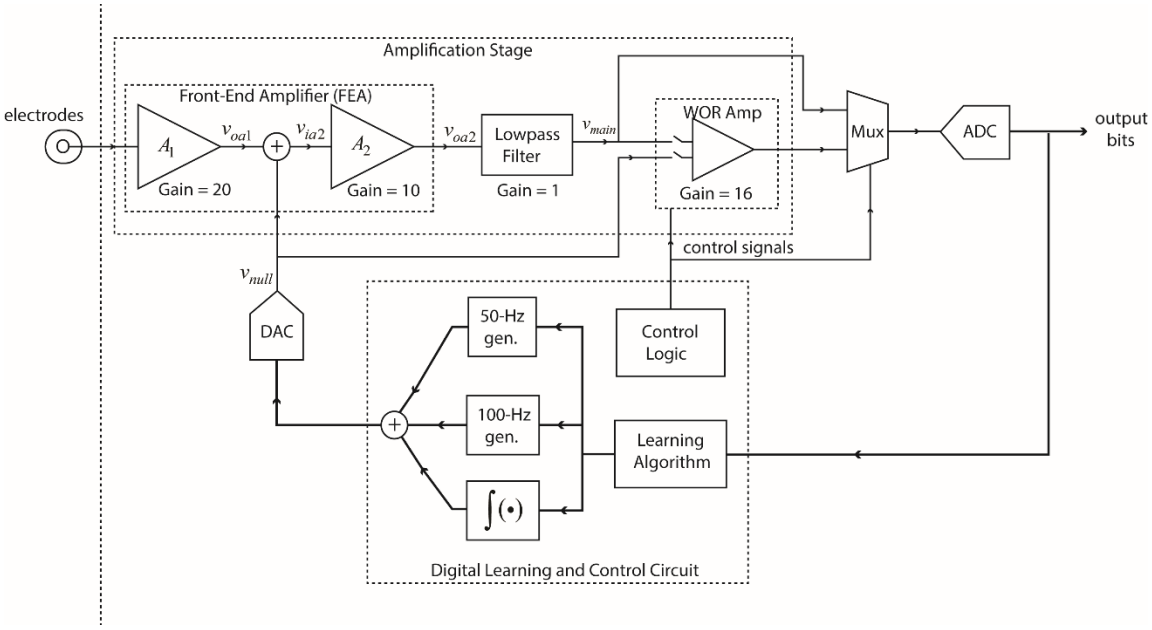


Figure 2: System architecture of the ECG signal-conditioning IC.

Figure 2 shows the conceptual idea of our proposed signal-conditioning IC. The IC consists of the amplification stage, an ADC, a digital learning and control circuit, and a digital-to-analog converter (DAC). The amplification stage consists of an front-end amplifier (in the dashed box), a lowpass filter, and a wide-output-range amplifier (WOR Amp). The front-end amplifier consists of two gain stages A_1 and A_2; A_1 provides a gain of 20 (26 dB) while A_2 provides a gain of 10 (20 dB). The choice of the gain of A_1 is to ensure that it is high enough such that the input-referred noise of A_2 is negligible when referred to the input of A_1. The gain of A_1 is also chosen low enough to prevent signal saturation at the output of A_1 even with large interferences at the input: a 15-mV_{pp} input signal at the input of A_1 only results in a 300-mV_{pp} signal at the's output, which is easily handled by a standard amplifier operating from a 1.2-V supply voltage. To prevent signal saturation at the output of A_2, the system will suppress the interferences before the signal is amplified by the amplifier A_2. This suppression is shown in Figure 2 by the superposition of the output signal of A_1, v_{oa1}, and another signal, v_{null}. The signal v_{null} is the result of a learning feedback algorithm in the digital learning and control circuit that observes the output of the ADC and adapts v_{null} until it sufficiently suppresses interferences in v_{oa1}. Once the feedback algorithm converges, the input into A_2, v_{ia2}, will consist mainly of the components from the desired ECG, and probably with little remnants of the interferences. After interference suppression, if the amplitude of v_{ia2} is no larger than 60 mV_{pp}, assuming some remnants of the interferences, the amplitude of the output of A_2, v_{oa2}, will be smaller than 600 mV_{pp}, which is still within the supply rails of an amplifier with a supply voltage of 1.2 V.

To amplify the output of A_2 further, we will pass it to the discrete-time amplifier called the wide-output-range amplifier (WOR amp) whose gain is 16 (24 dB). Note that the amplifier A_1 and A_2 are continuous-time amplifiers while v_{null} is generated from a DAC. Therefore, v_{oa2} will contain high-frequency contents due to the switching activities within the DAC. To prevent aliasing due to the sampling of v_{oa2} by the WOR amp, we use a lowpass filter to filter out the high frequency contents in v_{oa2} before feeding the signal into the WOR amplifier's input. Also notice that the total gain of the amplifier chain is now $200 \times 16 = 3200$ (70.1 dB). Assuming an input-referred noise of the front-end amplifier of 1 μV_{rms}, the noise due to the front-end amplifier at the ADC's input will be 3.2 mV_{rms}. An 8-bit ADC with a full-scale voltage of 1.2 V has a quantization noise of 1.35 mV_{rms}. Therefore, with this choice of the gain of the amplification stage, it is sufficient to use an 8-bit ADC to digitize the acquired signal, thus lowering the power of the overall system. In section **Error! Reference source not found.**, we will explain the operation of the WOR amplifier that prevents signal saturation at its output.

The major effort of this research is on the design and implementation of the architecture in Figure 2. For this research, we have published the explanation of the overall architecture and some of the measured results in [38]. As [38] is only a conference paper, we did not have enough space to delve into details of the important circuit blocks. For the 3-year period of this research, we only have enough time to go into details of the design and test of three important circuit blocks, including 1) the motion artifact estimator 2) the wide-effective-output-range amplifier and 3) the front-end amplifier. The motion artifact estimator is intended for use in the feedback path of the architecture in Figure 2. However, due to some robustness issues, we decided to replace it with just an integrator to create a lowpass response that helps filter out the motion artifacts. Nevertheless, our in-depth analysis on the design of the motion artifact estimator results in a journal publication [39] in the IEEE Transactions on Biomedical Circuits and Systems, which is one of the foremost publication in the field of biomedical circuits and systems design. The wide-effective-output-range amplifier garners more success in the architecture as it is the instrumental block in allowing us to achieve the high gain required without saturating the signal chain. We have presented our in-depth analysis and the measured results of this important circuit block in another journal article [40]. Finally, at the time of this report writing, we are still writing the third journal article of the project, particularly on the design of the front-end amplifier and its use in our proposed high-gain architecture with high impedance electrodes.

Results

We can divide the main results from this project into four parts. The first three parts are on the design of the architecture and its circuit blocks. The fourth part is on the design of a wireless ECG recording prototype, which demonstrates the functionality and the effectiveness of the proposed IC. In this section, we provide a summary of each part of the results. Interested readers are referred to the conference paper and the journal articles in the report's appendices for further details.

The High-Gain ECG Readout Architecture

This part of the research involves the overall design of the ECG readout architecture. The actual architecture that we have built for this research project is shown in Figure 3. This IC is fabricated in a 0.18 μm CMOS process from United Microelectronic Corp, whose chip micrograph is shown in Figure 4.

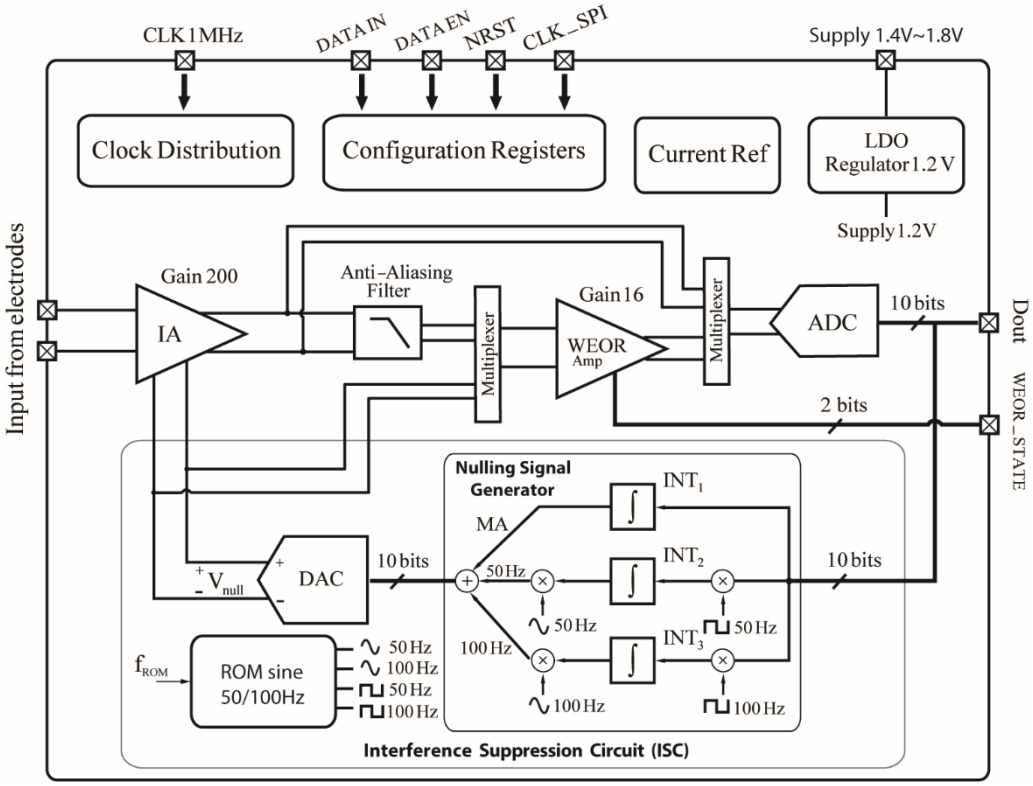


Figure 3: The architecture of the fabricated ECG readout IC

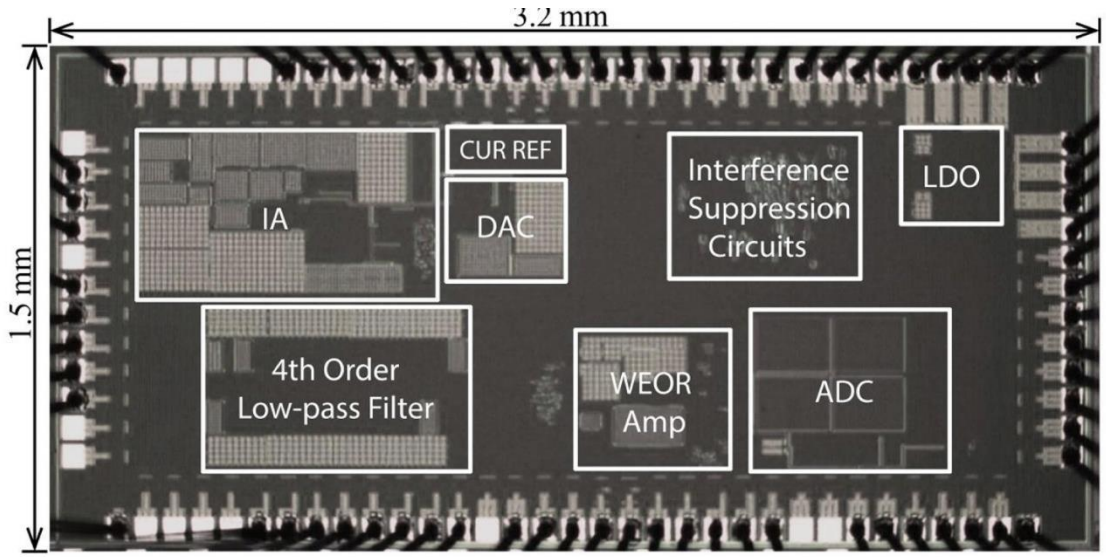


Figure 4: Chip micrograph of the ECG readout IC

The central thesis of this architecture is the use of a very high gain (70 dB) in the amplification stage to reduce the resolution requirement of the ADC. The amplification stage consists of the instrumentation amplifier (the IA) with a gain of 46 dB and the wide-effective-output-range amplifier (WEOR amplifier) with a gain of 24 dB. Due to such high gain, the required ADC's resolution is only 8 bits for its noise and distortion to be negligible when referred to the input of the readout system. However, we reason that the benefit of a very high gain comes the risk of signal saturation in the presence of large interferences—i.e., the motion artifacts and powerline interferences—at the input. Hence, to prevent such saturation, we incorporate an interference suppression circuit, which feeds back cancellation signals to the IA to suppress the interferences. The interference suppression circuit consists of a digital nulling signal generator and a digital-to-analog converter (DAC) to produce an analog cancellation signal that is fed back to cancel with the interferences at an internal node within the IA. The nulling signal generator consists of three components. The 50-Hz and 100-Hz sinusoidal generators produce sinusoidal waveforms whose frequencies and amplitudes are the same as but whose phases opposite to those of the first and second harmonics of the powerline interferences. The integrator extracts the low-frequency components of the output, which, after being fed back to the IA, creates the overall lowpass transfer function to filter out the motion artifact. To implement this signal nulling generator, we utilize the direct digital synthesis (DDS) approach and an adaptive least-mean-square algorithm to adjust the amplitudes and phases of the outputs to achieve good interference suppression. The chip also contains other peripheral circuits such as a low dropout voltage regulator to provide a stable and clean 1.2-V supply to the chip from a 3.3-V battery voltage, and

the clock distribution circuit to provide clock signals to the WEOR amplifier and the digital circuits on chip.

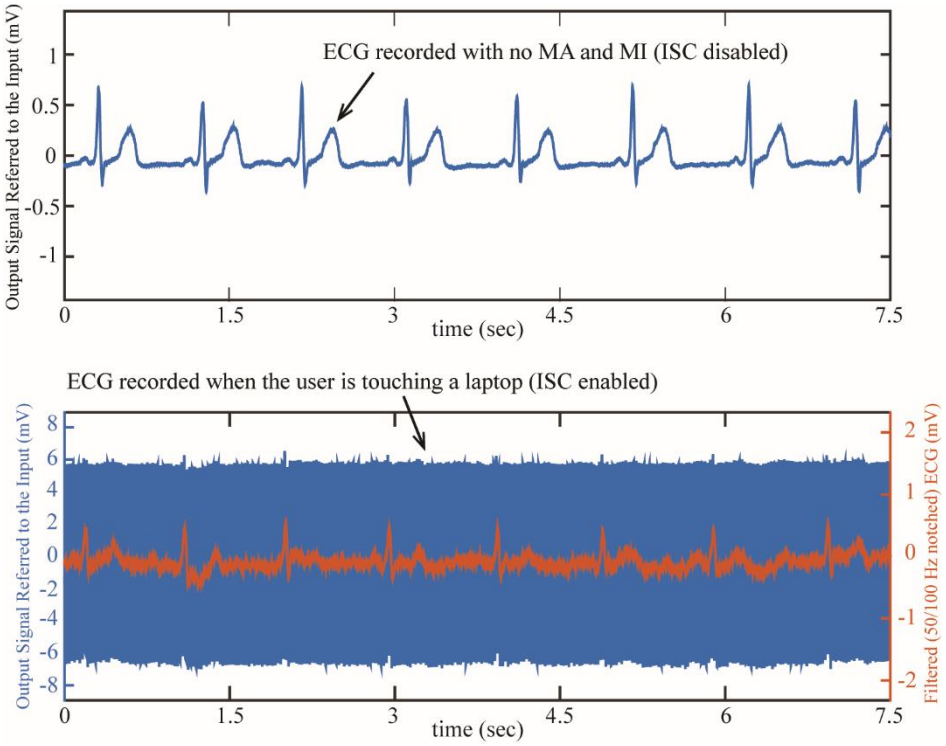


Figure 5: ECG Recording from the proposed ECG readout IC

The fabricated readout IC functions as we expected. The IC can record ECG amidst large interferences without saturating the signal chain. To demonstrate this, we use the IC to record ECG while the user was touching a laptop plugged into an electrical wall outlet. The result is shown in Figure 5. Despite the high gain of 70 dB, the IC was able to record the 12-mV_{pp} ECG-plus-interferences without saturating the signal (blue curve of the bottom figure), thanks to the use of the Interference Cancellation Circuit (ISC). Since no saturation occurs, all the information of the ECG is preserved, thus allowing us to post-process the recorded signal in the digital backend to recover the desired ECG. After filtering the recorded signal in the digital backend, we obtained the ECG shown in the red curve of the bottom figure. We can see that the filtered ECG is somewhat noisy. We finally found that the noise is due to the imperfect reconstruction scheme used in reconstructing the original signal from the nulling signal. Nevertheless, the QRS complex of the ECG waveform is still well preserved. Therefore, we reason that though the proposed interference cancellation architecture is not yet ready for clinical-quality recording due to it distorting the ECG waveform, the scheme can still be useful in some non-demanding applications such as in heart rate detection for fitness and sports.

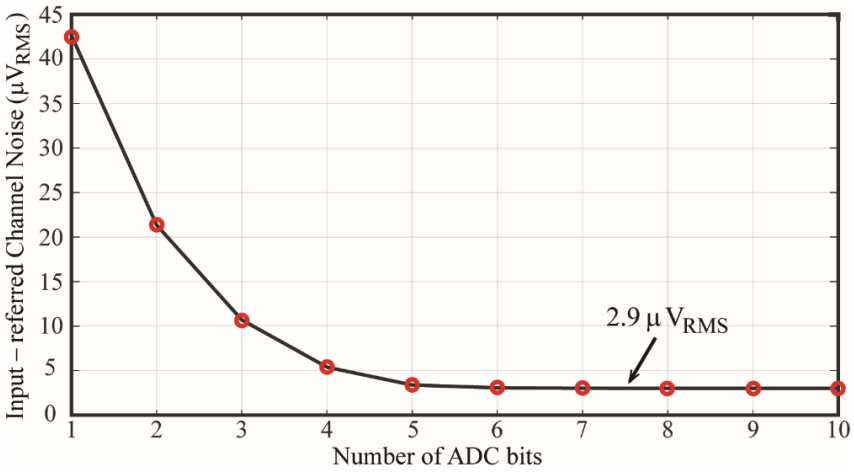


Figure 6: Input-referred noise of the readout system vs. the ADC's resolution

However, the finding above demands us to question our assumption about the need for interference cancellation. The distortion in the waveform is due to the imperfect reconstruction process of combining the nulling signal and the output of the WEOR amplifier. We have argued that we need this process when the interferences are large such as when the user is touching poorly-grounded electrical appliances. We finally figured out later that such large powerline interference occurs when the readout system has a low-impedance path from its ground to earth ground. However, in the real wireless recording environment, such scenario does not usually happen, as the readout system's ground and the earth ground are normally isolated. Therefore, in wireless ECG recording, the interference cancellation circuit may not be necessary. If that's the case, we can use our high-gain architecture to record the ECG without the worry of signal saturation, thanks to the very wide input range of the WEOR amplifier. With this architecture, we only need an ADC with a resolution of 7 bits. An example of ECG waveform recorded by the IC when the Interference Suppression Circuit is not used is shown in the top figure of Figure 5. To show that we only need the resolution of 7 bits in the ADC, we record the ADC's output and calculate the input-referred noise of the readout system while discarding the least significant bits from the output samples. The plot of the system's input noise vs. the number of ADC's bits is shown in Figure 6. We can see that when the number of ADC's bits is above 7, the noise floor remains relatively constant. But when the number of ADC's bits decreases below 6, the noise floor starts to increase. Hence, we can conclude that the ADC's resolution of higher than 7 bits is no longer necessary since the high gain of the amplification stage makes the ADC's noise negligible compared to the noise of the amplification stage when referred to the input.

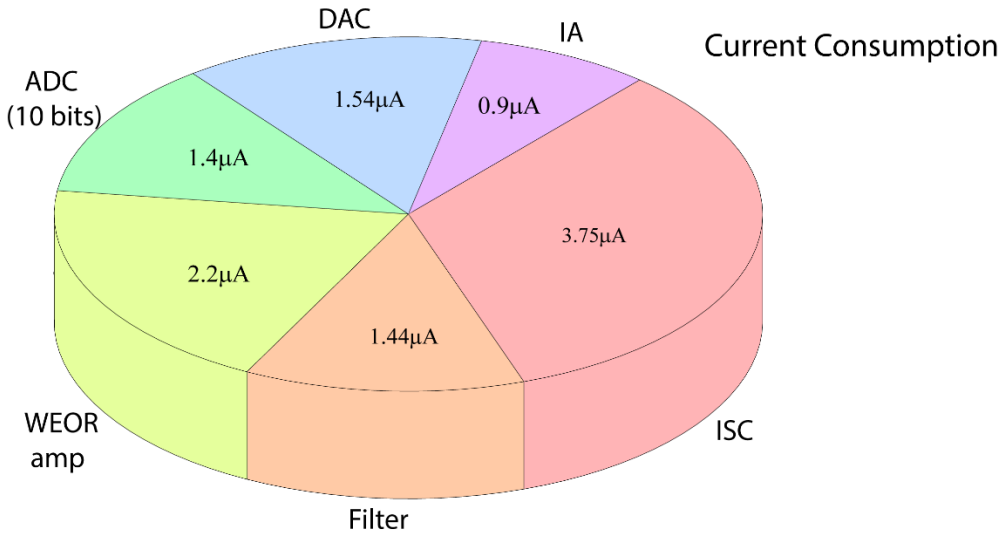


Figure 7: Current breakdown between the circuit blocks of the ECG readout IC

The proposed ECG readout IC consumes very low power. Figure 7 shows the power breakdown among the circuit blocks of the IC. We can see that the overall IC consumes a total current of 11.23 µA, 3.75 µA of which is dedicated to the operation of the ISC. Thus, if the ISC is not needed, the total current of the chip would amount to 7.48 µA, or an equivalent total power consumption of 9 µW from a 1.2-V supply. For further information on the design of this IC, please refer to [38].

The Micropower Motion Artifact Estimator

The next part of the results for this research involves the nulling signal generator in the architecture of Figure 2. The nulling signal generator in Figure 2 uses jus an integrator to create a highpass transfer function in the overall amplification chain. This method is only a crude way of removing motion artifacts (by just highpass filtering it out), and thus requires a reconstruction process to recover the original signal. This reconstruction process can also add distortion to the recorded signal unless the digital-to-analog converter used is of a very high resolution. Hence, to avoid this issue, we proposed the use of a low-power mixed-signal motion artifact estimator that can be used to estimate the motion artifact in the input signal accurately. This estimate can then be subtracted from the input signal near the front of the signal chain to prevent signal saturation if the input signal is to undergo large amplification. The architecture employs an adaptive filtering technique with low-power analog filters to create the nulling signal from the output of the IA. Thus, the output of the architecture is already in the analog form; therefore, a DAC is not required to create an analog nulling signal from its digital counterpart. Though its output is analog, the architecture employs a digital adaptation algorithm to avoid the use of large analog integrators in

adjusting the weights of the filters. This design choice results in a compact architecture, which makes it feasible to include the proposed estimator on chip.

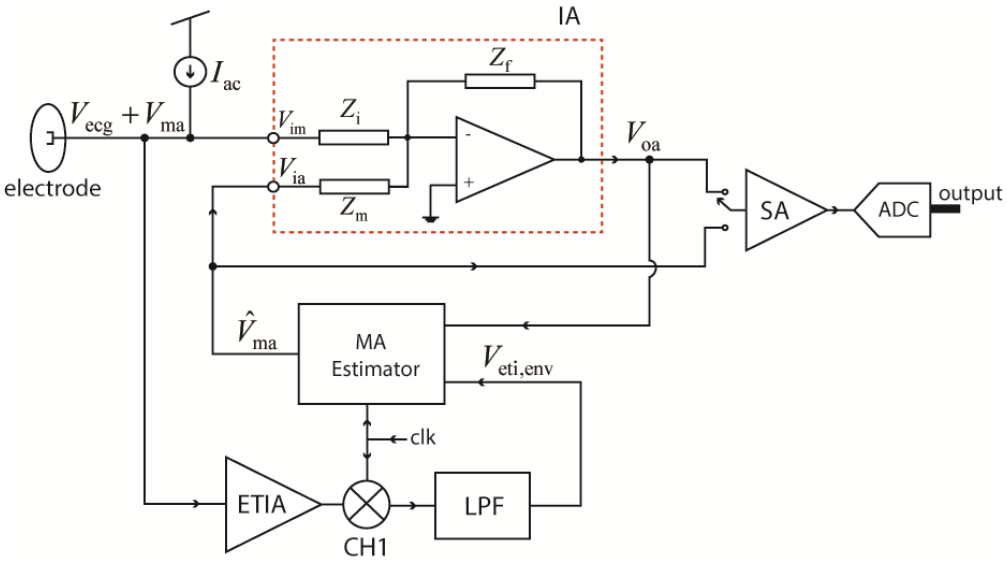


Figure 8: The architecture of the proposed motion artifact estimator

Figure 8 shows the concept of the proposed motion artifact estimator. The estimator produces its output V_{ma} by utilizing two sources of information: the output of the IA, V_{oa}, and the envelope of the electrode impedance information $V_{eti,env}$. For this scheme to work, we have assumed that the motion artifact in the recorded signal has a strong correlation to $V_{eti,env}$. Thus, the estimator should be able to use $V_{eti,env}$ to produce its output which is a reasonable estimate of the motion artifact in the recorded signal. To know whether the estimator's output is already optimal, we need to observe V_{oa} and let the adaptive circuit in the estimator adjust the weights of the analog filters until the mean-square-error of V_{oa} is minimized.

To obtain $V_{eti,env}$, we inject an AC current, I_{ac}, into the electrodes. The variation in electrode impedance due to motion then results in an amplitude-modulated waveform at the input of the IA, with the carrier frequency (modulating frequency) equal to that of the AC current source. To extract the envelope of this modulated signal, we amplify it with an electrode-impedance-information (ETI) amplifier and then demodulate the resulting signal with the chopper switch CH1. The demodulated signal is then lowpass filtered to provide the electrode impedance information into the estimator.

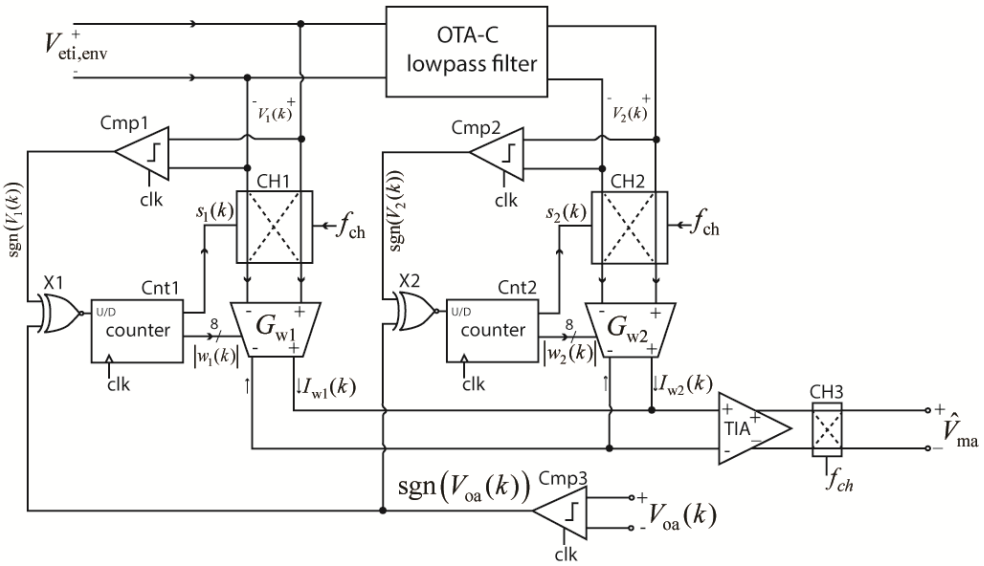


Figure 9: The architecture of the proposed MA estimator

In this part of the research, we have proposed for the MA estimator a mixed-signal architecture shown in Figure 9. The core of the estimator is the transconductance-capacitance (OTA-C) lowpass filter to create two basis functions for producing V_{ma}—the two basis functions are $V_1(k)$ and $V_2(k)$. The main function of the OTA-C lowpass filter is to create a relative phase shift between these two bases. To produce the output of the estimator, the architecture linearly combines the two bases with adjustable weights provided by the two weight transconductors G_{w1} and G_{w2}. To adjust the weights, we use an adaptive algorithm to adjust the effective transconductances of the weight transconductors in a discrete-time fashion—via the up-down counters Cnt1 and Cnt2. To minimize the flicker noise of the two transconductors, we also apply chopper stabilization through the chopper switches CH1-CH3. We then sum the output currents of the weight transconductors and pass the result to a transimpedance amplifier (TIA) to provide the output voltage V_{ma}.

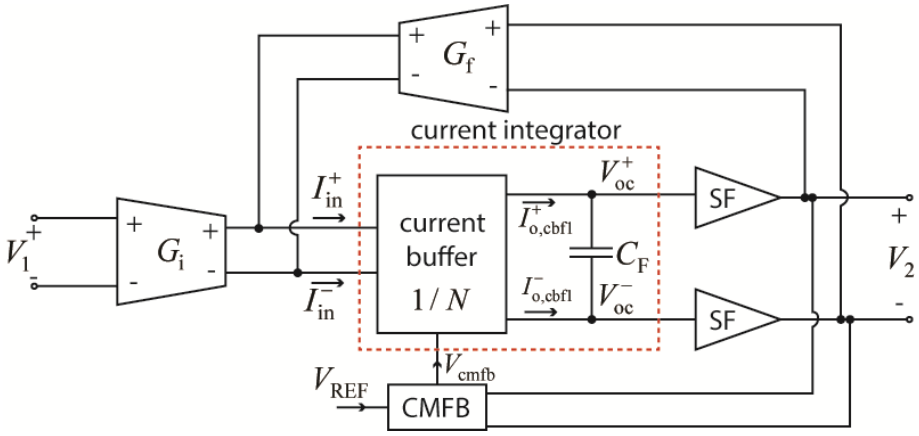


Figure 10: High-level schematic of the OTA-C lowpass filter

Figure 10 shows the high-level schematic of the OTA-C lowpass filter. It consists of the input OTA, G_{i}, and the feedback transconductor, G_{f}. The output currents of the two OTAs are then buffered by the current buffer, before charging the integrating capacitor C_{F}. The overall transfer function of the OTA-C lowpass filter is given by

$$\frac{V_{\mathrm{o}}}{V_{\mathrm{i}}} = \frac{G_{\mathrm{i}}}{G_{\mathrm{f}}} \frac{1}{1+s/\omega_{\mathrm{f}}},$$

where G_{i} and G_{f} are the effective transconductance of the input and the feedback OTA. The main challenge in the design of this architecture is that we need the cutoff frequency, ω_{f}, to be very small—on the order of less than $2\pi(10\ \mathrm{Hz})$—which makes the design of G_{i} and G_{f} OTA difficult since we need to bias them with a very small current. Therefore, we need to apply many degeneration techniques to reduce their effective transconductances—such as using the bulk input and the source degeneration—to reduce the effective transconductances of the two OTA without biasing them with excessively small bias currents.

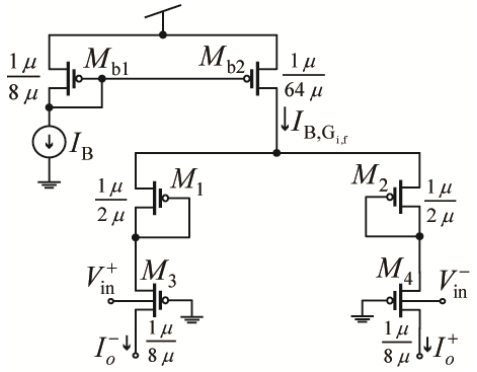


Figure 11: Schematic of the G_{i} and G_{f} OTAs

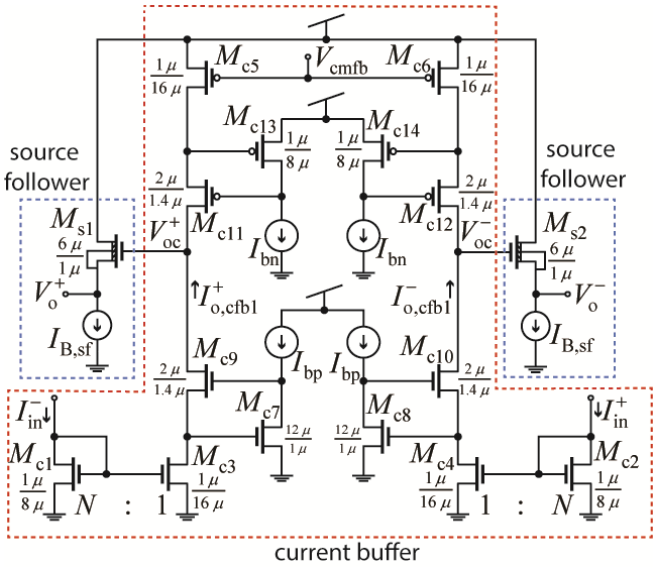


Figure 12: Schematic of the current buffer used in the OTA-C lowpass filter

Figure 11 shows the schematic of the G_i and G_f OTA while Figure 12 shows the schematic of the current buffer for the current integrator used in the OTA-C lowpass filter. Please note the use of the bulk inputs for the transistors M_3 and M_4 of the G_i and G_f OTAs, and the source degeneration provided by the diode-connected M_1 and M_2. To provide a very low cutoff frequency for the lowpass filter, the current buffer needs to provide a very high output resistance. Thus, we use the regulated-cascode technique to augment the output resistance of the current buffer in Figure 12. However, with all these techniques to prevent biasing the OTAs with very small bias current, we still observe large offset voltages in the OTA-C lowpass filter, which unfortunately limits the dynamic range of the overall architecture. If we are to use this architecture in a real ECG readout system, addressing the offset problem in the OTA-C lowpass filter should be one of the main design objectives.

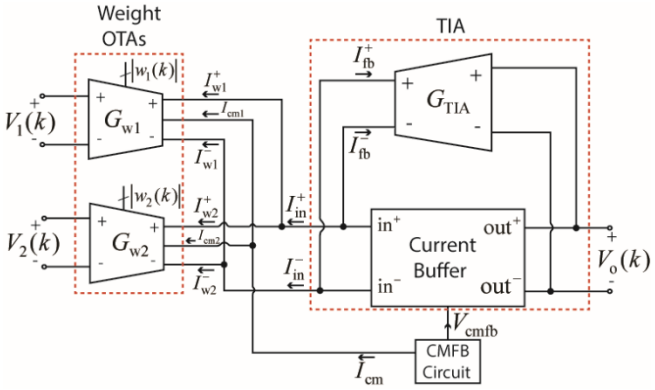


Figure 13: Overall schematic of the weight OTAs along with the TIA

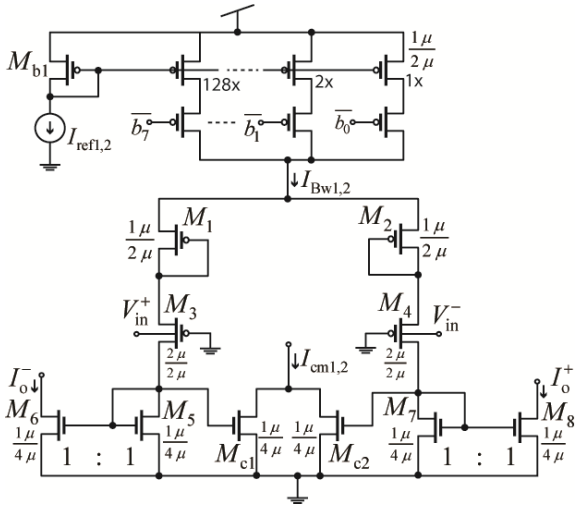


Figure 14: Schematic of the weight OTAs

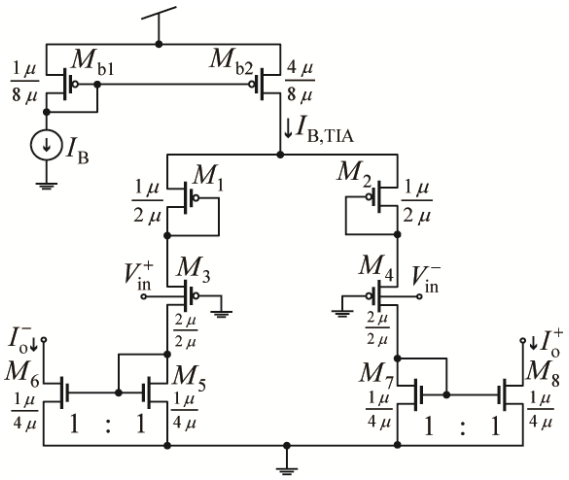


Figure 15: Schematic of the OTA in the TIA

Figure 13 shows the schematic of the weight OTAs along with the TIA for converting the weight OTAs' output currents into the estimator's output voltage. Shown in Figure 14, the architecture of the weight OTA is similar to those of the OTAs in the lowpass filter except that its current source is implemented with a current DAC for tuning the overall bias current, and, in turn, the weight provided by the OTA. Figure 15 shows the schematic of the OTA used in the TIA. In this research, a lot of our effort is put into theoretically analyzing the noise performance of the overall estimator. The details of those analyses are beyond the scope of this report and we refer the interested readers to [39] for further information.

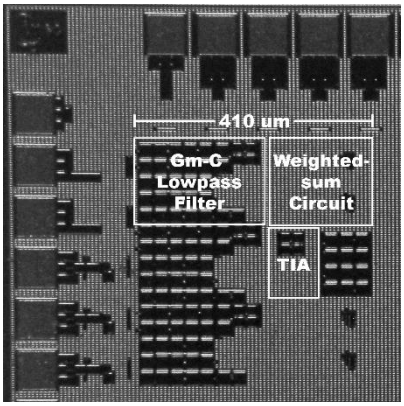


Figure 16: The chip micrograph of the motion artifact estimator

The proposed motion artifact estimator was fabricated in a standard 0.18-μm CMOS process from United Microelectronic Corp (UMC). The overall estimator occupies an active area of 0.11 mm^2, whose micrograph is shown in Figure 16. The estimator operates from a supply voltage of 1 V and consumes a total bias current between 2.4 μA and 3.2 μA depending on the weight setting.

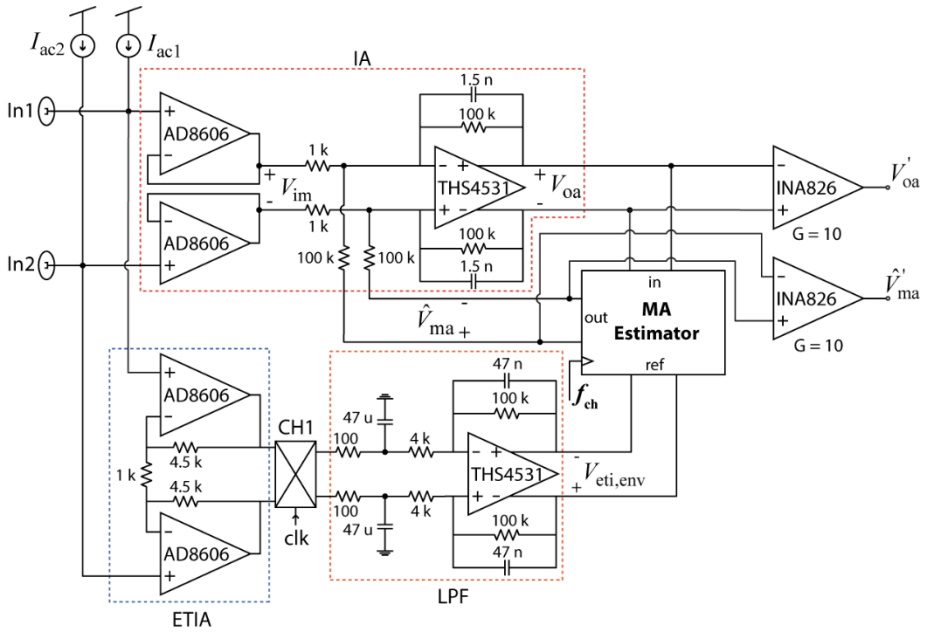


Figure 17: Schematic of the ECG readout emulator

To show the operation of the estimator in the real setting, we have built an ECG readout emulator from off-the-shelf components with our estimator chip on a printed circuit board (PCB) as shown schematically in Figure 17. The IA consists of two unity-gain voltage followers (AD8606 from Analog Devices) to provide high-impedance buffering from the electrodes, In1 and In2, and a summing amplifier built from the opamp THS4531 from Texas Instruments Inc. We built the ETI amplifier using a two-opamp topology (AD8606). The chopper switch CH1 is built from off-the-shelf MOS switches. The lowpass filter is built with a standard RC topology from the opamp THS4531. The signals of interest for this experiment are V_{im} (the input voltage into the IA), V_{ma} (the output of the MA estimator), and V_{oa} (the output voltage of the IA). For correct operation, V_{ma} should cancel with the motion artifact in V_{im} such that V_{oa} is virtually free of motion artifacts.

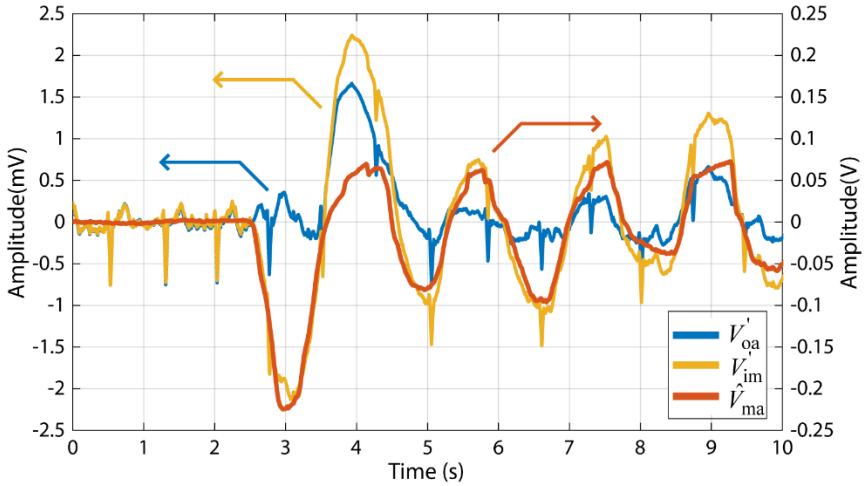
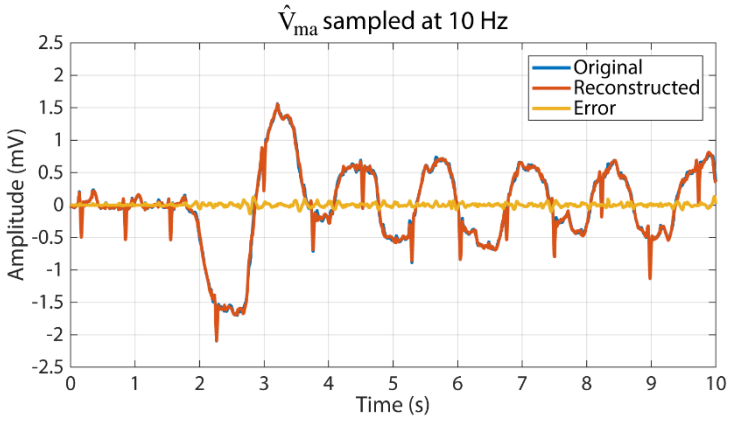
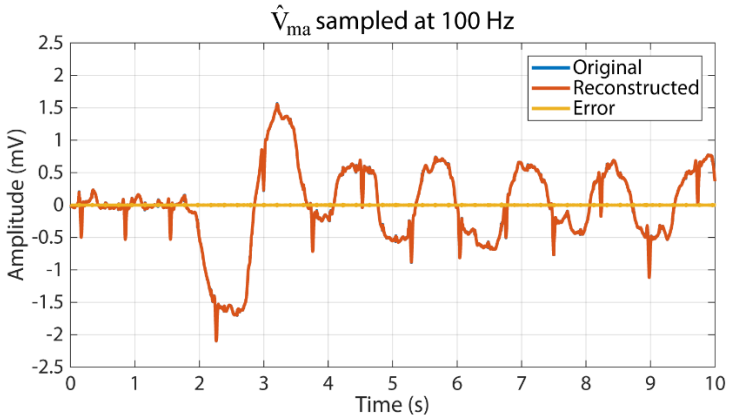


Figure 18: Measured results from the ECG emulator board

Figure 18 shows the buffered versions of the three signals of interest when the user pushes on the recording electrodes, starting from t=2 seconds onward, to induce motion artifact in V_{im}. We can see that V_{ma} tracks V_{im} quite well such that motion artifact in V_{oa} is suppressed.



(a)



(b)

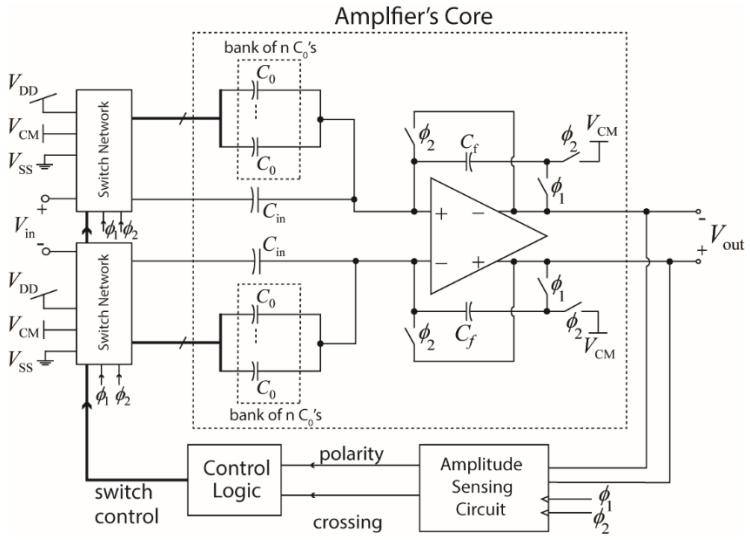
Figure 19: Waveforms showing the reconstruction process in the case of low correlation between V_{ma} and the motion artifact in the input signal.

However, we have found from this study that how well the architecture suppresses motion artifact depends largely on the correlation between the electrode impedance information and the motion artifact in the recorded signal. If the correlation between the two signals are low, it is impossible for the estimator to produce V_{ma} to cancel with the motion artifact in the recorded signal. In this case, V_{ma} will introduce undesirable noise and distortion into the recorded signal, causing information loss. To prevent this scenario, we allow for the reconstruction of the original signal. To do so, we propose that the readout system digitizes V_{ma} and also report off-chip, such that we can use the digitized V_{ma} and V_{oa} to recover the original recorded signal in the digital backend. Since all the information is preserved, we can apply other sophisticated digital processing techniques to remove motion artifacts from the reconstructed data. Figure 19 shows

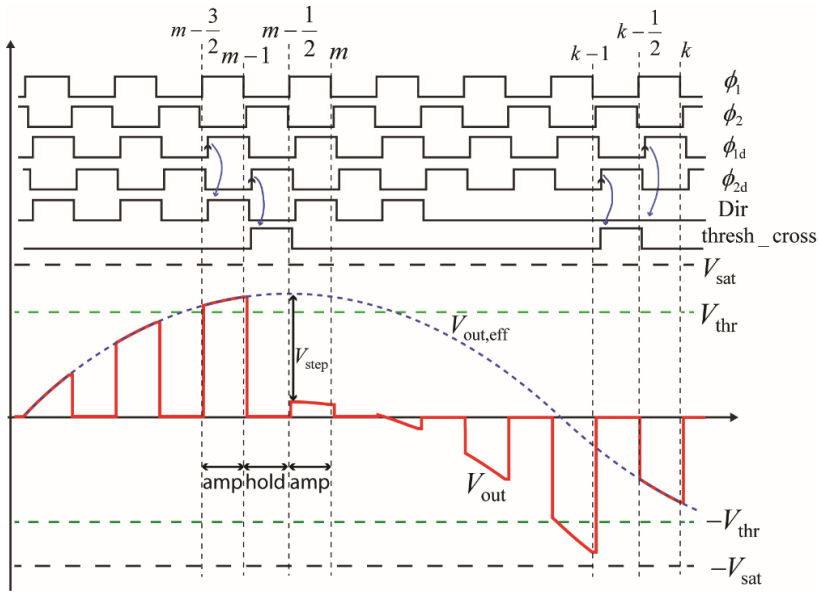
such reconstruction concept for the's sample rates of 10 Hz and 100 Hz. We can see that for both cases, the reconstructed signals track the original signals quite well, but the high sample rate on V_{ma} consistently produces lower mean-square error between the original and reconstructed signals. Indeed, the reconstruction error from the 100-Hz sample rate case is only 3.27 μV_{rms} when referred to the input of the readout system. This noise level is on the same level as the noise introduced by the front-end IA. Thus, we can conclude that the proposed scheme can help lower the dynamic range in ECG recording even with the presence of large motion artifacts. Even when the correlation between the electrode impedance information and the motion artifact in the recorded signal is low, our proposed scheme also provides a safety measure in preventing the corruption of the recorded signal.

The Wide-Effective-Output-Range Amplifier

This part of the research focuses on the wide-effective-output-range amplifier (WEOR amplifier in Figure 3). The WEOR amplifier is at the heart of our proposed high-gain architecture as it allows for the use of a very high gain in the amplification chain without the risk of signal saturation. We have explained the design of the WEOR amplifier and presented its detailed measured results in [40]. In this report, we only summarize the important concepts of this crucial circuit block.



(a)



(b)

Figure 20: (a) The overall schematic of the WEOR amplifier (b) Timing diagram showing the signal-folding operation.

The main objective of the WEOR amplifier is to provide an additional gain to the amplification stage—provide an additional gain of 24 dB (16 V/V) for a total of 70 dB gain of the amplification stage—while preventing signal saturation. To do so, the WEOR amplifier utilizes a discrete-time signal folding technique; this technique uses a feedback network to monitor the amplifier's output level and, if it exceeds specific voltage thresholds, fold it back to the middle of the rail. As a result of this folding, the amplifier's output level will stay within a pre-defined range near the middle of the rail, without reaching the saturation level dictated by the voltage headroom of the output stage. Figure 20(a) shows the overall schematic of the WEOR amplifier, which consists of the amplifier's core, the feedback monitoring network (the amplitude sensing circuit and the control logic), and the input switch networks. The amplifier's core is based on the standard switched-capacitor gain circuit normally used in conventional switched-capacitor circuit design. The amplifier has its gain determined by the capacitance ratio C_{in}/C_f. However, it also incorporates the offset capacitor banks—those consisting of C_o' s—for adding offset voltages into the input signal to effectively fold the output voltage to the desired level. The operation of the WEOR amplifier can be understood by the timing diagram in Figure 20(b). When the clock signal ϕ_2 is high, the amplifier is in the hold phase, with the information of the output voltage V_{out} stored in the feedback capacitors's. During this hold phase, the control logic adds appropriate offset into the offset capacitor banks based on the state of the amplifier. Once the clock signal ϕ_1 goes high, the amplifier enters the amplifying phase, and the amplifier amplifies the input

signal V_{in} to produce V_{out}. During the amplifying phase, the amplitude sensing circuit senses whether the output V_{out} has exceeded either of the threshold levels ($\pm V_{\text{thr}}$). If so, the control logic adjusts the state of the amplifier such that, in the next amplifying phase, an appropriate offset voltage is added to the input signal to constrain V_{out} to within the threshold levels. To recover the original signal, we keep track of the amplifier's state at every folding instant. Since a fixed value of offset voltage is either added or subtracted from V_{out} at every folding instant, we can use the information on the amplifier's state to reverse the operation to produce the original V_{out} from its folded counterpart.

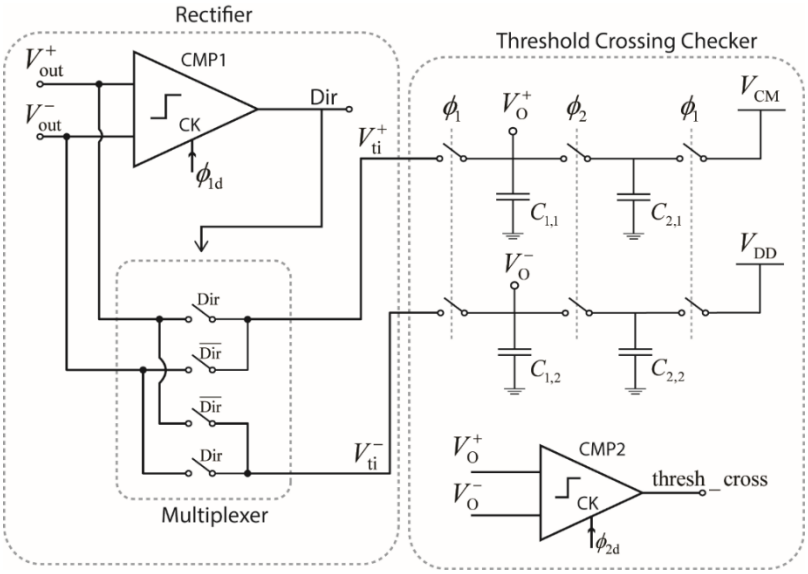


Figure 21: Schematic of the amplitude sensing circuit

Figure 21 shows the schematic of the amplitude sensing circuit, which consists of a rectifier and a threshold crossing checker. The rectifier is responsible for producing the output $V_{\text{ti}}^{+} - V_{\text{ti}}^{-}$ which is the absolute value of V_{out}. Then the threshold crossing checker determines whether $V_{\text{ti}}^{+} - V_{\text{ti}}^{-}$ has exceeded the threshold value or not. If so, it flags the signal thresh_cross to the control logic to configure the amplifier into an appropriate state. Note that the amplitude sensing circuit performs all of its computations using a switched-capacitor network and a dynamic comparator, thus consuming no bias current. This implementation choice results in a very low power consumption for the amplitude sensing circuit.

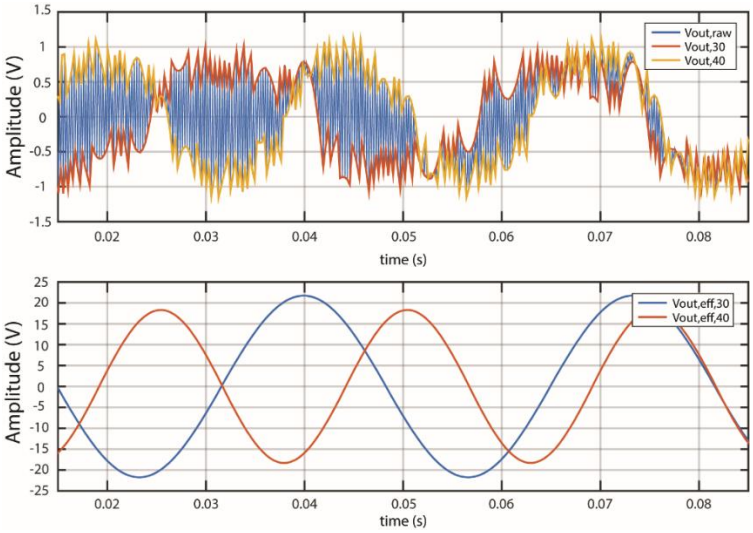


Figure 22: Measured results from the WEOR amplifier

The WEOR amplifier was fabricated as part of the ECG readout system in a standard 0.18-μm CMOS process from UMC. The amplifier occupies a total active area of 0.254 mm^2. Operating from a 1.2-V supply voltage, the amplifier exhibits a gain of 17.8 V/V (instead of its nominal value of 16 V/V) due to inaccuracies in the layout modeling of our process. To test the functionality of the WEOR amplifier, we feed two rail-to-rail input signals as input into the amplifier and record its output, one signal a sinusoidal waveform at 30 Hz and the other at 40 Hz. The top pane of Figure 22 shows the raw output waveform of the amplifier, while the red and yellow curves indicate parts of the waveforms corresponding to the 30-Hz and 40-Hz input signals, respectively. After using the information on the state of the amplifier to reconstruct the original input, we obtain the plot in the bottom pane of Figure 22. We can see that the two reconstructed outputs have amplitudes of approximately 40 V_{pp}, which are much larger than the 2.4 V maximum differential output swing of the WEOR amplifier, thanks to the use of the signal-folding technique.

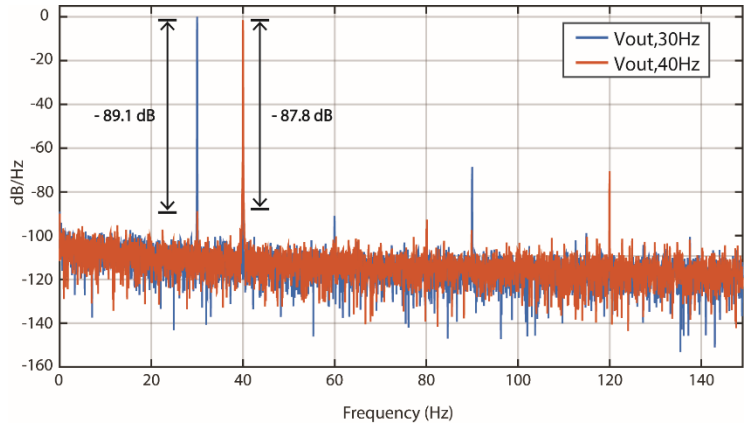


Figure 23: Power spectrum of the 30-Hz and 40-Hz output waveforms showing their crosstalk

Having a large amplitude is practically useless if the output waveform is highly distorted. In other words, we must ensure that the WEOR exhibits excellent linearity if it is to be useful in

ECG recording applications. To test the linearity of the WEOR amplifier, we analyzed the two reconstructed output signals in the frequency domain and obtained the power spectral density plots as shown in Figure 23. Also indicated on the plots are the levels of crosstalk from one input to the other. We can see that the crosstalks are on the order of -90 dB, thus indicating that the amplifier can amplify two signals without having them interfere with each other.

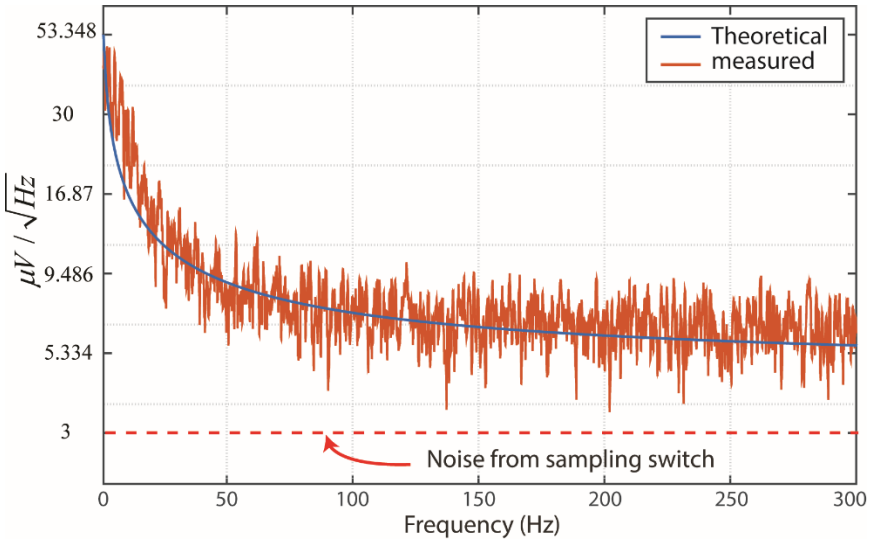


Figure 24: Measured input-referred noise power spectral density of the WEOR amplifier

As a significant part of this research, we spent a considerable effort in theoretically analyzing the noise performance of the WEOR amplifier. The detail of the analysis is beyond the scope of this report and we refer interested readers to [40]. Nevertheless, we have shown in our measurement result that our theoretical noise analysis matches very well with the measured result. Figure 24 shows the power spectral density of the WEOR amplifier's input-referred noise along with the result obtained from our theoretical analysis. Integrating under the red curve yields a total input-referred integrated noise of 143.6 μV_{rms}. Such input noise level indicates that if we are to precede the WEOR amplifier with an IA whose gain is around 200 V/V, the WEOR amplifier's noise referred to the input of the system would be around 0.7 μV_{rms}, which is less than the input-referred integrated noise of the IA.

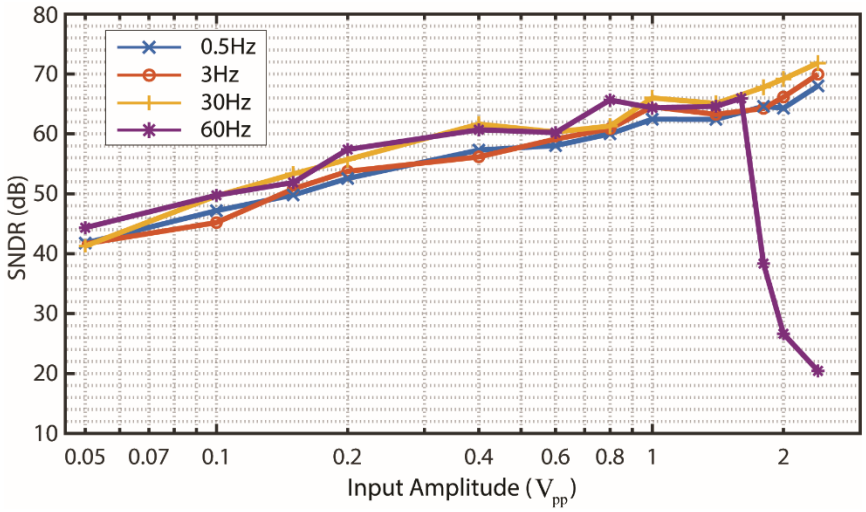


Figure 25: SNDR as a function of the input amplitude at various frequencies of the input

Though the discrete-time folding technique is very accurate and can be implemented with low-power consumption, it has one important inherent limitation: speed. Since the technique uses a clock, we must ensure that the WEOR amplifier's output do not change too fast and cross a threshold in one clock period. This scenario can happen for fast input with large amplitude. Fortunately, the interferences into the ECG readout system are normally slow signals: the motion artifact has energy concentrated below 5 Hz while the powerline interference's frequency is at 50 or 60 Hz. Therefore, if these interferences are not extremely large, the WEOR amplifier should be fast enough to constrain its output to within the threshold levels such that no signal saturation occur. We tested the amplifier's performance for the input frequencies of 0.5 Hz, 3 Hz, 30 Hz, and 60 Hz. For a given frequency of the input, we increased its amplitude and measured the signal-to-noise-plus-distortion (SNDR) of the output. Figure 25 shows the resulting SNDR for this measurement. We can see that for the test frequencies below 60 Hz, the SNDR (dB) is approximately a linear function of the logarithm of the input amplitude up to the input amplitude of as high as 2.4 V_{pp}. This indicates that, for these input frequencies, the amplifier behaves linearly for the whole rail-to-rail input range. However, when the input frequency is 60 Hz (the frequency of the powerline interference), the SNDR falls sharply when the input amplitude reaches 1.8 V_{pp}. This happens because the amplitude sensing circuit cannot operate fast enough in folding the output signal away from the saturation level of the WEOR amplifier's output stage. Fortunately, such input saturation level occurs when the 60-Hz signal is as large as 1.8 V_{pp}, a level much larger than the maximum powerline interference expected in our system.

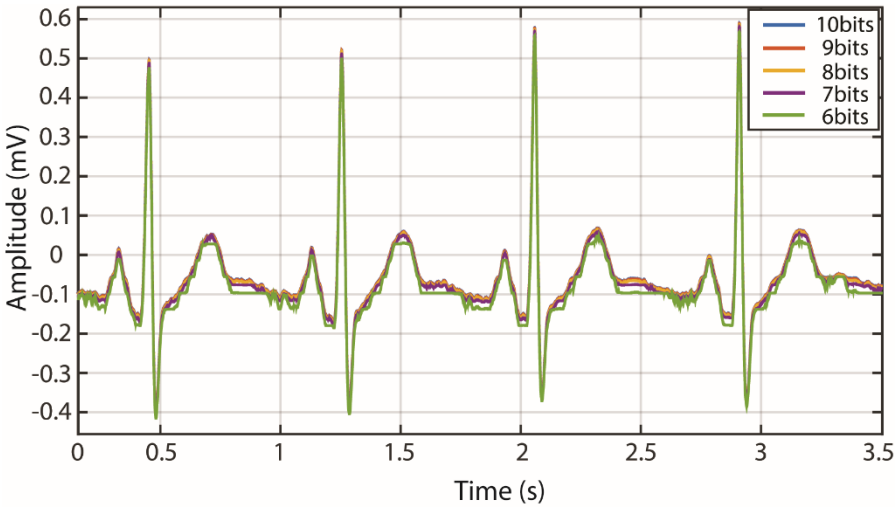


Figure 26: The ECG waveforms as digitized by the ADC at various resolutions.

The major benefit of the WEOR amplifier is to allow the very high gain in the amplification stage without the risk of signal saturation. Such high gain helps relax the resolution requirement of the ADC that follows the amplification stage. As a result, an ADC of only 7-8 bit of resolution is required for digitizing the WEOR amplifier's output signal. To illustrate this concept, we recorded an ECG from standard Ag-AgCl electrodes using the ECG readout IC discussed in [38]. We then amplified the ECG in digital with a gain of 200 and fed the result to the WEOR amplifier's input and then digitized its output signal. Then, we discarded specific numbers of the least significant bits to mimic the digitization by ADCs of lower resolution. Figure 26 shows the resulting digitized waveforms referred to the input of the readout system by various ADC's resolutions. We can see that the ECG waveforms from the digitization at higher than 7 bits are nearly indistinguishable from each other, thus indicating that increasing the resolution beyond 7-bits provides negligible SNR improvement.

The ECG Readout System Prototype

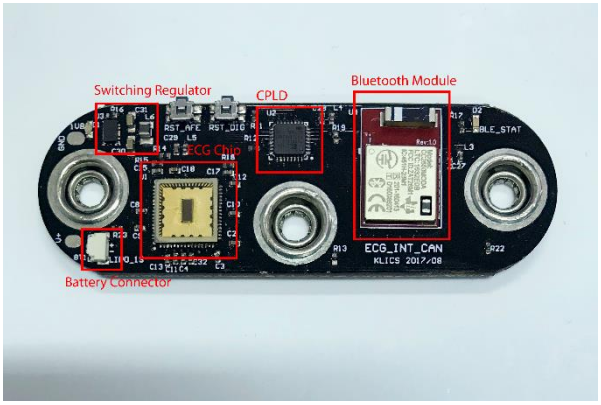


Figure 27: A battery-powered wireless ECG readout system.

To illustrate the functionality of the ECG readout IC in real recording environment, we have built a battery-powered wireless ECG readout system on a PCB with our ECG readout IC at its core. Figure 27 shows our readout system. The system can be attached directly to the chest of the user and can transmit the recorded data wirelessly to a receiver at the remote computer. We have demonstrated that the system functions correctly. We have exhibited this system at งาน 25 ปี สกว: สร้างคน สร้างความรู้ สร้างอนาคต at Siam Paragon on 25-26 August 2017. The atmosphere during the exhibition of our system is shown in Figure 28.

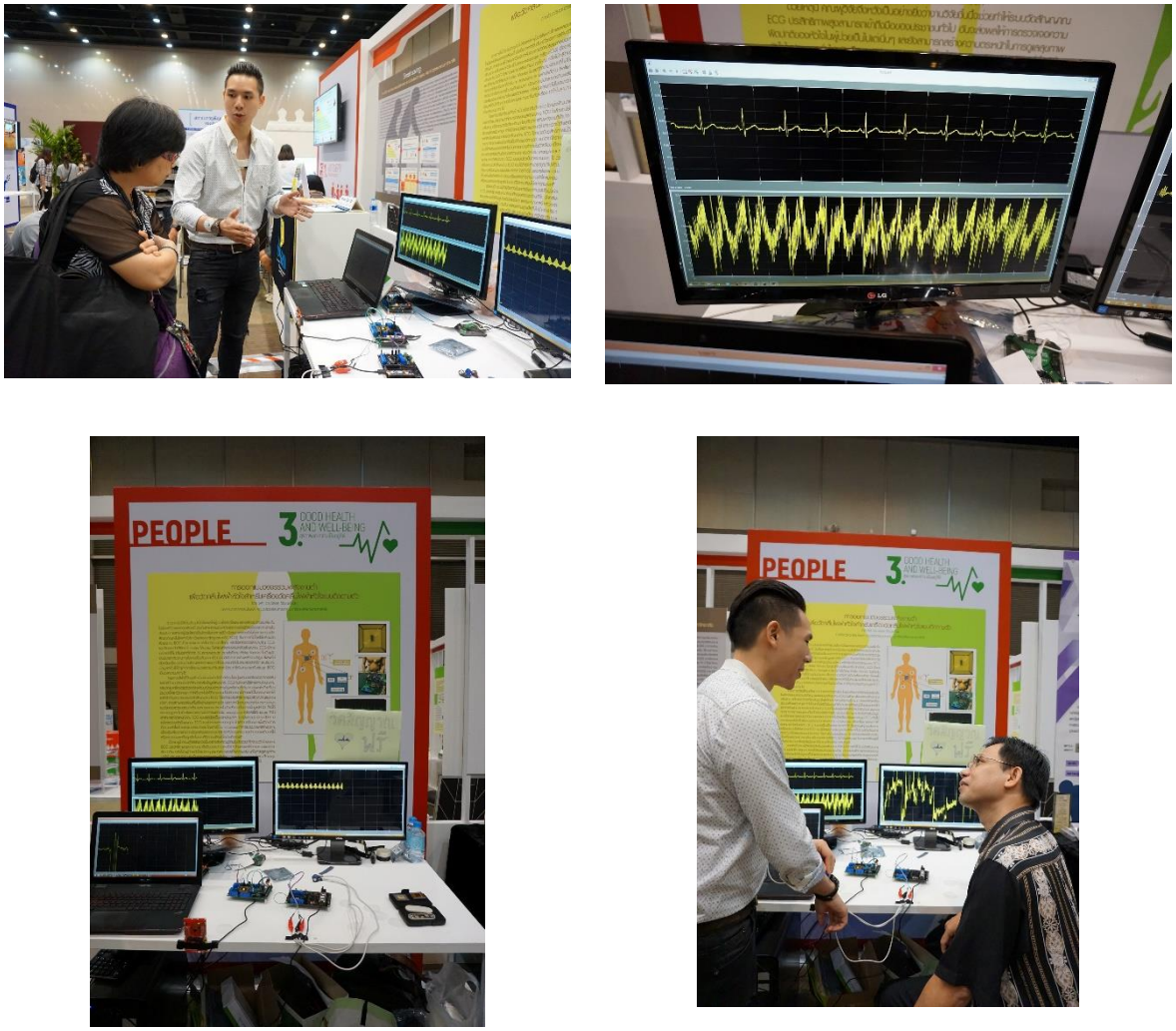


Figure 28: The exhibition of the wireless ECG recording system at *งาน ปี สกว 25: สร้างคน สร้างความรู้ สร้างอนาคต* at Siam Paragon on 25-26 August 2017

Conclusion

In this research, we have designed, built, and tested a wide-dynamic-range ECG signal-conditioning IC suitable for use in battery-powered wireless active-electrode ECG readout systems. The IC consists of many circuit building blocks, each of which can be a research project on its own. As part of this research, we delved into the design and analysis of each circuit block to study its behavior and optimize its performance. The first topic we dealt with is the study of the interference cancellation architecture to reject large motion artifacts and powerline interferences. Though being able to reject those interferences with large amplitudes, we ran into the problem of signal distortion due to the circuit nonidealities of the feedback cancellation network. Unless this distortion problem is solved, such cancellation structure is not yet suitable for use in clinical applications. The other parts of the project involve the design and analysis of the motion artifact estimator and the WEOR amplifier. Though promising, the motion artifact estimator still faces many problems of circuit nonidealities at very low bias current—i.e., the offset voltage that limits the overall dynamic range of the estimator. Nevertheless, the discovery of these problems helps us pave the way for the improvement of such architecture for its future use in real ECG readout systems. The work on the WEOR amplifier is the most promising among all the subprojects. We have demonstrated that, with the help of the WEOR, we can use a very high gain in the amplification stage without the worry of signal saturation. Such high gain helps relax the resolution requirement of the ADC, thus reducing the power consumption of the overall readout system. The WEOR amplifier is very robust and also exhibits excellent linearity, which is an important attribute if it is to be used in a commercial-grade ECG readout system. Finally, we have integrated the ECG readout IC into a wireless ECG readout system, which can record ECG from dry electrodes and send the recorded data wirelessly to a remote host. Currently, we are in the last stage of the manuscript preparation on the design of the front-end instrumentation amplifier and its use in the wireless ECG readout system. The manuscript will be sent out for review within the next few weeks.

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Outputs

1. C. Ratametha, C. Buaban, B. Pholpoke, T. Limpisawas, P. Prasopsin, S. Tepwimonpetkun, et al., "A low-power high-input-impedance 70-dB gain ECG readout system with high interference tolerance," in The 2018 IEEE Biomedical Circuits and Systems Conference, Cleveland, Ohio, USA, 2018.
2. B. Pholpoke, T. Songthawornpong, and W. Wattanapanitch, "A Micropower Motion Artifact Estimator for Input Dynamic Range Reduction in Wearable ECG Acquisition Systems," IEEE Transactions Biomedical Circuits and Systems, vol. 13, pp. 1021-1035, 2019.
3. C. Ratametha, S. Tepwimonpetkun, and W. Wattanapanitch, "A 2.64-uW 71-dB SNDR Discrete-Time Signal-Folding Amplifier for Reducing ADC's Resolution Requirement in Wearable ECG Acquisition Systems," IEEE Transactions Biomedical Circuits and Systems, vol. 14, pp. 48-64, Feb 2020 2020.

Appendix A

A Low-Power High-Input-Impedance 70-dB Gain ECG Readout System with High Interference Tolerance

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***Abstract*—This paper presents a low-power high-input-impedance electrocardiogram (ECG) readout system for recording from high-impedance electrodes. To minimize power, the system employs large amplification to minimize the required resolution of the analog-to-digital converter (ADC)—with a gain of 70 dB, only 7-bit ADC is required to not degrade the overall signal-to-noise ratio. Such a high gain is made feasible by a discrete-time signal-folding amplifier and an interference suppression circuit (ISC). Fabricated in a 0.18-μm CMOS process and operating from a 1.2-V supply, the system achieves an input-referred noise of 2.9 $\mu\mathrm{V_{rms}}$, while consuming 7.1 μW of power. With the ISC enabled for strong interference cases, the system can tolerate upto 100 $\mathrm{mV_{pp}}$ of interference while consuming 13.1 μW of power.**

***Index Terms*—ECG readout system, high-impedance electrodes, interference suppression feedback, signal-folding amplifier.**

I. Introduction

Recently, wearable electrocardiogram (ECG) readout systems are being developed for use in chronic non-invasive remote monitoring of the heart. Once such systems come into widespread use, they can act as an important platform for monitoring various heart conditions, giving patients with limited means accesses to high-quality personal cardiac diagnosis tools. Nevertheless, for such systems to be feasible as real wearable devices, they must deliver quality ECG recording, be very easy and comfortable to use, and consume very low power to eliminate the nuances of frequent battery recharging; this means that the ECG recording circuitry must be robust against all forms of interferences—i.e., the motion artifacts (MA) due to the movement of electrodes with respect to the skin and the 50/60 Hz mains interference (MI)—and be capable of recording from high-impedance (high-Z) electrodes (dry/non-contact electrodes) for maximum user's comfort.

Compared to the conventional Ag-AgCl gel electrodes, high-Z electrodes are very susceptible to MA and MI, which increase the input dynamic range of the recording system. To prevent signal clipping in the cases of strong interferences, most existing systems employ low overall gains, which, to prevent the quantization noise from degrading the signal-to-noise ratio (SNR), necessitates the use of high-resolution analog-to-digital-converters (ADCs), consequently resulting in higher overall power consumption. For examples, [1], [2] employ $\Delta\Sigma$ ADCs with 13.5b and 18b of resolutions, while consuming 50 and 83.6 μW of power, respectively. Other systems that employ low gains and low-resolution ADCs [3], [4] to minimize power achieve high input-referred noise, thus degrading the systems' sensitivities.

It is revealing to note that, on average, most recording systems infrequently encounter strong interferences—strong MA and MI may occur during the user's movements or his touching appliances plugged to poorly-grounded outlets. Thus, specifying the gain and ADC's resolution for such worst-case scenarios is suboptimal and wasteful of power. Instead, the overall power consumption can be much reduced if the system is designed for the normal scenarios (with small interferences) but is equipped with capabilities to handle strong interferences as needs arise.

In this paper, we present an ECG readout system which employs a very high gain (70 dB) and a low-resolution ADC, without significantly degrading the overall SNR. To prevent signal clipping due to the high gain, we employ two techniques: first, the signal-folding technique keeps the physical output level of the amplification stage within the ADC's input range, even though the actual output level may well exceed the supply rails; second, to handle the situations of strong interferences, the system incorporates an interference suppression circuit (ISC) to suppress interferences near the input of the system before the signal undergoes large amplification. Combining the two techniques ensure that, most of the time, the system operates in the most energy efficient fashion, while still capable of handling large interferences if they arise.

II. System Design Considerations

In this work, we design the readout system to have an input-referred noise below 3 $\mu\mathrm{V_{rms}}$ in a 150-Hz bandwidth—still well below the specification by The Association for The Advancement of Medical Instrumentation (AAMI) [5]—while being capable of recording 1-2 $\mathrm{mV_{pp}}$ ECG. To relax the ADC's resolution requirement, we employ the overall gain of 70 dB before the ADC. The 3 $\mu\mathrm{V_{rms}}$ system's input-referred noise will be amplified to 9.6 $\mathrm{mV_{rms}}$ at the ADC's input. Hence, for a differential full-scale voltage of 2.4 V, an effective-number-of-bits (ENOB) of only 6.2 suffices to keep

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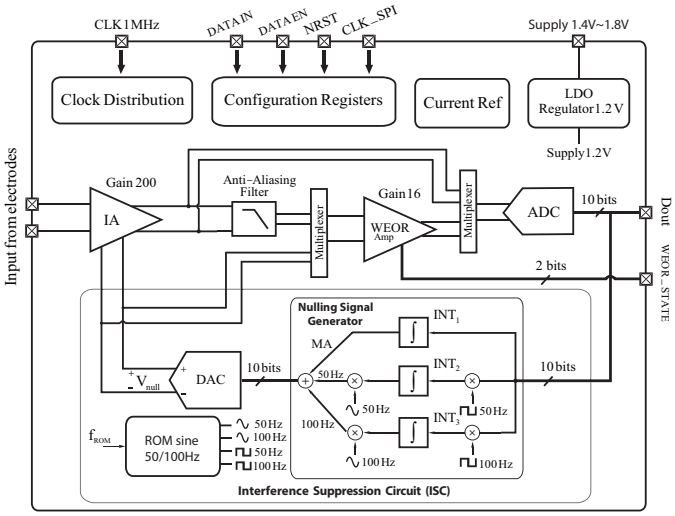


Fig. 1. High-level schematic of the proposed ECG readout system.

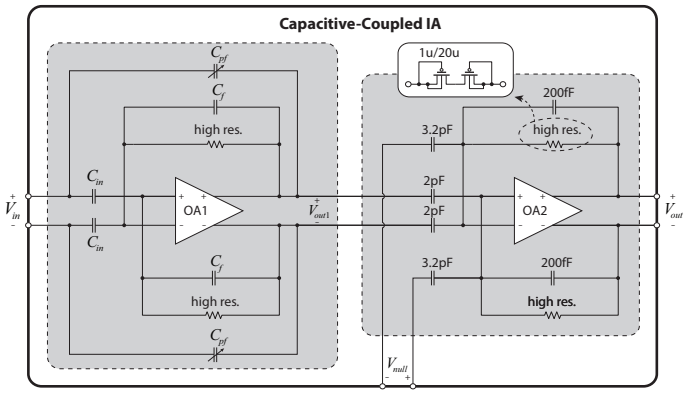


Fig. 2. Schematic of the instrumentation amplifier (IA)

the overall noise of the ADC below such value, thus resulting in a much simpler and more energy-efficient ADC.

Nevertheless, strong interferences determine the maximum input amplitude that the system must accommodate. To understand the worst-case scenario, we constructed a simple 3-wire ECG recording system from a commercially-available instrumentation amplifier (IA) [6] and used it to record ECG from dry electrodes made in-house from metallic buttons, each having a surface area of 1.5 cm^2. We found that pushing on one of the sensing electrodes can result in MA as large as tens of millivolts. We also estimated the worst-case MI by recording ECG when the user was touching a laptop plugged into an outlet without proper ground connection. We found that the recorded MI referred to the input is much larger than the desired ECG ($\approx 16\ \mathrm{mV_{pp}}$/1 $\mathrm{mV_{pp}}$) and that the recorded MI not only consists of the fundamental but also strong 2^{nd} harmonic. Such strong MI occurs despite the 120-dB common-mode-rejection-ratio (CMRR) of the IA, suggesting that it is due to mismatch in electrode impedance converting the common-mode MI into a differential-mode input into the IA. Hence, to handle such worst case, we ensure that our system can handle differential interferences with a combined amplitude of upto 100 $\mathrm{mV_{pp}}$.

III. Overall System

Fig. 1 shows the architecture of our proposed ECG readout system. To achieve a gain of 70 dB, the amplification chain is divided into two stages: i) the instrumentation amplifier (IA) with an overall gain of 46 dB, and ii) the signal-folding wide-effective-output-range amplifier (WEOR amp) with a gain of 24 dB. Between the two stages lies a lowpass filter for anti-aliasing. The system contains a 10-bit ADC—it will be shown in Section VI that much lower resolution can be used without significantly degrading the SNR—to digitize the WEOR amp's output. The WEOR amp also reports its state (WEOR_STATE) to allow the digital backend to reconstruct the actual signal from its folded output. In normal operations (without strong interference), the IA-WEOR-ADC chain suffices to amplify the ECG input without causing signal clipping at any point in the signal chain.

In cases of strong interferences, the system can enable the Interference Suppression Circuit (ISC) to generate the cancellation signal V_{null} to suppress MA and MI near the input of the system. The ISC takes as input the digitized output of the IA by bypassing the WEOR amp directly into the ADC to avoid having to reconstruct the folded signal. At the heart of the ISC is the nulling generator that generates all the components of V_{null}. The generator consists of three paths; the first path (MA), for suppressing MA, contains an integrator (INT_1) to establish a highpass corner at 2 Hz in the overall transfer function of the readout system; the other two paths (50 Hz/100 Hz) generate two sinusoidal signals to suppress the 1^{st} and 2^{nd} harmonics of MI. The two sinusoidal signals are generated with the direct-digital-synthesis (DDS) technique and least-mean-square (LMS) adaptive filtering as described in [7]. All the three components are then added and converted into V_{null} via a 10-bit digital-to-analog converter (DAC). To avoid distorting the ECG, V_{null} is also digitized and reported off-chip for reconstructing the original signal in the digital backend.

IV. The Instrumentation Amplifier

The IA is designed to achieve $> 1\ \mathrm{G\Omega}$ of input impedance at frequencies upto 150 Hz. Fig. 2 shows the schematic of the IA, which is divided into two stages, the first providing a gain of 26 dB and the second providing a gain of 20 dB. Each stage employs the capacitive-coupling technique to achieve high intrinsic input impedance at low frequencies and to block electrode offset. To suppress interferences, the 2^{nd}-stage IA, which operates as a summing amplifier, receives the cancellation signal $\mathrm{V_{null}}$ from the ISC. The 26-dB in-band gain of the 1^{st}-stage IA's allows for as large as 100 $\mathrm{mV_{pp}}$ interferences at the input without causing output clipping, which can then be suppressed with V_{null} of only 1.25 $\mathrm{V_{pp}}$, a comfortable output swing for the DAC in the ISC.

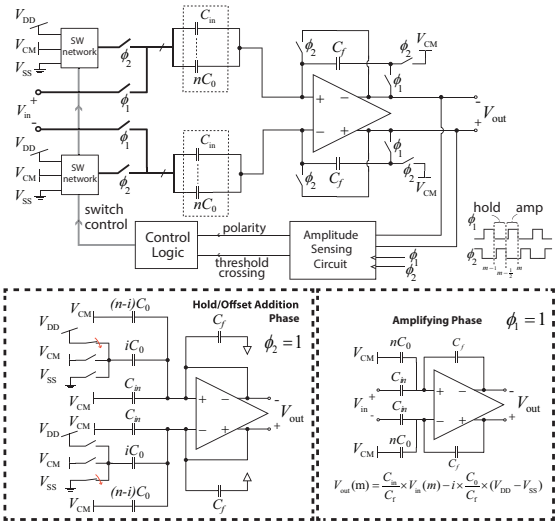


Fig. 3. Schematic of the WEOR amp

The 1^{st}-stage IA employs a relatively large input capacitance (C_{in}) of 20 pF to avoid degrading the overall input-referred noise due to parasitic capacitances at the opamp's input. To maximize the input impedance, we employ C_{pf}'s connected in a positive-feedback fashion between the output and the input of the 1^{st}-stage IA. With the 1^{st}-stage IA's gain of 26 dB, the optimum C_{pf} to maximize the input impedance is 1.05 pF. To account for errors in C_{in} due to parasitic capacitances of the electrode wiring and the ESD pads, we allow 5-bit tuning of C_{pf}'s with a unit capacitance of 32.8 fF—an achievable value in most IC processes—to achieve the targeted input impedance.

Note that the proposed IA does not employ chopping at the capacitive input network since the effective resistance due to chopping significantly lowers the input impedance. To minimize 1/f noise, the opamps in both stages (OA1,2) employ: 1) the complementary input differential pair to maximize the effective transconductance for a given bias current 2) the bulk switching technique [8] applied to both types of the differential pairs to minimize the generation of their 1/f noise. The overall IA consumes a total of 0.9 μA from a 1.2-V supply.

V. The Wide Effective Output Range Amplifier

The WEOR amp utilizes the signal-folding technique to keep its output within the ADC's input range. Fig. 3 shows the schematic of the WEOR amplifier. At its core is a switched-capacitor gain circuit with input capacitances C_{in}'s and feedback capacitances C_{f}'s to provide a gain of $C_{\text{in}}/C_{\text{f}}$. Each side of the capacitive input network also incorporates the "offset" capacitance—divided into n units, each with a capacitance of C_0—for adding appropriate offset to the output voltage V_{out} such that it always stays within the ADC's input range.

The operation of the circuit is divided into two phases—the hold (offset addition) phase and the amplifying phase—as explained by the bottom insets of Fig. 3. During the hold phase ($\phi_2 = 1$), a fraction of the offset capacitances, iC_0 ($0 \le i \le n$), are connected to either V_{DD} or V_{SS} to add offset charges into the offset capacitances, while the rest of the offset capacitances and the input capacitances C_{in} are connected to the common-mode voltage V_{CM}; the value of i and which supply to which each iC_0 must connect are determined by the amplitude sensing circuit and the control logic.

In the amplifying phase ($\phi_1 = 1$), C_{in}'s are connected to the input while all the offset capacitances are connected to V_{CM}, making the changes in the total charges of the input network appear across the feedback capacitances C_{f}'s. For the particular configuration shown, the output voltage is of the form

$$V_{\text{out}}(m) = \frac{C_{\text{in}}}{C_{\text{f}}} \cdot V_{\text{in}}(m) - i\frac{C_0}{C_{\text{f}}}\left(V_{\text{DD}} - V_{\text{SS}}\right).$$

In this case, a negative offset voltage is added to the actual output of the circuit, confining V_{out} to within the ADC's input range. If a positive offset voltage is required, the control logic will appropriately connect the iC_0 capacitances to the opposite supply rails in the hold phase.

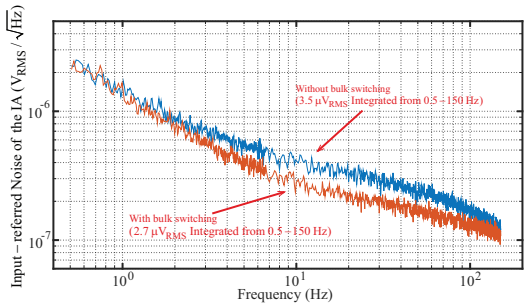
VI. Experimental Results

The proposed ECG readout system has been fabricated in a 0.18-μm CMOS technology and occupies an active area of 2770 $\times$ 1060 μm^2. With the ISC disabled, the system consumes a total current of 5.94 μA—0.9 μA IA, 1.44 μA lowpass filter, 2.2 μA WEOR amp, and 1.4 μA 10b ADC—or 7.13 μW from a 1.2-V supply. An additional 5.29 μA is added—3.75 μA ISC, and 1.54 μA DAC— resulting in a maximum power of 13.5 μW when the ISC is enabled.

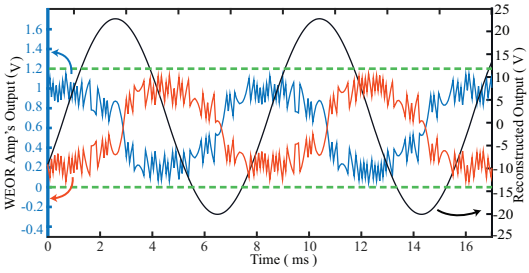
Fig. 4(a) shows the input-referred noise of the IA with and without bulk switching; the technique helps reduce the integrated noise from 3.5 μV_{rms} to 2.7 μV_{rms} (0.5-150 Hz), a significant reduction. Fig. 4(b) shows the output of the WEOR amp and the corresponding reconstructed waveform from the ADC's output data when applying a 128-Hz sinusoid into the WEOR amp's input. Notice that the WEOR amp's output never exceeds the supply rails, but the magnitude of the reconstructed waveform exceeds 40 V_{pp}.

Fig. 4(c) shows the integrated input-referred noise of the system as a function of the ADC's number of bits/sample calculated by taking the FFT of a 40-second ADC's output data stream; the reduction in the number of bits is achieved by discarding appropriate LSBs before taking the FFT. Note that the integrated input-referred noise of the system stays fairly constant at 2.9 μV_{rms} down to around 6 bits, thus suggesting that the system only requires around 6-7 bits of resolution in the ADC to meet the targeted input-referred noise.

Fig. 5 shows the recorded ECG from the system using the in-house high-Z electrodes. The top plot shows an input-referred ECG (lead 1) recorded in a highly-shielded environment (ISC disabled). The bottom plot shows the input-referred reconstructed waveform when the user was touching a laptop plugged into an ungrounded outlet. Clearly, without the ISC, such 13.6 mV_{pp} MI would otherwise saturate the



(a)



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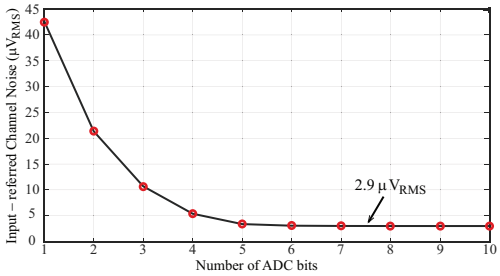

(c)

Fig. 4. Benchtop results: (a) Input-referred noise of the IA with and without bulk switching (b) The raw and reconstructed waveforms of the WEOR amp's output (c) Input-referred noise of the system as a function of ADC's resolution.

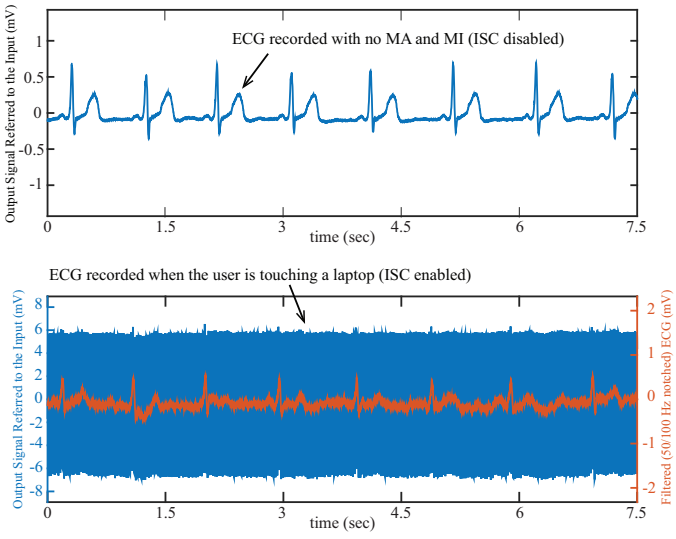

Fig. 5. ECG recordings from high-Z electrods.

TABLE I
PERFORMANCE SUMMARY AND COMPARISON TO PREVIOUS WORKS.

Ref.	Proposed	[1]	[2]	[3]	[4]
Tech. (μm)	0.18	0.18	n.a.	0.18	0.04
Supply (V)	1.2	1.2	1.1	1.3-1.8	0.6
Input Noise (μV_{rms})	2.9	0.605	0.82	4.9	7.8
Input offset rejec. (mV)	railt-to -rail	$\pm$ 400	$\pm$ 300	rail-to -rail	$\pm$ 150
Max. diff. input (mV_{pp})	100*	30	30	110	40
Diff. Z_{in} (GΩ)	$>$ 1	$>$ 0.5 @ 50 Hz	1.5	$>$ 0.4	0.05
Power/chan. (μW)	7.1/13.5	50	83.6	0.884	3.3
ADC Res. (bits)	6	13.5	18	7-10	2
Area (mm^2)	2.93	1.48	n.a.	8.6	0.015

* Tested with 30 mV_{pp} 1 Hz MA + 38 mV_{pp} 50-Hz MI+38 mV_{pp} 100-Hz MI.

IA's output. With the ISC enabled however, the ECG can be recovered after notching out the 50-Hz and 100-Hz MI from the reconstructed data in the digital backend. Although not as clean due to imperfect reconstruction, the recovered ECG still exhibits clear QRS peaks and thus can be used in peak detection applications. Table I summarizes the performances of the proposed system compared to the state-of-the-arts.

VII. Conclusion

This work proposes a low-power high-input-impedance ECG recording system for recording from high-Z electrodes. By employing the signal-folding technique and the interference suppression feedback, the system achieves a very high gain, which allows for the use of a low-resolution ADC without degrading the system's input-referred noise, thus resulting in low power consumption.

VIII. Acknowledgement

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Appendix B

A Micropower Motion Artifact Estimator for Input Dynamic Range Reduction in Wearable ECG Acquisition Systems

Bhirawich Pholpoke, Techapon Songthawornpong, and Woradorn Wattanapanitch, *Member, IEEE*

***Abstract*—This work presents the design and analysis of a compact low-power motion artifact estimator for reducing the input dynamic range in wearable ECG acquisition systems. The estimator employs a novel mixed-signal architecture that performs adaptive filtering on the electrode impedance information to derive a cancellation signal to suppress the motion artifact at the input of the acquisition system. A detailed noise analysis and optimization strategies are also provided to minimize the estimator's noise referred to the acquisition system's input. Fabricated in a 0.18-μm CMOS process and operating from a 1-V supply, the estimator occupies an active area of 0.11 mm^2 and consumes 2.6-3.2 μW of power depending on the final weights used. The low power consumption and small area thus make the estimator suitable for local placement at each recording channel in multi-channel ECG acquisition systems.**

***Index Terms*—ECG acquisition system, motion-artifact suppression, adaptive least-mean-square algorithm, mixed-signal adaptive filtering.**

I. Introduction

ACCORDING to recent statistics from The World Health Organization (WHO), more than 17.9 millions people worldwide succumb to some forms of cardiovascular diseases (CVDs) annually (equivalent to 31% of all the global deaths), making CVDs the leading cause of death among the world population [1]. Though still challenging, reducing CVD deaths is becoming feasible due to the emergence of low-power wearable electrocardiogram (ECG) recording devices that can noninvasively monitor ECG from the body's surface and send data to be interpreted by software or skilled cardiologists. Such technology can help provide immediate feedbacks to patients on their heart's healths, or even alert them of imminent heart failures; if widely available, it can not only save lives, but also help raise health awareness among users, thus lowering their chances of acquiring CVDs.

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To be useful in clinical applications, wearable ECG recording devices must address the problem of baseline fluctuations due to the movements of electrodes with respect to the skin—i.e., the motion artifact (MA) [2], [3]. MA increases the input dynamic range (DR) of the recording devices, necessitating most existing systems to employ low gain in their amplification chains followed by high-resolution analog-to-digital converters (ADCs); such approach incurs significant power overhead, thus resulting in higher power consumption. To minimize power, it is important to minimize the DR of the input signal such that the recording system can be designed with a high-gain instrumentation amplifier (IA) followed by a low-to-moderate-resolution ADC. This can be achieved by suppressing MA locally, near the input of the recording system, before the signal undergoes large amplification.

Currently, there exist several commercial wearable ECG monitors on the market. Only one product (QardioCore [4]) has full continuous monitoring capability while the rest—e.g., Whiting Move ECG [5], AliveCor [6], Apple Watch [7]—are designed to be wrist-worn, thus not intended for continuous ECG monitoring. To record ECG from these wrist-worn devices, the user needs to make two electrical contacts to complete the circuit, while staying still to avoid generating MA and let the devices record the clean ECG. Thus, MA suppression is less of a concern in these devices. However, MA suppression is critical for ECG devices with continuous monitoring capability such as QardioCore. Even though how QardioCore deals with the problematic MA is not revealed to the public, we speculate that it must employ an existing commercial analog frontend (AFE) chip, most of them dealing with MA in a very rudimentary manner such as using a high-pass corner to filter out MA [8]. Unfortunately, such simple filtering of MA from the recorded ECG inevitably leads to signal distortion as the MA's frequency contents overlap those of the ECG and its morphology typically resembles those of the P and T waves [9]. Therefore, most existing works in the literature address the MA suppression problem by utilizing computationally-expensive algorithms—e.g., filter bank [10], wavelet transforms [11]–[13], and the principal component analysis (PCA) and independent component analysis [14], [15]—thus are not suitable for on-chip implementation. One promising method due to its low computational complexity is the adaptive noise cancelling [9], [16]–[22], most employing the least-mean-square (LMS) adaptive filtering. To suppress MA, an adaptive filter, employing a reference signal correlated

to the MA in the recorded ECG, adjusts its coefficients to map the reference signal to the MA; the mapped reference signal is then subtracted from the recorded signal, leaving the output with relatively clean ECG waveforms. Note that for the adaptive noise canceling to be effective, there must exist a strong correlation between the reference signal and the MA in the recorded ECG as the low correlation between the two often leads to contamination of the desired ECG signal by the reference. To address the problem of low correlation, [23] proposed a two-stage algorithm: the first stage employs the weighed adaptive noise filtering (WAF) while the second stage employs a recursive Hampel filter. The WAF stage uses a cross-correlation factor to address the impact of the low correlation while the Hampel filter employs the spatial correlation between successive ECG waves to filter out MA. Nevertheless, due to their still high computational complexity, all the works mentioned suppress MA in the digital backend, thus requiring recording devices with high input DR to prevent signal saturation even in the cases of strong MA.

To reduce the system's input DR requirement, the work in [24] employs LMS filtering to generate a cancellation signal and feeds it back to cancel with the MA near the system's input. With MA already suppressed, the signal can undergo additional amplification by the programmable amplifier without the worry of saturating its output range; the large amplification then allows the use of a moderate-resolution ADC without compromising the signal-to-noise ratio (SNR). Nevertheless, the system in [24] employs an off-chip microcontroller unit (MCU) to realize the LMS filter for estimating MA, which poses a certain disadvantages: First, a high-resolution digital-to-analog converter (DAC) is required to convert the MA cancellation signal produced by the MCU into an analog form to suppress MA in the analog domain—the DAC and its associated interface incur sizable power consumption and area; Second, the MCU incurs significant power overhead to the recording channel—the MSP430 MCU from Texas Instruments [25] normally used in low-power applications consumes at least 230 μA of current from a 2.2-V supply while operating at a clock rate of 1 MHz. In [26], the MCU used is responsible for 55% of the total power—amounting to more than 3 mW—mostly for streaming out the raw ECG and ETI signals. Also, the work in [24] demonstrates that the power consumption associated with the MCU can be significantly reduced by first performing feature extraction in the analog domain before performing digital signal processing in the MCU. Third, scaling to a higher-channel-count system can prove problematic since implementing an adaptive filter for every channel would require significant resources in the MCU, thus necessitating an MCU with higher performance and, consequently, higher power consumption. Finally, for scaling to the multi-lead active electrode scheme [27] in which a recording circuitry is placed directly on top of the electrode, sharing an MCU as a central unit to implement adaptive filtering for all the channels may result in very complicated signal distribution schemes and cabling requirements. Due to these reasons, we propose that a low-power low-complexity LMS filter be implemented locally at each recording site to reduce the overall system's power consumption and lower the signaling complexity and cabling requirements in multi-lead systems.

In this paper, we present a compact low-power MA estimator to derive a cancellation signal from a reference to help suppress MA near the input. The estimator employs a mixed-signal adaptive filter architecture based on a simple transconductance-capacitance (OTA-C) filter, counters, and chopper switches, thus resulting in a small area and low power consumption, making it suitable for local placement at each recording channel in multi-lead ECG recording systems. In this work, only the MA estimator is implemented on-chip, which is integrated into an ECG recording system built on a printed circuit board (PCB) for demonstration.

Many forms of reference signals have been employed for MA suppression such as the skin stretch signal [17], [28], the electrode motion [18], [19], the optical bend signal [29], and the change in electrode impedance (ETI) [29]–[31]. Among the mentioned reference signals, ETI seems a promising candidate since not only does it exhibit high correlation with MA, which allows for the superior performance of the beat detection algorithms compared to the use of other reference signals [29], [31], it also is very amenable to low-power circuit design since no additional sensor is required to produce ETI: ETI can be generated relatively conveniently by injecting AC currents into the sensing electrodes and amplifying the resulting voltage [32], [33]. Since the injected AC currents have their spectral contents outside the ECG band, they do not corrupt the ECG's morphology. Thus, this work will assume the use of ETI as the reference signal, but other forms of reference signals should be applicable to the proposed topology as well.

In using adaptive filtering for MA suppression, we assume that there exists a strong correlation between the reference signal and MA in the recorded ECG. As discussed in [26], the ETI-MA correlation and the MA's amplitude depend on the types of movement artifacts, with the push/pull artifacts exhibiting the highest correlation and strongest MA's amplitude. In other artifact types (twisting/stretching the skin and other random artifacts), both the ETI-MA correlation and MA's amplitude are weaker, making the increase in the input DR not as severe as in the high-correlation case; but the low ETI-MA correlation may distort the recorded ECG when the proposed scheme is used. In this paper, we also investigate a scheme to preserve the original input ECG in cases of poor ETI-MA correlation such that other powerful digital algorithms [14], [15], [34] may be employed in the digital backend to separate MA from the recorded ECG.

The paper is organized as follows: Section II provides some physical insight into the generation of MA and how it inspires the simple transfer function of the proposed estimator. Section III then explains how to realize the estimator at the architectural level. Section IV then provides details on the circuit implementation and analysis. Section V provides noise analysis and discusses how the estimator can be incorporated into ECG acquisition systems without much noise penalty. Section VI shows the measured results. Finally, Section VII concludes the paper.

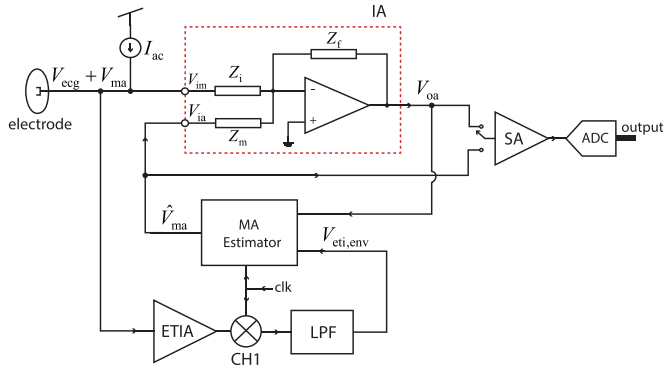


Fig. 1. The proposed MA estimator employed in an ECG recording channel.

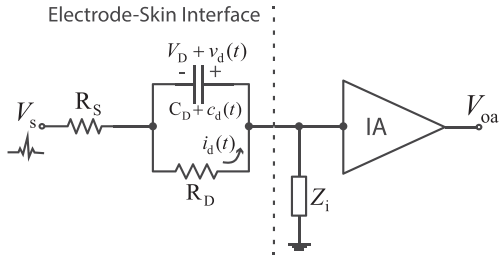


Fig. 2. A circuit model for understanding the MA generation mechanism.

II. General Considerations

A. An ECG Recording Channel With Embedded MA Estimator

Fig. 1 illustrates the concept of an ECG recording channel housing the proposed MA estimator. The instrumentation amplifier IA consisting of two inputs—i) the main input $V_{\rm im}$ and ii) the auxiliary input $V_{\rm ia}$—retrieves the MA-corrupted ECG from the electrode ($V_{\rm ecg}+V_{\rm ma}$) on $V_{\rm im}$, and the MA-cancellation signal ($\hat{V}_{\rm ma}$) from the MA estimator on $V_{\rm ia}$. The estimator's task is to produce $\hat{V}_{\rm ma}$ to cancel with $V_{\rm ma}$ in the main input such that the output of the IA, $V_{\rm oa}$, contains negligible components of $V_{\rm ma}$. To provide an ability to reconstruct the original recorded signal in the case of poor ETI-MA correlation, the sampling amplifier SA samples and amplifies both $V_{\rm oa}$ and $\hat{V}_{\rm ma}$ before an ADC digitizes the SA's output and reports it to the digital backend, where they can be appropriately combined to reconstruct the original input signal.

In this work, the MA estimator uses ETI as the reference signal to produce $\hat{V}_{\rm ma}$; the ETI can be obtained by injecting common-mode AC currents into the two sensing electrodes as explained in [32]: in Fig. 1, the current source $I_{\rm ac}$ injects an AC current into the sensing electrode; the resulting modulated signal, centered at the frequency of the AC current, is amplified by the electrode impedance amplifier (ETIA), demodulated to baseband by the chopper switch CH1, and lowpass filtered to produce an envelope signal $V_{\rm eti,env}$ proportional to the ETI.

B. Mechanism of MA Generation

For on-chip local placement in each recording channel, the MA estimator should employ as simple an algorithm as possible to minimize area and power consumption. To understand our proposed topology, let's first understand how the MA in the input signal gives rise to the ETI. The analysis to be provided is by no means so accurate as to precisely predict the MA from the ETI. Instead, we will utilize a simple circuit model to provide just enough motivation for our proposed topology.

As discussed in [35], MA arises from the change in the electrode's half-cell potential due to mechanical disturbance of the double-layer capacitance. Illustrated in Fig. 2 is a widely-adopted model of the electrode-skin interface when connected to an IA, in which $R_{\rm S}$ represents the nominal value of the electrolyte contact resistance, $C_{\rm D}$ of the double-layer capacitance, $R_{\rm D}$ of the leakage resistance through the double layer, $V_{\rm D}$ of the half-cell potential due to the total charge in the double layer, and $Z_{\rm i}$ of the input impedance of the IA. Let's assume that mechanical disturbance changes the value of the double-layer capacitance to $C_{\rm D}+c_{\rm d}(t)$, while negligibly affecting other parameters; this causes the redistribution of charge in the double layer as manifested by the incremental current $i_{\rm d}(t)$ flowing through it, thus changing the half-cell potential to $V_{\rm D}+v_{\rm d}(t)$; $v_{\rm d}(t)$ is then sensed by the IA. With $i_{\rm d}(t)=-v_{\rm d}(t)/R_{\rm D}$, we can relate $c_{\rm d}(t)$ to $v_{\rm d}(t)$ by

$$\frac{-v_{\rm d}(t)}{R_{\rm D}} = C_{\rm D}\frac{dv_{\rm d}(t)}{dt} + V_{\rm D}\frac{dc_{\rm d}(t)}{dt}. \tag{1}$$

The relationship in (1) can be easily understood in the frequency domain. Let $C_{\rm d}(j\omega)$ and $V_{\rm d}(j\omega)$ be the Fourier transforms of $c_{\rm d}(t)$ and $v_{\rm d}(t)$, respectively. It follows that the response $v_{\rm d}(t)$ due to $c_{\rm d}(t)$ can be expressed as a frequency response

$$\frac{V_{\rm d}(j\omega)}{C_{\rm d}(j\omega)} = \frac{(\omega R_{\rm D}C_{\rm D})^2}{1+(\omega R_{\rm D}C_{\rm D})^2}\cdot\frac{V_{\rm D}}{C_{\rm D}}\cdot\left(1-\frac{j}{\omega C_{\rm D}R_{\rm D}}\right), \tag{2}$$

which can be written in a polar form as $V_{\rm d}(j\omega)/C_{\rm d}(j\omega) = A\exp(j\theta)$, where $A=\sqrt{\frac{(\omega R_{\rm D}C_{\rm D})^2}{1+(\omega R_{\rm D}C_{\rm D})^2}}\cdot\frac{V_{\rm D}}{C_{\rm D}}$ and $\theta=-\tan^{-1}\left(\frac{1}{\omega R_{\rm D}C_{\rm D}}\right)$. Hence, the task of the MA estimator is reduced to finding a frequency mapping expressed in (2) by providing appropriate amplitude and phase responses to a quantity that is proportional to the change in the double-layer capacitance—i.e., the ETI in this work.

C. Extracting ETI With Common-Mode AC Currents

In this part, we consider how to extract the change in the double-layer capacitance in a differential recording setting. We adopt, with some modifications, the impedance measurement method proposed in [32] as shown in Fig. 3; in-phase AC currents of the form $I_{\rm o}\cos(\omega_{\rm c}t)$ are injected into the two sensing electrodes to produce a voltage input into ETIA, $V_{\rm eti,in}$. To ease the analysis, let's assume identical nominal values of the two double-layer capacitances, $C_{\rm D}$, and the contact resistances, $R_{\rm S}$, for the two recording electrodes, and ignore the leakage resistances $R_{\rm D}$ by assuming that the frequency of the AC currents, $\omega_{\rm c}$, is much larger than $1/(R_{\rm D}C_{\rm D})$. If $Z_{\rm i}$ of the ETIA is much

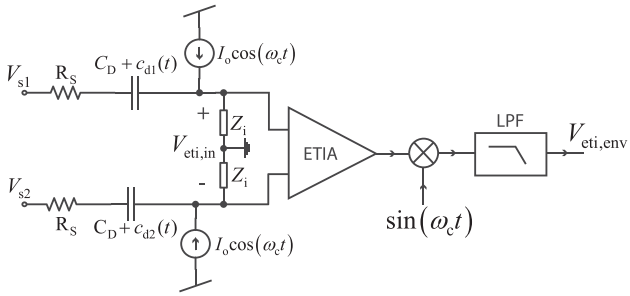


Fig. 3. Extraction of ETI in a differential recording setting.

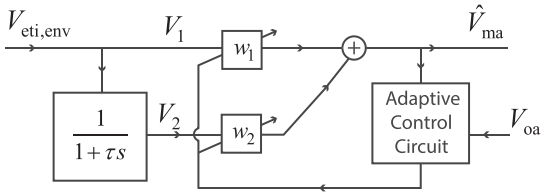


Fig. 4. High-level topology of the MA estimator.

larger than the electrode impedance, $V_{\mathrm{eti,in}}$ can be expressed as

$$V_{\mathrm{eti,in}} = \frac{I_{\mathrm{o}}}{\omega_{\mathrm{c}}}\left(\frac{1}{C_{\mathrm{D}}+c_{\mathrm{d1}}(t)} - \frac{1}{C_{\mathrm{D}}+c_{\mathrm{d2}}(t)}\right)\sin(\omega_{\mathrm{c}}t)\,. \quad (3)$$

By assuming that $C_{\mathrm{D}} \gg c_{\mathrm{d1}}(t), c_{\mathrm{d2}}(t)$ and letting $c_{\mathrm{d}}(t) = c_{\mathrm{d1}}(t) - c_{\mathrm{d2}}(t)$, we can reduce (3) to

$$V_{\mathrm{eti,in}} \approx -I_{\mathrm{o}} \cdot \frac{c_{\mathrm{d}}(t)}{C_{\mathrm{D}}^2\omega_{\mathrm{c}}}\sin(\omega_{\mathrm{c}}t)\,, \quad (4)$$

which shows that the amplitude (envelope) of $V_{\mathrm{eti,in}}$ is proportional to $c_{\mathrm{d}}(t)$. Another interesting point to note from (4) is that $V_{\mathrm{eti,in}}$ has a quadrature phase with respect to that of the injected AC currents, which also agrees with the finding in [26] that the correlation between MA and the complex impedance is much stronger than that between MA and the real impedance. Thus, instead of employing quadrature demodulation as in [24], [26], we choose to demodulate the output of the ETIA with just $\sin(\omega_{\mathrm{c}}t)$ and lowpass filter the result to produce $V_{\mathrm{eti,env}}$.

III. The Proposed MA Estimator

A. High-Level Considerations

Fig. 4 shows our proposed MA estimator that takes as input $V_{\mathrm{eti,env}}$ (also referred to as V_1) and provides the magnitude and phase mappings to produce $\hat{V}_{\mathrm{ma}}$. The MA estimator consists of a 1st-order lowpass filter—whose transfer function is $1/(1+\tau s)$—and two adjustable weights w_1 and w_2 controlled by an adaptive control circuit. The adaptive control circuit takes as input the output of the IA, V_{oa}, and performs an adaptive algorithm to adjust w_1 and w_2 to produce $\hat{V}_{\mathrm{ma}}$ that minimizes the mean-squared value of V_{oa}.

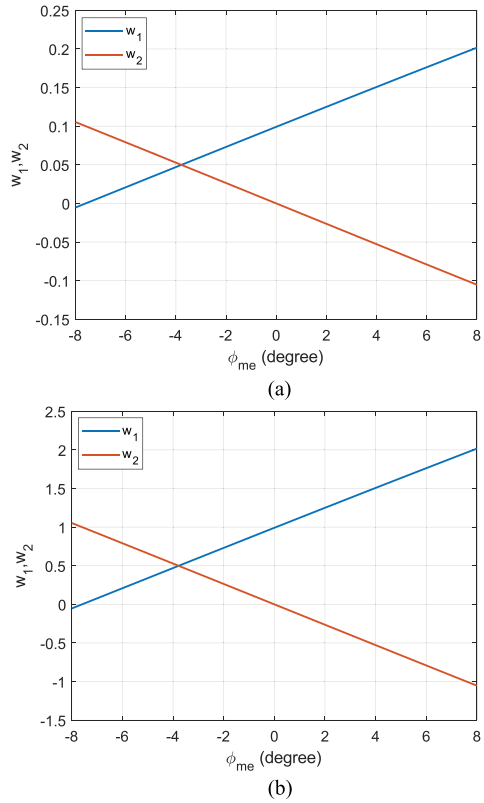


Fig. 5. The required values of w_1 and w_2 to achieve $-8^\circ \le \phi_{\mathrm{me}} \le 8^\circ$ for $1/\tau = 2\pi(15\,\mathrm{Hz})$ and $\omega_{\mathrm{ma}} = 2\pi(2\,\mathrm{Hz})$: (a) $A_{\mathrm{me}} = 0.1$ (b) $A_{\mathrm{me}} = 1.0$.

From Fig. 4, we can derive the transfer function from $V_{\mathrm{eti,env}}$ to $\hat{V}_{\mathrm{ma}}$ as

$$\frac{\hat{V}_{\mathrm{ma}}}{V_{\mathrm{eti,env}}}(s) = (w_1+w_2)\left(\frac{1+\frac{w_1}{w_1+w_2}\cdot\tau s}{1+\tau s}\right). \quad (5)$$

By choosing $1/\tau$ to be significantly higher than the frequency of the MA (ω_{ma}), we can approximate (5) near ω_{ma} as

$$\frac{\hat{V}_{\mathrm{ma}}}{V_{\mathrm{eti,env}}}(j\omega_{\mathrm{ma}}) \approx (w_1+w_2)\left(1+\frac{w_1}{w_1+w_2}\cdot j\omega_{\mathrm{ma}}\tau\right), \quad (6)$$

which is in the same form as (2). The magnitude and phase responses of the transfer function in (6) can be written as $A_{\mathrm{me}} = (w_1+w_2)\sqrt{1+(\frac{w_1}{w_1+w_2}\cdot\tau\omega_{\mathrm{ma}})^2}$ and $\phi_{\mathrm{me}} = \tan^{-1}(\frac{w_1}{w_1+w_2}\cdot\tau\omega_{\mathrm{ma}})$, respectively.

For proper circuit implementation, it is important to determine the required ranges of w_1 and w_2. In this work, we assume that the gain of the ETIA is large enough such that the required value of A_{me} never exceeds unity. For a particular value of A_{me}, we can analytically solve (6) for w_1 and w_2 to achieve a certain value of ϕ_{me}. Fig. 5(a) plots the values of w_1 and w_2 to achieve $A_{\mathrm{me}} = 0.1$ and obtain ϕ_{me} in the range of -8° to 8°, while Fig. 5(b) plots w_1 and w_2 to achieve the same range of ϕ_{me} for $A_{\mathrm{me}} = 1$. Both cases assume $\omega_{\mathrm{ma}} = 2\pi(2\,\mathrm{Hz})$ and $\tau = 1/(2\pi 15\,\mathrm{Hz})$. Note that we only limit $|\phi_{\mathrm{me}}|$ to within 8° because this range covers a sufficiently long time delay between $V_{\mathrm{eti,env}}$ and $\hat{V}_{\mathrm{ma}}$:

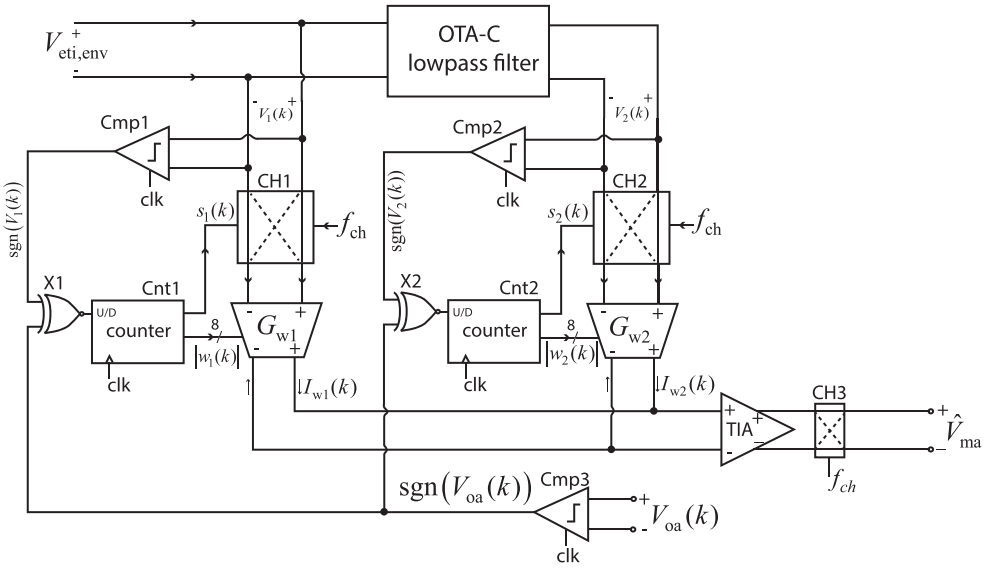


Fig. 6. The high-level schematic of the proposed motion artifact estimator.

for $\omega_{\rm ma} = 2\pi(2\,{\rm Hz})$, a 8° phase shift corresponds to 11.1 ms, which should be longer than the expected delay from the change in the double-layer capacitance to that in the half-cell potential.

We can see that the higher is $A_{\rm me}$, the higher are the magnitudes of w_1 and w_2. With $A_{\rm me} = 1$, the required value of w_1 is at the maximum, but still less than 2. It is not difficult to show that if we simply reverse the polarity of $A_{\rm me}$ while keeping its magnitude constant, the required w_1 and w_2 will attain the same magnitudes but opposite polarities. The forgoing analysis suggests that the appropriate range of w_1 and w_2 be $[-2, 2]$, provided that $|A_{\rm me}| \leq 1$ and $|\phi_{\rm me}| \leq 8^\circ$.

B. The Least-Mean-Square (LMS) Algorithm

In this section, we describe the adaptive algorithm for adjusting w_1 and w_2. To achieve low power and small area, we adopt an LMS algorithm [16] to minimize the mean-squared value of $V_{\rm oa}$ in a gradient-descent manner. Due to the very slow adaptation rate, we choose to implement the proposed topology in discrete time to avoid the use of continuous-time analog integrators, which consume large area and are prone to output saturation due to offsets [36].

To move $w_{1,2}$ in the directions opposite to the gradients of $V_{\rm oa}$, we employ the adaptation rule

$$w_{1,2}(k+1) = w_{1,2}(k) - \mu \frac{\partial(E(V_{\rm oa}^2(k)))}{\partial w_{1,2}}, \qquad (7)$$

in which k is the time step, μ is a constant determining the rate of adaptation, and $E(V_{\rm oa}^2(k))$ is the mean-squared value of $V_{\rm oa}$. We then approximate that $E(V_{\rm oa}^2(k)) \approx V_{\rm oa}^2(k)$ [36], which helps simplify (7) to

$$w_{1,2}(k+1) = w_{1,2}(k) - 2\mu \cdot V_{\rm oa}(k) \cdot \frac{\partial V_{\rm oa}(k)}{\partial w_{1,2}}. \qquad (8)$$

Recall from Fig. 1 that $V_{\rm oa}$ is a superposition of $V_{\rm ecg}$, $V_{\rm ma}$, and $\hat{V}_{\rm ma}$, while the algorithm can assert control only over $\hat{V}_{\rm ma}$. Assuming a negative gain from $V_{\rm ma}$ to $V_{\rm oa}$, we have $\partial V_{\rm oa}/\partial w_{1,2} \propto -\partial \hat{V}_{\rm ma}/\partial w_{1,2}$. From Fig. 4, we have $\hat{V}_{\rm ma}(k) = w_1 \cdot V_1(k) + w_2 \cdot V_2(k)$. Thus, substituting $\partial V_{\rm oa}(k)/\partial w_{1,2}$ in (8) with $\partial \hat{V}_{ma}(k)/\partial w_{1,2}$ gives

$$w_{1,2}(k+1) = w_{1,2}(k) + 2\mu \cdot V_{\rm oa}(k) \cdot V_{1,2}(k), \qquad (9)$$

where μ in (9) is different from that in (8) by a scale factor.

To simplify the circuit implementation, we adopt the sign-sign LMS (SS-LMS) algorithm [37], which helps reduce (9) to

$$w_{1,2}(k+1) = w_{1,2}(k) + 2\mu \cdot {\rm sgn}(V_{\rm oa}(k)) \cdot {\rm sgn}(V_{1,2}(k)), \qquad (10)$$

where ${\rm sgn}(\cdot)$ denotes the signum function. Due to this simplification, the ${\rm sgn}(\cdot)$ function can be implemented with a clocked comparator, which can be realized in a small area and consumes almost no static power; the multiplication of the signs can be implemented with just an exclusive-NOR (XNOR) gate, instead of a full-blown multiplier circuit; the integrators and the storage of the $w_{1,2}$ can be simultaneously realized with an up/down counter, while the step size μ and its rate of adaptation will be automatically determined by the resolution and the counting speed of the up/down counter, respectively.

C. The Circuit Topology

Fig. 6 shows the proposed MA estimator; at its heart are the operational transconductance amplifier-capacitance (OTA-C) lowpass filter to provide the required phase shift, and two up/down counters Cnt1 and Cnt2 to store and perform necessary integration of the weights w_1 and w_2. The clocked comparators Cmp1, Cmp2, and Cmp3 determine the signs of $V_1(k)$, $V_2(k)$, and $V_{\rm oa}(k)$, respectively. The XNOR gates X1 and X2 then multiply the signs of $V_1(k)$ and $V_2(k)$ to that of $V_{\rm oa}(k)$, whose results

update the counters Cnt1 and Cnt2: the counter Cnt1,2 counts up if $\mathrm{sgn}(V_{1,2}(k)) \cdot \mathrm{sgn}(V_{\mathrm{oa}}) = 1$, otherwise it counts down. For $w_{1,2}(k)$ to attain either polarity, the up/down counters are implemented in the sign-magnitude format—the 8-bit $|w_{1,2}(k)|$ represents the magnitude while the 1-bit $s_{1,2}(k)$ represents the sign.

To produce $\hat{V}_{\mathrm{ma}}$, the G_{w1} and G_{w2} OTAs, whose effective transconductances G_{w1} and G_{w2} are proportional to $w_1(k)$ and $w_2(k)$, first convert $V_1(k)$ and $V_2(k)$ into currents $I_{\mathrm{w1}}(k)$ and $I_{\mathrm{w2}}(k)$, respectively; that $G_{\mathrm{w1,2}} \propto w_{1,2}(k)$ thus makes $I_{\mathrm{w1,2}}(k) \propto w_{1,2}(k) \cdot V_{1,2}(k)$. The currents $I_{\mathrm{w1}}(k)$ and $I_{\mathrm{w2}}(k)$ are then summed and converted into $\hat{V}_{\mathrm{ma}}$ via a transimpedance amplifier TIA, providing $\hat{V}_{\mathrm{ma}} \propto w_1(k)V_1(k) + w_2(k)V_2(k)$.

Unlike the low-bandwidth OTA-C lowpass filter, the $G_{\mathrm{w1,2}}$ OTAs and the TIA are wideband circuits, whose 1/f noise dominates the ECG band. We therefore utilize the chopper stabilization technique—via the chopping switches CH1,2 and CH3—to suppress their 1/f noise: the switches CH1 and CH2 up-modulate $V_1(k)$ and $V_2(k)$ to the chopping frequency f_{ch}—at which the $G_{\mathrm{w1,2}}$-OTAs and the TIA exhibit only thermal noise—before they are transformed into currents and summed. The switch CH3 then demodulates the TIA's output to baseband to produce $\hat{V}_{\mathrm{ma}}$. Besides 1/f noise suppression, the three chopper switches, working in conjunction, control the polarities of the weights with respect to $\hat{V}_{\mathrm{ma}}$ as instructed by the sign bit $s_{1,2}(k)$: when $s_{1,2}(k) = 0$, the chopper switch CH1,2 operates in phase with CH3, effectively making $w_{1,2}(k)$ positive; on the contrary, $s_{1,2}(k) = 1$ instructs CH1,2 to operate in the opposite phase to that of CH3, effectively making $w_{1,2}(k)$ negative.

IV. Circuit Implementation

For the circuit implementation of the MA estimator, we decide on the fully-differential architecture, even at the expense of increased circuit complexity, due to two reasons: First, operating under a limited supply voltage (1 V), fully-differential circuit blocks allow sizable output swings and input linear ranges with minimal 2^{nd}-order nonlinearity, as deemed essential for minimizing the estimator's noise contribution to the overall system (see Sec. V-C); Second, fully-differential signaling facilitates the implementation of bipolar weights needed for the $G_{\mathrm{w1,2}}$ OTAs by just swapping between the two sides of their input/output terminals.

A. The Gm-C Lowpass Filter

Fig. 7(a) shows the OTA-C lowpass filter, consisting of two OTAs with the effective transconductances of G_{i} and G_{f}, a current integrator, and two source-follower buffers; the current integrator consists of a high-output-impedance current buffer with a current gain of 1/N and an integrating capacitance C_{F}. The source followers after the current integrator help shield the high-impedance nodes, V_{oc}^{+} and V_{oc}^{-} such that the output V_2 can drive the chopper switch CH2.

Fig. 7(b) shows the block diagram of the lowpass filter with R_{o} representing the current buffer's output impedance and A_{sf} the voltage gain of the source followers; $\overline{i_{\mathrm{no},G_{\mathrm{i}}}^2}$, $\overline{i_{\mathrm{no},G_{\mathrm{f}}}^2}$, and $\overline{i_{\mathrm{no,cbf1}}^2}$

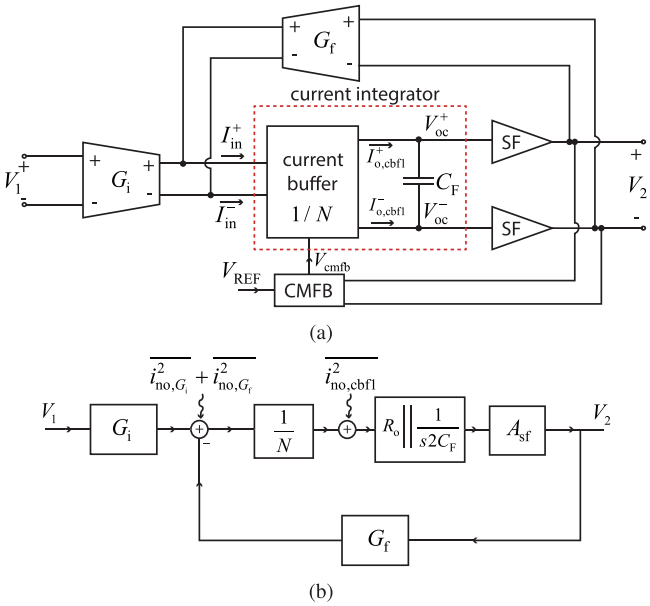


Fig. 7. (a) High-level schematic of the OTA-C lowpass filter. (b) Block diagram for the analysis of the OTA-C lowpass filter.

represent the output noise currents of the G_{i} and G_{f} OTAs, and the current buffer, respectively. From this block diagram, we can express the lowpass filter's transfer function as

$$\frac{V_2}{V_1}(s) \approx \frac{G_{\mathrm{i}}}{G_{\mathrm{f}}} \cdot \frac{1}{1 + s/\omega_{\mathrm{f}}}, \tag{11}$$

where $\omega_{\mathrm{f}} = G_{\mathrm{f}}A_{\mathrm{sf}}/(2NC_{\mathrm{F}})$, provided that $G_{\mathrm{f}}R_{\mathrm{o}}A_{\mathrm{sf}} \gg N$. In this implementation, we make $G_{\mathrm{i}} = G_{\mathrm{f}}$ to achieve a low-frequency gain of unity, while setting $\omega_{\mathrm{f}} \approx 2\pi(15\,\mathrm{Hz})$ with $C_{\mathrm{F}} = 10\,\mathrm{pF}$ to keep the overall area small. With $N = 2$, and $A_{\mathrm{sf}} \approx 1$, the required value for $G_{\mathrm{i,f}}$ to achieve such ω_{f} is 3.77 nA/V. A standard differential pair with each input transistor operating in subthreshold at 1-nA bias current provides approximately 27 nA/V of effective transconductance (assuming a gate coupling coefficient (κ) of 0.7), still far above the value required to achieve the desired ω_{f}. Hence, to achieve the required ω_{f} while keeping C_{F} around 10 pF, we need to reduce the values of $G_{\mathrm{i,f}}$ by a factor of 0.14 as will be described next.

1) The G_i and G_f OTAs: The most energy-efficient method to reduce $G_{\mathrm{i,f}}$ is to lower the bias currents of both OTAs, but at an expense of making the OTAs more prone to mismatches due to all the transistors running in very deep subthreshold. Since the OTA's bias current of a few nanoamperes is considered already low, while reducing it further proves unnecessarily risky, we opt for the bulk-input technique to reduce the OTAs' effective transconductances without lowering their bias currents. Shown in Fig. 8(a), the $G_{\mathrm{i,f}}$ OTA employs the bulk input and the source degeneration techniques [38] to reduce its transconductance for a given bias current. Let $I_{\mathrm{o}} = I_{\mathrm{o}}^{+} - I_{\mathrm{o}}^{-}$ and $V_{\mathrm{in}} = V_{\mathrm{in}}^{+} - V_{\mathrm{in}}^{-}$ be the differential output current and the differential input voltage of the OTA, respectively. The feedback diagram in Fig. 8(b) summarizes the OTAs' operation in which $g_{\mathrm{m,i}}$, $g_{\mathrm{mb,i}}$, $g_{\mathrm{s,i}} = g_{\mathrm{m,i}} + g_{\mathrm{mb,i}}$, and $\overline{i_{\mathrm{n,i}}^2}$ are the transconductance, the body

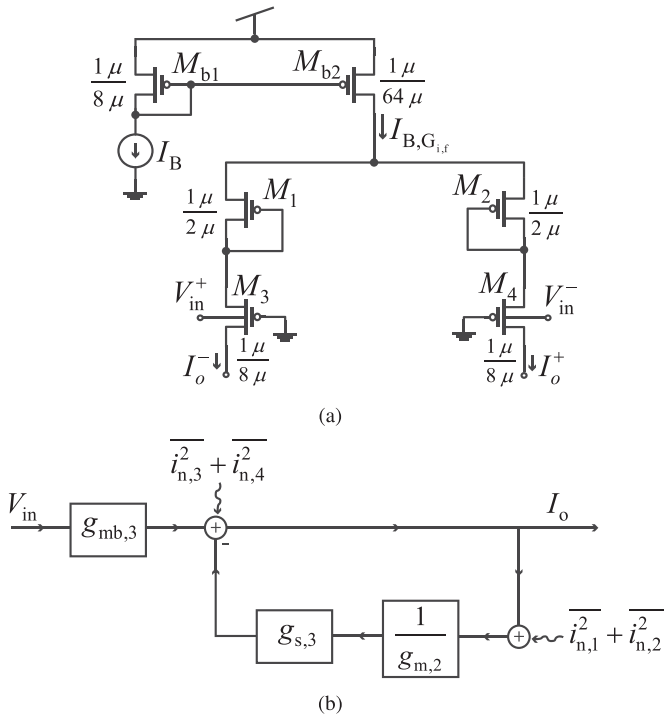


Fig. 8. (a) Schematic of the $G_{\rm i}$ and $G_{\rm f}$ OTAs. (b) The block diagram of the $G_{\rm i}$ and $G_{\rm f}$ OTAs including the noise sources.

effect conductance, the source conductance, and the output current noise of the transistor $M_{\rm i}$, respectively. Assuming that all the transistors are in subthreshold such that their small-signal conductances can be expressed as $g_{\rm m,i} = \kappa I_{\rm D,i}/\phi_{\rm t}$, $g_{\rm mb,i} = (1-\kappa)I_{\rm D,i}/\phi_{\rm t}$, and $g_{\rm s,i} = I_{\rm D,i}/\phi_{\rm t}$ [39]—where $I_{\rm D,i}$ is the drain current of $M_{\rm i}$, κ the gate coupling coefficient, and $\phi_{\rm t}$ the thermal voltage—we can derive the OTA's effective transconductance as

$$G_{\rm i,f} = \frac{I_{\rm o}}{V_{\rm in}}(s) = g_{\rm mb,3} \cdot \frac{g_{\rm m,1}}{g_{\rm m,1} + g_{\rm s,3}} = \frac{1-\kappa}{1+\kappa} g_{m,3}. \quad (12)$$

For $\kappa \approx 0.7$, we have $G_{\rm i,f} \approx 0.17 g_{\rm m,3}$, an attenuation factor closed to what we aimed.

2) The Current Integrator: Fig. 9(a) shows the schematic of the current buffer in the current integrator followed by the source-follower buffers. The $1/N$ current mirrors ($M_{\rm c1}$-$M_{\rm c4}$) pass the scaled-down version of the input current to be integrated onto C_F connecting between $V_{\rm oc}^+$ and $V_{\rm oc}^-$. The current buffer employs the regulated cascode technique—$M_{\rm c7}$-$M_{\rm c10}$ and $M_{\rm c11}$-$M_{\rm c14}$—to maximize its output impedance while minimizing the input impedance into the source of $M_{\rm c9,10}$ such that most of the signal current flows to the current buffer's output nodes, instead of being shunted away by the output conductance of $M_{\rm c3,4}$. The source followers ($M_{\rm s1}$ and $M_{\rm s2}$) then buffer the high-impedance nodes $V_{\rm oc}^+$ and $V_{\rm oc}^-$ to produce the output, $V_{\rm o} = V_{\rm o}^+ - V_{\rm o}^-$, that drives the chopper switch CH2 and the input of the $G_{\rm f}$ OTA. The source-follower buffers employ low-threshold devices for $M_{\rm s1}$ and $M_{\rm s2}$, whose bulks are tied to the sources, to eliminate the body effect and prevent significant DC level shift, which might otherwise limit the output voltage swing of the current integrator.

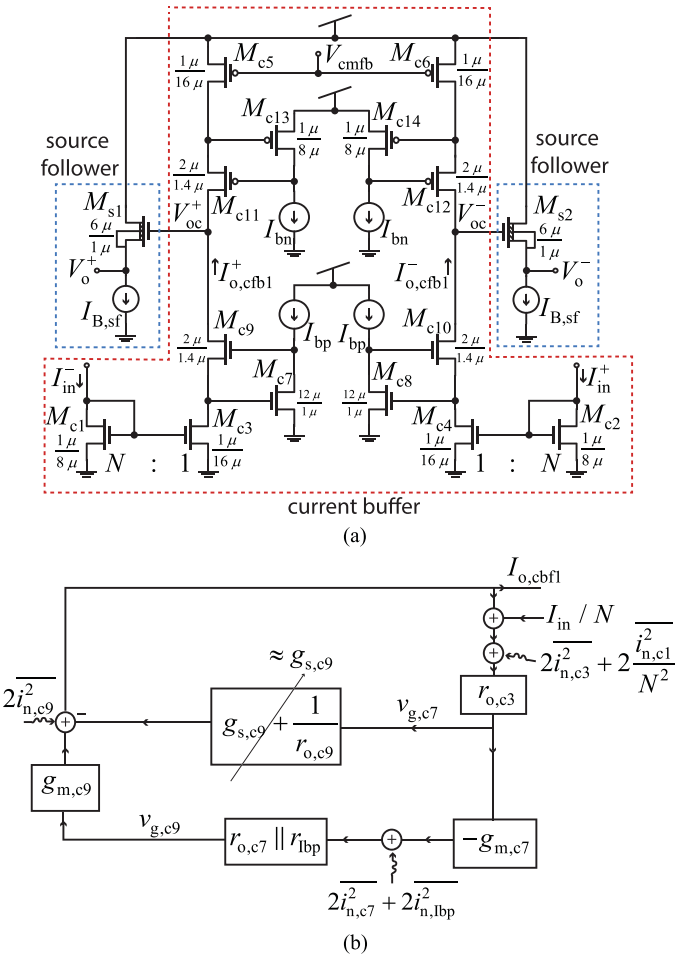


Fig. 9. (a) Schematic of the current buffer in the current integrator followed by the source-follower buffers. (b) Block diagram of the bottom half of the current buffer.

Fig. 9(b) shows the block diagram summarizing the small-signal analysis of the bottom-half of the current buffer—$M_{\rm c1}$-$M_{\rm c4}$, $M_{\rm c7}$-$M_{\rm c10}$ and the two $I_{\rm bp}$ current sources—in which $I_{\rm in} = I_{\rm in}^+ - I_{\rm in}^-$ and $I_{\rm o,cbf1} = I_{\rm o,cbf1}^+ - I_{\rm o,cbf1}^-$; $r_{\rm Ibp}$ and $\overline{i_{\rm n,Ibp}^2}$ are the output resistance and the noise current associated with each $I_{\rm bp}$ current source, respectively. The transfer function from $I_{\rm in}$ to $I_{\rm o,cbf1}$ can be written as

$$\frac{I_{\rm o,cbf1}}{I_{\rm in}} = \frac{1}{N} \frac{g_{\rm s,c9} r_{\rm o,c3} + g_{\rm m,c7}\left(r_{\rm o,c7} \parallel r_{\rm Ibp}\right) g_{\rm m,c9} r_{\rm o,c3}}{1 + g_{\rm s,c9} r_{\rm o,c3} + g_{\rm m,c7}\left(r_{\rm o,c7} \parallel r_{\rm Ibp}\right) g_{\rm m,c9} r_{\rm o,c3}} \approx \frac{1}{N}, \quad (13)$$

provided that $g_{\rm s,c9} r_{\rm o,c3} + g_{\rm m,c7}(r_{\rm o,c7} \parallel r_{\rm Ibp})\, g_{\rm m,c9} r_{\rm o,c3} \gg 1$.

B. The Weighted-Sum Circuit

Fig. 10(a) shows the high-level schematic of the weighted sum circuit, consisting of the $G_{\rm w1,2}$ OTAs and a transimpedance amplifier (TIA), also implemented as a current buffer with an OTA ($G_{\rm TIA}$) in feedback. The circuit computes $V_{\rm o}(k)$ as a weighted sum of the inputs $V_1(k)$ and

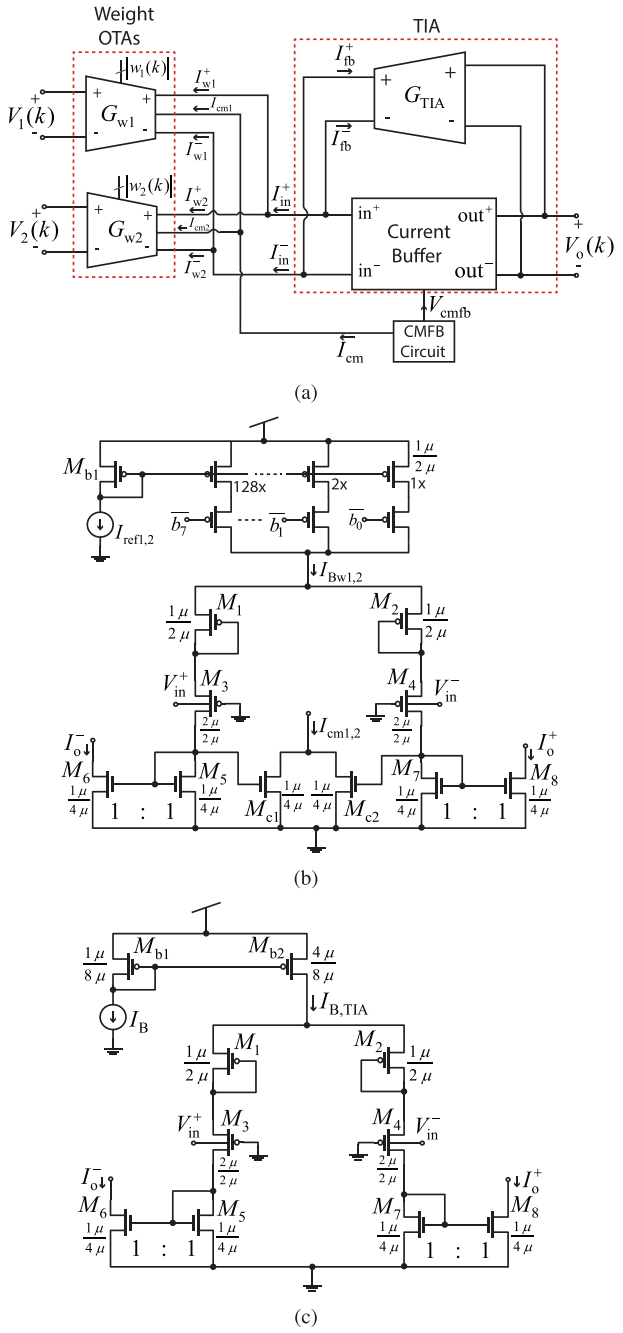


Fig. 10. The weighted-sum circuit: (a) High-level schematic. (b) Schematic of the weight OTAs ($G_{w1,2}$). (c) Schematic of the G_{TIA} OTA.

$V_2(k)$—i.e., $V_{\mathrm{o}}(k) = w_1(k)V_1(k) + w_2(k)V_2(k)$; the magnitude of each weight is programmable by the corresponding weight OTA's effective transconductance—$|w_{1,2}(k)| = G_{\mathrm{w1,2}}(k)/G_{\mathrm{TIA}}$. Fig. 10(b) shows the schematic of the $G_{\mathrm{w1,2}}$ OTAs whose input transistors operate in subthreshold to make their effective transconductances proportional to their bias currents; the weight's magnitude $|w_{1,2}(k)|$, implemented as eight programmable bits $\overline{b_7}, \ldots, \overline{b_0}$, determines the $G_{\mathrm{w1,2}}$ OTA's effective transconductance by controlling the bias current $I_{\mathrm{Bw1,2}}$. Note that changing the bias current of each weight OTA also alters its common-mode (CM) output current and, hence, the CM input current into the current buffer, which may subsequently disturb the CM output voltage of the overall weighted sum circuit. To avoid this issue, the weight OTAs provide their CM output currents ($I_{\mathrm{cm1,2}}$) to the common-mode feedback circuit (CMFB), which uses them to set the CM output voltage of the weighted sum circuit.

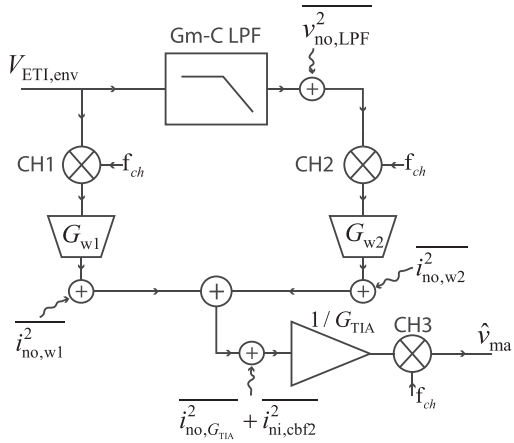


Fig. 11. Diagram for the noise analysis of the MA estimator.

To convert current to voltage, the TIA employs the same technique as that of the lowpass filter, but without the integrating capacitor: the G_{TIA} OTA provides voltage-current feedback around the current buffer to realize a transimpedance gain of $1/G_{\mathrm{TIA}}$. Fig. 10(c) shows the schematic of the G_{TIA} OTA, whose topology is almost identical to the $G_{\mathrm{i,f}}$ OTA in Fig. 8(a) except the G_{TIA} OTA incorporates the 1:1 current mirrors (M_5-M_8) at the output to reverse the polarity of the output current. The schematic of the TIA's current buffer is similar to that in Fig. 9(a), but with the input current mirrors (M_{c1}-M_{c4}) removed.

V. Noise Analysis

In this section, we derive an expression of the estimator's noise referred to the IA's input to understand how to optimize it based on other design parameters. Please note that all the noise expressions derived in this section refer to the power spectral density (PSD), even though we use just the word "noise" for short. First, let's derive an expression of the estimator's output noise using the high-level diagram in Fig. 11; $\overline{v^2_{\mathrm{no,LPF}}}$, $\overline{i^2_{\mathrm{no,w1,2}}}$, $\overline{i^2_{\mathrm{no,G_{TIA}}}}$, $\overline{i^2_{\mathrm{ni,cbf2}}}$ are the output voltage noise of the lowpass filter, the output current noise of the $G_{\mathrm{w1,2}}$ OTA, the output current noise of the G_{TIA} OTA, and the input-referred noise of the TIA's current buffer, respectively. With the TIA's gain of $1/G_{\mathrm{TIA}}$, the noise referred to the output node $\hat{V}_{\mathrm{ma}}$ can be calculated as

$$\overline{v^2_{\mathrm{no,MA}}} = \overline{v^2_{\mathrm{no,LPF}}}\left(\frac{G_{\mathrm{w2}}}{G_{\mathrm{TIA}}}\right)^2 + \left(\overline{i^2_{\mathrm{no,w1}}} + \overline{i^2_{\mathrm{no,w2}}} + \overline{i^2_{\mathrm{no,G_{TIA}}}} + \overline{i^2_{\mathrm{ni,cbf2}}}\right)\frac{1}{G^2_{\mathrm{TIA}}}. \quad (14)$$

Next, let's derive the expressions for all the noise sources in Fig. 11.

A. Noise of the Lowpass Filter

From the block diagram in Fig. 7(b), the output noise of the lowpass filter can be written as

$$\overline{v^2_{\mathrm{no,LPF}}}(f) \approx \left(\overline{i^2_{\mathrm{no},G_\mathrm{i}}} + \overline{i^2_{\mathrm{no},G_\mathrm{f}}} + N^2\overline{i^2_{\mathrm{no,cbf1}}}\right)\frac{1/G_\mathrm{f}^2}{1+(f/f_\mathrm{f})^2}, \tag{15}$$

where $f_\mathrm{f} = \omega_\mathrm{f}/2\pi$. To evaluate this expression, we need to derive $\overline{i^2_{\mathrm{no},G_{\mathrm{i,f}}}}$ and $\overline{i^2_{\mathrm{no,cbf1}}}$. From the block diagram in Fig. 8(b) and assuming that $g_{\mathrm{m},2} = \kappa g_{\mathrm{s},3}$ and $g_{\mathrm{mb},3} = (1-\kappa)g_{\mathrm{s},3}$, we can derive $\overline{i^2_{\mathrm{no},G_{\mathrm{i,f}}}}$ in terms of κ as

$$\overline{i^2_{\mathrm{no},G_{\mathrm{i,f}}}} = 2\overline{i^2_{\mathrm{n},1}}\left(\frac{1}{1+\kappa}\right)^2 + 2\overline{i^2_{\mathrm{n},3}}\left(\frac{\kappa}{1+\kappa}\right)^2. \tag{16}$$

To find $\overline{i^2_{\mathrm{no,cbf1}}}$, we first consider the bottom half of the current buffer in Fig. 9(a), whose block diagram is given in Fig. 9(b). Let $\overline{i^2_{\mathrm{no,bl}}}$ be the output current noise of this structure. It can be shown that

$$\overline{i^2_{\mathrm{no,bl}}} \approx 2\frac{\overline{i^2_{\mathrm{n,c1}}}}{N^2} + 2\overline{i^2_{\mathrm{n,c3}}}, \tag{17}$$

provided that $g_{\mathrm{m,c7}}(r_{\mathrm{o,c7}} \parallel r_{\mathrm{Ibp}})g_{\mathrm{m,c9}}r_{\mathrm{o,c3}} \gg 1$. In other words, virtually all the noises of M_{c1}-M_{c4} flow to the output of the current buffer while the noises of $M_{\mathrm{c7,8}}$, $M_{\mathrm{c9,10}}$, and the two I_{bp} current sources can be ignored. Similarly, for the top half of the current buffer—$M_{\mathrm{c5,6}}$, M_{c11}-M_{c14}, and the two I_{bn} current sources—only the noises of M_{c5} and M_{c6} need to be taken into account. As a result, the total output current noise of the current buffer can be approximated as

$$\overline{i^2_{\mathrm{no,cbf1}}} \approx 2\left(\frac{\overline{i^2_{\mathrm{n,c1}}}}{N^2} + \overline{i^2_{\mathrm{n,c3}}} + \overline{i^2_{\mathrm{n,c5}}}\right). \tag{18}$$

Next, we can find the total output voltage noise $\overline{v^2_{\mathrm{no,LPF}}}$ by substituting $\overline{i^2_{\mathrm{no},G_{\mathrm{i,f}}}}$ in (16) and $\overline{i^2_{\mathrm{no,cbf1}}}$ in (18) into the expression of $\overline{v^2_{\mathrm{no,LPF}}}$ in (15), and using the expression of G_f in (12) to obtain

$$\overline{v^2_{\mathrm{no,LPF}}} = \left[4\frac{\overline{i^2_{\mathrm{n},1}}}{g^2_{\mathrm{m},3}}\frac{1}{(1-\kappa)^2} + 4\frac{\overline{i^2_{\mathrm{n},3}}}{g^2_{\mathrm{m},3}}\left(\frac{\kappa}{1-\kappa}\right)^2 + \left(\frac{1+\kappa}{1-\kappa}\right)^2 \left(2\frac{\overline{i^2_{\mathrm{n,c1}}}}{g^2_{\mathrm{m},3}} + 2N^2\frac{\overline{i^2_{\mathrm{n,c3}}}}{g^2_{\mathrm{m},3}} + 2N^2\frac{\overline{i^2_{\mathrm{n,c5}}}}{g^2_{\mathrm{m},3}}\right)\right]\cdot\frac{1}{1+(f/f_\mathrm{f})^2}, \tag{19}$$

in which $\overline{i^2_{\mathrm{n},1}}$, $\overline{i^2_{\mathrm{n},3}}$, and $g_{\mathrm{m},3}$ refer to the noises of M_1 and M_3 and the transconductance of M_3 in either of the G_i or G_f OTA since the two OTAs are assumed identical and consume the same bias current. Due to its operation at low frequency, the lowpass filter is dominated by 1/f noise. Therefore, we can express the noise current of a transistor M_i in (19) as $\overline{i^2_{\mathrm{n,i}}} = K_{\mathrm{n(p)}}g^2_{\mathrm{m,i}}/(W_\mathrm{i}L_\mathrm{i}\cdot f)$, where $K_{\mathrm{n(p)}}$ is the 1/f noise coefficient of the n-type (p-type) transistor and $W_\mathrm{i}L_\mathrm{i}$ represents the gate area of M_i. Since the current in M_{c1} is the sum of the currents in M_3's of the G_i and G_f OTAs, we have $g_{\mathrm{m,c1}} = 2g_{\mathrm{m},3}$. Also, since the current in M_{c1} is N times the current in M_{c3}, we have $g_{\mathrm{m,c3}} = 2g_{\mathrm{m},3}/N$. And since M_1 and M_3 pass the same current, we have $g_{\mathrm{m},1} = g_{\mathrm{m},3}$. With some algebraic manipulations, we can simplify (19) into a compact form as

$$\overline{v^2_{\mathrm{no,LPF}}} = \left(\frac{K_\mathrm{p}}{A_{\mathrm{p,eff}}} + \frac{K_\mathrm{n}}{A_{\mathrm{n,eff}}}\right)\cdot\frac{1}{f}\cdot\frac{1}{1+(f/f_\mathrm{f})^2}, \tag{20}$$

where

$$A_{\mathrm{p,eff}} = \left(\frac{1-\kappa}{2}\right)^2(W_1L_1) \left\| \left(\frac{1-\kappa}{2\kappa}\right)^2(W_3L_3) \right\| \left(\frac{1-\kappa}{2\sqrt{2}\,(1+\kappa)}\right)^2(W_{\mathrm{c5}}L_{\mathrm{c5}}) \tag{21}$$

and

$$A_{\mathrm{n,eff}} = \left(\frac{1-\kappa}{2\sqrt{2}\,(1+\kappa)}\right)^2(W_{\mathrm{c1}}L_{\mathrm{c1}}) \left\| \left(\frac{1-\kappa}{2\sqrt{2}\,(1+\kappa)}\right)^2(W_{\mathrm{c3}}L_{\mathrm{c3}}). \right. \tag{22}$$

The parameters $A_{\mathrm{p,eff}}$ and $A_{\mathrm{n,eff}}$ in (20) can be thought of as the effective areas of all the combined noise-contributing p-type and n-type transistors in the lowpass filter, respectively—the gate areas of the noise contributing transistors are multiplied by appropriate coefficients before being combined in a parallel fashion—thus, they can provide some insight into which transistors have stronger effects on the overall noise of the lowpass filter: among the transistors of the same type and the same physical gate area, the one with smaller coefficient dominates the parallel combination, hence limiting how large $A_{\mathrm{p(n),eff}}$ can be. For $A_{\mathrm{p,eff}}$, with $\kappa \approx 0.7$, the coefficients of W_1L_1 and W_3L_3 are calculated to be 2.25×10^{-2} and 4.6×10^{-2}, respectively, while the coefficient of $W_{\mathrm{c5}}L_{\mathrm{c5}}$ is 3.89×10^{-3}; therefore, M_{c5} has stronger effect on the overall noise compared to M_1 and M_3. Thus, if noise reduction from the p-type transistors is desired, we should focus on increasing the physical gate areas of M_{c5}. For $A_{\mathrm{n,eff}}$, M_{c1} and M_{c3} have the same coefficient, which is also equal to the p-type M_{c5}'s.

B. Noise of the Weighted Sum Circuit

The noise analysis of the $G_{\mathrm{w1,2}}$ and G_{TIA} OTAs are similar to that of the G_i and G_f OTAs except for the additional noise of the output current mirrors (M_5-M_8 in Fig. 10(b) and 10(c)). Borrowing from (16) and incorporating the noise from M_5-M_8, we can express the output noise of the $G_{\mathrm{w1,2}}$ and the G_{TIA} OTAs as

$$\overline{i^2_{\mathrm{no},G_\mathrm{j}}} = 2\overline{i^2_{\mathrm{n},1}}\left(\frac{1}{1+\kappa}\right)^2 + 2\overline{i^2_{\mathrm{n},3}}\left(\frac{\kappa}{1+\kappa}\right)^2 + 2\overline{i^2_{\mathrm{n},5}} + 2\overline{i^2_{\mathrm{n},7}}, \tag{23}$$

where $j \in \{w1, w2, \mathrm{TIA}\}$ and $\overline{i^2_{\mathrm{n,i}}}$ is the output current noise of M_i in the respective OTA. The topology of the current buffer in

the TIA is similar to that in the lowpass filter, except that it does not have the input current mirrors (no M_{c1}-M_{c4} in Fig. 9(a)). Borrowing from (18) while discarding the noise from M_{c1}-M_{c4}, we can write an expression for the input-referred noise of the TIA's current buffer, $\overline{i^2_{\mathrm{ni,cbf2}}}$, as

$$\overline{i^2_{\mathrm{ni,cbf2}}} \approx 2\overline{i^2_{\mathrm{n,c5}}}. \tag{24}$$

Recall the chopping operation in Fig. 6. Assuming that the chopping frequency f_{ch} is higher than the 1/f noise corners of the $G_{\mathrm{w1,w2,TIA}}$ OTAs, we then only need to consider their thermal noise contributions—i.e., $\overline{i^2_{\mathrm{n,i}}} = 4kT\gamma g_{\mathrm{m,i}}$ where k is the Boltzmann's constant, T is the absolute temperature, and γ is the thermal noise excess factor. Since all the transistors in each OTA operate in subthreshold and carry the same bias current, we can approximate that their transconductances, and hence their thermal noise currents, are the same. Using (12) to write $g_{\mathrm{m,i}}$ in terms of G_{j}, we can write the current noise of each transistor as $\overline{i^2_{\mathrm{n,i}}} = 4kT\gamma G_{\mathrm{j}}(\frac{1+\kappa}{1-\kappa})$. Consequently, we can simplify (23) to

$$\overline{i^2_{\mathrm{no},G_{\mathrm{j}}}} = 4kT\gamma G_{\mathrm{j}} \cdot N_{\mathrm{G}}, \tag{25}$$

where $N_{\mathrm{G}} = 2(3\kappa^2 + 4\kappa + 3)/(1-\kappa^2)$; the total output noise of the G_{j} OTA in (25) can be interpreted as the sum of the noise currents from N_G devices, each with an effective transconductance of G_{j}.

Similarly, we can express $\overline{i^2_{\mathrm{ni,cbf2}}}$ in (24) in terms of G_{j}. Since the current in $M_{\mathrm{c5,6}}$ of the current buffer is equal to the sum of the currents of the $G_{\mathrm{w1,w2,TIA}}$ OTAs' input transistors, we can then write $g_{\mathrm{m,c5}} = \sum_j g_{\mathrm{m3,j}} = (\frac{1+\kappa}{1-\kappa})\sum_j G_{\mathrm{j}}$, where $g_{\mathrm{m3,j}}$ is the transconductance of M_3 in the G_{j} OTA. Substituting this $g_{\mathrm{m,c5}}$ into (24), we can express $\overline{i^2_{\mathrm{ni,cbf2}}}$ as

$$\overline{i^2_{\mathrm{ni,cbf2}}} \approx 4kT\gamma \left(\sum_{j\in\{\mathrm{w1,w2,TIA}\}} G_{\mathrm{j}} \right) \cdot N_{\mathrm{cbf2}}, \tag{26}$$

where $N_{\mathrm{cbf2}} = 2\cdot(1+\kappa)/(1-\kappa)$.

C. Optimization of the Overall MA Estimator's Noise

We will now derive the expression of the MA estimator's noise referred to the IA's input to understand how to optimize it. First, let's derive the output noise of the MA estimator by substituting (25) and (26) into (14) to obtain

$$\overline{v^2_{\mathrm{no,MA}}} = \overline{v^2_{\mathrm{no,LPF}}} \left(\frac{G_{\mathrm{w2}}}{G_{\mathrm{TIA}}}\right)^2 + \frac{4kT\gamma}{G_{\mathrm{TIA}}} \cdot \left(1 + \frac{G_{\mathrm{w1}}}{G_{\mathrm{TIA}}} + \frac{G_{\mathrm{w2}}}{G_{\mathrm{TIA}}}\right)(N_{\mathrm{G}} + N_{\mathrm{cbf2}}). \tag{27}$$

To refer this noise to the input of the IA, let A_{me} and A_{sig} be the gains from $\hat{V}_{\mathrm{ma}}$ to V_{oa} and from V_{im} to V_{oa} in Fig. 1, respectively. Then the MA estimator's noise referred to the IA's input, $\overline{v^2_{\mathrm{nIA,ME}}}$, can be calculated as $\overline{v^2_{\mathrm{nIA,ME}}} = \overline{v^2_{\mathrm{no,MA}}} \cdot (A_{\mathrm{me}}/A_{\mathrm{sig}})^2$. Thus, to make $\overline{v^2_{\mathrm{nIA,ME}}}$ small, we need to minimize the ratio $A_{\mathrm{me}}/A_{\mathrm{sig}}$ while still allowing the suppression of most of the MA in the input signal—i.e., $A_{\mathrm{me}}/A_{\mathrm{sig}}$ must still be large enough to allow $\hat{V}_{\mathrm{ma}}$ to suppress the strongest expected MA's amplitude, $V_{\mathrm{ma,max}}$, in the ECG signal. Let V_{L} be the linear range of the G_{TIA} OTA, which is assumed to be the largest value of $\hat{V}_{\mathrm{ma}}$ that the estimator can produce without significant distortion. The minimum value of $A_{\mathrm{me}}/A_{\mathrm{sig}}$ that still allows the estimator to suppress the MA in the input signal occurs when $V_{\mathrm{L}} \cdot A_{\mathrm{me}} \approx V_{\mathrm{ma,max}} \cdot A_{\mathrm{sig}}$. In other words, the minimum value of the ratio is given by

$$\left.\frac{A_{\mathrm{me}}}{A_{\mathrm{sig}}}\right|_{\mathrm{min}} \approx \frac{V_{\mathrm{ma,max}}}{V_{\mathrm{L}}}. \tag{28}$$

Writing $I_{\mathrm{B},G_{\mathrm{TIA}}} = G_{\mathrm{TIA}}V_{\mathrm{L}}$ [38], where $I_{\mathrm{B},G_{\mathrm{TIA}}}$ is the bias current of the G_{TIA} OTA, and assuming that $A_{\mathrm{me}}/A_{\mathrm{sig}}$ is chosen according to (28), we can write $\overline{v^2_{\mathrm{nIA,ME}}}$ as

$$\overline{v^2_{\mathrm{nIA,ME}}} = \overline{v^2_{\mathrm{no,LPF}}} \cdot \frac{(G_{\mathrm{w2}}V_{\mathrm{ma,max}})^2}{I^2_{\mathrm{B},G_{\mathrm{TIA}}}} + \frac{4kT\gamma}{I_{\mathrm{B},G_{\mathrm{TIA}}}} \cdot \frac{V^2_{\mathrm{ma,max}}}{V_{\mathrm{L}}} \cdot \left(1 + \frac{G_{\mathrm{w1}}}{G_{\mathrm{TIA}}} + \frac{G_{\mathrm{w2}}}{G_{\mathrm{TIA}}}\right)(N_{\mathrm{G}} + N_{\mathrm{cbf2}}). \tag{29}$$

The expression in (29) summarizes the noise contributions from the lowpass filter and the weighted sum circuit—i.e., the 1st and the 2nd terms on the right-hand side, respectively. It also suggests that the estimator's noise referred to the IA's input depends on the values of the weights after convergence ($G_{\mathrm{w1,2}}/G_{\mathrm{TIA}}$), the bias current of the TIA ($I_{\mathrm{B},G_{\mathrm{TIA}}}$), and the ratio of the expected maximum MA's amplitude to the maximum achievable output range of the estimator ($V_{\mathrm{ma,max}}/V_{\mathrm{L}}$). Table I provides typical values of the noise-determining parameters in (29). To show the relative importance of the two noise contributions, we plot the noise contribution of the lowpass filter (red trace) and that of the weighted sum circuit (blue trace) in Fig. 12 using the parameters in Table I. With the aide of the AC noise simulation, we assume that the output noise of the lowpass filter, $\overline{v^2_{\mathrm{no,LPF}}}$, follows the form $\overline{v^2_{\mathrm{no,LPF}}} = K/(f(1+f^2/f_{\mathrm{f}}^2))$; $K = 1.18 \times 10^{-8}\,\mathrm{V}^2$ and f_{f} is the 3-dB bandwidth of the lowpass filter, which is assumed to be 15 Hz for this work. Calculating the total noise from these two plots in the bandwidth from 0.1–100 Hz yields 2.8 $\mu\mathrm{V_{rms}}$ and 760 $\mathrm{nV_{rms}}$ for the lowpass filter and the weighted sum circuit, respectively, thus suggesting that the lowpass filter is the dominant noise source of the estimator.

An obvious approach to minimize $\overline{v^2_{\mathrm{nIA,ME}}}$ in (29) is to increase $I_{\mathrm{B},G_{\mathrm{TIA}}}$, but at the expense of higher power consumption. We might also be tempted to conclude that increasing V_{L} can significantly reduce $\overline{v^2_{\mathrm{nIA,ME}}}$ due to the smaller $A_{\mathrm{me}}/A_{\mathrm{sig}}$ that

TABLE I
TYPICAL PARAMETERS FOR THE CALCULATION OF THE ESTIMATOR'S NOISE

Parameters	Values
G_{w1}, G_{w2}	60 nA/V
G_{TIA}	100 nA/V
$I_{\mathrm{B,G_{TIA}}}$	100 nA
γ	1
κ	0.7
N_{G}	28.5
N_{cbf2}	11.33
V_{L}	1 V
$V_{\mathrm{ma,max}}$	20 mV

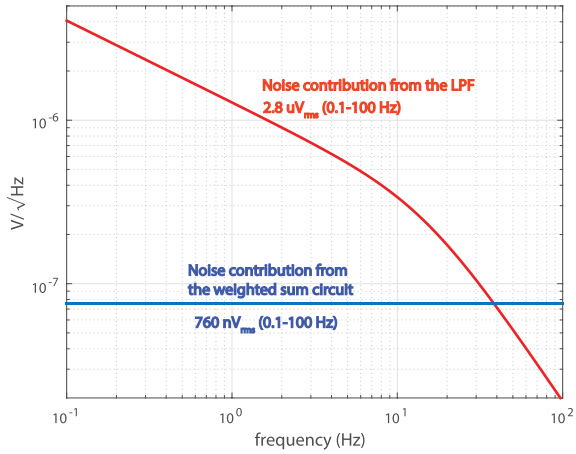


Fig. 12. Noise contributions of the lowpass filter and the weighted sum circuit to the IA's input-referred noise in (29).

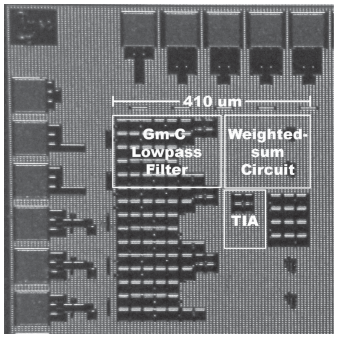
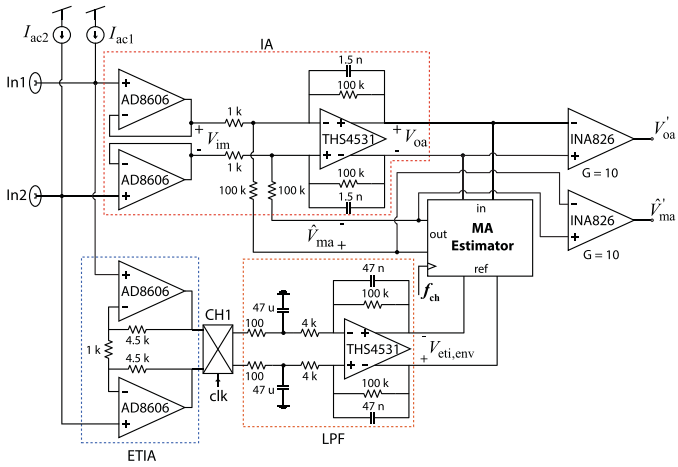
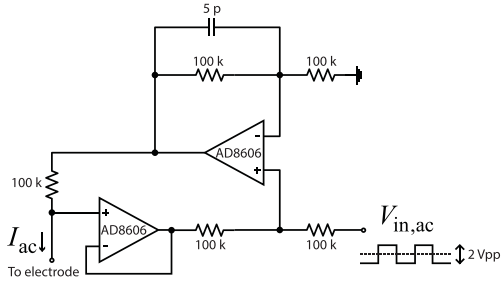


Fig. 13. Micrograph of the proposed MA estimator.



(a)



(b)

Fig. 14. (a) Schematic of the ECG acquisition system with real-time MA suppression capability. (b) Schematic of the AC current source for ETI extraction.

we can employ. However, increasing $V_{\rm L}$ raises both $\overline{v^2_{\rm no,LPF}}$ and $N_{\rm G}+N_{\rm cbf2}$, thus obscuring the noise reduction advantage. Nevertheless, the main benefit of increasing $V_{\rm L}$ is the larger allowable amplitude of the input into the MA estimator ($V_{\rm eti,env}$), thus allowing for a larger gain in the ETIA; this, in turn, results in smaller required weights $G_{\rm w1,2}/G_{\rm TIA}$ needed to suppress MA in the input signal and, subsequently, smaller $\overline{v^2_{\rm nIA,ME}}$. In this work, we opt for maximizing $V_{\rm L}$ to around 1 V by applying the source-degeneration and the bulk-input techniques to all the OTAs, such that the gain of the ETIA can be maximized. Such approach makes the dominant noise source of the MA reduction path be that of the ETIA, which should be relatively easy to design for low noise due to many well-known noise minimization techniques.

VI. Measurement Results

The proposed MA estimator was fabricated in a standard 0.18-μm CMOS process from the United Microelectronic Crop. (UMC). Fig. 13 shows the chip micrograph whose active area is 0.11 mm^2. The estimator operates from a 1-V supply and consumes a total bias current from 2.4 to 3.2 μA depending on the specific values of w_1 and w_2—measured by first turning off the adaptation algorithm, and then manually programming w_1 and w_2 to various values and probing by an electrometer (Keithley 6514) the total current consumed by the estimator. The objectives of this section are as follows:

1) Evaluate the estimator's performance on real-time MA suppression with ETI as a reference signal and explore the feasibility of signal reconstruction in the digital backend.
2) Evaluate the noise performance of the estimator.

To achieve the first objective, we have constructed an ECG acquisition system as proposed in Fig. 1—with our proposed MA estimator at its core—on a PCB, whose schematic is shown in Fig. 14(a). The IA consists of the unity-gain buffers (AD8606 from Analog Devices, Inc.), to provide high-impedance recording from the two electrodes, and the summing amplifier (THS4531, Texas Instruments Inc.), to superimpose the MA cancellation signal ($\hat{V}_{\rm ma}$) on the recorded ECG ($V_{\rm im}$) to suppress MA. The summing amplifier provides the signal-path gain $|A_{\rm sig}|=|V_{\rm oa}/V_{\rm im,d}|$ of 40 dB and the MA-cancellation-path gain $|A_{\rm me}|=|V_{\rm oa}/\hat{V}_{\rm ma}|$ of 0 dB to minimize the ratio $|A_{\rm me}/A_{\rm sig}|$ as discussed in Section V-C. The summing amplifier also provides lowpass filtering at 1 kHz to attenuate high-frequency noise without introducing a low-frequency pole in the MA suppression loop. The outputs of the summing amplifier ($V_{\rm oa}$) and the MA estimator $\hat{V}_{\rm ma}$ are then further amplified by an additional gain of 20 dB—making the overall gain of the signal path to be 60 dB—before being digitized by a 14-bit digital

oscilloscope (Analog Discovery 2, Digilent Inc.) to allow for signal reconstruction in the digital backend.

To extract ETI as a reference signal for the MA estimator, we incorporate two AC current sources, $I_{\rm ac1}$ and $I_{\rm ac2}$, which inject 20 $\mu{\rm V_{pp}}$ common-mode AC currents at 5 kHz into the two electrodes as discussed in Section II-C. Fig. 14(b) shows the schematic of each AC current source [40] whose output current, $I_{\rm ac}$, is related to the AC input voltage, $V_{\rm in,ac}$, by $I_{\rm ac} = V_{\rm in,ac}/100\,{\rm k}\Omega$. In our experiments, we used a 2-$\rm V_{pp}$ square wave for $V_{\rm in,ac}$ to produce 20-$\mu\rm V_{pp}$ square-wave current as the output of each AC current source. The resulting differential AC voltage from the two electrodes is then amplified by the ETI amplifier (AD8606 from Analog Devices, Inc.) whose gain is 20 dB before being demodulated to baseband by the chopper switch CH1 (TS5A23159, Texas Instruments Inc.). The output of the chopper switch is then filtered by a $2^{\rm nd}$-order lowpass filter (THS4531, Texas Instruments Inc.)—with a cutoff frequency of 33 Hz and a midband gain of 28 dB—to remove high-frequency noises and produce a clean ETI signal, $V_{\rm eti,env}$, as input into the MA estimator.

A. MA Suppression at Various Update Rates

To evaluate the estimator's performance at various algorithm's update rates, we connected the input of the ECG acquisition system in Fig. 14(a) to the experimenter's body in the lead-I configuration via standard Ag-AgCl electrodes. While the ECG acquisition system was recording ECG with the MA estimator running at a particular update rate, the experimenter pushed on the two electrodes alternately to generate a strong MA in the ECG waveform. Such experiment was performed at two different update rates—200 and 500 Hz—to illustrate how well at each update rate can the estimator attenuate MA. The outputs of the acquisition system, $V'_{\rm oa}$, and the estimator, $\hat{V}'_{\rm ma}$, were recorded by a 14-bit digital oscilloscope (Analog Discovery 2, Digilent, Inc.) at 6 kS/s. To mimic the use of a moderate-resolution/speed ADC (8-bit) in acquiring the data, we discarded six least significant bits and downsampled the two signals to a data rate of 600 S/s before plotting the results in Fig. 15(a) and 15(b).

The blue traces in Fig. 15(a) and 15(b) show the resulting $V'_{\rm oa}$ referred to the input of the acquisition system (normalized by a gain of 1000 V/V) while the red traces show $\hat{V}'_{\rm ma}$ referred to the output of the MA estimator (normalized by a gain of 10 V/V). To obtain the original input into the ECG acquisition system, we linearly combined $V'_{\rm oa}$ and $\hat{V}'_{\rm ma}$—with the sampling rate for both signals of 6 kS/s—with the appropriate signal-path and MA-cancellation-path gains to reconstruct $V_{\rm im}$ shown as the orange traces in Fig. 15(a) and 15(b). We can see in both of these cases that whenever $\hat{V}'_{\rm ma}$ exhibits a good correlation with $V_{\rm im}$—as when the red traces effectively track the orange traces—the baseline variations in $V'_{\rm oa}$ are strongly suppressed. Also, compared to when the update rate is 200 Hz, $\hat{V}'_{\rm ma}$ seems to track $V_{\rm im}$ better when the update rate is 500 Hz, which results in better suppression of MA in the recorded $V'_{\rm oa}$. However, the faster update rate also results in the more ringing (the high-frequency ringing seen in the $V'_{\rm oa}$ curve of Fig. 15(b)) in the output waveform—a result of the sign-sign LMS algorithm trying to follow noise even after the algorithm has converged. The ringing is normally small, thus does not affect the linearity of the output. Moreover, the information on the ringing is already contained in $\hat{V}'_{\rm ma}$, which we can later use to calibrate out the ringing in the output signal. This issue will be addressed next.

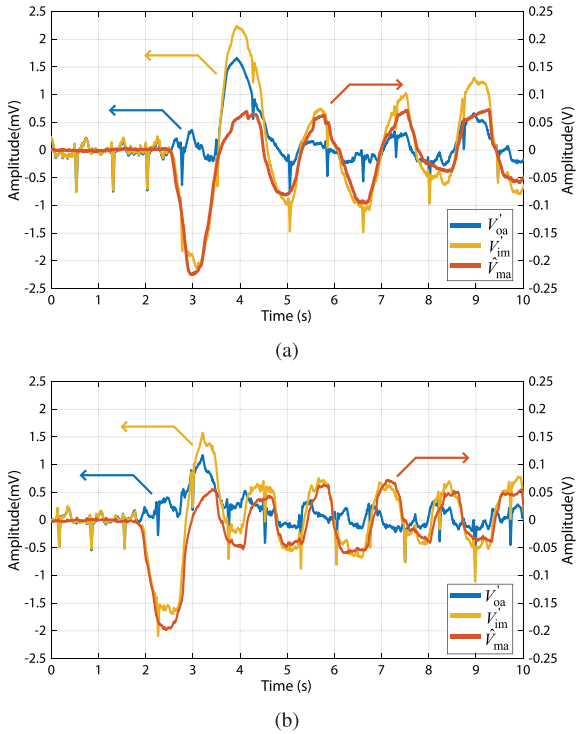


Fig. 15. Real-time MA suppression at the estimator's update rates of: (a) 200 Hz (b) 500 Hz.

B. Signal Reconstruction

In addition to the ringing artifact, imperfect correlation between MA and ETI due to nonlinearities in the MA generation process, and distortions introduced by the estimator itself may distort the ECG waveform. Thus, we should not view the proposed topology as a perfect mean to remove MA from the recorded ECG. Instead, the estimator is aimed to provide MA suppression to reduce the system's input DR, while allowing for the preservation of the original input signal. Fortunately, in the proposed scheme of Fig. 1, the MA estimator's output, $\hat{V}_{\rm ma}$, contains all the information subtracted from the original input signal. Thus, we can reconstruct the original input signal by combining, with appropriate scaling, $V_{\rm oa}$ and $\hat{V}_{\rm ma}$ in the digital backend. Also, due to the low-frequency nature of the MA (normally <2 Hz), $\hat{V}_{\rm ma}$ may be sampled at a relatively low sampling rate compared to $V_{\rm oa}$'s to help reduce the ADC's power overhead from digitizing additional signal.

Using the recorded $V'_{\rm oa}$ and $\hat{V}'_{\rm ma}$ from the experiment with the 500-Hz algorithm's update rate, we have reconstructed the

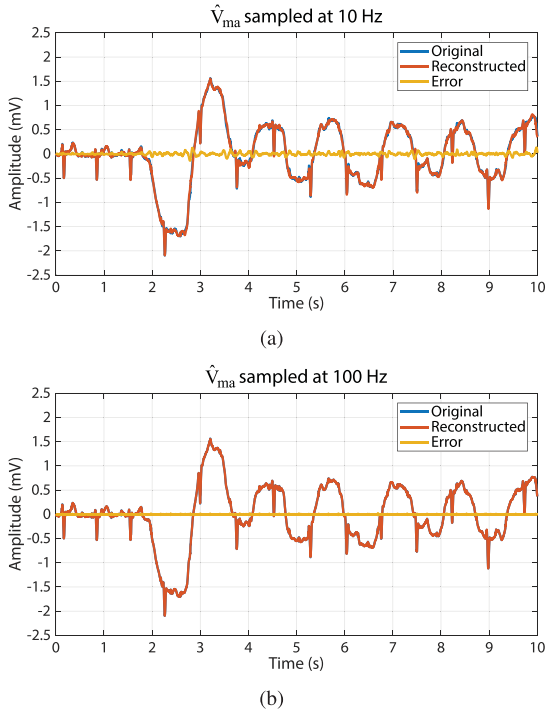


Fig. 16. Reconstructed input into the acquisition system when $\hat{V}'_{\rm ma}$ is sampled at: (a) 10 Hz (b) 100 Hz.

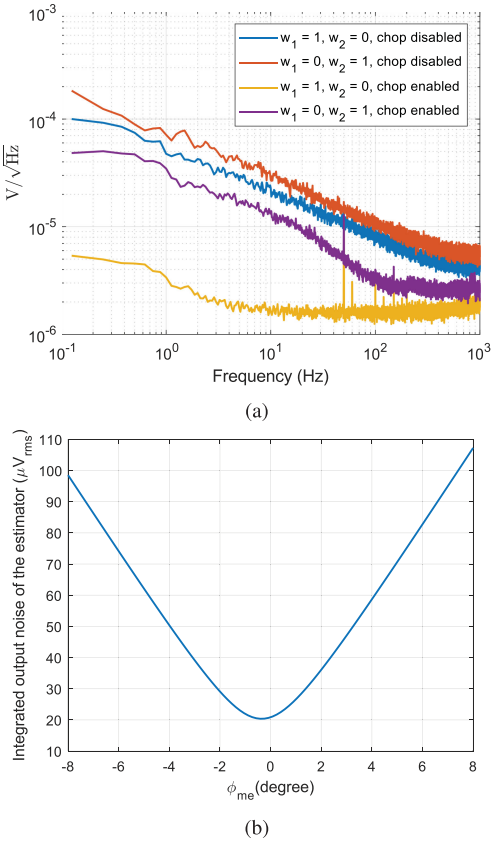


Fig. 17. (a) The MA estimator's output noise PSDs at different conditions (b) Total integrated output noise as a function of the estimator's phase shift.

input into the ECG acquisition system shown as the red traces in Fig. 16(a) and 16(b) with $\hat{V}'_{\rm ma}$ being sampled at 10 Hz and 100 Hz, respectively. $V'_{\rm oa}$ is always sampled at 600 Hz for both cases. The original signal is shown as blue traces in both plots—though barely visible as they are obscured by the reconstructed signal (red traces). The reconstruction errors for the $\hat{V}'_{\rm ma}$'s sampling rates of 10 Hz and 100 Hz are 27.92 and 3.27 $\mu{\rm V_{rms}}$, respectively. The result shows that both sampling rates result in successful reconstructions of the original signal, though the 10-Hz sampling rate exhibits larger reconstruction error.

C. Noise Performance

The integrated output noise of the estimator depends on the values of w_1 and w_2 after convergence. If little phase shift is required in the mapping ($w_1 \gg w_2$), the total noise is due mainly to the $G_{\rm w1}$ OTA and the TIA, which is mostly thermal due to the chopping operation; however, if the mapping requires a significant phase shift ($w_1 \ll w_2$), the estimator's noise will be dominated by the flicker noise of the lowpass filter. To depict the estimator's noise performance at all possible pairs of w_1 and w_2, we did the following: First, we measured the estimator's output noise at the two extremes—i) $w_1 = 1$ and $w_2 = 0$ (thermal noise dominant) and ii) $w_1 = 0$ and $w_2 = 1$ (flicker noise dominant). In the first case, the first term in (27) is nullified, making $\overline{v^2_{\rm no,MA}} \approx \frac{8kT\gamma}{G_{\rm TIA}}(N_{\rm G} + N_{\rm cbf2})$. In the second case, we assume that the first term in (27), which is flicker noise dominant, overwhelms the second term. Hence, with $w_2 = G_{\rm w2}/G_{\rm TIA} = 1$, we can approximate that $\overline{v^2_{\rm no,MA}} \approx \overline{v^2_{\rm no,LPF}}$.

Fig. 17(a) shows the power spectral densities (PSD) of the MA estimator's output noise ($\overline{v^2_{\rm no,MA}}$) from a dynamic signal analyzer (SR785 Stanford Research Systems) for the $(w_1 = 1, w_2 = 0)$ and $(w_1 = 0, w_2 = 1)$ cases, both when the chopping operation is disabled and enabled. It is evident that, with the chopping disabled, the noise PSDs in both cases are dominated by flicker noise (blue and red curves). With the chopping enabled, however, the noise PSD of the $(w_1 = 1, w_2 = 0)$ case is mostly thermal, with the 1/f noise corner well below 10 Hz (yellow curve). However, for the $(w_1 = 0, w_2 = 1)$ case in which the flicker noise of the lowpass filter can still pass through $G_{\rm w2}$ OTA to the output, the flicker noise is dominant up to around 150 Hz (purple curve). Integrating the two curves (chopping-enabled) from 0.1 Hz to 150 Hz yields the total integrated noise of 20.3 and 91.18 $\mu{\rm V_{rms}}$ for $(w_1 = 1, w_2 = 0)$ and $(w_1 = 0, w_2 = 1)$ cases, respectively. To estimate the total integrated noise for other sets of w_1 and w_2, we can calculate the weighted sum of the noise power using (27). Fig. 17(b) shows the integrated output noise of the MA estimator for w_1 and w_2 in Fig. 5(b) in which the MA estimator provides a gain of unity and a phase shift between $\pm 8^\circ$. As expected, small phase shift results in minimal integrated noise while large phase shift results in higher integrated noise due to the more noise contribution from the lowpass filter. The maximum integrated noise is 106 $\mu{\rm V_{rms}}$ at $\phi_{\rm me} = 8^\circ$ while the minimum integrated noise is 19.7 $\mu{\rm V_{rms}}$ at $\phi_{\rm me} = -0.4^\circ$.

TABLE II
PERFORMANCE SUMMARY AND COMPARISON TO PREVIOUS WORK

Ref.	This work	[24]
Tech. (μm)	0.18	Off-Chip (MSP430 MCU)
LMS variants	Sign-Sign LMS	Standard LMS
Adaptive filter's order	2	4
Delay element	G_{m}-C	Digital delay line
Cancellation scheme	TIA to AFE	12-bit DAC to PGA
AFE integration	Off-chip	On-chip
Estimator's power	3.2 μW (max)	NA*
Loop latency	2 ms (500-Hz update rate)	10 ms

* The power of the 12-bit DAC and MSP430 MCU were not reported.

The estimator's noise referred to the input of the recording system depends on the values of A_{me} and A_{sig} used—i.e., we have to scale the plot in Fig. 17(b) by $A_{\mathrm{me}}/A_{\mathrm{sig}}$. If we assume a typical value of $V_{\mathrm{ma,max}} \approx 20$ mV, the required $A_{\mathrm{me}}/A_{\mathrm{sig}}$ for the proposed estimator with $V_{\mathrm{L}} \approx 1$ V is just 1/50. Hence, the estimator's noise referred to the input of the recording system will range from 0.39 to 2.12 $\mu\mathrm{V}_{\mathrm{rms}}$, still an insignificant fraction of the input noise required by the standard in ECG acquisition [41].

One interesting question remains as to how the noises of other circuits in the ETI extraction path affect the quality of the recorded ECG. Due to the high gain of the ETIA required to produce a full-swing $V_{\mathrm{eti,env}}$, the ETIA's noise is the dominant noise source of the ETI extraction path. However, to keep the ETIA's noise referred to the main IA's input sufficiently low, it is important to avoid using too large an ETIA's gain. Nevertheless, it is difficult to pinpoint an optimal value of the ETIA's gain as this depends on many factors such as the magnitude and frequency of the AC currents injected into the electrodes, and the values of electrode impedances during the measurement; all these factors affect the amplitude of the input ETI signal, making the design and the optimization of the ETI extraction path an interesting active research area.

VII. CONCLUSION

We present the design of a compact low-power MA estimator to help reduce the input dynamic range of wearable ECG acquisition systems. By employing a simple OTA-C lowpass filter, clocked comparators, digital counters, switches, and other analog building blocks, the estimator performs linear filtering to derive a cancellation signal from an ETI reference, which can then be fed back to cancel with the MA near the system's input. Since the estimator aims to cancel MA right at the acquisition system's input, its noise can be a major concern. Table II summarizes the performance of the estimator compared to the state-of-the-art. In this paper, we also present a detailed analysis of the estimator's noise performance and provide recommendations on how to incorporate it into an ECG acquisition system without much noise penalty. To the best of the authors' knowledge, this work is the first on-chip motion artifact estimator to help suppress MA near the system's input before final amplification. Due to its low power consumption and small area, the estimator is suitable for local placement at each recording channel, thus attractive for use in multi-channel ECG acquisition systems.

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Appendix C

A 2.64-μW 71-dB SNDR Discrete-Time Signal-Folding Amplifier for Reducing ADC's Resolution Requirement in Wearable ECG Acquisition Systems

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***Abstract*—This paper presents the design of a low-power discrete-time signal-folding amplifier intended for use in place of programmable-gain amplifiers (PGA) in electrocardiogram (ECG) acquisition systems. The amplifier provides a fixed high gain while preventing output signal saturation even with rail-to-rail inputs, thanks to the proposed discrete-time signal folding technique; the fixed gain eliminates the need of gain-control circuitry while the high gain helps relax the resolution requirement of the analog-to-digital converter (ADC) that follows, thus resulting in lower power consumption and design complexity for the ADC. Fabricated in a standard 0.18-μm CMOS process, the amplifier occupies an active area of 0.254 mm^2 and consumes 2.64 μW from a 1.2-V supply voltage. While amplifying a rail-to-rail input (2.4 V_{pp} differential) with a gain of 17.8 V/V, the amplifier achieves a signal-to-noise-plus-distortion ratio (SNDR) of 71 dB, thus making it very attractive for high-fidelity ECG recording amid large input interferences.**

***Index Terms*—ECG acquisition system, high signal-to-noise-plus-distortion ratio, mains interference, motion artifact, programmable-gain amplifier, signal-folding amplifier, switched-capacitor amplifier.**

I. Introduction

In RECENT years, cardiovascular diseases (CVDs) have become by far the leading cause of death among the world population, with the death rate more than twice that of all cancer types combined [1]. Moreover, with many countries being in the transition into aging/aged societies, the proportion of health ailments and deaths due to CVDs will inevitably increase in the near future, hence, putting severe pressure on institutions and personnel responsible for treating CVDs. It has been projected that the cost of treating CVDs will likely triple by the year 2030 [2].

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Electrocardiogram (ECG)—the heart's electrical signal measured from the body's surface—is considered one of the most important vital sign in the diagnosis and treatment of CVDs. Traditionally performed at fully-equipped health centers by bulky ECG stations, the measurement of ECGs are now being transformed toward the use of wearable, personalized devices intended for continuous monitoring with real-time networking and analysis capabilities—thanks to the advances in microelectronics, communication, and artificial intelligence. If fully developed and widely adopted by the mass, such devices can pave new ways for the remote monitoring and diagnosis of the heart, thus providing the general public access to state-of-the-art diagnostic tools without the need for frequent hospital visits. Such technology will not only save lives but will also reduce healthcare costs and alleviate the problem of personnel shortage in treating CVDs.

For such devices to become ubiquitous, they must be low-price, robust, and comfortable to wear. For the device to be low-price, its circuitry should be fully integrated to reduce the number of external components and the overall power consumption; the latter, in turn, helps reduce the battery's size, which is a crucial cost-determining factor in most electronics. However, low-power consumption requires that the device operate from a limited supply, thus putting a severe limit on the input range of the signal being recorded. For wearing comfort, the devices must be able to record from high-impedance electrodes—dry, noncontact [3], which we will collectively call high-Z electrodes—instead of from just the conventional gel electrodes, which may cause skin irritation after prolonged use. However, high-Z electrodes pose serious concerns on the quality of the recorded signal. First, high-Z electrodes are not as effective for use as grounding electrodes compared to the low-impedance gel electrodes, thus resulting in larger common-mode mains interference on the body. Second, as for recording, high-Z electrodes make the recording systems whose input impedances are not sufficiently high more prone to electrode mismatch, which can cause common-mode-to-differential-mode (CM-to-DM) conversion of the mains interference. Such CM-to-DM conversion may result in large differential mains interference at the device's input [4]–[6]. Finally, high-Z electrodes with impedances consisting of mostly the capacitive part are more

prone to motion artifacts (MA) [7], [8], which can severely increase the input dynamic range (DR) of the device. All these aggressors may lead to signal saturation if a high gain is used in the amplification chain, thus reducing the reliability and robustness of the ECG monitoring device.

To accommodate this increased input DR, most existing systems [9]–[14] utilize programmable-gain amplifiers (PGAs) in their signal chains to ensure the appropriate amplification of the input signal to suit the ADC's input range. With small input, as in the absence of interference, the PGA's gain can be maximized such that the high overall channel gain helps mitigate the ADC's noise contribution. Conversely, with large input, as in the presence of strong interferences, the PGA's gain can be minimized to prevent signal saturation in the amplification stage. In most commercial systems ([9], [10]), the total channel gains are quite low—1–12 V/V in [9] and 20–160 V/V in [10]—thus necessitating the use of high-resolution ADCs (24 and 18 bits in [9] and [10], respectively) at the cost of high per-channel power consumption (335 and 85 μW in [9] and [10], respectively). To reduce power consumption, other works [11]–[14] employ higher channel gains (up to 300 V/V in [12] and 1,300 V/V in [11]) to allow for lower resolutions of the ADCs.

Nevertheless, there are two drawbacks to the use of PGA in the readout system. First, for optimal performance, the PGA requires an additional automatic gain-control circuitry, thus increasing the overall system's complexity, power consumption, and silicon area; as the commercial systems in [9], [10] require external gain setting, external microcontrollers will need to be integrated at the printed-circuit-board (PCB) level to incorporate automatic gain control features into the final readout systems. Second, even with programmable gain, the ADC's resolution is often determined by the worst case (that of the lowest gain setting)—i.e., all the works in [11]–[14] use ADCs with resolutions from 11–14 bits to ensure that the noise contributions from the ADCs remain negligible even at the lowest gain settings. As a result, the ADC in each system often consumes higher power consumption and occupies a larger area than necessary.

To minimize the system's complexity and power consumption, it is advantageous to replace the PGA by a fixed high-gain amplifier as a 2$^{\text{nd}}$-stage amplifier. Fixed gain eliminates the need for automatic gain-control circuitry while high gain mitigates the noise/distortion requirement of the ADC, permitting the use of an ADC with low-to-moderate resolution without degrading the signal-to-noise ratio (SNR). The major challenge of employing a high overall gain in the amplification stage, especially in low-voltage low-power systems, is the risk of signal saturation at the output of the 2$^{\text{nd}}$-stage amplifier. Interestingly, there is a technique first introduced in [15] for ECG acquisition and, subsequently, in [16] for neural signal recording that utilizes a concept of signal folding to allow the use of high gain in the analog front-ends (AFEs) while avoiding output signal saturation. The signal-folding scheme employs feedback to monitor the output level and fold it back to the common-mode value whenever it is about to cross a threshold such that no output saturation occurs. The folded output sampled by an ADC can then be reconstructed in the digital backend to provide the original (effective) output signal. Such method allows the effective output swing to significantly exceed the supply voltage, thus permitting larger gain than normally possible in the conventional scheme.

Nevertheless, there are several drawbacks in applying the signal-folding scheme to the AFE, instead of in a later amplifier stage. First, most AFEs usually operate in a continuous-time fashion to prevent noise folding from the sampling operation. Hence, the signal folding scheme applied to such AFEs requires continuous-time detection of the appropriate folding instants, which is proved to be susceptible to various nonidealities—such as input noise, charge injections, and delays from the operational transconductance amplifiers (OTAs) or the comparators. As a result, sophisticated reconstruction algorithms are often required, which, unfortunately, lead to poor signal-to-noise-and-distortion ratio (SNDR) at large input amplitudes. For the amplifier in [15], even with only 1 $\mu\mathrm{V_{rms}}$ input noise, the SNDR of the reconstructed output signal from a 20-Hz sinusoidal input saturates to around 40 dB when the amplitude of the input is only around 2 mV. In [16], for a 30-Hz sinusoidal input signal, the SNDR of the output signal saturates to a value less than 30 dB even when the input amplitude is lower than 1 $\mathrm{mV_{pp}}$. The two mentioned performances are equivalent to attempting to resolve tiny ECG waveforms amid large differential interferences with ADCs whose effective-number-of-bits (ENOB) are only 6.35 and 4.7 bits, respectively. Hence, significant improvement is needed.

Another drawback in applying the signal-folding technique to the AFE is that if the folding mechanism is implemented at the input, the resulting circuit's nonidealities may degrade the SNDR, or even compromise the user's safety. For example, the design in [15] employs current-mode digital-to-analog converters (DACs) and resistors to implement programmable floating battery voltages in series with the input terminals of the AFE as a mean to introduce appropriate differential offset voltage to the input to keep the output within the threshold. Unfortunately, mismatches in the current DACs result in large input offset currents, reported to be as large as 58 nA, which can cause large DC offset voltage and high filtered shot noise especially when the AFE is interfaced with high-Z electrodes.

To avoid all these drawbacks, we propose in this work a discrete-time amplifier with a fixed high gain intended to follow a high-gain AFE to maximize the total gain of the amplification stage. The proposed amplifier employs a switched-capacitor gain topology [17] since its feedback nature provides excellent linearity even at large output amplitude. To prevent output saturation due to large input interference, we employ a discrete-time signal-folding scheme, which can be naturally integrated into the switched-capacitor gain circuit and is more immune to circuit nonidealities than its continuous-time variants presented in the existing works. Operating from a 1.2-V supply and consuming only 2.2 μA of bias current while driving a 5-pF capacitive load—assumed to be the capacitive load of the next-stage ADC—the proposed amplifier provides a gain of 17.8 V/V, a noise floor of 150 $\mu\mathrm{V_{rms}}$, and an SNDR of 71 dB when amplifying a rail-to-rail (2.4 $\mathrm{V_{pp}}$) 30-Hz sinusoidal input. The proposed amplifier is part of a high-gain ECG acquisition system proposed

in [18]. In this work, we provide thorough explanations, analysis, and present more detailed measured results to fully illustrate its performances.

The paper is organized as follows. Section II discusses the motivations behinds the use of a high-gain 2nd-stage amplifier to reduce the resolution requirement of the ADC. Section III explains the overall operation of the proposed amplifier and the designs of its building blocks. Section IV derives the amplifier's input-referred noise to pinpoint important parameters for noise optimization. Section V shows the measured performances of the amplifier and Section VI concludes the paper.

II. General Considerations

To be useful in clinical applications, the ECG monitoring device should at least be able to resolve the smallest feature of the ECG waveform—i.e., the P-wave whose amplitude rarely exceeds 0.25 $\mathrm{mV_{pp}}$ [19]. To be conservative, we will just assume that the amplitude of the P wave is on the order of 0.1 $\mathrm{mV_{pp}}$ and, to resolve this P wave, the device should be able to quantize it to at least 5 quantization levels, resulting in the width of each quantization level of around 20 $\mu\mathrm{V_{pp}}$. For the device to achieve such resolution, let us assume that its peak-to-peak input-referred noise-and-distortion (NAD) should be smaller than this quantization level. Consequently, assuming that such NAD follows the Gaussian distribution for simplicity, we can estimate the root-mean-square (rms) input-referred NAD of the acquisition system from $V_{\mathrm{ni,rms}} < 20\ \mu\mathrm{V_{pp}}/6 \approx 3.33\ \mu\mathrm{V_{rms}}$.

Given the specification of around 3 $\mu\mathrm{V_{rms}}$ input-referred NAD, how do we appropriately determine a suitable gain for the amplification stage and a suitable ADC's resolution? An ADC with the resolution too high wastes power and area, while an ADC with the resolution too low degrades the SNDR of the desired ECG. Let us consider a general ECG acquisition system in Fig. 1(a) consisting of an amplification stage with a total gain of A_{v} followed by an ADC. Let V_{FS} and ENOB be the ADC's full-scale voltage and the effective-number-of-bits, respectively. The ADC's NAD referred to the input of the acquisition system ($V_{\mathrm{ni,ADC,rms}}$) can be calculated from

$$V_{\mathrm{ni,ADC,rms}} = \frac{1}{A_{\mathrm{v}}} \cdot \frac{V_{\mathrm{FS}}}{2^{\mathrm{ENOB}}\sqrt{12}}. \tag{1}$$

Fig. 1(b) plots the required ENOB as a function of A_{v}—in the range of 120 V/V to 2400 V/V for $V_{\mathrm{FS}} = 2.4$ V (typical for a fully-differential ADC operating from a 1.2-V supply)—to make $V_{\mathrm{ni,ADC,rms}}$ equal to 3 $\mu\mathrm{V_{rms}}$. The chosen range of A_{v} is determined from two extremes. On one extreme, the input interference is very strong ($\approx 20\ \mathrm{mV_{pp}}$) such that A_{v} can be at most 120 V/V to keep the output of the amplification stage within the 2.4-V full-scale voltage of the ADC. On the other extreme, the input interference is not present such that A_{v} can be made as large as 2,400 V/V to amplify 1-$\mathrm{mV_{pp}}$ ECG to the full-scale voltage of the ADC. Notice that such range of A_{v} results in the range of ENOB from 10.9 bits ($A_{\mathrm{v}} = 120$ V/V) down to 6.6 bits ($A_{\mathrm{v}} = 2,400$ V/V). For successive-approximation-register (SAR) ADCs, preferable in this application due to its excellent energy efficiency, the power consumption and area of the capacitive digital-to-analog converter (DAC) increase as an exponential function of the ENOB. Therefore, the span of the required ADC's resolution by more than 4 bits gives a strong motivation to maximize the gain of the amplification stage such that the ADC's ENOB can be minimized to save power and area.

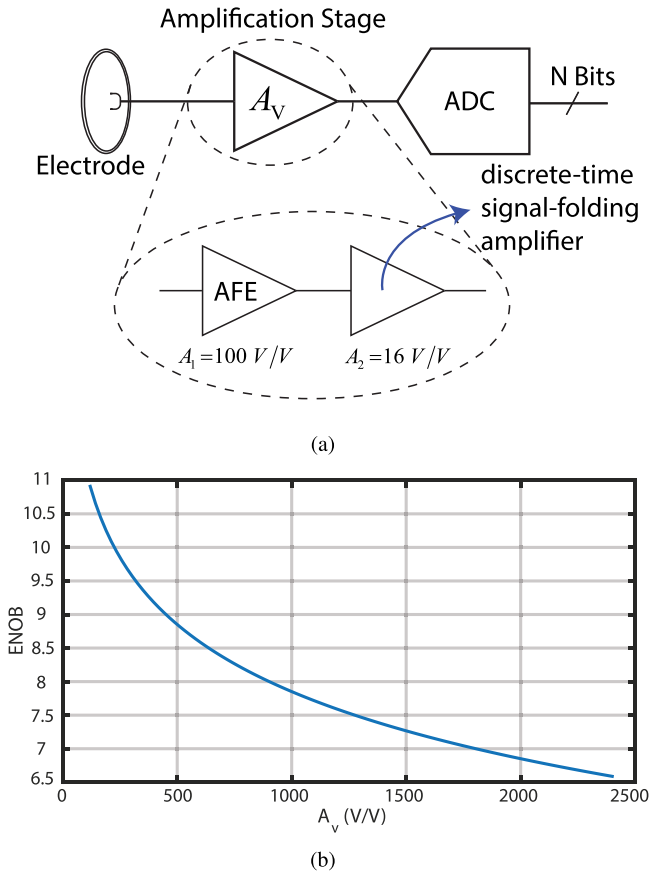

Fig. 1. (a) Consideration for the gain of the amplification stage and the required ADC's resolution. (b) The required ADC's ENOB as a function of A_{v} to keep the ADC's NAD referred to the acquisition system's input equal to 3 $\mu\mathrm{V_{rms}}$.

To maximize the gain of the amplification stage, we propose the use of a discrete-time signal-folding amplifier to follow a fixed-gain AFE, as shown in the inset of Fig. 1(a). The main objective of the proposed amplifier is to provide a very wide effective output swing, thus allowing for a very high gain in the amplification stage, while keeping the physical output swing within the input range of the ADC. Besides, the proposed amplifier should provide excellent linearity at large output amplitude to ensure that distortions due to large input interference do not degrade the SNDR of the desired ECG signal. Since the proposed amplifier is to follow an AFE, its noise and distortion requirement can be mitigated if the AFE's gain is sufficiently high. In this work, we will assume that the AFE exhibits a gain of 100 V/V and a maximum output swing of 2 $\mathrm{V_{pp}}$, which allows the maximum differential interference's amplitude at the input of the acquisition system to be as high as 20 $\mathrm{mV_{pp}}$ without saturating the AFE's output range. The gain of the proposed amplifier is chosen to be 16 V/V, resulting in the overall amplification stage's gain of 1600 V/V. According to Fig. 1(b),

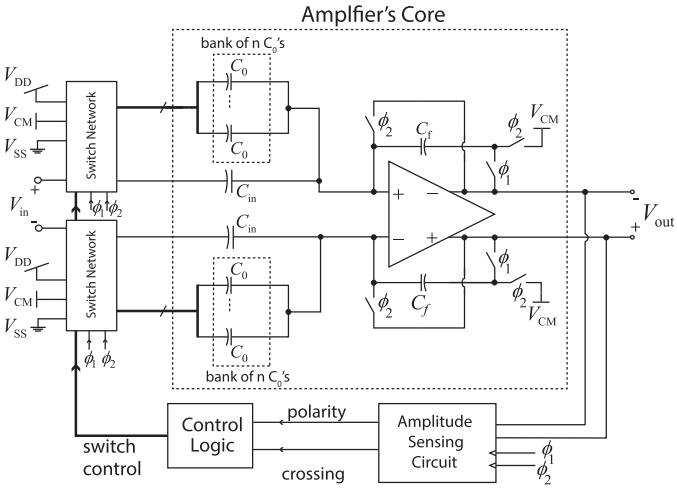

Fig. 2. High-level schematic of the proposed discrete-time signal-folding amplifier.

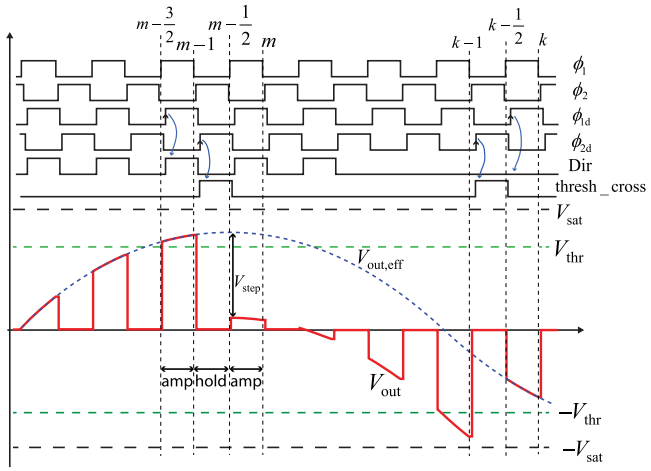

Fig. 3. A timing diagram showing the signal-folding operation of the proposed amplfier.

such total gain results in the required ADC's ENOB of less than 8 bits to keep the overall noise of the acquisition system within our specification. Many ADCs with 8-bit resolution have been demonstrated to achieve ultra-low-power operation and compact area [20]–[24], which can be readily applied to our application.

III. Circuit Operation

Fig. 2 shows the high-level schematic of the proposed discrete-time signal-folding amplifier whose core is the switched-capacitor gain circuit with the input capacitor banks—each consisting of an input capacitor $C_{\rm in}$ and an offset capacitor bank with n units of offset capacitor C_0—and the feedback capacitors $C_{\rm f}$'s. Around this core are the amplitude sensing circuit, the control logic, and the switch networks for performing the signal-folding operation. The amplifier's core functions as a switched-capacitor gain circuit [17], [25], with the input capacitance $C_{\rm in}$ and the feedback capacitance $C_{\rm f}$ setting the closed-loop gain of the circuit to $C_{\rm in}/C_{\rm f}$. To check if the amplifier's output is exceeding the valid range, the amplitude sensing circuit compares the value of the amplifier's output $V_{\rm out}$ to the predefined (upper/lower) thresholds. If $V_{\rm out}$ has exceeded either of the thresholds—i.e., lower than the lower threshold or higher than the upper threshold—the amplitude sensing circuit then instructs the control logic to appropriately configure the switch networks to add appropriate offset charges into the offset capacitor banks. These offset charges will then be added to charges in the input capacitors $C_{\rm in}$'s when the amplifier is amplifying the input $V_{\rm in}$ such that $V_{\rm out}$ becomes centered at zero, instead of further exceeding the valid output range. By tracking the state of the control logic and, hence, the added offset voltages, we can unwind (reconstruct) $V_{\rm out}$ to its original value in the digital backend, as will be described in Section V-A.

In addition to its excellent linearity and the convenience in introducing the input offset voltage, its sampling nature allows the proposed amplifier to function as a time-multiplexed amplifier, which can simultaneously amplify many input signals; this can be beneficial in multi-channel ECG recording in which the 2nd-stage amplifier takes inputs from many AFEs, or when the ECG acquisition system acquires other information such as the electrode impedance for use in motion artifact suppression [12]; in such cases, one amplifier can be shared to amplify many signals, thus saving area. Furthermore, in contrast to the design in [16] which requires high-resistance elements to set the DC bias point at the opamp's input terminals—which results in low-frequency drift due to the leakage current of the high-resistance elements—the proposed amplifier does not suffer from such drift as it does not use any high-resistance element.

A. Addition of Input Offset Voltage

Next, let us understand how the proposed amplifier amplifies the input while simultaneously constraining $V_{\rm out}$ to within a predefined output range to prevent output signal saturation. The operation of the amplifier can be divided into two phases—1) the amplifying phase and 2) the hold (offset addition) phase—which can be understood by an aid of the timing diagram in Fig. 3. The clocks ϕ_1 and ϕ_2 are two non-overlapping clocks, with ϕ_1 and ϕ_2 being high indicating the amplifying phase and the hold phase, respectively. The signal $V_{\rm out,eff}$ (dashed trace) represents the effective output signal of the amplifier if the input $V_{\rm in}$ was amplified by an ideal amplifier with a gain of $C_{\rm in}/C_{\rm f}$, while the signal $V_{\rm out}$ (red trace) represents the physical output of the proposed amplifier. Notice that the physical output is constrained to within $\pm V_{\rm thr}$ about zero by the signal-folding operation.

First, let us consider the time before the amplifying phase ending at $t = m - 1$ in Fig. 3 in which $V_{\rm out}$ resides comfortably within the upper and lower thresholds ($\pm V_{\rm thr}$) and, hence, the control logic (and the switch networks) does not add any offset charges to the offset capacitor banks to constrain $V_{\rm out}$, resulting in $V_{\rm out}$ just following $V_{\rm out,eff}$ as in regular switched-capacitor amplifiers. However, during the amplifying phase ending at $t = m - 1$ ($t \in [m - \frac{3}{2}, m - 1]$), the amplitude sensing circuit detects that $V_{\rm out}$ has already exceeded $+V_{\rm thr}$. Thus, in the next hold phase ($t \in [m - 1, m - \frac{1}{2}]$), the control logic instructs the switch networks to add appropriate offset charges into the offset

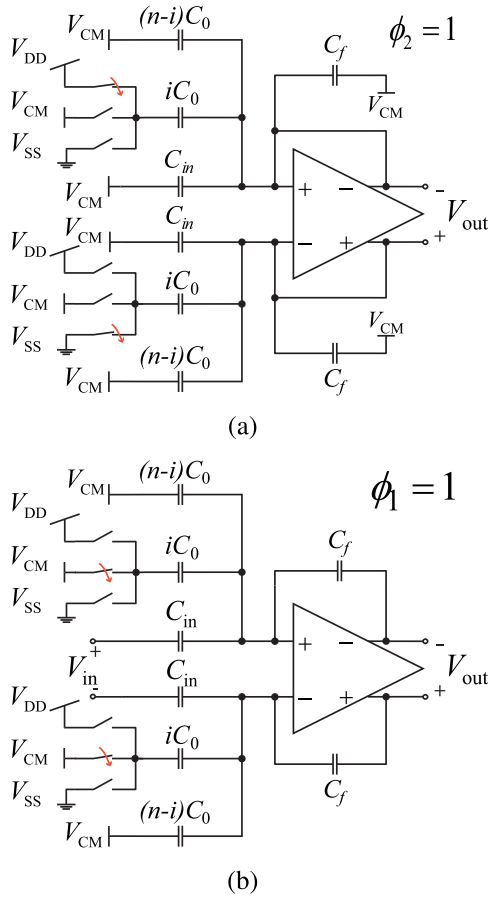

Fig. 4. Equivalent circuits for: (a) Hold phase. (b) Amplifying phase.

capacitor banks. Once the amplifier enters the next amplifying phase ($t \in [m - \frac{1}{2}, m]$), the offset charges will combine with the charges in the input capacitors $C_{\rm in}$'s such that $V_{\rm out}$ is pulled down from $V_{\rm out,eff}$ by an amount of $V_{\rm step}$. With the value of $V_{\rm step}$ close to that of $V_{\rm thr}$, $V_{\rm out}$ can be folded to a value very close to zero, thus making the voltages on the two sides of the opamp's output close to the common-mode voltage $V_{\rm CM}$ such that all the transistors in the opamp's output stage operate comfortably in saturation.

Fig. 4(a) illustrates a circuit scenario in the hold phase ($t \in [m-1, m-\frac{1}{2}]$) in which all the switches labeled ϕ_2 are closed such that the opamp is configured into the unity-feedback configuration; concurrently, the control logic connects the bottom plates of the input capacitors $C_{\rm in}$'s to the common-mode voltage $V_{\rm CM}$, connects i out of n offset capacitors C_0's of each offset capacitor bank, for a total capacitance of iC_0, to either $V_{\rm DD}$ or $V_{\rm SS}$, and connects the rest of the offset capacitance ($(n-i)C_0$) to $V_{\rm CM}$. Let $Q^+_{\rm tot}$ and $Q^-_{\rm tot}$ be the total charges in all the capacitors connected to the positive and negative input terminals of the opamp, respectively. With the common-mode feedback circuit pinning the voltage of each opamp's input to $V_{\rm CM}$, we can write $Q^+_{\rm tot}$ and $Q^-_{\rm tot}$ at the end of the hold phase ($t = m - \frac{1}{2}$) as $Q^+_{\rm tot}(m-\frac{1}{2}) = iC_{\rm o}(V_{\rm DD} - V_{\rm CM})$ and $Q^-_{\rm tot}(m-\frac{1}{2}) = iC_{\rm o}(V_{\rm SS} - V_{\rm CM})$.

In the next amplifying phase ($t \in [m - \frac{1}{2}, m]$), the switches labeled ϕ_1 in Fig. 2 are closed, configuring the circuit into a feedback amplifier; concurrently, the control logic instructs the switch networks to connect the bottom plates of $C_{\rm in}$'s to the input signal $V_{\rm in}$, and those of all the offset capacitors to $V_{\rm CM}$ as illustrated in Fig. 4(b). After charge redistribution, the total charges $Q^+_{\rm tot}$ and $Q^-_{\rm tot}$ at the end of the amplifying phase can be written as $Q^+_{\rm tot}(m) = C_{\rm in}(V^+_{\rm in} - V_{\rm CM}) + C_{\rm f}(V^-_{\rm out} - V_{\rm CM})$ and $Q^-_{\rm in}(m) = C_{\rm in}(V^-_{\rm in}(m) - V_{\rm CM}) + C_{\rm f}(V^+_{\rm out}(m) - V_{\rm CM})$. Since $Q^+_{\rm tot}$ and $Q^-_{\rm tot}$ must be conserved from the end of the hold phase to the end of the amplifying phase, we can solve for $V_{\rm out} = V^+_{\rm out} - V^-_{\rm out}$ in terms of $V_{\rm in} = V^+_{\rm in} - V^-_{\rm in}$ as

$$V_{\rm out}(m) = \frac{C_{\rm in}}{C_{\rm f}} V_{\rm in}(m) - i\frac{C_{\rm o}}{C_{\rm f}}\left(V_{\rm DD} - V_{\rm SS}\right). \qquad (2)$$

The term $(C_{\rm in}/C_{\rm f})V_{\rm in}(m)$ in (2) represents the sample of the effective output, i.e., $V_{\rm out,eff}(m)$. However, if the amplitude of $V_{\rm in}$ in the amplifying phase becomes so large that $|V_{\rm out}|$ has exceeded $V_{\rm thr}$, the intentional offset term $i\frac{C_{\rm o}}{C_{\rm f}}(V_{\rm DD} - V_{\rm SS}) = iV_{\rm step}$ is introduced such that at the end of the amplifying phase $|V_{\rm out}(m)| < V_{\rm thr}$. The value of i is determined and, if necessary, updated by ± 1 at the end of every amplifying phase to decrease or increase $V_{\rm out}$ by one $V_{\rm step}$. In Fig. 3, the period $t \in [k-1, k]$ illustrates a scenario when i is decremented by one in the hold phase to introduce a positive offset of $V_{\rm step}$ into $V_{\rm out}$ in the next amplifying phase.

The value of i can be either positive or negative and can range from $-n$ to $+n$, with $n = 31$ in this design, such that the maximum offset of $\pm nV_{\rm step}$ can be introduced to the amplifier's output. A positive i corresponds to the switch configuration of the input capacitor banks shown in Fig. 1(a), while a negative i corresponds to switching the iC_o capacitance in each offset capacitor bank to the opposite supply rail—i.e., the top iC_o becomes connected to $V_{\rm SS}$ and the bottom iC_o becomes connected to $V_{\rm DD}$ instead. In this design, we use $C_{\rm in} = 2$ pF, $C_{\rm f} = 125$ fF to achieve the nominal gain of 16 V/V. The value of $C_{\rm o}$ is chosen to be 75 fF, which results in $V_{\rm step}$ of 720 mV. Referred to the input of the amplifier, such $V_{\rm step}$ corresponds to an input step change of 45 mV. With $n = 31$, the proposed amplifier can accommodate an input range of ± 1.395 V, which conveniently covers the maximum output range of an AFE operating from a 1.2-V supply assumed to drive the proposed amplifier.

B. Amplitude Sensing Circuit

To determine whether and in which direction $V_{\rm out}$ has already exceeded the thresholds, we employ the amplitude sensing circuit shown in Fig. 5(a). The circuit provides two flag indicators, "Dir," and "thresh_cross"; the flag Dir indicates the polarity of $V_{\rm out}$, while thresh_cross indicates whether $|V_{\rm out}|$ is already larger than $V_{\rm thr}$. By knowing the polarity of $V_{\rm out}$ and whether its magnitude has exceeded the threshold, the control logic can adapt its internal state to provide appropriate configurations for the switch networks.

The amplitude sensing circuit can be divided into two parts: i) the rectifier and ii) the threshold crossing checker. The rectifier consists of the clocked comparator CMP1 and the multiplexer to

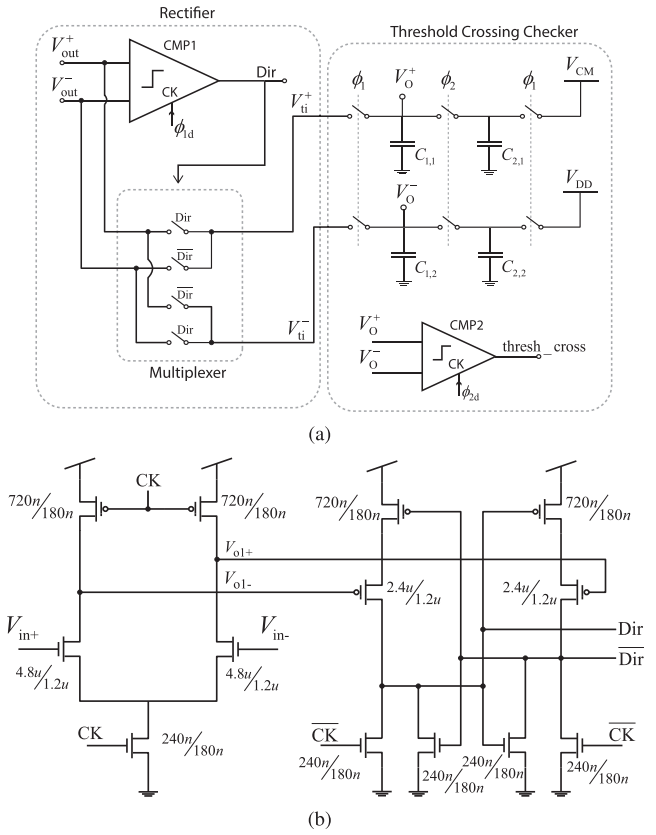

Fig. 5. (a) The amplitude sensing circuit. (b) The schematic of comparators used in the amplitude sensing circuit.

determine the polarity and the magnitude of $V_{\rm out}$, respectively. The threshold crossing checker consists of a charge redistribution network and the comparator CMP2 to determine whether $|V_{\rm out}|$ is higher than $V_{\rm thr}$. Due to the discrete-time nature of the amplitude sensing operation, we implement CMP1 and CMP2 using a dynamic comparator topology [26] shown in Fig. 5(b), which consumes almost no static power and makes fast decision on the rising edge of its clock signal (CK); with a load capacitance of 50 fF, transient simulations show that the comparator achieves a 90% settling time of around 2.4 ns after CK goes high. The comparators CMP1 and CMP2 operate on the rising edges of $\phi_{1\rm d}$ and $\phi_{2\rm d}$, the delayed versions of the nonoverlapping clocks ϕ_1 and ϕ_2 in Fig. 3, respectively. Shortly after the amplifier enters the amplifying phase—i.e., on the rising edge of $\phi_{1\rm d}$—the comparator CMP1 flags the signal Dir if $V_{\rm out}=V_{\rm out}^+-V_{\rm out}^->0$, which then controls the multiplexer such that its output $V_{\rm ti}=V_{\rm ti}^+-V_{\rm ti}^-$ is equal to $|V_{\rm out}^+-V_{\rm out}^-|$: Dir $=1$, indicating that $V_{\rm out}>0$, results in $V_{\rm ti}=V_{\rm out}^+-V_{\rm out}^-$; conversely, Dir $=0$, indicating that $V_{\rm out}<0$, results in $V_{\rm ti}=V_{\rm out}^--V_{\rm out}^+$. From Fig. 3, on the rising edge of $\phi_{1\rm d}$ shortly after $t=m-\frac{3}{2}$, the comparator CMP1 senses that $V_{\rm out}>0$ and thus flags Dir $=1$. Conversely, on the rising edge of $\phi_{1\rm d}$ shortly after $t=k-\frac{1}{2}$, CMP1 senses that $V_{\rm out}<0$ and thus set Dir $=0$.

The magnitude signal $V_{\rm ti}$ is then passed on to the threshold crossing checker to determine if $|V_{\rm out}|$ exceeds $V_{\rm thr}$. In the amplifying phase when all the switches labeled ϕ_1 are closed, the capacitors $C_{1,1}$ and $C_{1,2}$ are charged to $V_{\rm ti}^+$ and $V_{\rm ti}-$, respectively, while the capacitors $C_{2,1}$ and $C_{2,2}$ are charged to $V_{\rm CM}$ and $V_{\rm DD}$, respectively. The charges on these capacitors are then equal to $C_{1,1}V_{\rm ti}^+$, $C_{1,2}V_{\rm ti}^-$, $C_{2,1}V_{\rm CM}$, and $C_{2,2}V_{\rm DD}$. Once the amplifier enters the hold phase ($\phi_2=1$), the switches labeled ϕ_2 are closed, connecting the top plate of $C_{1,1}$ to that of $C_{2,1}$ and the top plate of $C_{1,2}$ to that of $C_{2,2}$, allowing charges in each pair of the connected capacitors to redistribute. After charge redistribution, the voltage on the top plates of each connected-capacitor pair can be written as $V_{\rm o}^+=(C_{1,1}V_{\rm ti}^++C_{2,1}V_{\rm CM})/(C_{1,1}+C_{2,1})$ and $V_{\rm o}^-=(C_{1,2}V_{\rm ti}^-+C_{2,2}V_{\rm DD})/(C_{1,2}+C_{2,2})$. Shortly after the amplifier enters the hold phase (on the rising edge of $\phi_{2\rm d}$), the comparator CMP2 determines if $V_{\rm o}^+-V_{\rm o}^->0$ by asserting the flag thresh_cross—e.g., on the rising edge of $\phi_{2\rm d}$ shortly after $t=m-1$, CMP2 senses that $V_{\rm o}^+-V_{\rm o}^->0$ and thus set thresh_cross to 1. With $C_{1,1}=C_{1,2}=C_1$ and $C_{2,1}=C_{2,2}=C_2$, $V_{\rm o}^+-V_{\rm o}^-$ can be written as

$$V_{\rm o}^+-V_{\rm o}^-=\frac{C_1}{C_1+C_2}\left(V_{\rm ti}^+-V_{\rm ti}^-\right)-\frac{C_2}{C_1+C_2}\left(V_{\rm DD}-V_{\rm CM}\right). \tag{3}$$

Since $V_{\rm ti}^+-V_{\rm ti}^-=|V_{\rm out}|$, thresh_cross is asserted when

$$|V_{\rm out}|>\frac{C_2}{C_1}\left(V_{\rm DD}-V_{\rm CM}\right)=V_{\rm thr}. \tag{4}$$

In this work, we set $C_1=C_2=2.5$ pF and $V_{\rm CM}=V_{\rm DD}/2$ such that $V_{\rm thr}=V_{\rm DD}/2$.

C. Control Logic

The control logic determines the state of the proposed amplifier to devise suitable configurations for the switch networks. With a full differential input swing of 2.4 $\rm V_{pp}$, the amplifier's nominal gain of 16 V/V results in a full differential output swing of 38.4 $\rm V_{pp}$. Hence, for the output correction step, $V_{\rm step}$, of 720 mV, we need a total of $(38.4\ \rm V_{pp})/(720\ mV)\approx 54$ steps to cover the entire output swing, thus requiring 6 bits to encode all the states. Therefore, in this design, we employ a total of 63 states, one for no offset correction, and 31 for each of the positive and negative offset corrections.

Fig. 6 depicts the state evolution of the amplifier. The states can be divided into three categories—S_0, $S_{\rm p,i}$, and $S_{\rm m,i}$, $i\in\{1,\ldots,31\}$—according to the polarities of the correction to be introduced to $V_{\rm out}$: the state S_0, indicating that $V_{\rm out,eff}$ still remains within $\pm V_{\rm thr}$, introduces no correction to $V_{\rm out}$; the state $S_{\rm p,i}$, indicating that $V_{\rm out,eff}$ is higher than $V_{\rm thr}$, introduces $-iV_{\rm step}$ to keep $V_{\rm out}$ within $\pm V_{\rm thr}$; the state $S_{\rm m,i}$, indicating that $V_{\rm out,eff}$ is lower than $-V_{\rm thr}$, introduces $iV_{\rm step}$ to keep $V_{\rm out}$ within $\pm V_{\rm thr}$.

Upon reset, the amplifier enters the state S_0 in which all of the offset capacitors are connected to $V_{\rm CM}$ such that no correction voltage is to be introduced to $V_{\rm out}$ in the next amplifying phase. To move from one state to the next requires two input signals, UP and DN. The signal UP, derived from UP = (Dir = 1) & (thresh_cross=1) and indicating that $V_{\rm out}$ has exceeded $+V_{\rm thr}$, instructs the state to move "up"—to change from S_0 to $S_{\rm p,1}$ (or

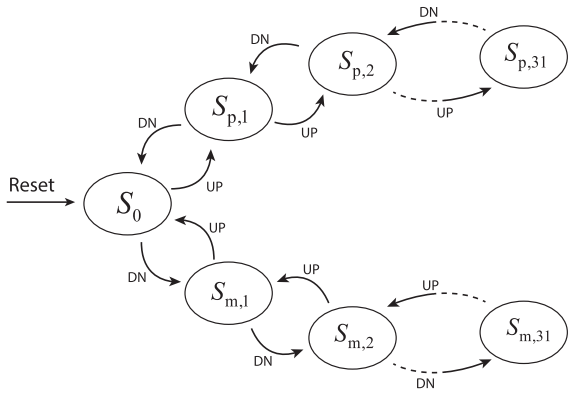

Fig. 6. Diagram showing the state evolution of the proposed amplifier.

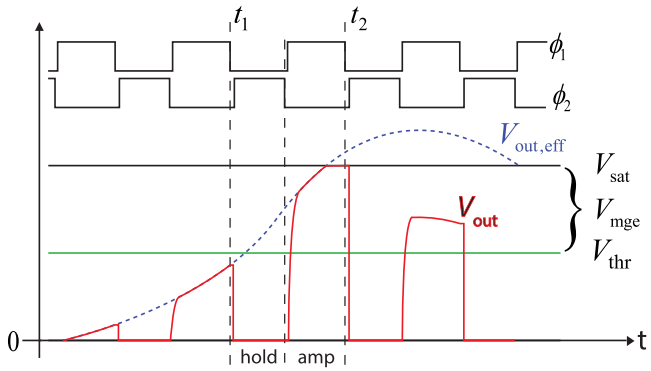

Fig. 7. A graph showing the saturation of $V_{\rm out}$ due to fast input.

from $S_{\rm p,i}$ to $S_{\rm p,i+1}$)—to subtract one additional $V_{\rm step}$ from $V_{\rm out}$ in the next amplifying phase. Conversely, the DN signal, derived from DN = (Dir = 0) & thresh_cross = 1 and indicating that $V_{\rm out}$ drops below $-V_{\rm thr}$, instructs the state to move "down"—to change from S_0 to $S_{\rm m,1}$ (or from $S_{\rm m,i}$ to $S_{\rm m,i+1}$)—to add one additional $V_{\rm step}$ to $V_{\rm out}$ in the next amplifying phase.

D. Maximum Amplitude vs. Frequency of the Input Signal

Since the amplitude sensing circuit monitors the threshold crossing in a discrete-time manner, it is possible for the amplifier's output to saturate, especially when the input changes very rapidly. Illustrated in Fig. 7 is an example of such a scenario for a positive output. At t_1, the amplitude sensing circuit determines that $V_{\rm out}$ is still below $V_{\rm thr}$; hence it does not flag the control logic to introduce a correction voltage for the next amplifying phase. Unfortunately, the input $V_{\rm in}$ changes so rapidly during t_1 and t_2 such that $V_{\rm out,eff}$ exceeds the saturation level $V_{\rm sat}$ of the amplifier's output stage. As a result, $V_{\rm out}$ could no longer track $V_{\rm out,eff}$ in the next amplifying phase and becomes clipped before the next threshold crossing check at t_2. If the ADC samples the amplifier's output right before t_2, information of $V_{\rm out,eff}$ will be lost, leading to increased distortion of the reconstructed output signal.

To avoid such scenario, we must ensure that the period between two consecutive threshold crossing checks, $T_{\rm clk} = t_2 - t_1$, must be short enough for $V_{\rm out,eff}$ not to traverse the entire margin of error, $V_{\rm mge} = V_{\rm sat} - V_{\rm thr}$. In other words, we have to enforce the condition:

$$\max\left(\Delta V_{\rm out,eff}\right) \approx \max\left(\left|\frac{dV_{\rm out,eff}}{dt}\right|\right) \cdot T_{\rm clk} < V_{\rm mge}. \quad (5)$$

Assuming a sinusoidal input into the amplifier of the form $V_{\rm in}(t) = V_{\rm p}\sin(2\pi f_{\rm in}t)$ and the amplifier's gain of $A_{\rm c} = C_{\rm in}/C_{\rm f}$, we have $\max(|\, dV_{\rm out,eff}\,/\,dt\,|) = A_{\rm c}V_{\rm p}2\pi f_{\rm in}$. Substituting this value into (5) and solving for the input amplitude, $V_{\rm p}$, we obtain

$$V_{\rm p} < \frac{V_{\rm mge}f_{\rm clk}}{2\pi A_{\rm c}} \cdot \frac{1}{f_{\rm in}}, \quad (6)$$

where $f_{\rm clk} = 1/T_{\rm clk}$ is the frequency of the clock signals ϕ_1 and ϕ_2.

The relationship in (6) suggests that the maximum input amplitude to guarantee no output clipping is inversely proportional to the frequency of the input signal $f_{\rm in}$, with the proportionality constant a function of $V_{\rm mge}$, $f_{\rm clk}$, and $A_{\rm c}$. Thus, to maximize $V_{\rm p}$ for given values of $f_{\rm in}$, $f_{\rm clk}$, and $A_{\rm c}$, we have to maximize $V_{\rm mge}$. This can be achieved by using an opamp whose open-loop gain remains high even when its output swings close to the supply rails such that the closed-loop gain of the amplifier remains relatively constant regardless of the output level. In this design with $V_{\rm mge} \approx 0.6$ V ($\approx V_{\rm DD} - V_{\rm thr}$) and the nominal $A_{\rm c}$ of 16 V/V, we use $f_{\rm clk} = 16$ kHz to allow the maximum input amplitude into the proposed amplifier of as large as 1.6 $\rm V_{pp}$ for the 60-Hz differential-mode mains interference without saturating the amplifier's output. This input amplitude is equivalent to 16 $\rm mV_{pp}$ when referred to the input of the ECG acquisition system if an AFE with a gain of 40 dB precedes the proposed amplifier. This level of tolerance to differential-mode mains interference should be adequate for most well designed ECG acquisition systems with proper grounding and low-to-moderate electrode impedance (< 10 MΩ). For motion artifact, whose frequency contents are normally well below 5 Hz, (6) indicates that a motion artifact of larger than 18 $V_{\rm pp}$ at the amplifier's input is required to saturate the output. Hence, the chosen $f_{\rm clk}$ of 16 kHz allows the amplifier to handle motion artifacts of any size provided that the output of the AFE preceding the proposed amplifier does not saturate.

It is worth mentioning that, in deriving (6), we assume a zero offset voltage for the comparator CMP2 in the amplitude sensing circuit (Fig. 5(a)). Even though the offset voltage of CMP2 does not affect the accuracy of the proposed amplifier—as the amount of the offset voltage introduced into $V_{\rm out}$ is independent of the characteristics of CMP2—it can affect the value of the margin of error $V_{\rm mge}$, and thus altering the achievable value of $V_{\rm p}$. Supposedly, if CMP2 has an offset voltage of $V_{\rm off}$ which reduces the margin of error to $V_{\rm mge} - V_{\rm off}$, the maximum achievable $V_{\rm p}$ then becomes a factor of $(1 - V_{\rm off}/V_{\rm mge})$ of its nominal value. For $V_{\rm off} = 50$ mV and $V_{\rm mge} = 0.6$ V, the reduction in $V_{\rm p}$ then amounts to a decrease in the SNDR of around 0.75 dB, which is negligible for our application. Besides, since the proposed amplifier employs a switched-capacitor input network, it presents an effective load resistance to the preceding AFE. Nevertheless,

the chosen frequency of $f_{\rm clk} = 16$ kHz and the input capacitance of $C_{\rm in} = 2$ pF results in the load resistance of around 31 MΩ on each side of the AFE's output. This level of load resistance is deemed high enough to not degrade the open-loop gain of the preceding AFE with μA-level bias current.

E. Notes on the Similarities to Other ADC/Frontend Architectures

At this point, some keen readers may have noticed that the proposed signal-folding scheme to prevent output saturation may look similar to the operation of a multiplying digital-to-analog converter (MDAC) in algorithmic or pipelined ADCs [25]. Besides, the use of capacitive feedback to subtract from the input a voltage proportional to the output may look similar to some of the $\Delta\Sigma$-based AFEs [27], [28]. The MDAC checks the input or, in later iterations, the output of the multiply-by-2 ($\times 2$) circuit and compares it to a reference voltage to perform appropriate level shifting such that the output of the $\times 2$ circuit stays within the rails in the next iteration. This process is performed iteratively until the least-significant-bit (LSB) is determined. What differentiates our proposed amplifier from the MDAC is that it uses a high-gain switched-capacitor amplifier to amplify the input signal only once, while having a signal-folding scheme to prevent the output from exceeding the rails. Compared to the MDAC, our proposed amplifier is more prone to output saturation when present with a large high-frequency interferences.

Nevertheless, there are certain advantages to our approach which makes it more amenable to low-power ECG acquisition systems compared to the MDAC. First, in the ECG acquisition system, the interferences (from MA and the mains) may be large but often slowly-varying. Since our signal-folding feedback only needs to correct for these large-but-low-frequency interferences, there is little risk of signal saturation, provided that the output of the preceding AFE does not saturate (see Section V-D). Second, since our high-gain amplifier amplifies the signal only once, there is no iterative addition of noise into the signal. For the MDAC, the use of low-gain amplification in each iteration results in the iterative addition of the $\times 2$ circuit's noise into the signal, resulting in an increased input-referred noise of the ADC to around twice the noise floor (in power units) of the $\times 2$ circuit. As a result, to achieve the same noise floor in a given bandwidth, our proposed amplifier can be designed with less stringent noise requirement, thus leading to power saving.

In the $\Delta\Sigma$-based AFEs, to prevent output saturation due to the large input offset voltage, the scheme in [27], [28] employs an integrator in the feedback path such that the output of the system represents the differentiation of the input, thus free of the input offset voltage. The output can then be reconstructed by integration. In our view, this $\Delta\Sigma$ approach relies on the conventional feedback concept by forcing the feedback signal to mimic the input as closely as possible to minimize error. To achieve this, $\Delta\Sigma$ amplifiers rely on oversampling—usually with an oversampling ratio (OSR) of 1,000—and noise shaping to overcome the ADC's quantization noise. Such high oversampling ratio can lead to high power consumption in the $\Delta\Sigma$ amplifiers and the clock generation circuitry. On the contrary, the signal-folding scheme in our proposed amplifier only tries to subtract a crude estimate from the input to keep the output within the rails, with the crude estimate normally determined by the large but slowly-varying interferences into the amplifier. As long as the input signal of interest is small, and the overall output is kept within the rails by the signal-folding scheme, the signal of interest can be amplified with a switched-capacitor amplifier without the need of a very high OSR. Thus, compared to the $\Delta\Sigma$ approach, our proposed amplifier only needs to operate at a much lower frequency, making it more amenable for low-power implementation.

TABLE I
TRANSISTORS' SIZES AND THE DC-OPERATING-POINT PARAMETERS OF THE OPAMP IN FIG. 8

Transistors	Aspect Ratio (μm/μm)	$g_{\rm m}$ (μA/V)	$r_{\rm o}$ (MΩ)
M_1, M_2	32/1	14.5	5.8
M_3, M_4	32/1	11.5	22.3
M_5, M_6	32/1	11.4	11.1
M_7, M_8	32/1	10.9	13.6
M_9, M_{10}	8/4	10.4	18
M_{11}, M_{12}	16/1	5.3	102.8
M_{13}, M_{14}	4/4	5.1	34.8
$M_{\rm b1}$, $M_{\rm b2}$	8/12	8.83	24.23
$M_{\rm b3}$, $M_{\rm b4}$	4/1	1.14	274

F. Opamp Design

We have seen from Section III that, during the hold phase, the opamp is connected in the unity-feedback configuration, resulting in the opamp's differential output being reset to zero; hence, it requires that the opamp be unity-gain stable. Besides, the proposed amplifier must also drive a sizable load capacitance—i.e., the input capacitance of the next-stage ADC. Thus, it must exhibit a sufficient slew rate for its output to reach the final value within half of $T_{\rm clk}$ once the amplifier re-enters the amplifying phase (31.25 μs in this design). Also, to maximize the input amplitude by maximizing $V_{\rm mge}$ as discussed in Section III-D, the opamp must exhibit a high open-loop gain even at large output swing. Besides being unity-gain stable, fast, and exhibiting high open-loop gain, the opamp must also consume low power to minimize the overall power consumption of the ECG acquisition system.

To meet all these requirements, we employ a fully-differential two-stage opamp shown in Fig. 8 with all the devices' sizes listed in Table I, along with their transconductances and output resistances from the DC operating point simulation. The transistors M_1-M_6 form the first gain stage while M_7-M_{14} form a class-AB output stage to provide a high driving strength while minimizing the overall quiescent current of the opamp. Since the opamp operates in a switched-capacitor fashion, we employ switched-capacitor common-mode feedback [29] circuits to generate $V_{\rm cmfb1}$ and $V_{\rm cmfb2}$ to set the common-mode outputs of the first and the second stages, respectively, without consuming static bias current. With the expected load capacitance of $C_{\rm L} \approx 5$ pF and $f_{\rm clk}$ of 16 kHz, we allocate in each branch the bias current labeled in Fig. 8 for the amplifier to function properly with

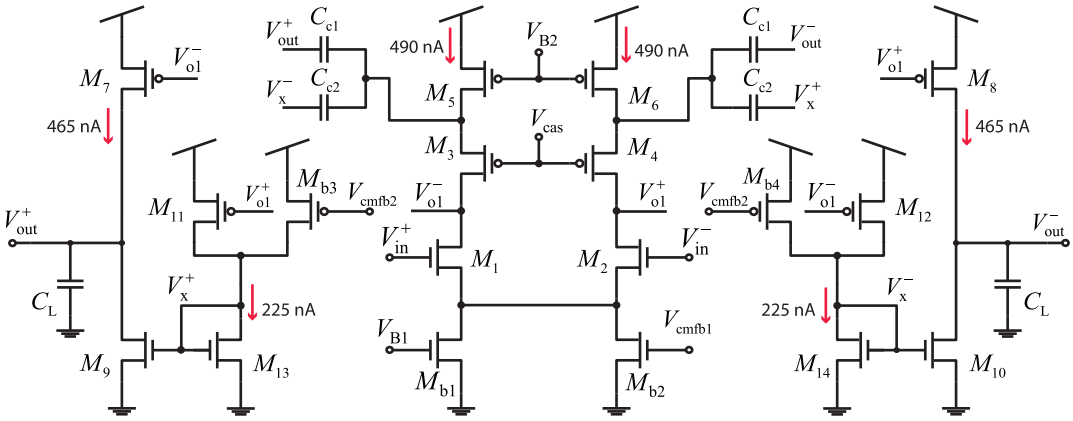

Fig. 8. Schematic of the opamp used in the proposed amplifier.

the expected ranges of input's frequency and amplitude. Due to the low bias current of the first stage, the pole formed by the source resistance of $M_{3,4}$ and the compensation capacitors situates at low frequency, thus requiring the use of a nested Miller compensation to achieve the settling time requirement. To avoid the use of zero-nulling resistors which may increase the chip area, we make the Miller compensation indirect by feeding capacitive feedback currents through the compensation capacitors $C_{c1} = 3$ pF and $C_{c2} = 1$ pF to the source nodes of M_3 and M_4. Through this design, with $C_L = 5$ pF, simulations show that the opamp achieves the low-frequency open-loop gain of 87 dB, the unity-gain frequency of 600 kHz, the phase margin of 46°, and the 0.1% settling time of 13 μs when the amplifier's output changes by 700 mV.

IV. Noise Analysis

The sampling nature of the proposed amplifier inevitably causes an increase of in-band noise due to aliasing. In this section, we consider the important determining factors of the amplifier's noise performance to pinpoint the control knobs for keeping the noise within our specification.

A. Noise From the Sampling Switches

All the sampling switches, when closed, exhibit finite resistances and hence thermal noise. Such thermal noise affects the amount of charge to be sampled onto the capacitor connected to each switch. To simplify our calculation, let us assume that the opamp is ideal with infinite gain and bandwidth. Such assumption leads to the upper bound for the calculation of the input-referred noise due to the sampling switches: the ideal opamp results in the true virtual ground condition at the opamp's inputs and, consequently, the maximum amount of noise sampled onto each capacitor.

Figure 9(a) and 9(b) show the half-circuit models for analyzing the amplifier's noise in the hold and the amplifying phases, respectively. The resistances $R_{\mathrm{sw,in}}$, $R_{\mathrm{sw,o}}$, and $R_{\mathrm{sw,f}}$ are the ON resistances of the switches connected to C_{in}, each of C_{o}, and C_{f}, respectively, while the thermal noise voltages associated

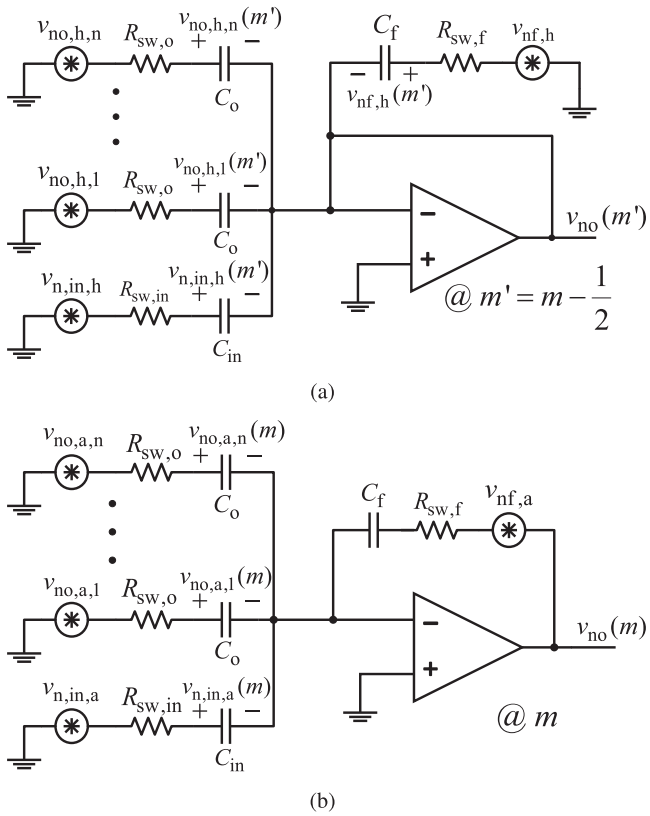

Fig. 9. Equivalent circuits for calculating the proposed amplifier's noise due to the sampling switches in: (a) hold phase (b) amplifying phase.

with these switches are denoted as the noise generators $v_{\mathrm{n,in,h}}$, $v_{\mathrm{no,h,i}}$ ($i \in \{1, \ldots, n\}$), and $v_{\mathrm{nf,h}}$. In the amplifying phase, each capacitor is connected to a different switch, whose noise is uncorrelated to that of the switch in the hold phase. Therefore, we denote the noise in the amplifying phase with a subscript "a" instead of "h"—e.g., the noise associated with the switch's resistance $R_{\mathrm{sw,in}}$ that is sampled onto C_{in} in the amplifying phase is denoted as $v_{\mathrm{n,in,a}}(m)$, and so on.

To find the total input-referred noise due to all the switches, we first write the total charges in all the capacitors at the end of the hold phase and the end of the amplifying phase:

$$Q_{\rm tot}\left(m-\frac{1}{2}\right)=C_{\rm in}v_{\rm n,in,h}\left(m-\frac{1}{2}\right)+\sum_{\rm i=1}^{n}C_{\rm o}v_{\rm no,h,i}\left(m-\frac{1}{2}\right)+C_{\rm f}v_{\rm nf,h}\left(m-\frac{1}{2}\right) \quad (7)$$

and

$$Q_{\rm tot}(m)=C_{\rm in}v_{\rm n,in,a}(m)+\sum_{\rm i=1}^{n}C_{\rm o}v_{\rm no,a,i}(m)+C_{\rm f}\left(v_{\rm no}(m)+v_{\rm nf,a}(m)\right). \quad (8)$$

From charge conservation, we can equate (7) to (8) and solve for $v_{\rm no}(m)$. We then use the fact that noises from different switches associated with the same capacitor are uncorrelated but exhibit the same spectrum, and that we have to double the noise power as we have two sets of these switches in our differential implementation. We can then express the output noise spectrum of the amplifier due to all the sampling switches as

$$\overline{V_{\rm no}^2}(f)=4\left(\frac{C_{\rm in}}{C_{\rm f}}\right)^2\overline{V_{\rm n,in,a}^2}(f)+4n\left(\frac{C_{\rm o}}{C_{\rm f}}\right)^2\overline{V_{\rm no,a,1}^2}(f)+4\overline{V_{\rm nf,a}^2}(f), \quad (9)$$

where we have assumed that $\overline{V_{\rm no,a,1}^2}(f)=\overline{V_{\rm no,a,i}^2}(f)$ for all i.

Note that each term of the noise spectrum on the right-hand-side of (9) represents the power spectral density (PSD) of a sampled switch's noise. Since an ON switch carries no DC current, thus exhibiting no 1/f noise, we only need to consider its thermal-noise contribution. For a particular switch with an ON resistance R connected to a capacitance C, the continuous-time spectrum of the switch's noise sampled onto C is a two-sided spectrum with a height of $2kTR$ and a noise bandwidth of $1/4RC$. This noise voltage across the capacitor is then sampled by the ADC's sampling rate, $f_{\rm s}$—$f_{\rm s}$ is normally several times lower than $f_{\rm clk}$ used in the switched-capacitor operation of the amplifier. Since $f_{\rm s}$ is normally much lower than the noise bandwidth, $1/4RC$, aliasing results in noise folding, which elevates the spectrum of the sampled noise to $kT/(f_{\rm s}C)$ [30]; this sampled noise's spectrum is periodic in the frequency domain with a periodicity of $f_{\rm s}$ such that we can regard its bandwidth to be $\pm f_{\rm s}/2$. Therefore, we can substitute $\overline{V_{\rm n,in,a}^2}(f)=kT/(C_{\rm in}f_{\rm s})$, $\overline{V_{\rm no,a,1}^2}(f)=kT/(C_{\rm o}f_{\rm s})$, $\overline{V_{\rm nf,a}^2}(f)=kT/(C_{\rm f}f_{\rm s})$, and divide the result by the square of the amplifier's gain, $(C_{\rm in}/C_{\rm f})^2$, to obtain the input-referred noise spectrum due to all the sampling switches as

$$\overline{V_{\rm ni,samp}^2}(f)=\frac{4kT}{C_{\rm in}}\left(1+\frac{nC_{\rm o}+C_{\rm f}}{C_{\rm in}}\right)\frac{1}{f_{\rm s}}. \quad (10)$$

B. Noise Due to the Opamp

Next, let us consider the noise contribution from the opamp itself. Fig. 10(a) and Fig 10(b) show the equivalent circuits for computing the noise of the opamp in the hold and the amplifying phases, respectively, in which $v_{\rm nA}$ represents the input-referred noise of the opamp. To simplify our analysis, let us assume that all the switches' ON resistances are zero, which represents the worst-case scenario for the opamp's noise contribution. Such assumption results in the sampled noise onto all the capacitors to be bandlimited by the opamp's transfer function and not by the wider bandwidth of the RC networks formed by the sampling switches and capacitors. Also, let us assume a first-order opamp's transfer function of the form $A(s)=\omega_{\rm c}/s$, where $\omega_{\rm c}$ is the unity-gain bandwidth of the opamp.

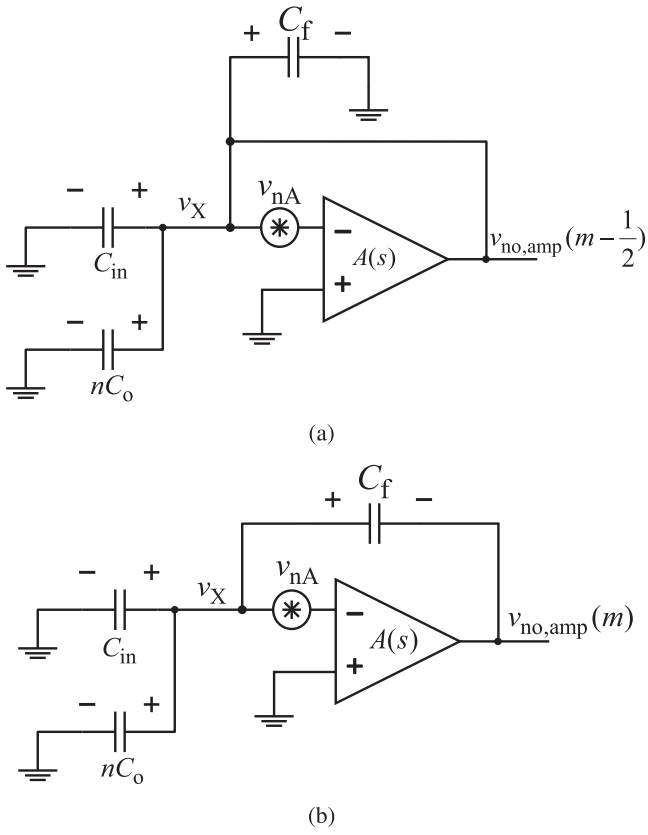

Fig. 10. Equivalent circuits for calculating the input-referred noise of the proposed amplifier due to the opamp: (a) hold phase (b) amplifying phase.

During the hold phase shown in Fig. 10(a)), $v_{\rm nA}$ is filtered by the opamp connected in the unity-gain configuration to produce the voltage $v_{\rm x}$ on the top plates of all the capacitors, producing, at the end of the hold phase ($t=m-1/2$), the total charge on all the capacitors of

$$Q_{\rm tot}\left(m-\frac{1}{2}\right)=(C_{\rm in}+nC_{\rm o}+C_{\rm f})v_{\rm x}\left(m-\frac{1}{2}\right). \quad (11)$$

In the amplifying phase, $C_{\rm f}$ is connected as feedback around the opamp as shown in Fig. 10(b). We can then write the total charge in all the capacitors at the end of the amplifying phase ($t=m$) as

$$Q_{\rm tot}(m)=(C_{\rm in}+nC_{\rm o})v_{\rm x}(m)+C_{\rm f}(v_{\rm x}(m)-v_{\rm no,amp}(m)). \quad (12)$$

Equating (12) to (11), we can solve for $v_{\mathrm{no,amp}}$ as

$$v_{\mathrm{no,amp}}(m) = \left(1 + \frac{C_{\mathrm{in}} + nC_{\mathrm{o}}}{C_{\mathrm{f}}}\right)\left(v_{\mathrm{x}}(m) - v_{\mathrm{x}}\left(m - \frac{1}{2}\right)\right). \tag{13}$$

Then, taking the z-transform of (13) with $z = e^{j2\pi f/f_{\mathrm{s}}}$ and computing the noise spectrum, we obtain

$$\overline{V^2_{\mathrm{no,amp}}}(f) = 4\left(1 + \frac{C_{\mathrm{in}} + nC_{\mathrm{o}}}{C_{\mathrm{f}}}\right)^2 \sin^2\left(\pi\frac{f}{2f_{\mathrm{s}}}\right)\overline{V^2_{\mathrm{x}}}(f). \tag{14}$$

Note that $\overline{V^2_{\mathrm{x}}}(f)$ in (14) is the discrete-time spectrum of the sampled noise voltage v_{x}. To compute $\overline{V^2_{\mathrm{x}}}(f)$, we first recognize that the continuous-time transfer functions from v_{nA} to v_{x} in the hold and the amplifying phases are given by $(V_{\mathrm{x}}/V_{\mathrm{nA}})_{\mathrm{hold}}(s) = -1/(1 + s/\omega_{\mathrm{c}})$ and $(V_{\mathrm{x}}/V_{\mathrm{nA}})_{\mathrm{amp}}(s) = -1/(1 + s/\omega'_{\mathrm{c}})$, respectively, where ω_{c} is the unity-gain frequency of the opamp and $\omega'_{\mathrm{c}} = \omega_{\mathrm{c}}C_{\mathrm{f}}/(C_{\mathrm{in}} + C_{\mathrm{f}} + nC_{\mathrm{o}})$. Since the amplifying phase experiences a smaller filtering bandwidth than the hold phase's, we can again simplify our analysis by assuming the worst-case scenario: that both phases experience a wider bandwidth of ω_{c}. Hence, we can write the continuous-time spectrum, $\overline{V^2_{\mathrm{x,c}}}(f)$, of the noise voltage at V_{x} as

$$\overline{V^2_{\mathrm{x,c}}}(f) = \overline{V^2_{\mathrm{nA}}}(f) \cdot \frac{1}{1 + f^2/f_{\mathrm{c}}^2}, \tag{15}$$

where $f_{\mathrm{c}} = \omega_{\mathrm{c}}/2\pi$.

To account for both the thermal and 1/f noise components of $\overline{V^2_{\mathrm{nA}}}$, let $\overline{V^2_{\mathrm{n,th}}}$ represent its thermal noise component and f_{fn} its $1/f$ noise corner such that we can represent the opamp's input-referred noise as $\overline{V^2_{\mathrm{nA}}}(f) = \overline{V^2_{\mathrm{n,th}}}(1 + f_{\mathrm{fn}}/f)$, thus allowing us to rewrite (15) as

$$\overline{V^2_{\mathrm{x,c}}}(f) = \overline{V^2_{\mathrm{n,th}}}\left(1 + \frac{f_{\mathrm{fn}}}{f}\right)\frac{1}{1 + f^2/f_{\mathrm{c}}^2}. \tag{16}$$

Recognizing that $\overline{V^2_{\mathrm{x}}}(f)$ is the aliased version of $\overline{V^2_{\mathrm{x,c}}}(f)$, which is given by $\overline{V^2_{\mathrm{x}}}(f) = \Sigma_{k=0}^{\infty}\overline{V^2_{\mathrm{x,c}}}(f - kf_{\mathrm{s}})$, we can then write $\overline{V^2_{\mathrm{x}}}(f)$ using (16) as

$$\overline{V^2_{\mathrm{x}}}(f) = \overline{V^2_{\mathrm{n,th}}}\sum_{k=0}^{\infty}\left(\left(1 + \frac{f_{\mathrm{fn}}}{|f - kf_{\mathrm{s}}|}\right)\cdot\frac{1}{1 + \frac{(f-kf_{\mathrm{s}})^2}{f_{\mathrm{c}}^2}}\right). \tag{17}$$

Finally, substituting (17) into (14) and dividing the result by the square of the amplifier's gain, we obtain the input-referred noise component of the amplifier due to the opamp's noise as

$$\overline{V^2_{\mathrm{ni,amp}}}(f) = 4\overline{V^2_{\mathrm{n,th}}}\left(1 + \frac{C_{\mathrm{f}} + nC_{\mathrm{o}}}{C_{\mathrm{in}}}\right)^2 \sin^2\left(\pi\frac{f}{2f_{\mathrm{s}}}\right) \cdot\sum_{k=0}^{\infty}\left(\left(1 + \frac{f_{\mathrm{fn}}}{|f - kf_{\mathrm{s}}|}\right)\cdot\frac{1}{1 + \frac{(f-kf_{\mathrm{s}})^2}{f_{\mathrm{c}}^2}}\right). \tag{18}$$

As will be seen in Section V-B, the noise due to the opamp in (18) is the dominant noise source of the proposed amplifier. We can also notice from (18) that, besides the thermal noise $\overline{V^2_{\mathrm{n,th}}}$, the 1/f noise corner, f_{fn}, of the opamp plays an important role in determining the overall input-referred noise of the amplifier, even though the noise at low frequency is attenuated by the highpass transfer function $\sin^2(\pi f/2f_{\mathrm{s}})$. In this design, we size the transistors such that the settling time in the amplifying phase is well below 31.25 μs while ensuring a low enough 1/f noise corner to yield the amplifier's input-referred noise of around 150 $\mu\mathrm{V_{rms}}$. If a lower input-referred noise for the amplifier is desired, given the achieved settling time of only 13 μs in the amplifying phase as discussed in Section III-F, we could trade the settling time with the opamp's 1/f noise—i.e., by increasing the transistors' sizes of the opamp.

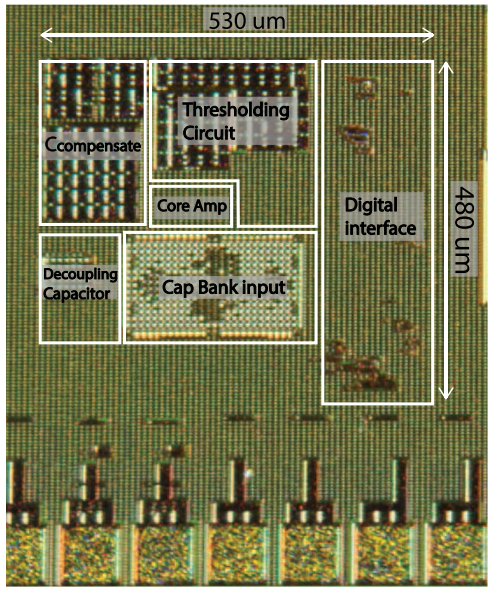

Fig. 11. Chip micrograph of the proposed amplifier.

V. Experimental Results

The proposed amplifier with the micrograph shown in Fig 11, was fabricated in a 0.18-μm CMOS process from United Microelectronics Corp. The amplifier occupies the total area of 0.254 mm^2 (530 $\mu\mathrm{m} \times 480\ \mu\mathrm{m}$), with 14.65% of the total area attributed to the input capacitor banks and 12% to the opamp's compensation capacitors. Operating from a 1.2 V supply, the amplifier consumes 2.64 μW of total power when amplifying a rail-to-rail (2.4 $\mathrm{V_{pp}}$) 32-Hz sinusoidal input to drive a capacitive load of 5 pF. The overall gain of the amplifier is measured to be 17.8 V/V, instead of the nominal value of 16 V/V. Such gain error is attributed to inaccuracy in the layout modeling as the error is observed across many chips.

A. Reconstruction

Due to the folding operation, the physical output of the amplifier (V_{out}) must be reconstructed to recover the effective output ($V_{\mathrm{out,eff}}$). Since the state kept by the control logic contains information on the correction voltage introduced into $V_{\mathrm{out,eff}}$ to create V_{out}, we can use such information to easily reconstruct $V_{\mathrm{out,eff}}$ from V_{out}. For example, if a particular sample of V_{out} corresponds to the state $S_{\mathrm{p,i}}$, $i \in \{1, \ldots, 31\}$, indicating that

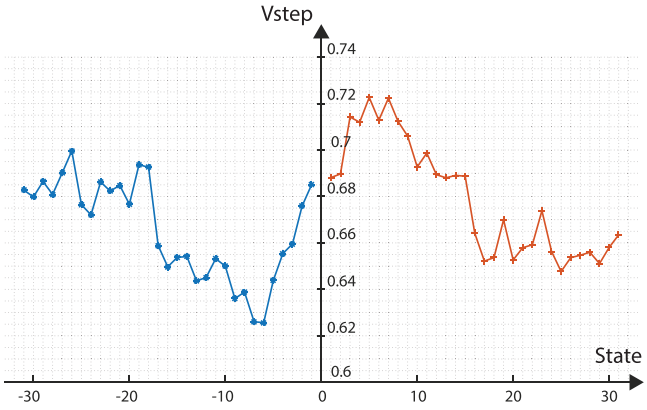

Fig. 12. Distribution of V_{step} as a function of the amplifier's state.

the sampled V_{out} has been effectively created by substracting $i \cdot V_{\text{step}}$ from $V_{\text{out,eff}}$, we can reconstruct $V_{\text{out,eff}}$ using

$$V_{\text{out,eff}} = V_{\text{out}} + i \cdot V_{\text{step}}(S), \tag{19}$$

where S is the amplifier's state corresponding to the sampled V_{out}. Note that we write V_{step} in (19) as a function of the state S because, due to process variations affecting the sizes of the unit capacitors, V_{step} is not constant but a function of the amplifier's state. To minimize distortion in the reconstructed $V_{\text{out,eff}}$, we recommend that initially V_{step}'s be determined for all the states S and stored in a memory in the digital backend such that they can be readily employed in the reconstruction process. Determining all the V_{step}'s can be easily achieved by feeding a slow ramp into the input of the amplifier—such that all the amplifier's states are utilized—while recording V_{out}. In this work, we fed a 1-Hz 2.4-V_{pp} ramp (sawtooth) signal into the input of the amplifier to cover its entire input range while recording V_{out}. We then plotted V_{out} in MATLAB and noted the discontinuities resulted from the signal folding operation as the amplifier transitioned from one state to the next. Each discontinuity was then taken as V_{step} of the state into which the amplifier just transitioned.

Fig. 12 shows the resulting V_{step} as a function of the amplifier's state. Marked on the x-axis, states $+i$ and $-i$ correspond to the states $S_{\text{p,i}}$ and $S_{\text{m,i}}$, respectively. The distribution of V_{step} shows a spread of around 100 mV, possibly due to process variations affecting the values of the unit capacitors C_{o}'s and the feedback capacitors C_{f}'s. Achieving a narrower spread in V_{step} can be achieved by increasing the unit sizes of C_{o}'s and C_{f}'s but at the expense of a larger area. Nevertheless, as long as the amplifier is calibrated once to obtain the values of V_{step} for all the states, V_{out} can be later reconstructed with high linearity. It is also worth noting that the reconstruction process recommended here aims to achieve maximum linearity despite the inherent nonlinearities in the circuit. If we opt for an easier reconstruction process, we may as well use just one value of V_{step} instead of a dedicated value for each of the amplifier's state, at the expense of lower linearity.

To test the effectiveness of the mentioned reconstruction process, we time-multiplexed two sinusoidal inputs into the amplifier, one with the frequency of 30 Hz and the amplitude of 2.4 V_{pp}, and the other with the frequency of 40 Hz and the

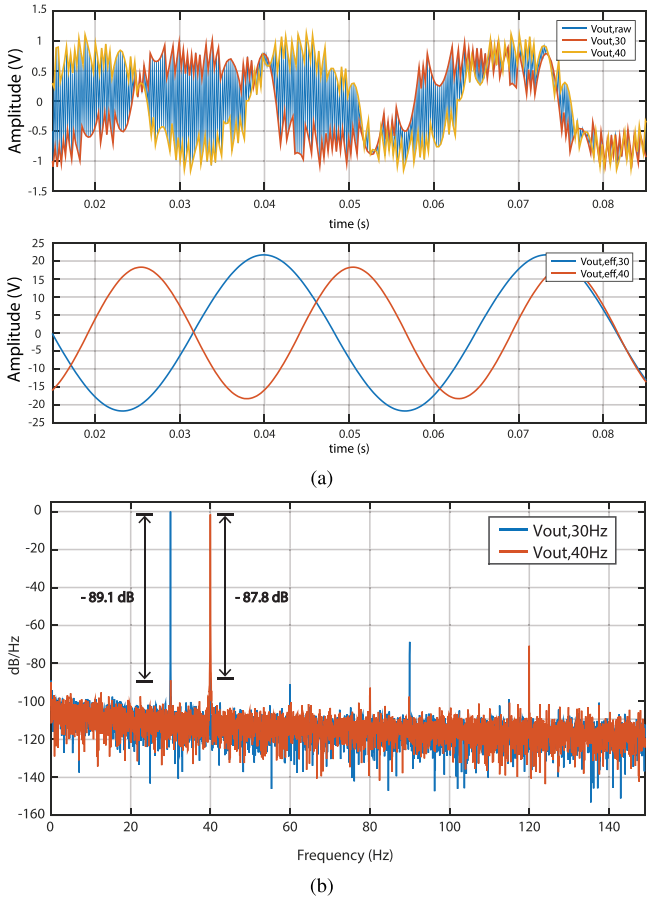

Fig. 13. (a) Raw output of the amplifier in response to 30-Hz and 40-Hz sinusoidal inputs. (b) Spectrum of the reconstructed 30-Hz and 40-Hz outputs showing the crosstalks of −87.8 dB from the 30-Hz into the 40-Hz signals and −89.1 dB from the 40-Hz into the 30-Hz signals.

amplitude of 2 V_{pp}. In the top panel of Fig. 13(a), the trace $V_{\text{out,raw}}$ represents the raw output of the proposed amplifier, while the traces $V_{\text{out,30}}$ and $V_{\text{out,40}}$ represent the digitized physical outputs of the amplifier corresponding to the 30-Hz and 40-Hz input signals, respectively, each sampled by an on-chip ADC with a 9-bit ENOB (in the bandwidth from DC to 150 Hz) at a rate of 4.096 kS/s. The bottom panel of Fig. 13(a) shows the effective outputs—$V_{\text{out,eff,30}}$ and $V_{\text{out,eff,40}}$—corresponding to the two input signals after reconstruction. The amplitudes of the 30-Hz and 40-Hz output signals are 42.6 and 35.5 V_{pp}, respectively, indicating an overall gain of 17.75 V/V (24.98 dB). From visual inspection, we notice negligible crosstalk between the two output signals. Fig. 13(b) shows the PSD of $V_{\text{out,eff,30}}$ and $V_{\text{out,eff,40}}$ with the fundamentals normalized to 0 dB. Note that the crosstalk from the 30-Hz to 40-Hz signals and from the 40-Hz to 30-Hz signals are −87.8 and −89.1 dB, respectively, thus suggesting that the proposed amplifier is suitable for amplifying two input signals with negligible crosstalk to permit area saving in multi-channel applications.

B. Linearity and Noise

The principal aim of the proposed amplifier is to allow accurate recording of ECG for a wide range of interference's

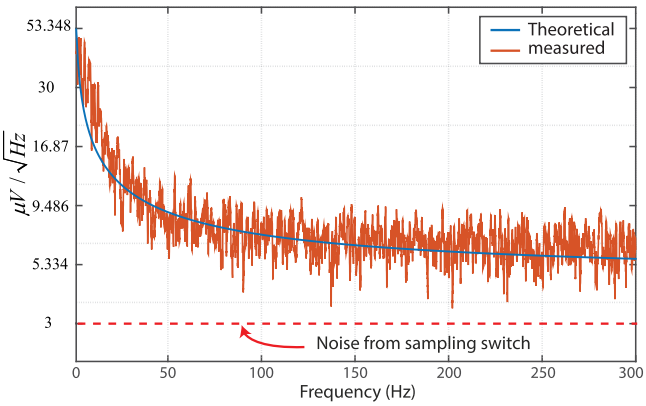

Fig. 14. Measured input-referred noise PSD of the proposed amplifier compared to the theoretical prediction. The total integrated input-referred noise is 143.6 μV_{rms}.

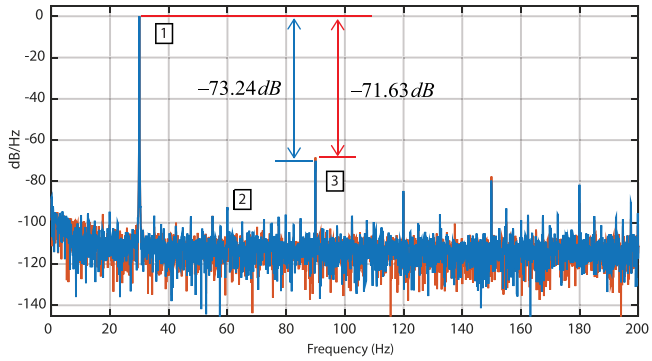

Fig. 15. Spectrums of the reconstructed output in response to a 30-Hz rail-to-rail input signal from the two reconstruction methods: (i) V_{step}-distribution method (blue trace) and (ii) fixed V_{step} method (red trace).

amplitude, without the need for an automatic gain control scheme. With small interference, the amplifier's intrinsic noise may degrade the SNR unless the gain of the preceding AFE is sufficiently large. With large interference, the amplifier's nonlinearity may introduce unwanted spectral contents into the desired ECG, thus limiting the system's ability for discerning tiny ECG from the interference. In this section, we explore the proposed amplifier's noise and nonlinearity to understand its limitation in preserving the SNDR of the desired signal.

1) Noise: To measure the intrinsic noise of the proposed amplifier, we grounded its input and sampled its output at 4.096 kS/s with the same on-chip ADC as in Section V-A. We then computed the power spectral density of these output samples and normalized the result by the overall gain of the amplifier to get the input-referred noise. Fig. 14 shows the resulting input-referred noise spectrum of the amplifier (red trace) in the frequency range from DC to 300 Hz along with the theoretical fit (blue trace) obtained from the sum of the switches' and opamp's noises in (10) and (18), respectively. For the opamp's noise, we use $\sqrt{\overline{V_{n,th}^2}}$=52.21 nV/$\sqrt{\text{Hz}}$, $f_{fn} = 80$ kHz, $f_c = 46$ kHz, and $f_s = 4.096$ kHz. The input-referred thermal noise $\overline{V_{n,th}^2}$ is obtained from the theoretical calculation—$\overline{i_n^2} = 4kT\gamma g_m$, where $\overline{i_n^2}$ is the power spectral density of the thermal noise current of a particular transistor, k the Boltzman's constant, T the absolute temperature, and g_m the small-signal transconductance of the transistor—with g_m's from Table I and $\gamma = 2/3$ as typical for long-channel devices; the crossover frequency f_c is obtained from AC simulation, while the 1/f noise corner f_{fn} is empirically adjusted for the theoretical plot to fit the measured result. A good fit between theory and the measured result indicates that our analysis in Section IV explains the noise behavior of the proposed amplifier with reasonable accuracy. Integrating the measured noise spectrum from DC to 150 Hz gives the total input-referred noise of 143.6 μV_{rms}.

Note that due to its fully-differential nature, the proposed amplifier is immune to noise on the V_{CM} line into the switch networks (see Fig. 2). However, it can be seen from (2) that the offset voltage added to $V_{in}(m)$ to properly fold the input signal directly depends on the value of V_{DD} (with respect to V_{SS})—with a gain of iC_o/C_f. Referred to the input of the proposed amplifier, the noise on this V_{DD} line experiences a gain of iC_o/C_{in}. To avoid degrading the input-referred noise and the power-supply-rejection-ratio (PSRR), we thus recommend that the V_{DD} line into the switch networks of Fig. 2 be separated from the main V_{DD} of the amplifier and properly lowpass filtered. Nevertheless, since the proposed amplifier is intended for use as a second-stage amplifier, the noise requirement of the quiet V_{DD} line is alleviated by the gain of the AFE. For the 150-μV_{rms} specification of the proposed amplifier, it follows that, in the worst case of offset voltage addition ($i = n = 31$), the total integrated noise on the quiet V_{DD} line should be less than 40 μV_{rms} for this noise to account for less than 10% of the overall noise power. Provided that the overall recording system is battery-powered such that the main V_{DD} contains negligible mains interference, the quiet V_{DD} line with such relaxed noise requirement can be easily achieved through filtering the main V_{DD} by an off-chip filtering network.

2) Linearity: To assess its linearity, we fed a rail-to-rail (2.4-V_{pp}) 30-Hz sinusoidal signal into the input of the amplifier and sampled its output with the same on-chip ADC as discussed in Section V-A. Due to the large input amplitude, the sampled output signal must first be reconstructed, as explained in Section V-A. To achieve maximum linearity, we can use the reconstruction method with one specific value of V_{step} for each of the amplifier's state discussed in Section V-A. However, one may choose to minimize the complexity of the reconstruction circuit in the digital backend by using just one value of V_{step} for the whole reconstruction process. This value of V_{step} may be chosen to be the median of the V_{step} distribution obtained during calibration—e.g., the median of the distribution in Fig. 12. Fig. 15 compares the spectrums of the amplifier's output, with the fundamentals normalized to 0 dB, as reconstructed from the two methods: i) using V_{step} distribution in Fig. 12 (blue trace) and ii) using $V_{step} = 0.674$ V (red trace). Within the 150-Hz bandwidth, the amplifier's nonlinearity is dominated by the 3rd harmonic, which is 73.2 dB and 71.6 dB below the fundamental for the V_{step}-distribution method and the fixed V_{step} method, respectively. Calculation of the SNDRs within this bandwidth yields 71 dB and 70.13 dB for the V_{step}-distribution method

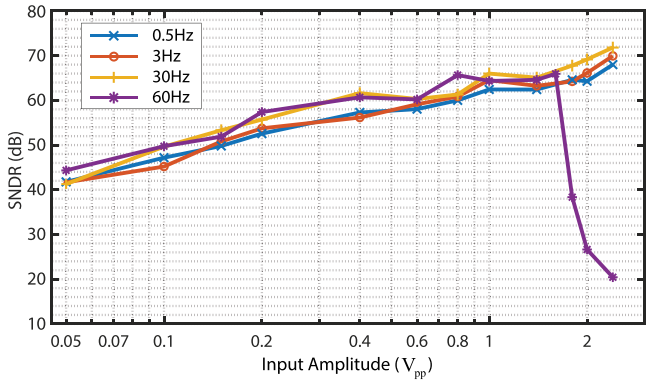

Fig. 16. SNDR vs. input amplitude at various frequencies of the input.

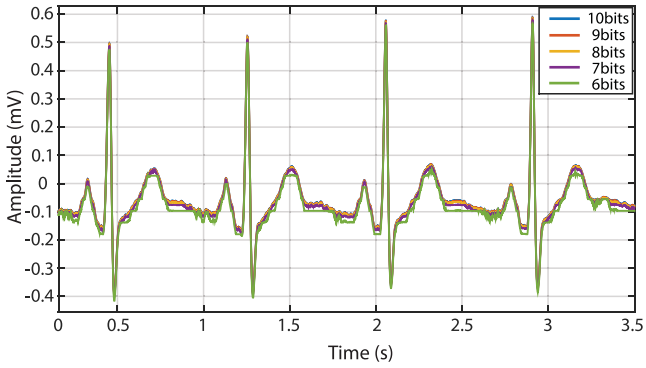

Fig. 17. Plot of the ECG waveforms as digitized by an ADC at various resolutions.

and the fixed $V_{\rm step}$ method, respectively, implying that the 3rd harmonic is indeed the dominant source of the amplifier's nonlinearity. For the proposed $V_{\rm step}$-distribution method, the SNDR of 71 dB amounts to an input-referred noise-plus-distortion of 213 $\mu{\rm V_{rms}}$. Removing the 3rd harmonic results in the SNR of 75 dB, which amounts to an integrated input-referred noise of 150 $\mu{\rm V_{rms}}$; this value agrees reasonably well with the measured input-referred noise of 143.6 $\mu{\rm V_{rms}}$ discussed earlier.

Since the frequency of the large interference stressing the proposed amplifier may vary—the interference can be either a low-frequency MA or a 60-Hz mains interference—it is instructive to assess the amplifier's nonlinearity at various input frequencies and amplitudes. Fig. 16 shows the SNDRs of the proposed amplifier as a function of the input amplitude for the input frequencies of 0.5, 3, 30, and 60 Hz. At low input frequencies (0.5, 3, and 30 Hz), the SNDR is approximately a linear function of the logarithm of the input amplitude for the entire amplifier's input range, reaching around 68–71 dB at the maximum input amplitude (2.4 ${\rm V_{pp}}$). Unlike [15] and [16] in which the SNDRs at high input amplitudes saturate at much lower values due to errors from the reconstruction processes, our proposed amplifier suffers no such reconstruction error, and thus achieves high SNDRs even at a very high input amplitude. Such SNDR performance indicates that the proposed amplifier is highly-tolerant to large low-frequency interferences such as the electrode offset or MA. For the 60-Hz interference, the SNDR drops appreciably once the input amplitude exceeds 1.6 ${\rm V_{pp}}$ due to saturation of the physical output as discussed in III-D. Hence, with a 40-dB gain AFE preceding the amplifier, the maximum tolerable amplitude for the 60-Hz mains interference into the input of the acquisition system amounts to around 16 ${\rm mV_{pp}}$. Keeping the differential mains interference below such level can be achieved through careful control of the common-mode interference [5], a proper grounding scheme [31], and the use of an AFE with high-enough common-mode input impedances to reduce the effect of the electrode-impedance mismatch.

From these measured results, we can thus see that the use of a reasonably high-gain AFE ($>$ 40dB) can help keep the amplifier's noise and noise-plus-distortion referred to the input of the acquisition system well below our targeted 3 $\mu{\rm V_{rms}}$ as discussed in Section II.

C. Reduction of the Required ADC's Resolution

The main benefit of the proposed amplifier is to allow the use of a very high gain in the amplification stage without the worry of output saturation even in the presence of large input interferences. Such high gain helps relax the ADC resolution requirement, which, consequently, helps reduce power consumption and the design complexity of the ADC.

To illustrate the concept discussed above, we recorded an ECG from standard Ag-AgCl electrodes placed in the lead-II configuration using our on-chip ECG acquisition system [18]. The acquisition system consists of an on-chip AFE—with a gain of 200 V/V and an input-referred noise of around 2.5 $\mu{\rm V_{rms}}$—followed by the proposed amplifier. The amplifier's output was then digitized with the same on-chip 10-bit ADC discussed earlier. To emulate the digitization by lower-resolution ADCs, we just discarded specific numbers of the LSBs from each sample. For instance, to emulate the digitization by a 6-bit ADC, we discard 4 LSBs, and so on. Fig. 17 shows the recorded ECG referred to the input of the ECG acquisition system for the digitization at 6 to 10 bits of resolution. We can see that the ECG waveforms from the digitization at higher than 7 bits are nearly indistinguishable from each other, indicating that increasing the resolution beyond 7 bits provides negligible SNR improvement.

D. Tolerance to Motion Artifacts and Mains Interference

In this part, we investigate the proposed amplifier's tolerance to large MA and mains interference. To test the tolerance to MA, we emulated the input into the amplifier by superimposing a 1.6-${\rm V_{pp}}$ 0.5-Hz sinusoidal signal as MA—which is large enough to saturate the amplifier's output—on top of a pre-processed ECG whose amplitude is around 100 ${\rm mV_{pp}}$ (assuming that the ECG has been amplified by an AFE with a 40-dB gain). The combined input was then fed into the amplifier whose output was digitized by an 8-bit ADC—i.e., by the same 10-bit ADC with two LSBs discarded. Fig. 18 (blue trace) illustrates the digitized output of the proposed amplifier after reconstruction—normalized by a gain of 1,780 V/V to refer to the input of the ECG acquisition system. We can see that even when stressed by such large MA, the amplifier's output is not saturated, thus permitting the recovery of the ECG in the digital backend. To

TABLE II
PERFORMANCE SUMMARY AND COMPARISON TO PREVIOUS WORKS

Parameters	[15] **TCAS1'09**	[16] **TBCAS'14**	[11] **JSSC'11**	[14] **JSSC'15**	[32] **TCAS2'18**	**This work**
Tech.	0.35 μm	0.18 μm	0.5 μm	0.18 μm	0.13 μm	0.18 μm
Supply	3 V	1 V	2 V	1.2 V	1.8 V	1.2 V
Gain Scheme	signal-folding	signal-folding	PGA	PGA	fixed	signal-folding
ADC Res.	16 bits	8 bits	11 bits	13.5 bits	-	7 bits [(3)]
Samp. Rate	5 kS/s	20 kS/s	64 S/s 1.024 kS/s	500 S/s	-	4.096 kS/s
Gain (V/V)	400	512	3, 5, 9, 13	1, 2, 4	53.7	17.8
THD (3 harmonics)	0.7%@ 20 mV_p, 20 Hz 0.9%@ 1 mV_p, 20 Hz	0.2%@ 2 mV_{pp}, 3 Hz	- -	- -	0.06%@ 5.5 mV_{pp}, 12 Hz 0.7%@ 22 mV_{pp}, 12 Hz	0.022%@ 1.2 V_p 0.5-32 Hz
DR	96 dB	66 dB	-	84.8 dB	68 dB	75 dB
SNDR	43 dB[(1)]	32 dB@ 2.2 mV_{pp}, 10 Hz 26 dB@ 2.2 mV_{pp}, 30 Hz	-	-	55.7 dB@ 5.5 mV_{pp} 37 dB@ 22 mV_{pp}	**71 dB**
Area	0.08 mm^2	0.124 mm^2	-	7 mm^2[(2)]	0.24 mm^2	0.25 mm^2
Power	180 μW	2.52 μW	125 nW	12 μW	1.8 μW	2.64 μW

[(1)]Calculated from 0.7% THD @ 20 mV_p input.
[(2)]Estimated area of the PGA.
[(3)]Only 7-bit resolution is used to achieve the stated DR and SNDR performances.

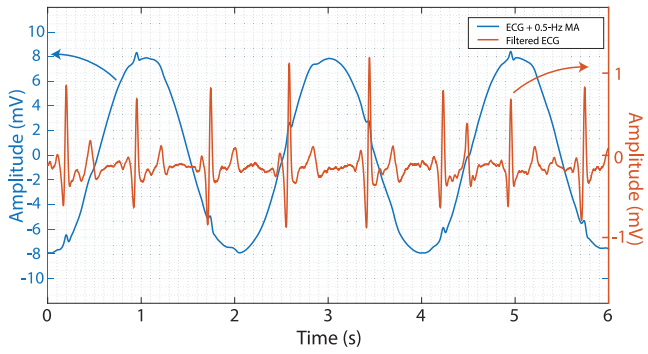

Fig. 18. Recording of an ECG corrupted by a very large MA.

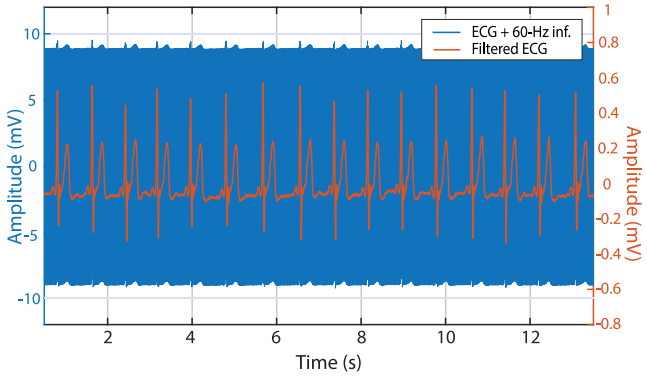

Fig. 19. Recording of an ECG corrupted by a very large mains interference.

illustrate this point, we applied a simple adaptive noise canceling technique using the generated MA as a reference to extract the clean ECG from the amplifier's output. The result is shown as the red trace in Fig. 18. We can see that even though the shapes of the P and T waves are affected by the filtering, the QRS complex is still clearly evident. It is worth noting that the quality of the filtered ECG depends much on the applied filtering algorithm, and not on the proposed amplifier as it only provides faithful ECG recording with minimal distortion to the ECG waveforms.

To test the tolerance of the proposed amplifier to mains interference, we emulated its input by superimposing a 1.6-V_{pp} 60-Hz sinusoidal signal as mains interference on top of a pre-processed ECG whose amplitude is around 100 mV_{pp}. Following the same procedure as in the MA case, we obtained the reconstructed output of the amplifier referred to the ECG acquisition system's input, as shown in Fig. 19 (blue trace). Not surprisingly, the amplifier's output exhibits no saturation, thus allowing us to recover the ECG from the recorded signal. Fig. 19 (red trace) shows the recovered ECG after the amplifier's output has been processed in MATLAB—by passing it through a 4th-order Butterworth notch filter centered at 60 Hz and then bandlimiting the result from DC to 150 Hz with a 4th-order Butterworth lowpass filter. Notice that, even when corrupted by a large 60-Hz interference, the features of the ECG waveforms are still quite well preserved, thanks to the excellent linearity of our proposed amplifier.

VI. CONCLUSION

This paper demonstrates a discrete-time amplifier that utilizes a signal-folding scheme to maximize its linearity even when the input is rail-to-rail. The proposed amplifier is suitable for use in place of PGAs to help eliminate the need for an automatic gain-control circuitry deemed necessary in most practical programmable-gain ECG acquisition systems. Also, the amplifier's high gain and excellent linearity help maximize the total gain of the amplification stage, thus allowing for the reduction of the ADC's resolution. Table II summarizes the performance of the proposed amplifier compared to previous works—including

previous signal-folding amplifiers [15], [16], PGAs in state-of-the-art ECG acquisition systems [11], [14], and a highly-linear AFE [32]. Note that, in Table II, the gains of the proposed work, [11], and [14] refer to the 2nd-stage amplifier's gain while the gains of [15], [16], and [32] refer to that of the entire AFE. It is also worth noting that our proposed amplifier achieves a very high SNDR of 71 dB while consuming only 2.64 μW of power from a 1.2-V supply. Such low-power consumption and high SNDR thus make the proposed amplifier attractive for ECG recording amid large differential interferences—e.g., in systems that use dry or non-contact electrodes.

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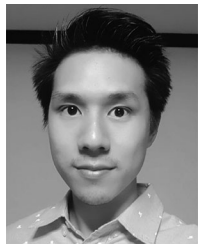

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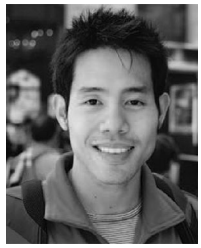

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A Micropower Motion Artifact Estimator for Input Dynamic Range Reduction in Wearable ECG Acquisition Systems

Bhirawich Pholpoke, Techapon Songthawornpong, and Woradorn Wattanapanitch, *Member, IEEE*

***Abstract*—This work presents the design and analysis of a compact low-power motion artifact estimator for reducing the input dynamic range in wearable ECG acquisition systems. The estimator employs a novel mixed-signal architecture that performs adaptive filtering on the electrode impedance information to derive a cancellation signal to suppress the motion artifact at the input of the acquisition system. A detailed noise analysis and optimization strategies are also provided to minimize the estimator's noise referred to the acquisition system's input. Fabricated in a 0.18-μm CMOS process and operating from a 1-V supply, the estimator occupies an active area of 0.11 mm^2 and consumes 2.6-3.2 μW of power depending on the final weights used. The low power consumption and small area thus make the estimator suitable for local placement at each recording channel in multi-channel ECG acquisition systems.**

***Index Terms*—ECG acquisition system, motion-artifact suppression, adaptive least-mean-square algorithm, mixed-signal adaptive filtering.**

I. Introduction

ACCORDING to recent statistics from The World Health Organization (WHO), more than 17.9 millions people worldwide succumb to some forms of cardiovascular diseases (CVDs) annually (equivalent to 31% of all the global deaths), making CVDs the leading cause of death among the world population [1]. Though still challenging, reducing CVD deaths is becoming feasible due to the emergence of low-power wearable electrocardiogram (ECG) recording devices that can noninvasively monitor ECG from the body's surface and send data to be interpreted by software or skilled cardiologists. Such technology can help provide immediate feedbacks to patients on their heart's healths, or even alert them of imminent heart failures; if widely available, it can not only save lives, but also help raise health awareness among users, thus lowering their chances of acquiring CVDs.

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To be useful in clinical applications, wearable ECG recording devices must address the problem of baseline fluctuations due to the movements of electrodes with respect to the skin—i.e., the motion artifact (MA) [2], [3]. MA increases the input dynamic range (DR) of the recording devices, necessitating most existing systems to employ low gain in their amplification chains followed by high-resolution analog-to-digital converters (ADCs); such approach incurs significant power overhead, thus resulting in higher power consumption. To minimize power, it is important to minimize the DR of the input signal such that the recording system can be designed with a high-gain instrumentation amplifier (IA) followed by a low-to-moderate-resolution ADC. This can be achieved by suppressing MA locally, near the input of the recording system, before the signal undergoes large amplification.

Currently, there exist several commercial wearable ECG monitors on the market. Only one product (QardioCore [4]) has full continuous monitoring capability while the rest—e.g., Whiting Move ECG [5], AliveCor [6], Apple Watch [7]—are designed to be wrist-worn, thus not intended for continuous ECG monitoring. To record ECG from these wrist-worn devices, the user needs to make two electrical contacts to complete the circuit, while staying still to avoid generating MA and let the devices record the clean ECG. Thus, MA suppression is less of a concern in these devices. However, MA suppression is critical for ECG devices with continuous monitoring capability such as QardioCore. Even though how QardioCore deals with the problematic MA is not revealed to the public, we speculate that it must employ an existing commercial analog frontend (AFE) chip, most of them dealing with MA in a very rudimentary manner such as using a high-pass corner to filter out MA [8]. Unfortunately, such simple filtering of MA from the recorded ECG inevitably leads to signal distortion as the MA's frequency contents overlap those of the ECG and its morphology typically resembles those of the P and T waves [9]. Therefore, most existing works in the literature address the MA suppression problem by utilizing computationally-expensive algorithms—e.g., filter bank [10], wavelet transforms [11]–[13], and the principal component analysis (PCA) and independent component analysis [14], [15]—thus are not suitable for on-chip implementation. One promising method due to its low computational complexity is the adaptive noise cancelling [9], [16]–[22], most employing the least-mean-square (LMS) adaptive filtering. To suppress MA, an adaptive filter, employing a reference signal correlated

to the MA in the recorded ECG, adjusts its coefficients to map the reference signal to the MA; the mapped reference signal is then subtracted from the recorded signal, leaving the output with relatively clean ECG waveforms. Note that for the adaptive noise canceling to be effective, there must exist a strong correlation between the reference signal and the MA in the recorded ECG as the low correlation between the two often leads to contamination of the desired ECG signal by the reference. To address the problem of low correlation, [23] proposed a two-stage algorithm: the first stage employs the weighed adaptive noise filtering (WAF) while the second stage employs a recursive Hampel filter. The WAF stage uses a cross-correlation factor to address the impact of the low correlation while the Hampel filter employs the spatial correlation between successive ECG waves to filter out MA. Nevertheless, due to their still high computational complexity, all the works mentioned suppress MA in the digital backend, thus requiring recording devices with high input DR to prevent signal saturation even in the cases of strong MA.

To reduce the system's input DR requirement, the work in [24] employs LMS filtering to generate a cancellation signal and feeds it back to cancel with the MA near the system's input. With MA already suppressed, the signal can undergo additional amplification by the programmable amplifier without the worry of saturating its output range; the large amplification then allows the use of a moderate-resolution ADC without compromising the signal-to-noise ratio (SNR). Nevertheless, the system in [24] employs an off-chip microcontroller unit (MCU) to realize the LMS filter for estimating MA, which poses a certain disadvantages: First, a high-resolution digital-to-analog converter (DAC) is required to convert the MA cancellation signal produced by the MCU into an analog form to suppress MA in the analog domain—the DAC and its associated interface incur sizable power consumption and area; Second, the MCU incurs significant power overhead to the recording channel—the MSP430 MCU from Texas Instruments [25] normally used in low-power applications consumes at least 230 μA of current from a 2.2-V supply while operating at a clock rate of 1 MHz. In [26], the MCU used is responsible for 55% of the total power—amounting to more than 3 mW—mostly for streaming out the raw ECG and ETI signals. Also, the work in [24] demonstrates that the power consumption associated with the MCU can be significantly reduced by first performing feature extraction in the analog domain before performing digital signal processing in the MCU. Third, scaling to a higher-channel-count system can prove problematic since implementing an adaptive filter for every channel would require significant resources in the MCU, thus necessitating an MCU with higher performance and, consequently, higher power consumption. Finally, for scaling to the multi-lead active electrode scheme [27] in which a recording circuitry is placed directly on top of the electrode, sharing an MCU as a central unit to implement adaptive filtering for all the channels may result in very complicated signal distribution schemes and cabling requirements. Due to these reasons, we propose that a low-power low-complexity LMS filter be implemented locally at each recording site to reduce the overall system's power consumption and lower the signaling complexity and cabling requirements in multi-lead systems.

In this paper, we present a compact low-power MA estimator to derive a cancellation signal from a reference to help suppress MA near the input. The estimator employs a mixed-signal adaptive filter architecture based on a simple transconductance-capacitance (OTA-C) filter, counters, and chopper switches, thus resulting in a small area and low power consumption, making it suitable for local placement at each recording channel in multi-lead ECG recording systems. In this work, only the MA estimator is implemented on-chip, which is integrated into an ECG recording system built on a printed circuit board (PCB) for demonstration.

Many forms of reference signals have been employed for MA suppression such as the skin stretch signal [17], [28], the electrode motion [18], [19], the optical bend signal [29], and the change in electrode impedance (ETI) [29]–[31]. Among the mentioned reference signals, ETI seems a promising candidate since not only does it exhibit high correlation with MA, which allows for the superior performance of the beat detection algorithms compared to the use of other reference signals [29], [31], it also is very amenable to low-power circuit design since no additional sensor is required to produce ETI: ETI can be generated relatively conveniently by injecting AC currents into the sensing electrodes and amplifying the resulting voltage [32], [33]. Since the injected AC currents have their spectral contents outside the ECG band, they do not corrupt the ECG's morphology. Thus, this work will assume the use of ETI as the reference signal, but other forms of reference signals should be applicable to the proposed topology as well.

In using adaptive filtering for MA suppression, we assume that there exists a strong correlation between the reference signal and MA in the recorded ECG. As discussed in [26], the ETI-MA correlation and the MA's amplitude depend on the types of movement artifacts, with the push/pull artifacts exhibiting the highest correlation and strongest MA's amplitude. In other artifact types (twisting/stretching the skin and other random artifacts), both the ETI-MA correlation and MA's amplitude are weaker, making the increase in the input DR not as severe as in the high-correlation case; but the low ETI-MA correlation may distort the recorded ECG when the proposed scheme is used. In this paper, we also investigate a scheme to preserve the original input ECG in cases of poor ETI-MA correlation such that other powerful digital algorithms [14], [15], [34] may be employed in the digital backend to separate MA from the recorded ECG.

The paper is organized as follows: Section II provides some physical insight into the generation of MA and how it inspires the simple transfer function of the proposed estimator. Section III then explains how to realize the estimator at the architectural level. Section IV then provides details on the circuit implementation and analysis. Section V provides noise analysis and discusses how the estimator can be incorporated into ECG acquisition systems without much noise penalty. Section VI shows the measured results. Finally, Section VII concludes the paper.

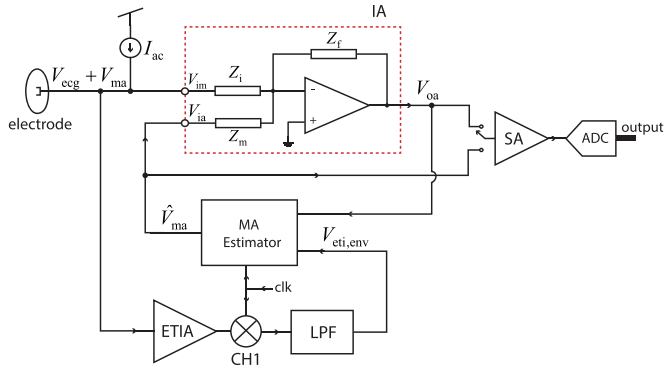


Fig. 1. The proposed MA estimator employed in an ECG recording channel.

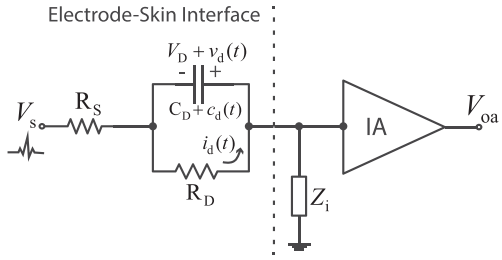


Fig. 2. A circuit model for understanding the MA generation mechanism.

II. General Considerations

A. An ECG Recording Channel With Embedded MA Estimator

Fig. 1 illustrates the concept of an ECG recording channel housing the proposed MA estimator. The instrumentation amplifier IA consisting of two inputs—i) the main input $V_{\rm im}$ and ii) the auxiliary input $V_{\rm ia}$—retrieves the MA-corrupted ECG from the electrode ($V_{\rm ecg}+V_{\rm ma}$) on $V_{\rm im}$, and the MA-cancellation signal ($\hat{V}_{\rm ma}$) from the MA estimator on $V_{\rm ia}$. The estimator's task is to produce $\hat{V}_{\rm ma}$ to cancel with $V_{\rm ma}$ in the main input such that the output of the IA, $V_{\rm oa}$, contains negligible components of $V_{\rm ma}$. To provide an ability to reconstruct the original recorded signal in the case of poor ETI-MA correlation, the sampling amplifier SA samples and amplifies both $V_{\rm oa}$ and $\hat{V}_{\rm ma}$ before an ADC digitizes the SA's output and reports it to the digital backend, where they can be appropriately combined to reconstruct the original input signal.

In this work, the MA estimator uses ETI as the reference signal to produce $\hat{V}_{\rm ma}$; the ETI can be obtained by injecting common-mode AC currents into the two sensing electrodes as explained in [32]: in Fig. 1, the current source $I_{\rm ac}$ injects an AC current into the sensing electrode; the resulting modulated signal, centered at the frequency of the AC current, is amplified by the electrode impedance amplifier (ETIA), demodulated to baseband by the chopper switch CH1, and lowpass filtered to produce an envelope signal $V_{\rm eti,env}$ proportional to the ETI.

B. Mechanism of MA Generation

For on-chip local placement in each recording channel, the MA estimator should employ as simple an algorithm as possible to minimize area and power consumption. To understand our proposed topology, let's first understand how the MA in the input signal gives rise to the ETI. The analysis to be provided is by no means so accurate as to precisely predict the MA from the ETI. Instead, we will utilize a simple circuit model to provide just enough motivation for our proposed topology.

As discussed in [35], MA arises from the change in the electrode's half-cell potential due to mechanical disturbance of the double-layer capacitance. Illustrated in Fig. 2 is a widely-adopted model of the electrode-skin interface when connected to an IA, in which $R_{\rm S}$ represents the nominal value of the electrolyte contact resistance, $C_{\rm D}$ of the double-layer capacitance, $R_{\rm D}$ of the leakage resistance through the double layer, $V_{\rm D}$ of the half-cell potential due to the total charge in the double layer, and $Z_{\rm i}$ of the input impedance of the IA. Let's assume that mechanical disturbance changes the value of the double-layer capacitance to $C_{\rm D}+c_{\rm d}(t)$, while negligibly affecting other parameters; this causes the redistribution of charge in the double layer as manifested by the incremental current $i_{\rm d}(t)$ flowing through it, thus changing the half-cell potential to $V_{\rm D}+v_{\rm d}(t)$; $v_{\rm d}(t)$ is then sensed by the IA. With $i_{\rm d}(t)=-v_{\rm d}(t)/R_{\rm D}$, we can relate $c_{\rm d}(t)$ to $v_{\rm d}(t)$ by

$$\frac{-v_{\rm d}(t)}{R_{\rm D}} = C_{\rm D}\frac{dv_{\rm d}(t)}{dt} + V_{\rm D}\frac{dc_{\rm d}(t)}{dt}. \tag{1}$$

The relationship in (1) can be easily understood in the frequency domain. Let $C_{\rm d}(j\omega)$ and $V_{\rm d}(j\omega)$ be the Fourier transforms of $c_{\rm d}(t)$ and $v_{\rm d}(t)$, respectively. It follows that the response $v_{\rm d}(t)$ due to $c_{\rm d}(t)$ can be expressed as a frequency response

$$\frac{V_{\rm d}(j\omega)}{C_{\rm d}(j\omega)} = \frac{(\omega R_{\rm D}C_{\rm D})^2}{1+(\omega R_{\rm D}C_{\rm D})^2}\cdot\frac{V_{\rm D}}{C_{\rm D}}\cdot\left(1-\frac{j}{\omega C_{\rm D}R_{\rm D}}\right), \tag{2}$$

which can be written in a polar form as $V_{\rm d}(j\omega)/C_{\rm d}(j\omega) = A\exp(j\theta)$, where $A=\sqrt{\frac{(\omega R_{\rm D}C_{\rm D})^2}{1+(\omega R_{\rm D}C_{\rm D})^2}}\cdot\frac{V_{\rm D}}{C_{\rm D}}$ and $\theta=-\tan^{-1}\left(\frac{1}{\omega R_{\rm D}C_{\rm D}}\right)$. Hence, the task of the MA estimator is reduced to finding a frequency mapping expressed in (2) by providing appropriate amplitude and phase responses to a quantity that is proportional to the change in the double-layer capacitance—i.e., the ETI in this work.

C. Extracting ETI With Common-Mode AC Currents

In this part, we consider how to extract the change in the double-layer capacitance in a differential recording setting. We adopt, with some modifications, the impedance measurement method proposed in [32] as shown in Fig. 3; in-phase AC currents of the form $I_{\rm o}\cos(\omega_{\rm c}t)$ are injected into the two sensing electrodes to produce a voltage input into ETIA, $V_{\rm eti,in}$. To ease the analysis, let's assume identical nominal values of the two double-layer capacitances, $C_{\rm D}$, and the contact resistances, $R_{\rm S}$, for the two recording electrodes, and ignore the leakage resistances $R_{\rm D}$ by assuming that the frequency of the AC currents, $\omega_{\rm c}$, is much larger than $1/(R_{\rm D}C_{\rm D})$. If $Z_{\rm i}$ of the ETIA is much

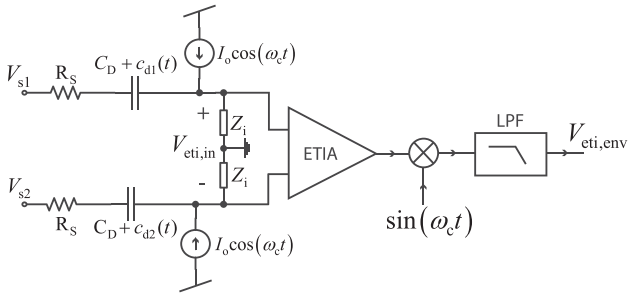


Fig. 3. Extraction of ETI in a differential recording setting.

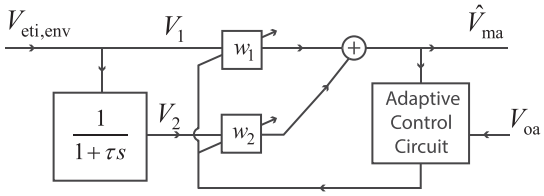


Fig. 4. High-level topology of the MA estimator.

larger than the electrode impedance, $V_{\mathrm{eti,in}}$ can be expressed as

$$V_{\mathrm{eti,in}} = \frac{I_{\mathrm{o}}}{\omega_{\mathrm{c}}}\left(\frac{1}{C_{\mathrm{D}}+c_{\mathrm{d1}}(t)} - \frac{1}{C_{\mathrm{D}}+c_{\mathrm{d2}}(t)}\right)\sin(\omega_{\mathrm{c}}t)\,. \quad (3)$$

By assuming that $C_{\mathrm{D}} \gg c_{\mathrm{d1}}(t), c_{\mathrm{d2}}(t)$ and letting $c_{\mathrm{d}}(t) = c_{\mathrm{d1}}(t) - c_{\mathrm{d2}}(t)$, we can reduce (3) to

$$V_{\mathrm{eti,in}} \approx -I_{\mathrm{o}} \cdot \frac{c_{\mathrm{d}}(t)}{C_{\mathrm{D}}^2\omega_{\mathrm{c}}}\sin(\omega_{\mathrm{c}}t)\,, \quad (4)$$

which shows that the amplitude (envelope) of $V_{\mathrm{eti,in}}$ is proportional to $c_{\mathrm{d}}(t)$. Another interesting point to note from (4) is that $V_{\mathrm{eti,in}}$ has a quadrature phase with respect to that of the injected AC currents, which also agrees with the finding in [26] that the correlation between MA and the complex impedance is much stronger than that between MA and the real impedance. Thus, instead of employing quadrature demodulation as in [24], [26], we choose to demodulate the output of the ETIA with just $\sin(\omega_{\mathrm{c}}t)$ and lowpass filter the result to produce $V_{\mathrm{eti,env}}$.

III. The Proposed MA Estimator

A. High-Level Considerations

Fig. 4 shows our proposed MA estimator that takes as input $V_{\mathrm{eti,env}}$ (also referred to as V_1) and provides the magnitude and phase mappings to produce $\hat{V}_{\mathrm{ma}}$. The MA estimator consists of a 1st-order lowpass filter—whose transfer function is $1/(1+\tau s)$—and two adjustable weights w_1 and w_2 controlled by an adaptive control circuit. The adaptive control circuit takes as input the output of the IA, V_{oa}, and performs an adaptive algorithm to adjust w_1 and w_2 to produce $\hat{V}_{\mathrm{ma}}$ that minimizes the mean-squared value of V_{oa}.

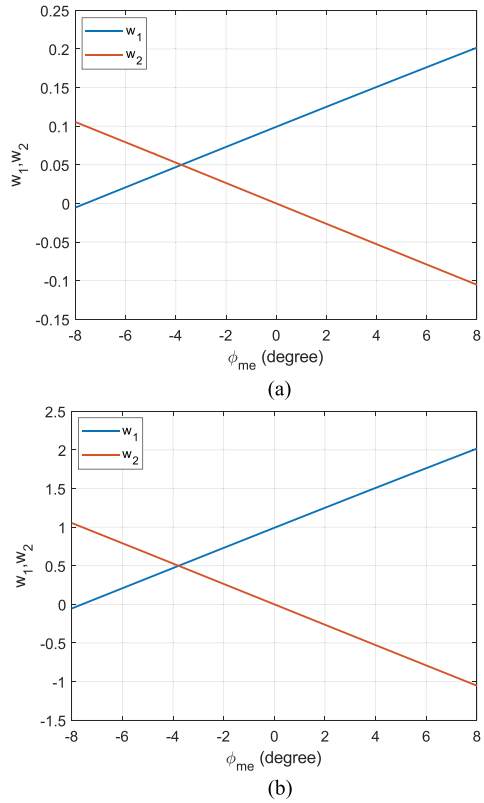


Fig. 5. The required values of w_1 and w_2 to achieve $-8^\circ \le \phi_{\mathrm{me}} \le 8^\circ$ for $1/\tau = 2\pi(15\,\mathrm{Hz})$ and $\omega_{\mathrm{ma}} = 2\pi(2\,\mathrm{Hz})$: (a) $A_{\mathrm{me}} = 0.1$ (b) $A_{\mathrm{me}} = 1.0$.

From Fig. 4, we can derive the transfer function from $V_{\mathrm{eti,env}}$ to $\hat{V}_{\mathrm{ma}}$ as

$$\frac{\hat{V}_{\mathrm{ma}}}{V_{\mathrm{eti,env}}}(s) = (w_1+w_2)\left(\frac{1+\frac{w_1}{w_1+w_2}\cdot\tau s}{1+\tau s}\right). \quad (5)$$

By choosing $1/\tau$ to be significantly higher than the frequency of the MA (ω_{ma}), we can approximate (5) near ω_{ma} as

$$\frac{\hat{V}_{\mathrm{ma}}}{V_{\mathrm{eti,env}}}(j\omega_{\mathrm{ma}}) \approx (w_1+w_2)\left(1+\frac{w_1}{w_1+w_2}\cdot j\omega_{\mathrm{ma}}\tau\right), \quad (6)$$

which is in the same form as (2). The magnitude and phase responses of the transfer function in (6) can be written as $A_{\mathrm{me}} = (w_1+w_2)\sqrt{1+(\frac{w_1}{w_1+w_2}\cdot\tau\omega_{\mathrm{ma}})^2}$ and $\phi_{\mathrm{me}} = \tan^{-1}(\frac{w_1}{w_1+w_2}\cdot\tau\omega_{\mathrm{ma}})$, respectively.

For proper circuit implementation, it is important to determine the required ranges of w_1 and w_2. In this work, we assume that the gain of the ETIA is large enough such that the required value of A_{me} never exceeds unity. For a particular value of A_{me}, we can analytically solve (6) for w_1 and w_2 to achieve a certain value of ϕ_{me}. Fig. 5(a) plots the values of w_1 and w_2 to achieve $A_{\mathrm{me}} = 0.1$ and obtain ϕ_{me} in the range of -8° to 8°, while Fig. 5(b) plots w_1 and w_2 to achieve the same range of ϕ_{me} for $A_{\mathrm{me}} = 1$. Both cases assume $\omega_{\mathrm{ma}} = 2\pi(2\,\mathrm{Hz})$ and $\tau = 1/(2\pi 15\,\mathrm{Hz})$. Note that we only limit $|\phi_{\mathrm{me}}|$ to within 8° because this range covers a sufficiently long time delay between $V_{\mathrm{eti,env}}$ and $\hat{V}_{\mathrm{ma}}$:

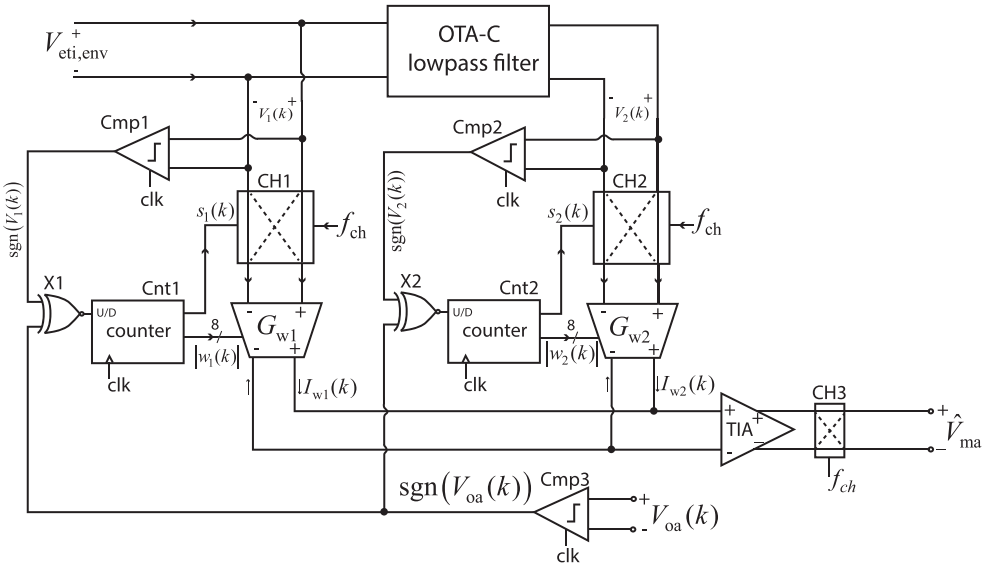


Fig. 6. The high-level schematic of the proposed motion artifact estimator.

for $\omega_{\rm ma} = 2\pi(2\,{\rm Hz})$, a 8° phase shift corresponds to 11.1 ms, which should be longer than the expected delay from the change in the double-layer capacitance to that in the half-cell potential.

We can see that the higher is $A_{\rm me}$, the higher are the magnitudes of w_1 and w_2. With $A_{\rm me} = 1$, the required value of w_1 is at the maximum, but still less than 2. It is not difficult to show that if we simply reverse the polarity of $A_{\rm me}$ while keeping its magnitude constant, the required w_1 and w_2 will attain the same magnitudes but opposite polarities. The forgoing analysis suggests that the appropriate range of w_1 and w_2 be $[-2, 2]$, provided that $|A_{\rm me}| \leq 1$ and $|\phi_{\rm me}| \leq 8^\circ$.

B. The Least-Mean-Square (LMS) Algorithm

In this section, we describe the adaptive algorithm for adjusting w_1 and w_2. To achieve low power and small area, we adopt an LMS algorithm [16] to minimize the mean-squared value of $V_{\rm oa}$ in a gradient-descent manner. Due to the very slow adaptation rate, we choose to implement the proposed topology in discrete time to avoid the use of continuous-time analog integrators, which consume large area and are prone to output saturation due to offsets [36].

To move $w_{1,2}$ in the directions opposite to the gradients of $V_{\rm oa}$, we employ the adaptation rule

$$w_{1,2}(k+1) = w_{1,2}(k) - \mu \frac{\partial(E(V_{\rm oa}^2(k)))}{\partial w_{1,2}}, \qquad (7)$$

in which k is the time step, μ is a constant determining the rate of adaptation, and $E(V_{\rm oa}^2(k))$ is the mean-squared value of $V_{\rm oa}$. We then approximate that $E(V_{\rm oa}^2(k)) \approx V_{\rm oa}^2(k)$ [36], which helps simplify (7) to

$$w_{1,2}(k+1) = w_{1,2}(k) - 2\mu \cdot V_{\rm oa}(k) \cdot \frac{\partial V_{\rm oa}(k)}{\partial w_{1,2}}. \qquad (8)$$

Recall from Fig. 1 that $V_{\rm oa}$ is a superposition of $V_{\rm ecg}$, $V_{\rm ma}$, and $\hat{V}_{\rm ma}$, while the algorithm can assert control only over $\hat{V}_{\rm ma}$. Assuming a negative gain from $V_{\rm ma}$ to $V_{\rm oa}$, we have $\partial V_{\rm oa}/\partial w_{1,2} \propto -\partial \hat{V}_{\rm ma}/\partial w_{1,2}$. From Fig. 4, we have $\hat{V}_{\rm ma}(k) = w_1 \cdot V_1(k) + w_2 \cdot V_2(k)$. Thus, substituting $\partial V_{\rm oa}(k)/\partial w_{1,2}$ in (8) with $\partial \hat{V}_{ma}(k)/\partial w_{1,2}$ gives

$$w_{1,2}(k+1) = w_{1,2}(k) + 2\mu \cdot V_{\rm oa}(k) \cdot V_{1,2}(k), \qquad (9)$$

where μ in (9) is different from that in (8) by a scale factor.

To simplify the circuit implementation, we adopt the sign-sign LMS (SS-LMS) algorithm [37], which helps reduce (9) to

$$w_{1,2}(k+1) = w_{1,2}(k) + 2\mu \cdot {\rm sgn}(V_{\rm oa}(k)) \cdot {\rm sgn}(V_{1,2}(k)), \qquad (10)$$

where ${\rm sgn}(\cdot)$ denotes the signum function. Due to this simplification, the ${\rm sgn}(\cdot)$ function can be implemented with a clocked comparator, which can be realized in a small area and consumes almost no static power; the multiplication of the signs can be implemented with just an exclusive-NOR (XNOR) gate, instead of a full-blown multiplier circuit; the integrators and the storage of the $w_{1,2}$ can be simultaneously realized with an up/down counter, while the step size μ and its rate of adaptation will be automatically determined by the resolution and the counting speed of the up/down counter, respectively.

C. The Circuit Topology

Fig. 6 shows the proposed MA estimator; at its heart are the operational transconductance amplifier-capacitance (OTA-C) lowpass filter to provide the required phase shift, and two up/down counters Cnt1 and Cnt2 to store and perform necessary integration of the weights w_1 and w_2. The clocked comparators Cmp1, Cmp2, and Cmp3 determine the signs of $V_1(k)$, $V_2(k)$, and $V_{\rm oa}(k)$, respectively. The XNOR gates X1 and X2 then multiply the signs of $V_1(k)$ and $V_2(k)$ to that of $V_{\rm oa}(k)$, whose results

update the counters Cnt1 and Cnt2: the counter Cnt1,2 counts up if $\mathrm{sgn}(V_{1,2}(k)) \cdot \mathrm{sgn}(V_{\mathrm{oa}}) = 1$, otherwise it counts down. For $w_{1,2}(k)$ to attain either polarity, the up/down counters are implemented in the sign-magnitude format—the 8-bit $|w_{1,2}(k)|$ represents the magnitude while the 1-bit $s_{1,2}(k)$ represents the sign.

To produce $\hat{V}_{\mathrm{ma}}$, the G_{w1} and G_{w2} OTAs, whose effective transconductances G_{w1} and G_{w2} are proportional to $w_1(k)$ and $w_2(k)$, first convert $V_1(k)$ and $V_2(k)$ into currents $I_{\mathrm{w1}}(k)$ and $I_{\mathrm{w2}}(k)$, respectively; that $G_{\mathrm{w1,2}} \propto w_{1,2}(k)$ thus makes $I_{\mathrm{w1,2}}(k) \propto w_{1,2}(k) \cdot V_{1,2}(k)$. The currents $I_{\mathrm{w1}}(k)$ and $I_{\mathrm{w2}}(k)$ are then summed and converted into $\hat{V}_{\mathrm{ma}}$ via a transimpedance amplifier TIA, providing $\hat{V}_{\mathrm{ma}} \propto w_1(k)V_1(k) + w_2(k)V_2(k)$.

Unlike the low-bandwidth OTA-C lowpass filter, the $G_{\mathrm{w1,2}}$ OTAs and the TIA are wideband circuits, whose 1/f noise dominates the ECG band. We therefore utilize the chopper stabilization technique—via the chopping switches CH1,2 and CH3—to suppress their 1/f noise: the switches CH1 and CH2 up-modulate $V_1(k)$ and $V_2(k)$ to the chopping frequency f_{ch}—at which the $G_{\mathrm{w1,2}}$-OTAs and the TIA exhibit only thermal noise—before they are transformed into currents and summed. The switch CH3 then demodulates the TIA's output to baseband to produce $\hat{V}_{\mathrm{ma}}$. Besides 1/f noise suppression, the three chopper switches, working in conjunction, control the polarities of the weights with respect to $\hat{V}_{\mathrm{ma}}$ as instructed by the sign bit $s_{1,2}(k)$: when $s_{1,2}(k) = 0$, the chopper switch CH1,2 operates in phase with CH3, effectively making $w_{1,2}(k)$ positive; on the contrary, $s_{1,2}(k) = 1$ instructs CH1,2 to operate in the opposite phase to that of CH3, effectively making $w_{1,2}(k)$ negative.

IV. Circuit Implementation

For the circuit implementation of the MA estimator, we decide on the fully-differential architecture, even at the expense of increased circuit complexity, due to two reasons: First, operating under a limited supply voltage (1 V), fully-differential circuit blocks allow sizable output swings and input linear ranges with minimal 2^{nd}-order nonlinearity, as deemed essential for minimizing the estimator's noise contribution to the overall system (see Sec. V-C); Second, fully-differential signaling facilitates the implementation of bipolar weights needed for the $G_{\mathrm{w1,2}}$ OTAs by just swapping between the two sides of their input/output terminals.

A. The Gm-C Lowpass Filter

Fig. 7(a) shows the OTA-C lowpass filter, consisting of two OTAs with the effective transconductances of G_{i} and G_{f}, a current integrator, and two source-follower buffers; the current integrator consists of a high-output-impedance current buffer with a current gain of 1/N and an integrating capacitance C_{F}. The source followers after the current integrator help shield the high-impedance nodes, V_{oc}^{+} and V_{oc}^{-} such that the output V_2 can drive the chopper switch CH2.

Fig. 7(b) shows the block diagram of the lowpass filter with R_{o} representing the current buffer's output impedance and A_{sf} the voltage gain of the source followers; $\overline{i_{\mathrm{no},G_{\mathrm{i}}}^2}$, $\overline{i_{\mathrm{no},G_{\mathrm{f}}}^2}$, and $\overline{i_{\mathrm{no,cbf1}}^2}$

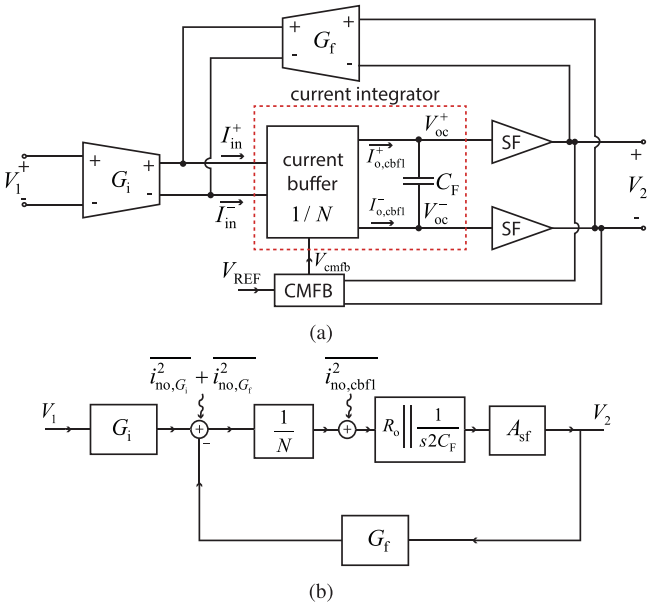


Fig. 7. (a) High-level schematic of the OTA-C lowpass filter. (b) Block diagram for the analysis of the OTA-C lowpass filter.

represent the output noise currents of the G_{i} and G_{f} OTAs, and the current buffer, respectively. From this block diagram, we can express the lowpass filter's transfer function as

$$\frac{V_2}{V_1}(s) \approx \frac{G_{\mathrm{i}}}{G_{\mathrm{f}}} \cdot \frac{1}{1 + s/\omega_{\mathrm{f}}}, \tag{11}$$

where $\omega_{\mathrm{f}} = G_{\mathrm{f}}A_{\mathrm{sf}}/(2NC_{\mathrm{F}})$, provided that $G_{\mathrm{f}}R_{\mathrm{o}}A_{\mathrm{sf}} \gg N$. In this implementation, we make $G_{\mathrm{i}} = G_{\mathrm{f}}$ to achieve a low-frequency gain of unity, while setting $\omega_{\mathrm{f}} \approx 2\pi(15\,\mathrm{Hz})$ with $C_{\mathrm{F}} = 10\,\mathrm{pF}$ to keep the overall area small. With $N = 2$, and $A_{\mathrm{sf}} \approx 1$, the required value for $G_{\mathrm{i,f}}$ to achieve such ω_{f} is 3.77 nA/V. A standard differential pair with each input transistor operating in subthreshold at 1-nA bias current provides approximately 27 nA/V of effective transconductance (assuming a gate coupling coefficient (κ) of 0.7), still far above the value required to achieve the desired ω_{f}. Hence, to achieve the required ω_{f} while keeping C_{F} around 10 pF, we need to reduce the values of $G_{\mathrm{i,f}}$ by a factor of 0.14 as will be described next.

1) The G_i and G_f OTAs: The most energy-efficient method to reduce $G_{\mathrm{i,f}}$ is to lower the bias currents of both OTAs, but at an expense of making the OTAs more prone to mismatches due to all the transistors running in very deep subthreshold. Since the OTA's bias current of a few nanoamperes is considered already low, while reducing it further proves unnecessarily risky, we opt for the bulk-input technique to reduce the OTAs' effective transconductances without lowering their bias currents. Shown in Fig. 8(a), the $G_{\mathrm{i,f}}$ OTA employs the bulk input and the source degeneration techniques [38] to reduce its transconductance for a given bias current. Let $I_{\mathrm{o}} = I_{\mathrm{o}}^{+} - I_{\mathrm{o}}^{-}$ and $V_{\mathrm{in}} = V_{\mathrm{in}}^{+} - V_{\mathrm{in}}^{-}$ be the differential output current and the differential input voltage of the OTA, respectively. The feedback diagram in Fig. 8(b) summarizes the OTAs' operation in which $g_{\mathrm{m,i}}$, $g_{\mathrm{mb,i}}$, $g_{\mathrm{s,i}} = g_{\mathrm{m,i}} + g_{\mathrm{mb,i}}$, and $\overline{i_{\mathrm{n,i}}^2}$ are the transconductance, the body

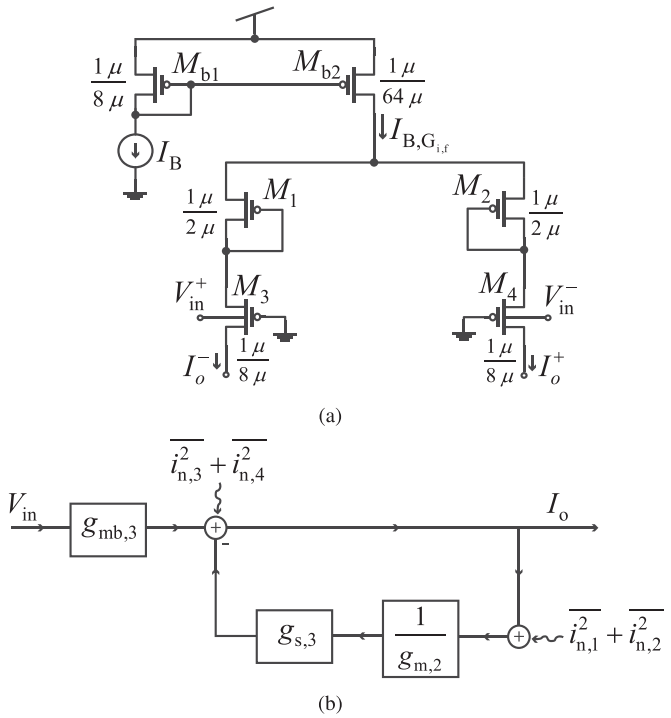


Fig. 8. (a) Schematic of the $G_{\rm i}$ and $G_{\rm f}$ OTAs. (b) The block diagram of the $G_{\rm i}$ and $G_{\rm f}$ OTAs including the noise sources.

effect conductance, the source conductance, and the output current noise of the transistor $M_{\rm i}$, respectively. Assuming that all the transistors are in subthreshold such that their small-signal conductances can be expressed as $g_{\rm m,i} = \kappa I_{\rm D,i}/\phi_{\rm t}$, $g_{\rm mb,i} = (1-\kappa)I_{\rm D,i}/\phi_{\rm t}$, and $g_{\rm s,i} = I_{\rm D,i}/\phi_{\rm t}$ [39]—where $I_{\rm D,i}$ is the drain current of $M_{\rm i}$, κ the gate coupling coefficient, and $\phi_{\rm t}$ the thermal voltage—we can derive the OTA's effective transconductance as

$$G_{\rm i,f} = \frac{I_{\rm o}}{V_{\rm in}}(s) = g_{\rm mb,3} \cdot \frac{g_{\rm m,1}}{g_{\rm m,1} + g_{\rm s,3}} = \frac{1-\kappa}{1+\kappa} g_{m,3}. \quad (12)$$

For $\kappa \approx 0.7$, we have $G_{\rm i,f} \approx 0.17 g_{\rm m,3}$, an attenuation factor closed to what we aimed.

2) The Current Integrator: Fig. 9(a) shows the schematic of the current buffer in the current integrator followed by the source-follower buffers. The $1/N$ current mirrors ($M_{\rm c1}$-$M_{\rm c4}$) pass the scaled-down version of the input current to be integrated onto C_F connecting between $V_{\rm oc}^+$ and $V_{\rm oc}^-$. The current buffer employs the regulated cascode technique—$M_{\rm c7}$-$M_{\rm c10}$ and $M_{\rm c11}$-$M_{\rm c14}$—to maximize its output impedance while minimizing the input impedance into the source of $M_{\rm c9,10}$ such that most of the signal current flows to the current buffer's output nodes, instead of being shunted away by the output conductance of $M_{\rm c3,4}$. The source followers ($M_{\rm s1}$ and $M_{\rm s2}$) then buffer the high-impedance nodes $V_{\rm oc}^+$ and $V_{\rm oc}^-$ to produce the output, $V_{\rm o} = V_{\rm o}^+ - V_{\rm o}^-$, that drives the chopper switch CH2 and the input of the $G_{\rm f}$ OTA. The source-follower buffers employ low-threshold devices for $M_{\rm s1}$ and $M_{\rm s2}$, whose bulks are tied to the sources, to eliminate the body effect and prevent significant DC level shift, which might otherwise limit the output voltage swing of the current integrator.

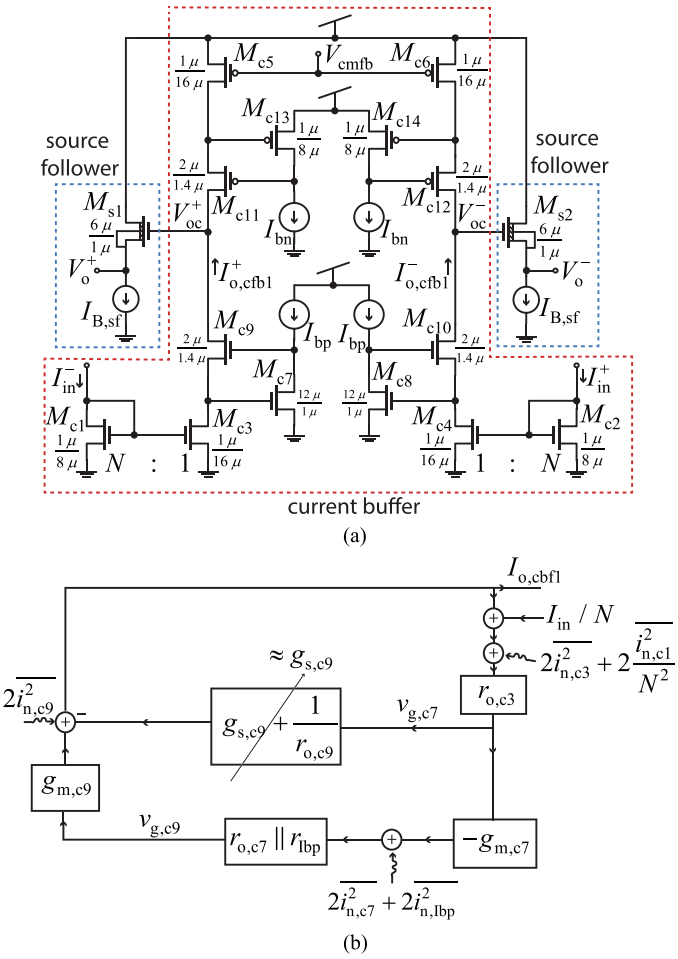


Fig. 9. (a) Schematic of the current buffer in the current integrator followed by the source-follower buffers. (b) Block diagram of the bottom half of the current buffer.

Fig. 9(b) shows the block diagram summarizing the small-signal analysis of the bottom-half of the current buffer—$M_{\rm c1}$-$M_{\rm c4}$, $M_{\rm c7}$-$M_{\rm c10}$ and the two $I_{\rm bp}$ current sources—in which $I_{\rm in} = I_{\rm in}^+ - I_{\rm in}^-$ and $I_{\rm o,cbf1} = I_{\rm o,cbf1}^+ - I_{\rm o,cbf1}^-$; $r_{\rm Ibp}$ and $\overline{i_{\rm n,Ibp}^2}$ are the output resistance and the noise current associated with each $I_{\rm bp}$ current source, respectively. The transfer function from $I_{\rm in}$ to $I_{\rm o,cbf1}$ can be written as

$$\frac{I_{\rm o,cbf1}}{I_{\rm in}} = \frac{1}{N} \frac{g_{\rm s,c9} r_{\rm o,c3} + g_{\rm m,c7}\left(r_{\rm o,c7} \parallel r_{\rm Ibp}\right) g_{\rm m,c9} r_{\rm o,c3}}{1 + g_{\rm s,c9} r_{\rm o,c3} + g_{\rm m,c7}\left(r_{\rm o,c7} \parallel r_{\rm Ibp}\right) g_{\rm m,c9} r_{\rm o,c3}} \approx \frac{1}{N}, \quad (13)$$

provided that $g_{\rm s,c9} r_{\rm o,c3} + g_{\rm m,c7}(r_{\rm o,c7} \parallel r_{\rm Ibp})\, g_{\rm m,c9} r_{\rm o,c3} \gg 1$.

B. The Weighted-Sum Circuit

Fig. 10(a) shows the high-level schematic of the weighted sum circuit, consisting of the $G_{\rm w1,2}$ OTAs and a transimpedance amplifier (TIA), also implemented as a current buffer with an OTA ($G_{\rm TIA}$) in feedback. The circuit computes $V_{\rm o}(k)$ as a weighted sum of the inputs $V_1(k)$ and

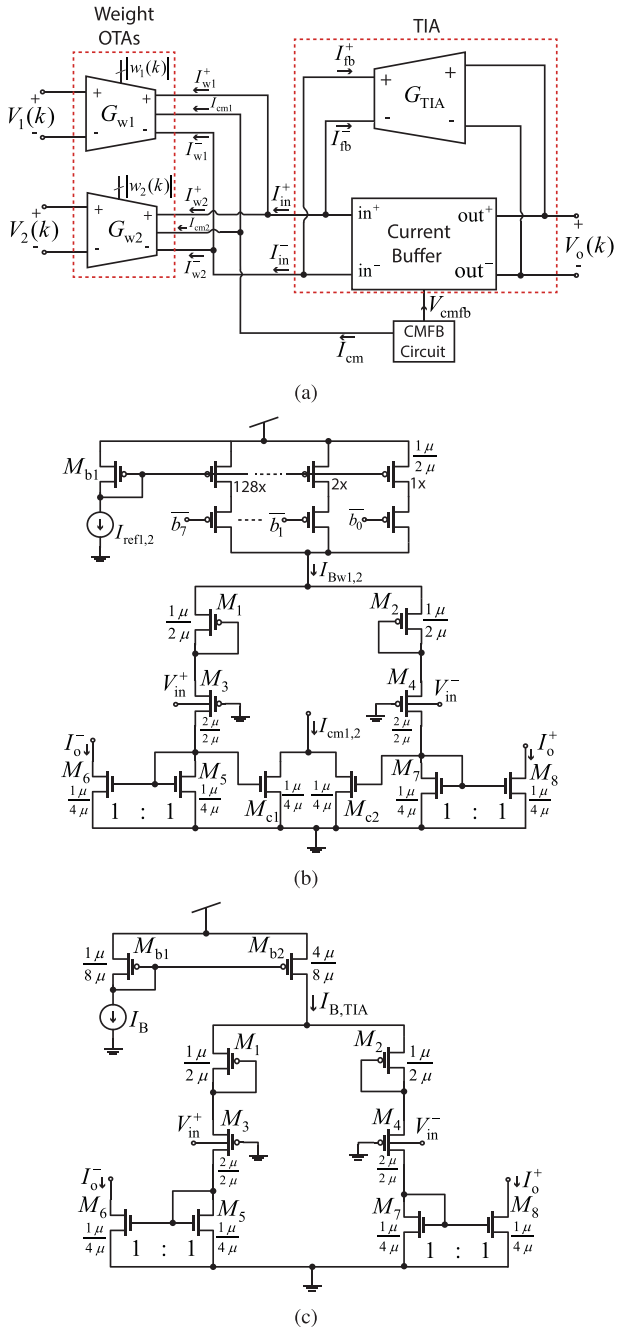


Fig. 10. The weighted-sum circuit: (a) High-level schematic. (b) Schematic of the weight OTAs ($G_{w1,2}$). (c) Schematic of the G_{TIA} OTA.

$V_2(k)$—i.e., $V_{\mathrm{o}}(k) = w_1(k)V_1(k) + w_2(k)V_2(k)$; the magnitude of each weight is programmable by the corresponding weight OTA's effective transconductance—$|w_{1,2}(k)| = G_{\mathrm{w1,2}}(k)/G_{\mathrm{TIA}}$. Fig. 10(b) shows the schematic of the $G_{\mathrm{w1,2}}$ OTAs whose input transistors operate in subthreshold to make their effective transconductances proportional to their bias currents; the weight's magnitude $|w_{1,2}(k)|$, implemented as eight programmable bits $\overline{b_7}, \ldots, \overline{b_0}$, determines the $G_{\mathrm{w1,2}}$ OTA's effective transconductance by controlling the bias current $I_{\mathrm{Bw1,2}}$. Note that changing the bias current of each weight OTA also alters its common-mode (CM) output current and, hence, the CM input current into the current buffer, which may subsequently disturb the CM output voltage of the overall weighted sum circuit. To avoid this issue, the weight OTAs provide their CM output currents ($I_{\mathrm{cm1,2}}$) to the common-mode feedback circuit (CMFB), which uses them to set the CM output voltage of the weighted sum circuit.

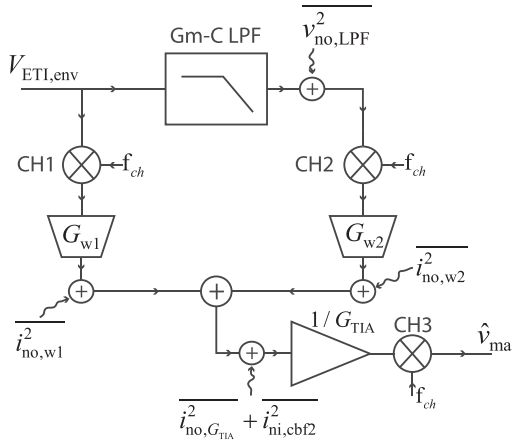


Fig. 11. Diagram for the noise analysis of the MA estimator.

To convert current to voltage, the TIA employs the same technique as that of the lowpass filter, but without the integrating capacitor: the G_{TIA} OTA provides voltage-current feedback around the current buffer to realize a transimpedance gain of $1/G_{\mathrm{TIA}}$. Fig. 10(c) shows the schematic of the G_{TIA} OTA, whose topology is almost identical to the $G_{\mathrm{i,f}}$ OTA in Fig. 8(a) except the G_{TIA} OTA incorporates the 1:1 current mirrors (M_5-M_8) at the output to reverse the polarity of the output current. The schematic of the TIA's current buffer is similar to that in Fig. 9(a), but with the input current mirrors (M_{c1}-M_{c4}) removed.

V. Noise Analysis

In this section, we derive an expression of the estimator's noise referred to the IA's input to understand how to optimize it based on other design parameters. Please note that all the noise expressions derived in this section refer to the power spectral density (PSD), even though we use just the word "noise" for short. First, let's derive an expression of the estimator's output noise using the high-level diagram in Fig. 11; $\overline{v^2_{\mathrm{no,LPF}}}$, $\overline{i^2_{\mathrm{no,w1,2}}}$, $\overline{i^2_{\mathrm{no,G_{TIA}}}}$, $\overline{i^2_{\mathrm{ni,cbf2}}}$ are the output voltage noise of the lowpass filter, the output current noise of the $G_{\mathrm{w1,2}}$ OTA, the output current noise of the G_{TIA} OTA, and the input-referred noise of the TIA's current buffer, respectively. With the TIA's gain of $1/G_{\mathrm{TIA}}$, the noise referred to the output node $\hat{V}_{\mathrm{ma}}$ can be calculated as

$$\overline{v^2_{\mathrm{no,MA}}} = \overline{v^2_{\mathrm{no,LPF}}}\left(\frac{G_{\mathrm{w2}}}{G_{\mathrm{TIA}}}\right)^2 + \left(\overline{i^2_{\mathrm{no,w1}}} + \overline{i^2_{\mathrm{no,w2}}} + \overline{i^2_{\mathrm{no,G_{TIA}}}} + \overline{i^2_{\mathrm{ni,cbf2}}}\right)\frac{1}{G^2_{\mathrm{TIA}}}. \quad (14)$$

Next, let's derive the expressions for all the noise sources in Fig. 11.

A. Noise of the Lowpass Filter

From the block diagram in Fig. 7(b), the output noise of the lowpass filter can be written as

$$\overline{v^2_{\mathrm{no,LPF}}}(f) \approx \left(\overline{i^2_{\mathrm{no},G_\mathrm{i}}} + \overline{i^2_{\mathrm{no},G_\mathrm{f}}} + N^2\overline{i^2_{\mathrm{no,cbf1}}}\right)\frac{1/G_\mathrm{f}^2}{1+(f/f_\mathrm{f})^2}, \tag{15}$$

where $f_\mathrm{f} = \omega_\mathrm{f}/2\pi$. To evaluate this expression, we need to derive $\overline{i^2_{\mathrm{no},G_{\mathrm{i,f}}}}$ and $\overline{i^2_{\mathrm{no,cbf1}}}$. From the block diagram in Fig. 8(b) and assuming that $g_{\mathrm{m},2} = \kappa g_{\mathrm{s},3}$ and $g_{\mathrm{mb},3} = (1-\kappa)g_{\mathrm{s},3}$, we can derive $\overline{i^2_{\mathrm{no},G_{\mathrm{i,f}}}}$ in terms of κ as

$$\overline{i^2_{\mathrm{no},G_{\mathrm{i,f}}}} = 2\overline{i^2_{\mathrm{n},1}}\left(\frac{1}{1+\kappa}\right)^2 + 2\overline{i^2_{\mathrm{n},3}}\left(\frac{\kappa}{1+\kappa}\right)^2. \tag{16}$$

To find $\overline{i^2_{\mathrm{no,cbf1}}}$, we first consider the bottom half of the current buffer in Fig. 9(a), whose block diagram is given in Fig. 9(b). Let $\overline{i^2_{\mathrm{no,bl}}}$ be the output current noise of this structure. It can be shown that

$$\overline{i^2_{\mathrm{no,bl}}} \approx 2\frac{\overline{i^2_{\mathrm{n,c1}}}}{N^2} + 2\overline{i^2_{\mathrm{n,c3}}}, \tag{17}$$

provided that $g_{\mathrm{m,c7}}(r_{\mathrm{o,c7}} \parallel r_{\mathrm{Ibp}})g_{\mathrm{m,c9}}r_{\mathrm{o,c3}} \gg 1$. In other words, virtually all the noises of M_{c1}-M_{c4} flow to the output of the current buffer while the noises of $M_{\mathrm{c7,8}}$, $M_{\mathrm{c9,10}}$, and the two I_{bp} current sources can be ignored. Similarly, for the top half of the current buffer—$M_{\mathrm{c5,6}}$, M_{c11}-M_{c14}, and the two I_{bn} current sources—only the noises of M_{c5} and M_{c6} need to be taken into account. As a result, the total output current noise of the current buffer can be approximated as

$$\overline{i^2_{\mathrm{no,cbf1}}} \approx 2\left(\frac{\overline{i^2_{\mathrm{n,c1}}}}{N^2} + \overline{i^2_{\mathrm{n,c3}}} + \overline{i^2_{\mathrm{n,c5}}}\right). \tag{18}$$

Next, we can find the total output voltage noise $\overline{v^2_{\mathrm{no,LPF}}}$ by substituting $\overline{i^2_{\mathrm{no},G_{\mathrm{i,f}}}}$ in (16) and $\overline{i^2_{\mathrm{no,cbf1}}}$ in (18) into the expression of $\overline{v^2_{\mathrm{no,LPF}}}$ in (15), and using the expression of G_f in (12) to obtain

$$\overline{v^2_{\mathrm{no,LPF}}} = \left[4\frac{\overline{i^2_{\mathrm{n},1}}}{g^2_{\mathrm{m},3}}\frac{1}{(1-\kappa)^2} + 4\frac{\overline{i^2_{\mathrm{n},3}}}{g^2_{\mathrm{m},3}}\left(\frac{\kappa}{1-\kappa}\right)^2 + \left(\frac{1+\kappa}{1-\kappa}\right)^2 \left(2\frac{\overline{i^2_{\mathrm{n,c1}}}}{g^2_{\mathrm{m},3}} + 2N^2\frac{\overline{i^2_{\mathrm{n,c3}}}}{g^2_{\mathrm{m},3}} + 2N^2\frac{\overline{i^2_{\mathrm{n,c5}}}}{g^2_{\mathrm{m},3}}\right)\right]\cdot\frac{1}{1+(f/f_\mathrm{f})^2}, \tag{19}$$

in which $\overline{i^2_{\mathrm{n},1}}$, $\overline{i^2_{\mathrm{n},3}}$, and $g_{\mathrm{m},3}$ refer to the noises of M_1 and M_3 and the transconductance of M_3 in either of the G_i or G_f OTA since the two OTAs are assumed identical and consume the same bias current. Due to its operation at low frequency, the lowpass filter is dominated by 1/f noise. Therefore, we can express the noise current of a transistor M_i in (19) as $\overline{i^2_{\mathrm{n,i}}} = K_{\mathrm{n(p)}}g^2_{\mathrm{m,i}}/(W_\mathrm{i}L_\mathrm{i}\cdot f)$, where $K_{\mathrm{n(p)}}$ is the 1/f noise coefficient of the n-type (p-type) transistor and $W_\mathrm{i}L_\mathrm{i}$ represents the gate area of M_i. Since the current in M_{c1} is the sum of the currents in M_3's of the G_i and G_f OTAs, we have $g_{\mathrm{m,c1}} = 2g_{\mathrm{m},3}$. Also, since the current in M_{c1} is N times the current in M_{c3}, we have $g_{\mathrm{m,c3}} = 2g_{\mathrm{m},3}/N$. And since M_1 and M_3 pass the same current, we have $g_{\mathrm{m},1} = g_{\mathrm{m},3}$. With some algebraic manipulations, we can simplify (19) into a compact form as

$$\overline{v^2_{\mathrm{no,LPF}}} = \left(\frac{K_\mathrm{p}}{A_{\mathrm{p,eff}}} + \frac{K_\mathrm{n}}{A_{\mathrm{n,eff}}}\right)\cdot\frac{1}{f}\cdot\frac{1}{1+(f/f_\mathrm{f})^2}, \tag{20}$$

where

$$A_{\mathrm{p,eff}} = \left(\frac{1-\kappa}{2}\right)^2(W_1L_1) \left\| \left(\frac{1-\kappa}{2\kappa}\right)^2(W_3L_3) \right\| \left(\frac{1-\kappa}{2\sqrt{2}\,(1+\kappa)}\right)^2(W_{\mathrm{c5}}L_{\mathrm{c5}}) \tag{21}$$

and

$$A_{\mathrm{n,eff}} = \left(\frac{1-\kappa}{2\sqrt{2}\,(1+\kappa)}\right)^2(W_{\mathrm{c1}}L_{\mathrm{c1}}) \left\| \left(\frac{1-\kappa}{2\sqrt{2}\,(1+\kappa)}\right)^2(W_{\mathrm{c3}}L_{\mathrm{c3}}). \right. \tag{22}$$

The parameters $A_{\mathrm{p,eff}}$ and $A_{\mathrm{n,eff}}$ in (20) can be thought of as the effective areas of all the combined noise-contributing p-type and n-type transistors in the lowpass filter, respectively—the gate areas of the noise contributing transistors are multiplied by appropriate coefficients before being combined in a parallel fashion—thus, they can provide some insight into which transistors have stronger effects on the overall noise of the lowpass filter: among the transistors of the same type and the same physical gate area, the one with smaller coefficient dominates the parallel combination, hence limiting how large $A_{\mathrm{p(n),eff}}$ can be. For $A_{\mathrm{p,eff}}$, with $\kappa \approx 0.7$, the coefficients of W_1L_1 and W_3L_3 are calculated to be 2.25×10^{-2} and 4.6×10^{-2}, respectively, while the coefficient of $W_{\mathrm{c5}}L_{\mathrm{c5}}$ is 3.89×10^{-3}; therefore, M_{c5} has stronger effect on the overall noise compared to M_1 and M_3. Thus, if noise reduction from the p-type transistors is desired, we should focus on increasing the physical gate areas of M_{c5}. For $A_{\mathrm{n,eff}}$, M_{c1} and M_{c3} have the same coefficient, which is also equal to the p-type M_{c5}'s.

B. Noise of the Weighted Sum Circuit

The noise analysis of the $G_{\mathrm{w1,2}}$ and G_{TIA} OTAs are similar to that of the G_i and G_f OTAs except for the additional noise of the output current mirrors (M_5-M_8 in Fig. 10(b) and 10(c)). Borrowing from (16) and incorporating the noise from M_5-M_8, we can express the output noise of the $G_{\mathrm{w1,2}}$ and the G_{TIA} OTAs as

$$\overline{i^2_{\mathrm{no},G_\mathrm{j}}} = 2\overline{i^2_{\mathrm{n},1}}\left(\frac{1}{1+\kappa}\right)^2 + 2\overline{i^2_{\mathrm{n},3}}\left(\frac{\kappa}{1+\kappa}\right)^2 + 2\overline{i^2_{\mathrm{n},5}} + 2\overline{i^2_{\mathrm{n},7}}, \tag{23}$$

where $j \in \{w1, w2, \mathrm{TIA}\}$ and $\overline{i^2_{\mathrm{n,i}}}$ is the output current noise of M_i in the respective OTA. The topology of the current buffer in

the TIA is similar to that in the lowpass filter, except that it does not have the input current mirrors (no M_{c1}-M_{c4} in Fig. 9(a)). Borrowing from (18) while discarding the noise from M_{c1}-M_{c4}, we can write an expression for the input-referred noise of the TIA's current buffer, $\overline{i^2_{\mathrm{ni,cbf2}}}$, as

$$\overline{i^2_{\mathrm{ni,cbf2}}} \approx 2\overline{i^2_{\mathrm{n,c5}}}. \tag{24}$$

Recall the chopping operation in Fig. 6. Assuming that the chopping frequency f_{ch} is higher than the 1/f noise corners of the $G_{\mathrm{w1,w2,TIA}}$ OTAs, we then only need to consider their thermal noise contributions—i.e., $\overline{i^2_{\mathrm{n,i}}} = 4kT\gamma g_{\mathrm{m,i}}$ where k is the Boltzmann's constant, T is the absolute temperature, and γ is the thermal noise excess factor. Since all the transistors in each OTA operate in subthreshold and carry the same bias current, we can approximate that their transconductances, and hence their thermal noise currents, are the same. Using (12) to write $g_{\mathrm{m,i}}$ in terms of G_{j}, we can write the current noise of each transistor as $\overline{i^2_{\mathrm{n,i}}} = 4kT\gamma G_{\mathrm{j}}(\frac{1+\kappa}{1-\kappa})$. Consequently, we can simplify (23) to

$$\overline{i^2_{\mathrm{no},G_{\mathrm{j}}}} = 4kT\gamma G_{\mathrm{j}} \cdot N_{\mathrm{G}}, \tag{25}$$

where $N_{\mathrm{G}} = 2(3\kappa^2 + 4\kappa + 3)/(1-\kappa^2)$; the total output noise of the G_{j} OTA in (25) can be interpreted as the sum of the noise currents from N_G devices, each with an effective transconductance of G_{j}.

Similarly, we can express $\overline{i^2_{\mathrm{ni,cbf2}}}$ in (24) in terms of G_{j}. Since the current in $M_{\mathrm{c5,6}}$ of the current buffer is equal to the sum of the currents of the $G_{\mathrm{w1,w2,TIA}}$ OTAs' input transistors, we can then write $g_{\mathrm{m,c5}} = \sum_j g_{\mathrm{m3,j}} = (\frac{1+\kappa}{1-\kappa})\sum_j G_{\mathrm{j}}$, where $g_{\mathrm{m3,j}}$ is the transconductance of M_3 in the G_{j} OTA. Substituting this $g_{\mathrm{m,c5}}$ into (24), we can express $\overline{i^2_{\mathrm{ni,cbf2}}}$ as

$$\overline{i^2_{\mathrm{ni,cbf2}}} \approx 4kT\gamma \left(\sum_{j\in\{\mathrm{w1,w2,TIA}\}} G_{\mathrm{j}} \right) \cdot N_{\mathrm{cbf2}}, \tag{26}$$

where $N_{\mathrm{cbf2}} = 2\cdot(1+\kappa)/(1-\kappa)$.

C. Optimization of the Overall MA Estimator's Noise

We will now derive the expression of the MA estimator's noise referred to the IA's input to understand how to optimize it. First, let's derive the output noise of the MA estimator by substituting (25) and (26) into (14) to obtain

$$\overline{v^2_{\mathrm{no,MA}}} = \overline{v^2_{\mathrm{no,LPF}}} \left(\frac{G_{\mathrm{w2}}}{G_{\mathrm{TIA}}}\right)^2 + \frac{4kT\gamma}{G_{\mathrm{TIA}}} \cdot \left(1 + \frac{G_{\mathrm{w1}}}{G_{\mathrm{TIA}}} + \frac{G_{\mathrm{w2}}}{G_{\mathrm{TIA}}}\right)(N_{\mathrm{G}} + N_{\mathrm{cbf2}}). \tag{27}$$

To refer this noise to the input of the IA, let A_{me} and A_{sig} be the gains from $\hat{V}_{\mathrm{ma}}$ to V_{oa} and from V_{im} to V_{oa} in Fig. 1, respectively. Then the MA estimator's noise referred to the IA's input, $\overline{v^2_{\mathrm{nIA,ME}}}$, can be calculated as $\overline{v^2_{\mathrm{nIA,ME}}} = \overline{v^2_{\mathrm{no,MA}}} \cdot (A_{\mathrm{me}}/A_{\mathrm{sig}})^2$. Thus, to make $\overline{v^2_{\mathrm{nIA,ME}}}$ small, we need to minimize the ratio $A_{\mathrm{me}}/A_{\mathrm{sig}}$ while still allowing the suppression of most of the MA in the input signal—i.e., $A_{\mathrm{me}}/A_{\mathrm{sig}}$ must still be large enough to allow $\hat{V}_{\mathrm{ma}}$ to suppress the strongest expected MA's amplitude, $V_{\mathrm{ma,max}}$, in the ECG signal. Let V_{L} be the linear range of the G_{TIA} OTA, which is assumed to be the largest value of $\hat{V}_{\mathrm{ma}}$ that the estimator can produce without significant distortion. The minimum value of $A_{\mathrm{me}}/A_{\mathrm{sig}}$ that still allows the estimator to suppress the MA in the input signal occurs when $V_{\mathrm{L}} \cdot A_{\mathrm{me}} \approx V_{\mathrm{ma,max}} \cdot A_{\mathrm{sig}}$. In other words, the minimum value of the ratio is given by

$$\left.\frac{A_{\mathrm{me}}}{A_{\mathrm{sig}}}\right|_{\mathrm{min}} \approx \frac{V_{\mathrm{ma,max}}}{V_{\mathrm{L}}}. \tag{28}$$

Writing $I_{\mathrm{B},G_{\mathrm{TIA}}} = G_{\mathrm{TIA}}V_{\mathrm{L}}$ [38], where $I_{\mathrm{B},G_{\mathrm{TIA}}}$ is the bias current of the G_{TIA} OTA, and assuming that $A_{\mathrm{me}}/A_{\mathrm{sig}}$ is chosen according to (28), we can write $\overline{v^2_{\mathrm{nIA,ME}}}$ as

$$\overline{v^2_{\mathrm{nIA,ME}}} = \overline{v^2_{\mathrm{no,LPF}}} \cdot \frac{(G_{\mathrm{w2}}V_{\mathrm{ma,max}})^2}{I^2_{\mathrm{B},G_{\mathrm{TIA}}}} + \frac{4kT\gamma}{I_{\mathrm{B},G_{\mathrm{TIA}}}} \cdot \frac{V^2_{\mathrm{ma,max}}}{V_{\mathrm{L}}} \cdot \left(1 + \frac{G_{\mathrm{w1}}}{G_{\mathrm{TIA}}} + \frac{G_{\mathrm{w2}}}{G_{\mathrm{TIA}}}\right)(N_{\mathrm{G}} + N_{\mathrm{cbf2}}). \tag{29}$$

The expression in (29) summarizes the noise contributions from the lowpass filter and the weighted sum circuit—i.e., the 1st and the 2nd terms on the right-hand side, respectively. It also suggests that the estimator's noise referred to the IA's input depends on the values of the weights after convergence ($G_{\mathrm{w1,2}}/G_{\mathrm{TIA}}$), the bias current of the TIA ($I_{\mathrm{B},G_{\mathrm{TIA}}}$), and the ratio of the expected maximum MA's amplitude to the maximum achievable output range of the estimator ($V_{\mathrm{ma,max}}/V_{\mathrm{L}}$). Table I provides typical values of the noise-determining parameters in (29). To show the relative importance of the two noise contributions, we plot the noise contribution of the lowpass filter (red trace) and that of the weighted sum circuit (blue trace) in Fig. 12 using the parameters in Table I. With the aide of the AC noise simulation, we assume that the output noise of the lowpass filter, $\overline{v^2_{\mathrm{no,LPF}}}$, follows the form $\overline{v^2_{\mathrm{no,LPF}}} = K/(f(1+f^2/f_{\mathrm{f}}^2))$; $K = 1.18 \times 10^{-8}\,\mathrm{V}^2$ and f_{f} is the 3-dB bandwidth of the lowpass filter, which is assumed to be 15 Hz for this work. Calculating the total noise from these two plots in the bandwidth from 0.1–100 Hz yields 2.8 $\mu\mathrm{V_{rms}}$ and 760 $\mathrm{nV_{rms}}$ for the lowpass filter and the weighted sum circuit, respectively, thus suggesting that the lowpass filter is the dominant noise source of the estimator.

An obvious approach to minimize $\overline{v^2_{\mathrm{nIA,ME}}}$ in (29) is to increase $I_{\mathrm{B},G_{\mathrm{TIA}}}$, but at the expense of higher power consumption. We might also be tempted to conclude that increasing V_{L} can significantly reduce $\overline{v^2_{\mathrm{nIA,ME}}}$ due to the smaller $A_{\mathrm{me}}/A_{\mathrm{sig}}$ that

TABLE I
TYPICAL PARAMETERS FOR THE CALCULATION OF THE ESTIMATOR'S NOISE

Parameters	Values
G_{w1}, G_{w2}	60 nA/V
G_{TIA}	100 nA/V
$I_{\mathrm{B,G_{TIA}}}$	100 nA
γ	1
κ	0.7
N_{G}	28.5
N_{cbf2}	11.33
V_{L}	1 V
$V_{\mathrm{ma,max}}$	20 mV

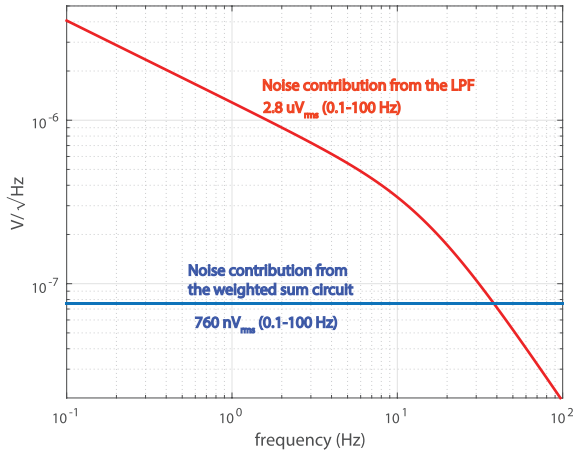


Fig. 12. Noise contributions of the lowpass filter and the weighted sum circuit to the IA's input-referred noise in (29).

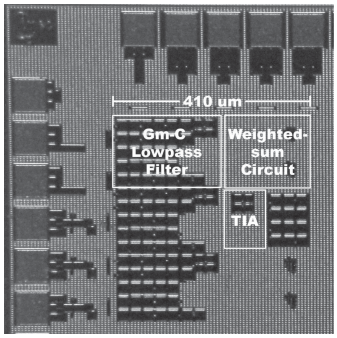
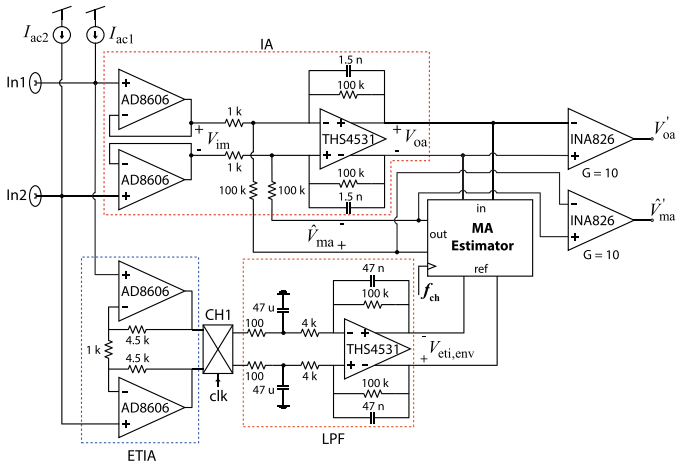
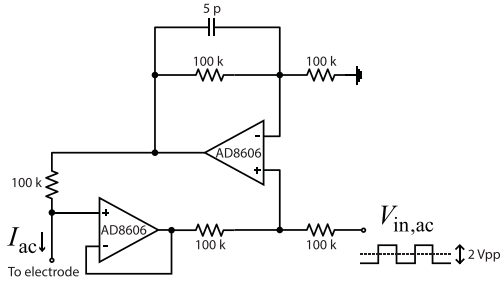


Fig. 13. Micrograph of the proposed MA estimator.



(a)



(b)

Fig. 14. (a) Schematic of the ECG acquisition system with real-time MA suppression capability. (b) Schematic of the AC current source for ETI extraction.

we can employ. However, increasing $V_{\rm L}$ raises both $\overline{v^2_{\rm no,LPF}}$ and $N_{\rm G}+N_{\rm cbf2}$, thus obscuring the noise reduction advantage. Nevertheless, the main benefit of increasing $V_{\rm L}$ is the larger allowable amplitude of the input into the MA estimator ($V_{\rm eti,env}$), thus allowing for a larger gain in the ETIA; this, in turn, results in smaller required weights $G_{\rm w1,2}/G_{\rm TIA}$ needed to suppress MA in the input signal and, subsequently, smaller $\overline{v^2_{\rm nIA,ME}}$. In this work, we opt for maximizing $V_{\rm L}$ to around 1 V by applying the source-degeneration and the bulk-input techniques to all the OTAs, such that the gain of the ETIA can be maximized. Such approach makes the dominant noise source of the MA reduction path be that of the ETIA, which should be relatively easy to design for low noise due to many well-known noise minimization techniques.

VI. Measurement Results

The proposed MA estimator was fabricated in a standard 0.18-μm CMOS process from the United Microelectronic Crop. (UMC). Fig. 13 shows the chip micrograph whose active area is 0.11 mm^2. The estimator operates from a 1-V supply and consumes a total bias current from 2.4 to 3.2 μA depending on the specific values of w_1 and w_2—measured by first turning off the adaptation algorithm, and then manually programming w_1 and w_2 to various values and probing by an electrometer (Keithley 6514) the total current consumed by the estimator. The objectives of this section are as follows:

1) Evaluate the estimator's performance on real-time MA suppression with ETI as a reference signal and explore the feasibility of signal reconstruction in the digital backend.
2) Evaluate the noise performance of the estimator.

To achieve the first objective, we have constructed an ECG acquisition system as proposed in Fig. 1—with our proposed MA estimator at its core—on a PCB, whose schematic is shown in Fig. 14(a). The IA consists of the unity-gain buffers (AD8606 from Analog Devices, Inc.), to provide high-impedance recording from the two electrodes, and the summing amplifier (THS4531, Texas Instruments Inc.), to superimpose the MA cancellation signal ($\hat{V}_{\rm ma}$) on the recorded ECG ($V_{\rm im}$) to suppress MA. The summing amplifier provides the signal-path gain $|A_{\rm sig}|=|V_{\rm oa}/V_{\rm im,d}|$ of 40 dB and the MA-cancellation-path gain $|A_{\rm me}|=|V_{\rm oa}/\hat{V}_{\rm ma}|$ of 0 dB to minimize the ratio $|A_{\rm me}/A_{\rm sig}|$ as discussed in Section V-C. The summing amplifier also provides lowpass filtering at 1 kHz to attenuate high-frequency noise without introducing a low-frequency pole in the MA suppression loop. The outputs of the summing amplifier ($V_{\rm oa}$) and the MA estimator $\hat{V}_{\rm ma}$ are then further amplified by an additional gain of 20 dB—making the overall gain of the signal path to be 60 dB—before being digitized by a 14-bit digital

oscilloscope (Analog Discovery 2, Digilent Inc.) to allow for signal reconstruction in the digital backend.

To extract ETI as a reference signal for the MA estimator, we incorporate two AC current sources, $I_{\rm ac1}$ and $I_{\rm ac2}$, which inject 20 $\mu{\rm V_{pp}}$ common-mode AC currents at 5 kHz into the two electrodes as discussed in Section II-C. Fig. 14(b) shows the schematic of each AC current source [40] whose output current, $I_{\rm ac}$, is related to the AC input voltage, $V_{\rm in,ac}$, by $I_{\rm ac} = V_{\rm in,ac}/100\,{\rm k}\Omega$. In our experiments, we used a 2-$\rm V_{pp}$ square wave for $V_{\rm in,ac}$ to produce 20-$\mu\rm V_{pp}$ square-wave current as the output of each AC current source. The resulting differential AC voltage from the two electrodes is then amplified by the ETI amplifier (AD8606 from Analog Devices, Inc.) whose gain is 20 dB before being demodulated to baseband by the chopper switch CH1 (TS5A23159, Texas Instruments Inc.). The output of the chopper switch is then filtered by a $2^{\rm nd}$-order lowpass filter (THS4531, Texas Instruments Inc.)—with a cutoff frequency of 33 Hz and a midband gain of 28 dB—to remove high-frequency noises and produce a clean ETI signal, $V_{\rm eti,env}$, as input into the MA estimator.

A. MA Suppression at Various Update Rates

To evaluate the estimator's performance at various algorithm's update rates, we connected the input of the ECG acquisition system in Fig. 14(a) to the experimenter's body in the lead-I configuration via standard Ag-AgCl electrodes. While the ECG acquisition system was recording ECG with the MA estimator running at a particular update rate, the experimenter pushed on the two electrodes alternately to generate a strong MA in the ECG waveform. Such experiment was performed at two different update rates—200 and 500 Hz—to illustrate how well at each update rate can the estimator attenuate MA. The outputs of the acquisition system, $V'_{\rm oa}$, and the estimator, $\hat{V}'_{\rm ma}$, were recorded by a 14-bit digital oscilloscope (Analog Discovery 2, Digilent, Inc.) at 6 kS/s. To mimic the use of a moderate-resolution/speed ADC (8-bit) in acquiring the data, we discarded six least significant bits and downsampled the two signals to a data rate of 600 S/s before plotting the results in Fig. 15(a) and 15(b).

The blue traces in Fig. 15(a) and 15(b) show the resulting $V'_{\rm oa}$ referred to the input of the acquisition system (normalized by a gain of 1000 V/V) while the red traces show $\hat{V}'_{\rm ma}$ referred to the output of the MA estimator (normalized by a gain of 10 V/V). To obtain the original input into the ECG acquisition system, we linearly combined $V'_{\rm oa}$ and $\hat{V}'_{\rm ma}$—with the sampling rate for both signals of 6 kS/s—with the appropriate signal-path and MA-cancellation-path gains to reconstruct $V_{\rm im}$ shown as the orange traces in Fig. 15(a) and 15(b). We can see in both of these cases that whenever $\hat{V}'_{\rm ma}$ exhibits a good correlation with $V_{\rm im}$—as when the red traces effectively track the orange traces—the baseline variations in $V'_{\rm oa}$ are strongly suppressed. Also, compared to when the update rate is 200 Hz, $\hat{V}'_{\rm ma}$ seems to track $V_{\rm im}$ better when the update rate is 500 Hz, which results in better suppression of MA in the recorded $V'_{\rm oa}$. However, the faster update rate also results in the more ringing (the high-frequency ringing seen in the $V'_{\rm oa}$ curve of Fig. 15(b)) in the output waveform—a result of the sign-sign LMS algorithm trying to follow noise even after the algorithm has converged. The ringing is normally small, thus does not affect the linearity of the output. Moreover, the information on the ringing is already contained in $\hat{V}'_{\rm ma}$, which we can later use to calibrate out the ringing in the output signal. This issue will be addressed next.

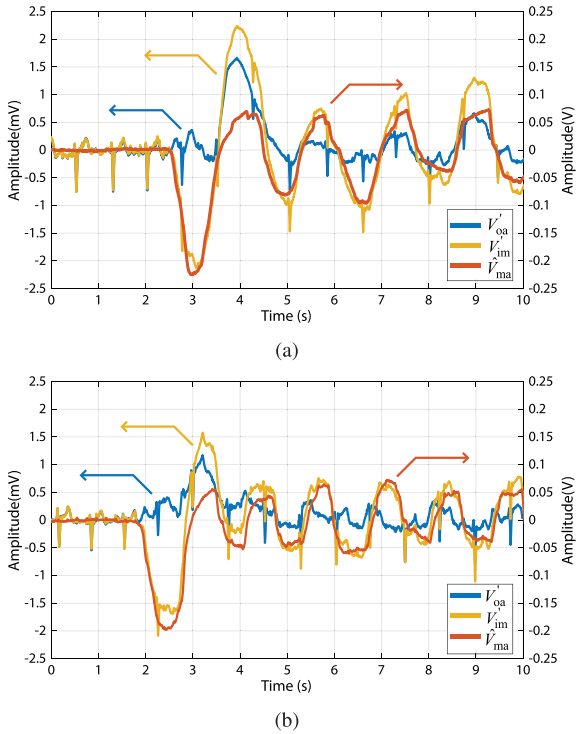


Fig. 15. Real-time MA suppression at the estimator's update rates of: (a) 200 Hz (b) 500 Hz.

B. Signal Reconstruction

In addition to the ringing artifact, imperfect correlation between MA and ETI due to nonlinearities in the MA generation process, and distortions introduced by the estimator itself may distort the ECG waveform. Thus, we should not view the proposed topology as a perfect mean to remove MA from the recorded ECG. Instead, the estimator is aimed to provide MA suppression to reduce the system's input DR, while allowing for the preservation of the original input signal. Fortunately, in the proposed scheme of Fig. 1, the MA estimator's output, $\hat{V}_{\rm ma}$, contains all the information subtracted from the original input signal. Thus, we can reconstruct the original input signal by combining, with appropriate scaling, $V_{\rm oa}$ and $\hat{V}_{\rm ma}$ in the digital backend. Also, due to the low-frequency nature of the MA (normally <2 Hz), $\hat{V}_{\rm ma}$ may be sampled at a relatively low sampling rate compared to $V_{\rm oa}$'s to help reduce the ADC's power overhead from digitizing additional signal.

Using the recorded $V'_{\rm oa}$ and $\hat{V}'_{\rm ma}$ from the experiment with the 500-Hz algorithm's update rate, we have reconstructed the

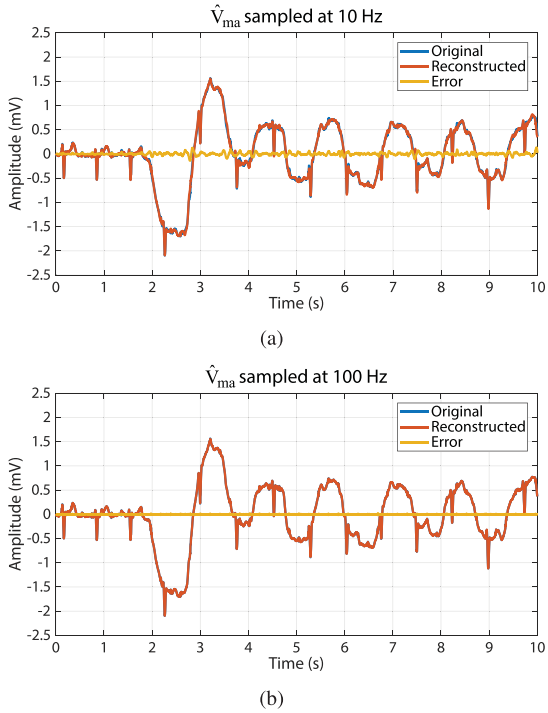


Fig. 16. Reconstructed input into the acquisition system when $\hat{V}'_{\rm ma}$ is sampled at: (a) 10 Hz (b) 100 Hz.

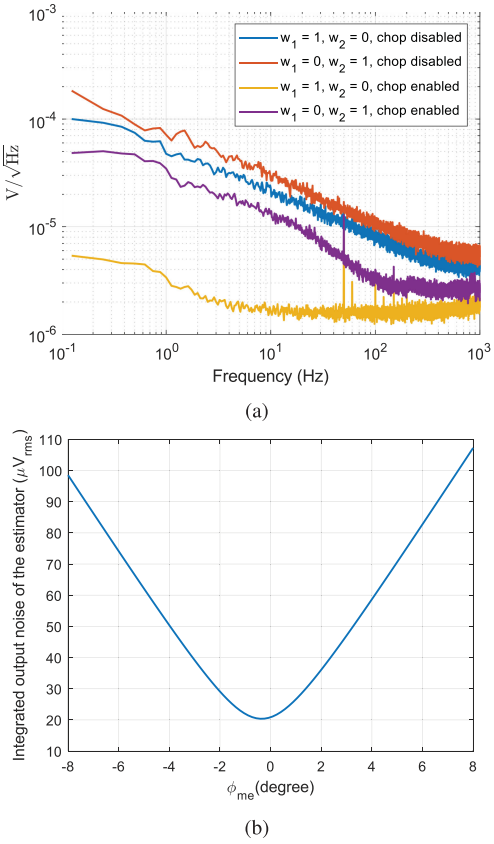


Fig. 17. (a) The MA estimator's output noise PSDs at different conditions (b) Total integrated output noise as a function of the estimator's phase shift.

input into the ECG acquisition system shown as the red traces in Fig. 16(a) and 16(b) with $\hat{V}'_{\rm ma}$ being sampled at 10 Hz and 100 Hz, respectively. $V'_{\rm oa}$ is always sampled at 600 Hz for both cases. The original signal is shown as blue traces in both plots—though barely visible as they are obscured by the reconstructed signal (red traces). The reconstruction errors for the $\hat{V}'_{\rm ma}$'s sampling rates of 10 Hz and 100 Hz are 27.92 and 3.27 $\mu{\rm V_{rms}}$, respectively. The result shows that both sampling rates result in successful reconstructions of the original signal, though the 10-Hz sampling rate exhibits larger reconstruction error.

C. Noise Performance

The integrated output noise of the estimator depends on the values of w_1 and w_2 after convergence. If little phase shift is required in the mapping ($w_1 \gg w_2$), the total noise is due mainly to the $G_{\rm w1}$ OTA and the TIA, which is mostly thermal due to the chopping operation; however, if the mapping requires a significant phase shift ($w_1 \ll w_2$), the estimator's noise will be dominated by the flicker noise of the lowpass filter. To depict the estimator's noise performance at all possible pairs of w_1 and w_2, we did the following: First, we measured the estimator's output noise at the two extremes—i) $w_1 = 1$ and $w_2 = 0$ (thermal noise dominant) and ii) $w_1 = 0$ and $w_2 = 1$ (flicker noise dominant). In the first case, the first term in (27) is nullified, making $\overline{v^2_{\rm no,MA}} \approx \frac{8kT\gamma}{G_{\rm TIA}}(N_{\rm G} + N_{\rm cbf2})$. In the second case, we assume that the first term in (27), which is flicker noise dominant, overwhelms the second term. Hence, with $w_2 = G_{\rm w2}/G_{\rm TIA} = 1$, we can approximate that $\overline{v^2_{\rm no,MA}} \approx \overline{v^2_{\rm no,LPF}}$.

Fig. 17(a) shows the power spectral densities (PSD) of the MA estimator's output noise ($\overline{v^2_{\rm no,MA}}$) from a dynamic signal analyzer (SR785 Stanford Research Systems) for the $(w_1 = 1, w_2 = 0)$ and $(w_1 = 0, w_2 = 1)$ cases, both when the chopping operation is disabled and enabled. It is evident that, with the chopping disabled, the noise PSDs in both cases are dominated by flicker noise (blue and red curves). With the chopping enabled, however, the noise PSD of the $(w_1 = 1, w_2 = 0)$ case is mostly thermal, with the 1/f noise corner well below 10 Hz (yellow curve). However, for the $(w_1 = 0, w_2 = 1)$ case in which the flicker noise of the lowpass filter can still pass through $G_{\rm w2}$ OTA to the output, the flicker noise is dominant up to around 150 Hz (purple curve). Integrating the two curves (chopping-enabled) from 0.1 Hz to 150 Hz yields the total integrated noise of 20.3 and 91.18 $\mu{\rm V_{rms}}$ for $(w_1 = 1, w_2 = 0)$ and $(w_1 = 0, w_2 = 1)$ cases, respectively. To estimate the total integrated noise for other sets of w_1 and w_2, we can calculate the weighted sum of the noise power using (27). Fig. 17(b) shows the integrated output noise of the MA estimator for w_1 and w_2 in Fig. 5(b) in which the MA estimator provides a gain of unity and a phase shift between $\pm 8^\circ$. As expected, small phase shift results in minimal integrated noise while large phase shift results in higher integrated noise due to the more noise contribution from the lowpass filter. The maximum integrated noise is 106 $\mu{\rm V_{rms}}$ at $\phi_{\rm me} = 8^\circ$ while the minimum integrated noise is 19.7 $\mu{\rm V_{rms}}$ at $\phi_{\rm me} = -0.4^\circ$.

TABLE II
PERFORMANCE SUMMARY AND COMPARISON TO PREVIOUS WORK

Ref.	This work	[24]
Tech. (μm)	0.18	Off-Chip (MSP430 MCU)
LMS variants	Sign-Sign LMS	Standard LMS
Adaptive filter's order	2	4
Delay element	G_{m}-C	Digital delay line
Cancellation scheme	TIA to AFE	12-bit DAC to PGA
AFE integration	Off-chip	On-chip
Estimator's power	3.2 μW (max)	NA*
Loop latency	2 ms (500-Hz update rate)	10 ms

* The power of the 12-bit DAC and MSP430 MCU were not reported.

The estimator's noise referred to the input of the recording system depends on the values of A_{me} and A_{sig} used—i.e., we have to scale the plot in Fig. 17(b) by $A_{\mathrm{me}}/A_{\mathrm{sig}}$. If we assume a typical value of $V_{\mathrm{ma,max}} \approx 20$ mV, the required $A_{\mathrm{me}}/A_{\mathrm{sig}}$ for the proposed estimator with $V_{\mathrm{L}} \approx 1$ V is just 1/50. Hence, the estimator's noise referred to the input of the recording system will range from 0.39 to 2.12 $\mu\mathrm{V}_{\mathrm{rms}}$, still an insignificant fraction of the input noise required by the standard in ECG acquisition [41].

One interesting question remains as to how the noises of other circuits in the ETI extraction path affect the quality of the recorded ECG. Due to the high gain of the ETIA required to produce a full-swing $V_{\mathrm{eti,env}}$, the ETIA's noise is the dominant noise source of the ETI extraction path. However, to keep the ETIA's noise referred to the main IA's input sufficiently low, it is important to avoid using too large an ETIA's gain. Nevertheless, it is difficult to pinpoint an optimal value of the ETIA's gain as this depends on many factors such as the magnitude and frequency of the AC currents injected into the electrodes, and the values of electrode impedances during the measurement; all these factors affect the amplitude of the input ETI signal, making the design and the optimization of the ETI extraction path an interesting active research area.

VII. CONCLUSION

We present the design of a compact low-power MA estimator to help reduce the input dynamic range of wearable ECG acquisition systems. By employing a simple OTA-C lowpass filter, clocked comparators, digital counters, switches, and other analog building blocks, the estimator performs linear filtering to derive a cancellation signal from an ETI reference, which can then be fed back to cancel with the MA near the system's input. Since the estimator aims to cancel MA right at the acquisition system's input, its noise can be a major concern. Table II summarizes the performance of the estimator compared to the state-of-the-art. In this paper, we also present a detailed analysis of the estimator's noise performance and provide recommendations on how to incorporate it into an ECG acquisition system without much noise penalty. To the best of the authors' knowledge, this work is the first on-chip motion artifact estimator to help suppress MA near the system's input before final amplification. Due to its low power consumption and small area, the estimator is suitable for local placement at each recording channel, thus attractive for use in multi-channel ECG acquisition systems.

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A Low-Power High-Input-Impedance 70-dB Gain ECG Readout System with High Interference Tolerance

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***Abstract*—This paper presents a low-power high-input-impedance electrocardiogram (ECG) readout system for recording from high-impedance electrodes. To minimize power, the system employs large amplification to minimize the required resolution of the analog-to-digital converter (ADC)—with a gain of 70 dB, only 7-bit ADC is required to not degrade the overall signal-to-noise ratio. Such a high gain is made feasible by a discrete-time signal-folding amplifier and an interference suppression circuit (ISC). Fabricated in a 0.18-μm CMOS process and operating from a 1.2-V supply, the system achieves an input-referred noise of 2.9 $\mu\mathrm{V_{rms}}$, while consuming 7.1 μW of power. With the ISC enabled for strong interference cases, the system can tolerate upto 100 $\mathrm{mV_{pp}}$ of interference while consuming 13.1 μW of power.**

***Index Terms*—ECG readout system, high-impedance electrodes, interference suppression feedback, signal-folding amplifier.**

I. Introduction

Recently, wearable electrocardiogram (ECG) readout systems are being developed for use in chronic non-invasive remote monitoring of the heart. Once such systems come into widespread use, they can act as an important platform for monitoring various heart conditions, giving patients with limited means accesses to high-quality personal cardiac diagnosis tools. Nevertheless, for such systems to be feasible as real wearable devices, they must deliver quality ECG recording, be very easy and comfortable to use, and consume very low power to eliminate the nuances of frequent battery recharging; this means that the ECG recording circuitry must be robust against all forms of interferences—i.e., the motion artifacts (MA) due to the movement of electrodes with respect to the skin and the 50/60 Hz mains interference (MI)—and be capable of recording from high-impedance (high-Z) electrodes (dry/non-contact electrodes) for maximum user's comfort.

Compared to the conventional Ag-AgCl gel electrodes, high-Z electrodes are very susceptible to MA and MI, which increase the input dynamic range of the recording system. To prevent signal clipping in the cases of strong interferences, most existing systems employ low overall gains, which, to prevent the quantization noise from degrading the signal-to-noise ratio (SNR), necessitates the use of high-resolution analog-to-digital-converters (ADCs), consequently resulting in higher overall power consumption. For examples, [1], [2] employ $\Delta\Sigma$ ADCs with 13.5b and 18b of resolutions, while consuming 50 and 83.6 μW of power, respectively. Other systems that employ low gains and low-resolution ADCs [3], [4] to minimize power achieve high input-referred noise, thus degrading the systems' sensitivities.

It is revealing to note that, on average, most recording systems infrequently encounter strong interferences—strong MA and MI may occur during the user's movements or his touching appliances plugged to poorly-grounded outlets. Thus, specifying the gain and ADC's resolution for such worst-case scenarios is suboptimal and wasteful of power. Instead, the overall power consumption can be much reduced if the system is designed for the normal scenarios (with small interferences) but is equipped with capabilities to handle strong interferences as needs arise.

In this paper, we present an ECG readout system which employs a very high gain (70 dB) and a low-resolution ADC, without significantly degrading the overall SNR. To prevent signal clipping due to the high gain, we employ two techniques: first, the signal-folding technique keeps the physical output level of the amplification stage within the ADC's input range, even though the actual output level may well exceed the supply rails; second, to handle the situations of strong interferences, the system incorporates an interference suppression circuit (ISC) to suppress interferences near the input of the system before the signal undergoes large amplification. Combining the two techniques ensure that, most of the time, the system operates in the most energy efficient fashion, while still capable of handling large interferences if they arise.

II. System Design Considerations

In this work, we design the readout system to have an input-referred noise below 3 $\mu\mathrm{V_{rms}}$ in a 150-Hz bandwidth—still well below the specification by The Association for The Advancement of Medical Instrumentation (AAMI) [5]—while being capable of recording 1-2 $\mathrm{mV_{pp}}$ ECG. To relax the ADC's resolution requirement, we employ the overall gain of 70 dB before the ADC. The 3 $\mu\mathrm{V_{rms}}$ system's input-referred noise will be amplified to 9.6 $\mathrm{mV_{rms}}$ at the ADC's input. Hence, for a differential full-scale voltage of 2.4 V, an effective-number-of-bits (ENOB) of only 6.2 suffices to keep

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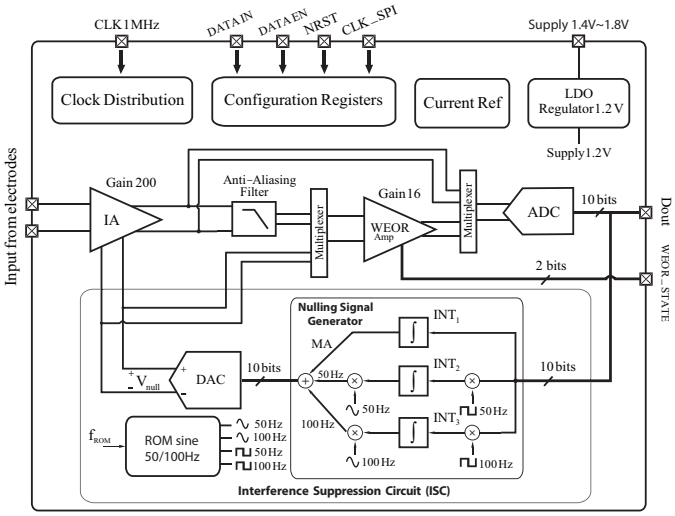


Fig. 1. High-level schematic of the proposed ECG readout system.

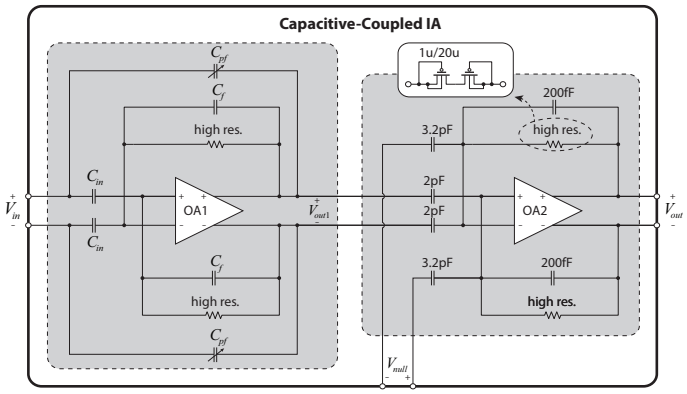


Fig. 2. Schematic of the instrumentation amplifier (IA)

the overall noise of the ADC below such value, thus resulting in a much simpler and more energy-efficient ADC.

Nevertheless, strong interferences determine the maximum input amplitude that the system must accommodate. To understand the worst-case scenario, we constructed a simple 3-wire ECG recording system from a commercially-available instrumentation amplifier (IA) [6] and used it to record ECG from dry electrodes made in-house from metallic buttons, each having a surface area of 1.5 cm^2. We found that pushing on one of the sensing electrodes can result in MA as large as tens of millivolts. We also estimated the worst-case MI by recording ECG when the user was touching a laptop plugged into an outlet without proper ground connection. We found that the recorded MI referred to the input is much larger than the desired ECG ($\approx 16\ \mathrm{mV_{pp}}$/1 $\mathrm{mV_{pp}}$) and that the recorded MI not only consists of the fundamental but also strong 2^{nd} harmonic. Such strong MI occurs despite the 120-dB common-mode-rejection-ratio (CMRR) of the IA, suggesting that it is due to mismatch in electrode impedance converting the common-mode MI into a differential-mode input into the IA. Hence, to handle such worst case, we ensure that our system can handle differential interferences with a combined amplitude of upto 100 $\mathrm{mV_{pp}}$.

III. Overall System

Fig. 1 shows the architecture of our proposed ECG readout system. To achieve a gain of 70 dB, the amplification chain is divided into two stages: i) the instrumentation amplifier (IA) with an overall gain of 46 dB, and ii) the signal-folding wide-effective-output-range amplifier (WEOR amp) with a gain of 24 dB. Between the two stages lies a lowpass filter for anti-aliasing. The system contains a 10-bit ADC—it will be shown in Section VI that much lower resolution can be used without significantly degrading the SNR—to digitize the WEOR amp's output. The WEOR amp also reports its state (WEOR_STATE) to allow the digital backend to reconstruct the actual signal from its folded output. In normal operations (without strong interference), the IA-WEOR-ADC chain suffices to amplify the ECG input without causing signal clipping at any point in the signal chain.

In cases of strong interferences, the system can enable the Interference Suppression Circuit (ISC) to generate the cancellation signal V_{null} to suppress MA and MI near the input of the system. The ISC takes as input the digitized output of the IA by bypassing the WEOR amp directly into the ADC to avoid having to reconstruct the folded signal. At the heart of the ISC is the nulling generator that generates all the components of V_{null}. The generator consists of three paths; the first path (MA), for suppressing MA, contains an integrator (INT_1) to establish a highpass corner at 2 Hz in the overall transfer function of the readout system; the other two paths (50 Hz/100 Hz) generate two sinusoidal signals to suppress the 1^{st} and 2^{nd} harmonics of MI. The two sinusoidal signals are generated with the direct-digital-synthesis (DDS) technique and least-mean-square (LMS) adaptive filtering as described in [7]. All the three components are then added and converted into V_{null} via a 10-bit digital-to-analog converter (DAC). To avoid distorting the ECG, V_{null} is also digitized and reported off-chip for reconstructing the original signal in the digital backend.

IV. The Instrumentation Amplifier

The IA is designed to achieve $> 1\ \mathrm{G\Omega}$ of input impedance at frequencies upto 150 Hz. Fig. 2 shows the schematic of the IA, which is divided into two stages, the first providing a gain of 26 dB and the second providing a gain of 20 dB. Each stage employs the capacitive-coupling technique to achieve high intrinsic input impedance at low frequencies and to block electrode offset. To suppress interferences, the 2^{nd}-stage IA, which operates as a summing amplifier, receives the cancellation signal $\mathrm{V_{null}}$ from the ISC. The 26-dB in-band gain of the 1^{st}-stage IA's allows for as large as 100 $\mathrm{mV_{pp}}$ interferences at the input without causing output clipping, which can then be suppressed with V_{null} of only 1.25 $\mathrm{V_{pp}}$, a comfortable output swing for the DAC in the ISC.

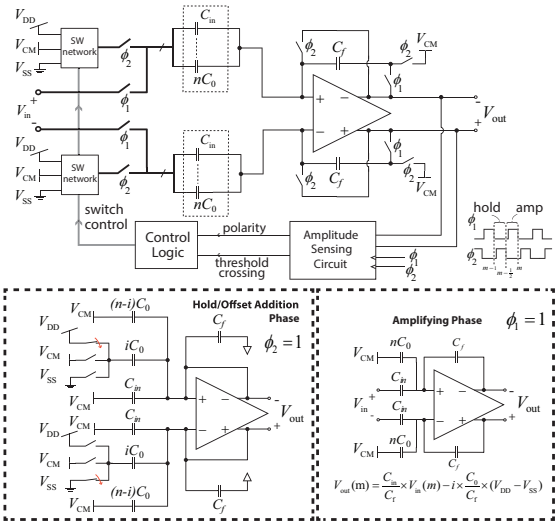


Fig. 3. Schematic of the WEOR amp

The 1^{st}-stage IA employs a relatively large input capacitance (C_{in}) of 20 pF to avoid degrading the overall input-referred noise due to parasitic capacitances at the opamp's input. To maximize the input impedance, we employ C_{pf}'s connected in a positive-feedback fashion between the output and the input of the 1^{st}-stage IA. With the 1^{st}-stage IA's gain of 26 dB, the optimum C_{pf} to maximize the input impedance is 1.05 pF. To account for errors in C_{in} due to parasitic capacitances of the electrode wiring and the ESD pads, we allow 5-bit tuning of C_{pf}'s with a unit capacitance of 32.8 fF—an achievable value in most IC processes—to achieve the targeted input impedance.

Note that the proposed IA does not employ chopping at the capacitive input network since the effective resistance due to chopping significantly lowers the input impedance. To minimize 1/f noise, the opamps in both stages (OA1,2) employ: 1) the complementary input differential pair to maximize the effective transconductance for a given bias current 2) the bulk switching technique [8] applied to both types of the differential pairs to minimize the generation of their 1/f noise. The overall IA consumes a total of 0.9 μA from a 1.2-V supply.

V. The Wide Effective Output Range Amplifier

The WEOR amp utilizes the signal-folding technique to keep its output within the ADC's input range. Fig. 3 shows the schematic of the WEOR amplifier. At its core is a switched-capacitor gain circuit with input capacitances C_{in}'s and feedback capacitances C_{f}'s to provide a gain of $C_{\text{in}}/C_{\text{f}}$. Each side of the capacitive input network also incorporates the "offset" capacitance—divided into n units, each with a capacitance of C_0—for adding appropriate offset to the output voltage V_{out} such that it always stays within the ADC's input range.

The operation of the circuit is divided into two phases—the hold (offset addition) phase and the amplifying phase—as explained by the bottom insets of Fig. 3. During the hold phase ($\phi_2 = 1$), a fraction of the offset capacitances, iC_0 ($0 \le i \le n$), are connected to either V_{DD} or V_{SS} to add offset charges into the offset capacitances, while the rest of the offset capacitances and the input capacitances C_{in} are connected to the common-mode voltage V_{CM}; the value of i and which supply to which each iC_0 must connect are determined by the amplitude sensing circuit and the control logic.

In the amplifying phase ($\phi_1 = 1$), C_{in}'s are connected to the input while all the offset capacitances are connected to V_{CM}, making the changes in the total charges of the input network appear across the feedback capacitances C_{f}'s. For the particular configuration shown, the output voltage is of the form

$$V_{\text{out}}(m) = \frac{C_{\text{in}}}{C_{\text{f}}} \cdot V_{\text{in}}(m) - i\frac{C_0}{C_{\text{f}}}\left(V_{\text{DD}} - V_{\text{SS}}\right).$$

In this case, a negative offset voltage is added to the actual output of the circuit, confining V_{out} to within the ADC's input range. If a positive offset voltage is required, the control logic will appropriately connect the iC_0 capacitances to the opposite supply rails in the hold phase.

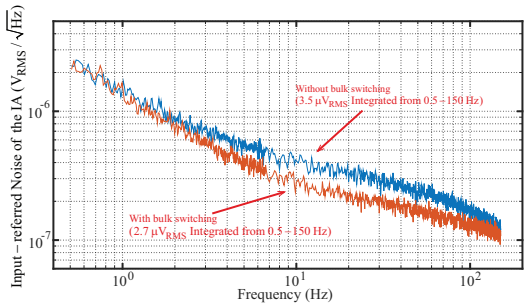
VI. Experimental Results

The proposed ECG readout system has been fabricated in a 0.18-μm CMOS technology and occupies an active area of 2770 $\times$ 1060 μm^2. With the ISC disabled, the system consumes a total current of 5.94 μA—0.9 μA IA, 1.44 μA lowpass filter, 2.2 μA WEOR amp, and 1.4 μA 10b ADC—or 7.13 μW from a 1.2-V supply. An additional 5.29 μA is added—3.75 μA ISC, and 1.54 μA DAC— resulting in a maximum power of 13.5 μW when the ISC is enabled.

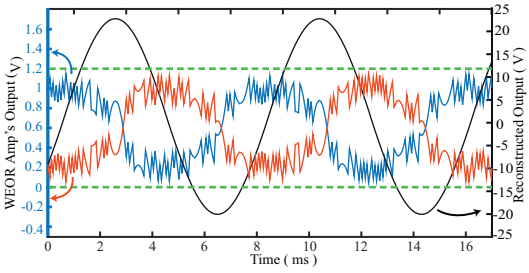
Fig. 4(a) shows the input-referred noise of the IA with and without bulk switching; the technique helps reduce the integrated noise from 3.5 μV_{rms} to 2.7 μV_{rms} (0.5-150 Hz), a significant reduction. Fig. 4(b) shows the output of the WEOR amp and the corresponding reconstructed waveform from the ADC's output data when applying a 128-Hz sinusoid into the WEOR amp's input. Notice that the WEOR amp's output never exceeds the supply rails, but the magnitude of the reconstructed waveform exceeds 40 V_{pp}.

Fig. 4(c) shows the integrated input-referred noise of the system as a function of the ADC's number of bits/sample calculated by taking the FFT of a 40-second ADC's output data stream; the reduction in the number of bits is achieved by discarding appropriate LSBs before taking the FFT. Note that the integrated input-referred noise of the system stays fairly constant at 2.9 μV_{rms} down to around 6 bits, thus suggesting that the system only requires around 6-7 bits of resolution in the ADC to meet the targeted input-referred noise.

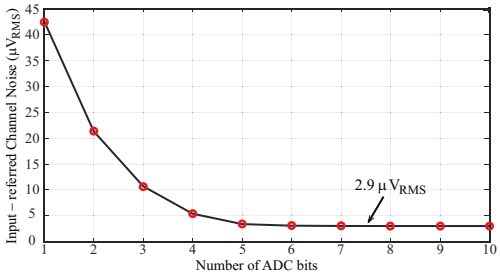
Fig. 5 shows the recorded ECG from the system using the in-house high-Z electrodes. The top plot shows an input-referred ECG (lead 1) recorded in a highly-shielded environment (ISC disabled). The bottom plot shows the input-referred reconstructed waveform when the user was touching a laptop plugged into an ungrounded outlet. Clearly, without the ISC, such 13.6 mV_{pp} MI would otherwise saturate the



(a)



(b)



(c)

Fig. 4. Benchtop results: (a) Input-referred noise of the IA with and without bulk switching (b) The raw and reconstructed waveforms of the WEOR amp's output (c) Input-referred noise of the system as a function of ADC's resolution.

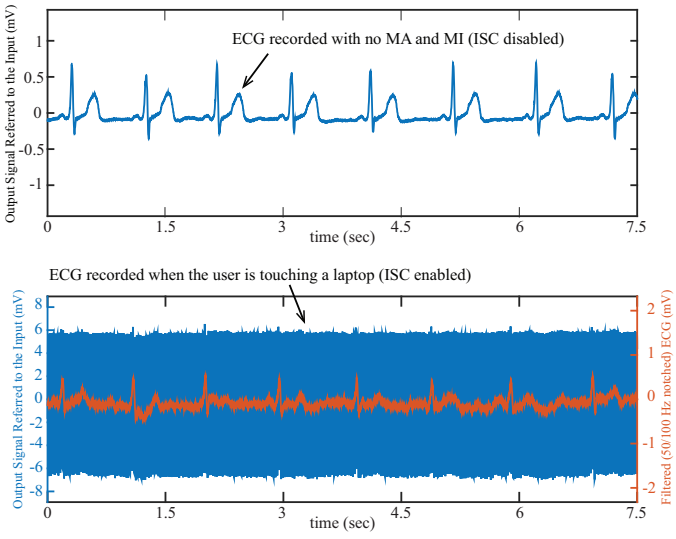


Fig. 5. ECG recordings from high-Z electrods.

TABLE I
PERFORMANCE SUMMARY AND COMPARISON TO PREVIOUS WORKS.

Ref.	Proposed	[1]	[2]	[3]	[4]
Tech. (μm)	0.18	0.18	n.a.	0.18	0.04
Supply (V)	1.2	1.2	1.1	1.3-1.8	0.6
Input Noise (μV_{rms})	2.9	0.605	0.82	4.9	7.8
Input offset rejec. (mV)	railt-to -rail	$\pm$ 400	$\pm$ 300	rail-to -rail	$\pm$ 150
Max. diff. input (mV_{pp})	100*	30	30	110	40
Diff. Z_{in} (GΩ)	$>$ 1	$>$ 0.5 @ 50 Hz	1.5	$>$ 0.4	0.05
Power/chan. (μW)	7.1/13.5	50	83.6	0.884	3.3
ADC Res. (bits)	6	13.5	18	7-10	2
Area (mm^2)	2.93	1.48	n.a.	8.6	0.015

* Tested with 30 mV_{pp} 1 Hz MA + 38 mV_{pp} 50-Hz MI+38 mV_{pp} 100-Hz MI.

IA's output. With the ISC enabled however, the ECG can be recovered after notching out the 50-Hz and 100-Hz MI from the reconstructed data in the digital backend. Although not as clean due to imperfect reconstruction, the recovered ECG still exhibits clear QRS peaks and thus can be used in peak detection applications. Table I summarizes the performances of the proposed system compared to the state-of-the-arts.

VII. Conclusion

This work proposes a low-power high-input-impedance ECG recording system for recording from high-Z electrodes. By employing the signal-folding technique and the interference suppression feedback, the system achieves a very high gain, which allows for the use of a low-resolution ADC without degrading the system's input-referred noise, thus resulting in low power consumption.

VIII. Acknowledgement

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A 2.64-μW 71-dB SNDR Discrete-Time Signal-Folding Amplifier for Reducing ADC's Resolution Requirement in Wearable ECG Acquisition Systems

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***Abstract*—This paper presents the design of a low-power discrete-time signal-folding amplifier intended for use in place of programmable-gain amplifiers (PGA) in electrocardiogram (ECG) acquisition systems. The amplifier provides a fixed high gain while preventing output signal saturation even with rail-to-rail inputs, thanks to the proposed discrete-time signal folding technique; the fixed gain eliminates the need of gain-control circuitry while the high gain helps relax the resolution requirement of the analog-to-digital converter (ADC) that follows, thus resulting in lower power consumption and design complexity for the ADC. Fabricated in a standard 0.18-μm CMOS process, the amplifier occupies an active area of 0.254 mm^2 and consumes 2.64 μW from a 1.2-V supply voltage. While amplifying a rail-to-rail input (2.4 V_{pp} differential) with a gain of 17.8 V/V, the amplifier achieves a signal-to-noise-plus-distortion ratio (SNDR) of 71 dB, thus making it very attractive for high-fidelity ECG recording amid large input interferences.**

***Index Terms*—ECG acquisition system, high signal-to-noise-plus-distortion ratio, mains interference, motion artifact, programmable-gain amplifier, signal-folding amplifier, switched-capacitor amplifier.**

I. Introduction

In RECENT years, cardiovascular diseases (CVDs) have become by far the leading cause of death among the world population, with the death rate more than twice that of all cancer types combined [1]. Moreover, with many countries being in the transition into aging/aged societies, the proportion of health ailments and deaths due to CVDs will inevitably increase in the near future, hence, putting severe pressure on institutions and personnel responsible for treating CVDs. It has been projected that the cost of treating CVDs will likely triple by the year 2030 [2].

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Electrocardiogram (ECG)—the heart's electrical signal measured from the body's surface—is considered one of the most important vital sign in the diagnosis and treatment of CVDs. Traditionally performed at fully-equipped health centers by bulky ECG stations, the measurement of ECGs are now being transformed toward the use of wearable, personalized devices intended for continuous monitoring with real-time networking and analysis capabilities—thanks to the advances in microelectronics, communication, and artificial intelligence. If fully developed and widely adopted by the mass, such devices can pave new ways for the remote monitoring and diagnosis of the heart, thus providing the general public access to state-of-the-art diagnostic tools without the need for frequent hospital visits. Such technology will not only save lives but will also reduce healthcare costs and alleviate the problem of personnel shortage in treating CVDs.

For such devices to become ubiquitous, they must be low-price, robust, and comfortable to wear. For the device to be low-price, its circuitry should be fully integrated to reduce the number of external components and the overall power consumption; the latter, in turn, helps reduce the battery's size, which is a crucial cost-determining factor in most electronics. However, low-power consumption requires that the device operate from a limited supply, thus putting a severe limit on the input range of the signal being recorded. For wearing comfort, the devices must be able to record from high-impedance electrodes—dry, noncontact [3], which we will collectively call high-Z electrodes—instead of from just the conventional gel electrodes, which may cause skin irritation after prolonged use. However, high-Z electrodes pose serious concerns on the quality of the recorded signal. First, high-Z electrodes are not as effective for use as grounding electrodes compared to the low-impedance gel electrodes, thus resulting in larger common-mode mains interference on the body. Second, as for recording, high-Z electrodes make the recording systems whose input impedances are not sufficiently high more prone to electrode mismatch, which can cause common-mode-to-differential-mode (CM-to-DM) conversion of the mains interference. Such CM-to-DM conversion may result in large differential mains interference at the device's input [4]–[6]. Finally, high-Z electrodes with impedances consisting of mostly the capacitive part are more

prone to motion artifacts (MA) [7], [8], which can severely increase the input dynamic range (DR) of the device. All these aggressors may lead to signal saturation if a high gain is used in the amplification chain, thus reducing the reliability and robustness of the ECG monitoring device.

To accommodate this increased input DR, most existing systems [9]–[14] utilize programmable-gain amplifiers (PGAs) in their signal chains to ensure the appropriate amplification of the input signal to suit the ADC's input range. With small input, as in the absence of interference, the PGA's gain can be maximized such that the high overall channel gain helps mitigate the ADC's noise contribution. Conversely, with large input, as in the presence of strong interferences, the PGA's gain can be minimized to prevent signal saturation in the amplification stage. In most commercial systems ([9], [10]), the total channel gains are quite low—1–12 V/V in [9] and 20–160 V/V in [10]—thus necessitating the use of high-resolution ADCs (24 and 18 bits in [9] and [10], respectively) at the cost of high per-channel power consumption (335 and 85 μW in [9] and [10], respectively). To reduce power consumption, other works [11]–[14] employ higher channel gains (up to 300 V/V in [12] and 1,300 V/V in [11]) to allow for lower resolutions of the ADCs.

Nevertheless, there are two drawbacks to the use of PGA in the readout system. First, for optimal performance, the PGA requires an additional automatic gain-control circuitry, thus increasing the overall system's complexity, power consumption, and silicon area; as the commercial systems in [9], [10] require external gain setting, external microcontrollers will need to be integrated at the printed-circuit-board (PCB) level to incorporate automatic gain control features into the final readout systems. Second, even with programmable gain, the ADC's resolution is often determined by the worst case (that of the lowest gain setting)—i.e., all the works in [11]–[14] use ADCs with resolutions from 11–14 bits to ensure that the noise contributions from the ADCs remain negligible even at the lowest gain settings. As a result, the ADC in each system often consumes higher power consumption and occupies a larger area than necessary.

To minimize the system's complexity and power consumption, it is advantageous to replace the PGA by a fixed high-gain amplifier as a 2$^{\text{nd}}$-stage amplifier. Fixed gain eliminates the need for automatic gain-control circuitry while high gain mitigates the noise/distortion requirement of the ADC, permitting the use of an ADC with low-to-moderate resolution without degrading the signal-to-noise ratio (SNR). The major challenge of employing a high overall gain in the amplification stage, especially in low-voltage low-power systems, is the risk of signal saturation at the output of the 2$^{\text{nd}}$-stage amplifier. Interestingly, there is a technique first introduced in [15] for ECG acquisition and, subsequently, in [16] for neural signal recording that utilizes a concept of signal folding to allow the use of high gain in the analog front-ends (AFEs) while avoiding output signal saturation. The signal-folding scheme employs feedback to monitor the output level and fold it back to the common-mode value whenever it is about to cross a threshold such that no output saturation occurs. The folded output sampled by an ADC can then be reconstructed in the digital backend to provide the original (effective) output signal. Such method allows the effective output swing to significantly exceed the supply voltage, thus permitting larger gain than normally possible in the conventional scheme.

Nevertheless, there are several drawbacks in applying the signal-folding scheme to the AFE, instead of in a later amplifier stage. First, most AFEs usually operate in a continuous-time fashion to prevent noise folding from the sampling operation. Hence, the signal folding scheme applied to such AFEs requires continuous-time detection of the appropriate folding instants, which is proved to be susceptible to various nonidealities—such as input noise, charge injections, and delays from the operational transconductance amplifiers (OTAs) or the comparators. As a result, sophisticated reconstruction algorithms are often required, which, unfortunately, lead to poor signal-to-noise-and-distortion ratio (SNDR) at large input amplitudes. For the amplifier in [15], even with only 1 $\mu\mathrm{V_{rms}}$ input noise, the SNDR of the reconstructed output signal from a 20-Hz sinusoidal input saturates to around 40 dB when the amplitude of the input is only around 2 mV. In [16], for a 30-Hz sinusoidal input signal, the SNDR of the output signal saturates to a value less than 30 dB even when the input amplitude is lower than 1 $\mathrm{mV_{pp}}$. The two mentioned performances are equivalent to attempting to resolve tiny ECG waveforms amid large differential interferences with ADCs whose effective-number-of-bits (ENOB) are only 6.35 and 4.7 bits, respectively. Hence, significant improvement is needed.

Another drawback in applying the signal-folding technique to the AFE is that if the folding mechanism is implemented at the input, the resulting circuit's nonidealities may degrade the SNDR, or even compromise the user's safety. For example, the design in [15] employs current-mode digital-to-analog converters (DACs) and resistors to implement programmable floating battery voltages in series with the input terminals of the AFE as a mean to introduce appropriate differential offset voltage to the input to keep the output within the threshold. Unfortunately, mismatches in the current DACs result in large input offset currents, reported to be as large as 58 nA, which can cause large DC offset voltage and high filtered shot noise especially when the AFE is interfaced with high-Z electrodes.

To avoid all these drawbacks, we propose in this work a discrete-time amplifier with a fixed high gain intended to follow a high-gain AFE to maximize the total gain of the amplification stage. The proposed amplifier employs a switched-capacitor gain topology [17] since its feedback nature provides excellent linearity even at large output amplitude. To prevent output saturation due to large input interference, we employ a discrete-time signal-folding scheme, which can be naturally integrated into the switched-capacitor gain circuit and is more immune to circuit nonidealities than its continuous-time variants presented in the existing works. Operating from a 1.2-V supply and consuming only 2.2 μA of bias current while driving a 5-pF capacitive load—assumed to be the capacitive load of the next-stage ADC—the proposed amplifier provides a gain of 17.8 V/V, a noise floor of 150 $\mu\mathrm{V_{rms}}$, and an SNDR of 71 dB when amplifying a rail-to-rail (2.4 $\mathrm{V_{pp}}$) 30-Hz sinusoidal input. The proposed amplifier is part of a high-gain ECG acquisition system proposed

in [18]. In this work, we provide thorough explanations, analysis, and present more detailed measured results to fully illustrate its performances.

The paper is organized as follows. Section II discusses the motivations behinds the use of a high-gain 2nd-stage amplifier to reduce the resolution requirement of the ADC. Section III explains the overall operation of the proposed amplifier and the designs of its building blocks. Section IV derives the amplifier's input-referred noise to pinpoint important parameters for noise optimization. Section V shows the measured performances of the amplifier and Section VI concludes the paper.

II. General Considerations

To be useful in clinical applications, the ECG monitoring device should at least be able to resolve the smallest feature of the ECG waveform—i.e., the P-wave whose amplitude rarely exceeds 0.25 $\mathrm{mV_{pp}}$ [19]. To be conservative, we will just assume that the amplitude of the P wave is on the order of 0.1 $\mathrm{mV_{pp}}$ and, to resolve this P wave, the device should be able to quantize it to at least 5 quantization levels, resulting in the width of each quantization level of around 20 $\mu\mathrm{V_{pp}}$. For the device to achieve such resolution, let us assume that its peak-to-peak input-referred noise-and-distortion (NAD) should be smaller than this quantization level. Consequently, assuming that such NAD follows the Gaussian distribution for simplicity, we can estimate the root-mean-square (rms) input-referred NAD of the acquisition system from $V_{\mathrm{ni,rms}} < 20\ \mu\mathrm{V_{pp}}/6 \approx 3.33\ \mu\mathrm{V_{rms}}$.

Given the specification of around 3 $\mu\mathrm{V_{rms}}$ input-referred NAD, how do we appropriately determine a suitable gain for the amplification stage and a suitable ADC's resolution? An ADC with the resolution too high wastes power and area, while an ADC with the resolution too low degrades the SNDR of the desired ECG. Let us consider a general ECG acquisition system in Fig. 1(a) consisting of an amplification stage with a total gain of A_{v} followed by an ADC. Let V_{FS} and ENOB be the ADC's full-scale voltage and the effective-number-of-bits, respectively. The ADC's NAD referred to the input of the acquisition system ($V_{\mathrm{ni,ADC,rms}}$) can be calculated from

$$V_{\mathrm{ni,ADC,rms}} = \frac{1}{A_{\mathrm{v}}} \cdot \frac{V_{\mathrm{FS}}}{2^{\mathrm{ENOB}}\sqrt{12}}. \tag{1}$$

Fig. 1(b) plots the required ENOB as a function of A_{v}—in the range of 120 V/V to 2400 V/V for $V_{\mathrm{FS}} = 2.4$ V (typical for a fully-differential ADC operating from a 1.2-V supply)—to make $V_{\mathrm{ni,ADC,rms}}$ equal to 3 $\mu\mathrm{V_{rms}}$. The chosen range of A_{v} is determined from two extremes. On one extreme, the input interference is very strong ($\approx 20\ \mathrm{mV_{pp}}$) such that A_{v} can be at most 120 V/V to keep the output of the amplification stage within the 2.4-V full-scale voltage of the ADC. On the other extreme, the input interference is not present such that A_{v} can be made as large as 2,400 V/V to amplify 1-$\mathrm{mV_{pp}}$ ECG to the full-scale voltage of the ADC. Notice that such range of A_{v} results in the range of ENOB from 10.9 bits ($A_{\mathrm{v}} = 120$ V/V) down to 6.6 bits ($A_{\mathrm{v}} = 2,400$ V/V). For successive-approximation-register (SAR) ADCs, preferable in this application due to its excellent energy efficiency, the power consumption and area of the capacitive digital-to-analog converter (DAC) increase as an exponential function of the ENOB. Therefore, the span of the required ADC's resolution by more than 4 bits gives a strong motivation to maximize the gain of the amplification stage such that the ADC's ENOB can be minimized to save power and area.

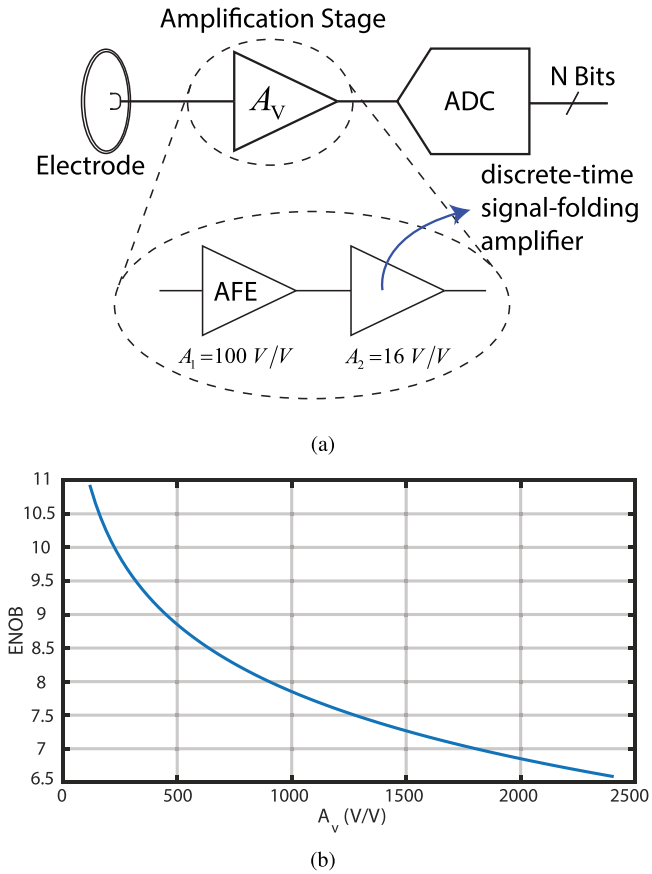

Fig. 1. (a) Consideration for the gain of the amplification stage and the required ADC's resolution. (b) The required ADC's ENOB as a function of A_{v} to keep the ADC's NAD referred to the acquisition system's input equal to 3 $\mu\mathrm{V_{rms}}$.

To maximize the gain of the amplification stage, we propose the use of a discrete-time signal-folding amplifier to follow a fixed-gain AFE, as shown in the inset of Fig. 1(a). The main objective of the proposed amplifier is to provide a very wide effective output swing, thus allowing for a very high gain in the amplification stage, while keeping the physical output swing within the input range of the ADC. Besides, the proposed amplifier should provide excellent linearity at large output amplitude to ensure that distortions due to large input interference do not degrade the SNDR of the desired ECG signal. Since the proposed amplifier is to follow an AFE, its noise and distortion requirement can be mitigated if the AFE's gain is sufficiently high. In this work, we will assume that the AFE exhibits a gain of 100 V/V and a maximum output swing of 2 $\mathrm{V_{pp}}$, which allows the maximum differential interference's amplitude at the input of the acquisition system to be as high as 20 $\mathrm{mV_{pp}}$ without saturating the AFE's output range. The gain of the proposed amplifier is chosen to be 16 V/V, resulting in the overall amplification stage's gain of 1600 V/V. According to Fig. 1(b),

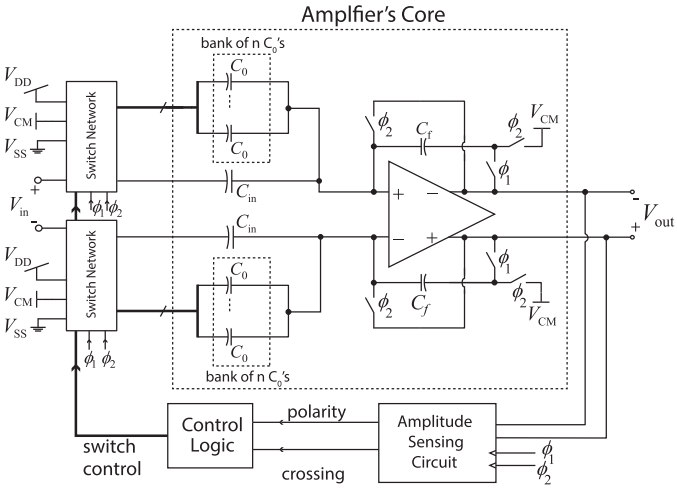

Fig. 2. High-level schematic of the proposed discrete-time signal-folding amplifier.

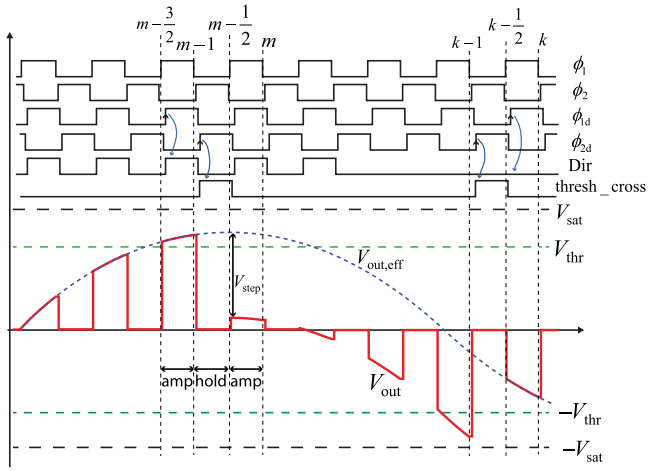

Fig. 3. A timing diagram showing the signal-folding operation of the proposed amplfier.

such total gain results in the required ADC's ENOB of less than 8 bits to keep the overall noise of the acquisition system within our specification. Many ADCs with 8-bit resolution have been demonstrated to achieve ultra-low-power operation and compact area [20]–[24], which can be readily applied to our application.

III. Circuit Operation

Fig. 2 shows the high-level schematic of the proposed discrete-time signal-folding amplifier whose core is the switched-capacitor gain circuit with the input capacitor banks—each consisting of an input capacitor $C_{\rm in}$ and an offset capacitor bank with n units of offset capacitor C_0—and the feedback capacitors $C_{\rm f}$'s. Around this core are the amplitude sensing circuit, the control logic, and the switch networks for performing the signal-folding operation. The amplifier's core functions as a switched-capacitor gain circuit [17], [25], with the input capacitance $C_{\rm in}$ and the feedback capacitance $C_{\rm f}$ setting the closed-loop gain of the circuit to $C_{\rm in}/C_{\rm f}$. To check if the amplifier's output is exceeding the valid range, the amplitude sensing circuit compares the value of the amplifier's output $V_{\rm out}$ to the predefined (upper/lower) thresholds. If $V_{\rm out}$ has exceeded either of the thresholds—i.e., lower than the lower threshold or higher than the upper threshold—the amplitude sensing circuit then instructs the control logic to appropriately configure the switch networks to add appropriate offset charges into the offset capacitor banks. These offset charges will then be added to charges in the input capacitors $C_{\rm in}$'s when the amplifier is amplifying the input $V_{\rm in}$ such that $V_{\rm out}$ becomes centered at zero, instead of further exceeding the valid output range. By tracking the state of the control logic and, hence, the added offset voltages, we can unwind (reconstruct) $V_{\rm out}$ to its original value in the digital backend, as will be described in Section V-A.

In addition to its excellent linearity and the convenience in introducing the input offset voltage, its sampling nature allows the proposed amplifier to function as a time-multiplexed amplifier, which can simultaneously amplify many input signals; this can be beneficial in multi-channel ECG recording in which the 2nd-stage amplifier takes inputs from many AFEs, or when the ECG acquisition system acquires other information such as the electrode impedance for use in motion artifact suppression [12]; in such cases, one amplifier can be shared to amplify many signals, thus saving area. Furthermore, in contrast to the design in [16] which requires high-resistance elements to set the DC bias point at the opamp's input terminals—which results in low-frequency drift due to the leakage current of the high-resistance elements—the proposed amplifier does not suffer from such drift as it does not use any high-resistance element.

A. Addition of Input Offset Voltage

Next, let us understand how the proposed amplifier amplifies the input while simultaneously constraining $V_{\rm out}$ to within a predefined output range to prevent output signal saturation. The operation of the amplifier can be divided into two phases—1) the amplifying phase and 2) the hold (offset addition) phase—which can be understood by an aid of the timing diagram in Fig. 3. The clocks ϕ_1 and ϕ_2 are two non-overlapping clocks, with ϕ_1 and ϕ_2 being high indicating the amplifying phase and the hold phase, respectively. The signal $V_{\rm out,eff}$ (dashed trace) represents the effective output signal of the amplifier if the input $V_{\rm in}$ was amplified by an ideal amplifier with a gain of $C_{\rm in}/C_{\rm f}$, while the signal $V_{\rm out}$ (red trace) represents the physical output of the proposed amplifier. Notice that the physical output is constrained to within $\pm V_{\rm thr}$ about zero by the signal-folding operation.

First, let us consider the time before the amplifying phase ending at $t = m - 1$ in Fig. 3 in which $V_{\rm out}$ resides comfortably within the upper and lower thresholds ($\pm V_{\rm thr}$) and, hence, the control logic (and the switch networks) does not add any offset charges to the offset capacitor banks to constrain $V_{\rm out}$, resulting in $V_{\rm out}$ just following $V_{\rm out,eff}$ as in regular switched-capacitor amplifiers. However, during the amplifying phase ending at $t = m - 1$ ($t \in [m - \frac{3}{2}, m - 1]$), the amplitude sensing circuit detects that $V_{\rm out}$ has already exceeded $+V_{\rm thr}$. Thus, in the next hold phase ($t \in [m - 1, m - \frac{1}{2}]$), the control logic instructs the switch networks to add appropriate offset charges into the offset

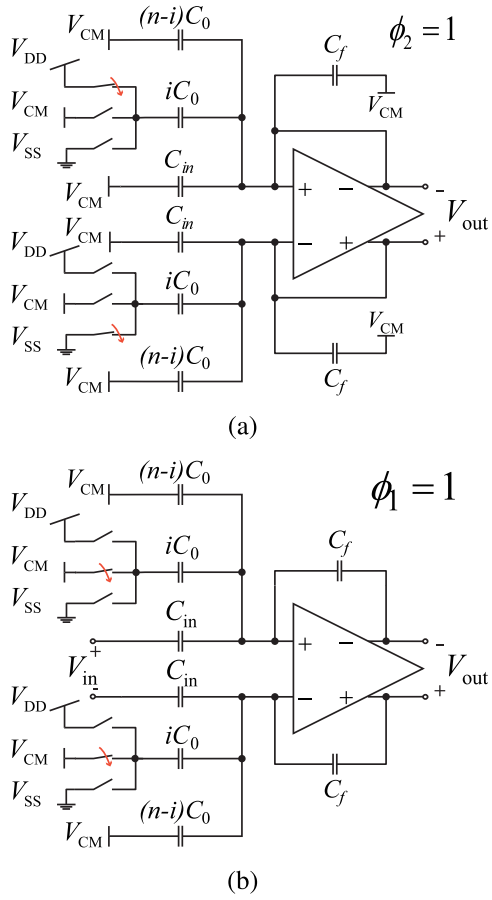

Fig. 4. Equivalent circuits for: (a) Hold phase. (b) Amplifying phase.

capacitor banks. Once the amplifier enters the next amplifying phase ($t \in [m - \frac{1}{2}, m]$), the offset charges will combine with the charges in the input capacitors $C_{\rm in}$'s such that $V_{\rm out}$ is pulled down from $V_{\rm out,eff}$ by an amount of $V_{\rm step}$. With the value of $V_{\rm step}$ close to that of $V_{\rm thr}$, $V_{\rm out}$ can be folded to a value very close to zero, thus making the voltages on the two sides of the opamp's output close to the common-mode voltage $V_{\rm CM}$ such that all the transistors in the opamp's output stage operate comfortably in saturation.

Fig. 4(a) illustrates a circuit scenario in the hold phase ($t \in [m-1, m-\frac{1}{2}]$) in which all the switches labeled ϕ_2 are closed such that the opamp is configured into the unity-feedback configuration; concurrently, the control logic connects the bottom plates of the input capacitors $C_{\rm in}$'s to the common-mode voltage $V_{\rm CM}$, connects i out of n offset capacitors C_0's of each offset capacitor bank, for a total capacitance of iC_0, to either $V_{\rm DD}$ or $V_{\rm SS}$, and connects the rest of the offset capacitance ($(n-i)C_0$) to $V_{\rm CM}$. Let $Q^+_{\rm tot}$ and $Q^-_{\rm tot}$ be the total charges in all the capacitors connected to the positive and negative input terminals of the opamp, respectively. With the common-mode feedback circuit pinning the voltage of each opamp's input to $V_{\rm CM}$, we can write $Q^+_{\rm tot}$ and $Q^-_{\rm tot}$ at the end of the hold phase ($t = m - \frac{1}{2}$) as $Q^+_{\rm tot}(m-\frac{1}{2}) = iC_{\rm o}(V_{\rm DD} - V_{\rm CM})$ and $Q^-_{\rm tot}(m-\frac{1}{2}) = iC_{\rm o}(V_{\rm SS} - V_{\rm CM})$.

In the next amplifying phase ($t \in [m - \frac{1}{2}, m]$), the switches labeled ϕ_1 in Fig. 2 are closed, configuring the circuit into a feedback amplifier; concurrently, the control logic instructs the switch networks to connect the bottom plates of $C_{\rm in}$'s to the input signal $V_{\rm in}$, and those of all the offset capacitors to $V_{\rm CM}$ as illustrated in Fig. 4(b). After charge redistribution, the total charges $Q^+_{\rm tot}$ and $Q^-_{\rm tot}$ at the end of the amplifying phase can be written as $Q^+_{\rm tot}(m) = C_{\rm in}(V^+_{\rm in} - V_{\rm CM}) + C_{\rm f}(V^-_{\rm out} - V_{\rm CM})$ and $Q^-_{\rm in}(m) = C_{\rm in}(V^-_{\rm in}(m) - V_{\rm CM}) + C_{\rm f}(V^+_{\rm out}(m) - V_{\rm CM})$. Since $Q^+_{\rm tot}$ and $Q^-_{\rm tot}$ must be conserved from the end of the hold phase to the end of the amplifying phase, we can solve for $V_{\rm out} = V^+_{\rm out} - V^-_{\rm out}$ in terms of $V_{\rm in} = V^+_{\rm in} - V^-_{\rm in}$ as

$$V_{\rm out}(m) = \frac{C_{\rm in}}{C_{\rm f}} V_{\rm in}(m) - i\frac{C_{\rm o}}{C_{\rm f}}\left(V_{\rm DD} - V_{\rm SS}\right). \qquad (2)$$

The term $(C_{\rm in}/C_{\rm f})V_{\rm in}(m)$ in (2) represents the sample of the effective output, i.e., $V_{\rm out,eff}(m)$. However, if the amplitude of $V_{\rm in}$ in the amplifying phase becomes so large that $|V_{\rm out}|$ has exceeded $V_{\rm thr}$, the intentional offset term $i\frac{C_{\rm o}}{C_{\rm f}}(V_{\rm DD} - V_{\rm SS}) = iV_{\rm step}$ is introduced such that at the end of the amplifying phase $|V_{\rm out}(m)| < V_{\rm thr}$. The value of i is determined and, if necessary, updated by ± 1 at the end of every amplifying phase to decrease or increase $V_{\rm out}$ by one $V_{\rm step}$. In Fig. 3, the period $t \in [k-1, k]$ illustrates a scenario when i is decremented by one in the hold phase to introduce a positive offset of $V_{\rm step}$ into $V_{\rm out}$ in the next amplifying phase.

The value of i can be either positive or negative and can range from $-n$ to $+n$, with $n = 31$ in this design, such that the maximum offset of $\pm nV_{\rm step}$ can be introduced to the amplifier's output. A positive i corresponds to the switch configuration of the input capacitor banks shown in Fig. 1(a), while a negative i corresponds to switching the iC_o capacitance in each offset capacitor bank to the opposite supply rail—i.e., the top iC_o becomes connected to $V_{\rm SS}$ and the bottom iC_o becomes connected to $V_{\rm DD}$ instead. In this design, we use $C_{\rm in} = 2$ pF, $C_{\rm f} = 125$ fF to achieve the nominal gain of 16 V/V. The value of $C_{\rm o}$ is chosen to be 75 fF, which results in $V_{\rm step}$ of 720 mV. Referred to the input of the amplifier, such $V_{\rm step}$ corresponds to an input step change of 45 mV. With $n = 31$, the proposed amplifier can accommodate an input range of ± 1.395 V, which conveniently covers the maximum output range of an AFE operating from a 1.2-V supply assumed to drive the proposed amplifier.

B. Amplitude Sensing Circuit

To determine whether and in which direction $V_{\rm out}$ has already exceeded the thresholds, we employ the amplitude sensing circuit shown in Fig. 5(a). The circuit provides two flag indicators, "Dir," and "thresh_cross"; the flag Dir indicates the polarity of $V_{\rm out}$, while thresh_cross indicates whether $|V_{\rm out}|$ is already larger than $V_{\rm thr}$. By knowing the polarity of $V_{\rm out}$ and whether its magnitude has exceeded the threshold, the control logic can adapt its internal state to provide appropriate configurations for the switch networks.

The amplitude sensing circuit can be divided into two parts: i) the rectifier and ii) the threshold crossing checker. The rectifier consists of the clocked comparator CMP1 and the multiplexer to

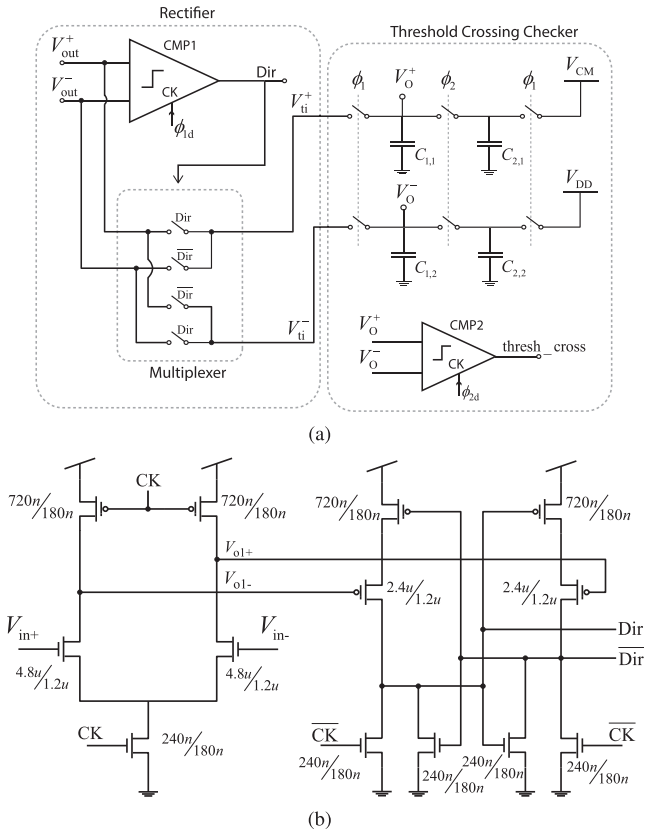

Fig. 5. (a) The amplitude sensing circuit. (b) The schematic of comparators used in the amplitude sensing circuit.

determine the polarity and the magnitude of $V_{\rm out}$, respectively. The threshold crossing checker consists of a charge redistribution network and the comparator CMP2 to determine whether $|V_{\rm out}|$ is higher than $V_{\rm thr}$. Due to the discrete-time nature of the amplitude sensing operation, we implement CMP1 and CMP2 using a dynamic comparator topology [26] shown in Fig. 5(b), which consumes almost no static power and makes fast decision on the rising edge of its clock signal (CK); with a load capacitance of 50 fF, transient simulations show that the comparator achieves a 90% settling time of around 2.4 ns after CK goes high. The comparators CMP1 and CMP2 operate on the rising edges of $\phi_{1\rm d}$ and $\phi_{2\rm d}$, the delayed versions of the nonoverlapping clocks ϕ_1 and ϕ_2 in Fig. 3, respectively. Shortly after the amplifier enters the amplifying phase—i.e., on the rising edge of $\phi_{1\rm d}$—the comparator CMP1 flags the signal Dir if $V_{\rm out}=V_{\rm out}^+-V_{\rm out}^->0$, which then controls the multiplexer such that its output $V_{\rm ti}=V_{\rm ti}^+-V_{\rm ti}^-$ is equal to $|V_{\rm out}^+-V_{\rm out}^-|$: Dir $=1$, indicating that $V_{\rm out}>0$, results in $V_{\rm ti}=V_{\rm out}^+-V_{\rm out}^-$; conversely, Dir $=0$, indicating that $V_{\rm out}<0$, results in $V_{\rm ti}=V_{\rm out}^--V_{\rm out}^+$. From Fig. 3, on the rising edge of $\phi_{1\rm d}$ shortly after $t=m-\frac{3}{2}$, the comparator CMP1 senses that $V_{\rm out}>0$ and thus flags Dir $=1$. Conversely, on the rising edge of $\phi_{1\rm d}$ shortly after $t=k-\frac{1}{2}$, CMP1 senses that $V_{\rm out}<0$ and thus set Dir $=0$.

The magnitude signal $V_{\rm ti}$ is then passed on to the threshold crossing checker to determine if $|V_{\rm out}|$ exceeds $V_{\rm thr}$. In the amplifying phase when all the switches labeled ϕ_1 are closed, the capacitors $C_{1,1}$ and $C_{1,2}$ are charged to $V_{\rm ti}^+$ and $V_{\rm ti}-$, respectively, while the capacitors $C_{2,1}$ and $C_{2,2}$ are charged to $V_{\rm CM}$ and $V_{\rm DD}$, respectively. The charges on these capacitors are then equal to $C_{1,1}V_{\rm ti}^+$, $C_{1,2}V_{\rm ti}^-$, $C_{2,1}V_{\rm CM}$, and $C_{2,2}V_{\rm DD}$. Once the amplifier enters the hold phase ($\phi_2=1$), the switches labeled ϕ_2 are closed, connecting the top plate of $C_{1,1}$ to that of $C_{2,1}$ and the top plate of $C_{1,2}$ to that of $C_{2,2}$, allowing charges in each pair of the connected capacitors to redistribute. After charge redistribution, the voltage on the top plates of each connected-capacitor pair can be written as $V_{\rm o}^+=(C_{1,1}V_{\rm ti}^++C_{2,1}V_{\rm CM})/(C_{1,1}+C_{2,1})$ and $V_{\rm o}^-=(C_{1,2}V_{\rm ti}^-+C_{2,2}V_{\rm DD})/(C_{1,2}+C_{2,2})$. Shortly after the amplifier enters the hold phase (on the rising edge of $\phi_{2\rm d}$), the comparator CMP2 determines if $V_{\rm o}^+-V_{\rm o}^->0$ by asserting the flag thresh_cross—e.g., on the rising edge of $\phi_{2\rm d}$ shortly after $t=m-1$, CMP2 senses that $V_{\rm o}^+-V_{\rm o}^->0$ and thus set thresh_cross to 1. With $C_{1,1}=C_{1,2}=C_1$ and $C_{2,1}=C_{2,2}=C_2$, $V_{\rm o}^+-V_{\rm o}^-$ can be written as

$$V_{\rm o}^+-V_{\rm o}^-=\frac{C_1}{C_1+C_2}\left(V_{\rm ti}^+-V_{\rm ti}^-\right)-\frac{C_2}{C_1+C_2}\left(V_{\rm DD}-V_{\rm CM}\right). \tag{3}$$

Since $V_{\rm ti}^+-V_{\rm ti}^-=|V_{\rm out}|$, thresh_cross is asserted when

$$|V_{\rm out}|>\frac{C_2}{C_1}\left(V_{\rm DD}-V_{\rm CM}\right)=V_{\rm thr}. \tag{4}$$

In this work, we set $C_1=C_2=2.5$ pF and $V_{\rm CM}=V_{\rm DD}/2$ such that $V_{\rm thr}=V_{\rm DD}/2$.

C. Control Logic

The control logic determines the state of the proposed amplifier to devise suitable configurations for the switch networks. With a full differential input swing of 2.4 $\rm V_{pp}$, the amplifier's nominal gain of 16 V/V results in a full differential output swing of 38.4 $\rm V_{pp}$. Hence, for the output correction step, $V_{\rm step}$, of 720 mV, we need a total of $(38.4\ \rm V_{pp})/(720\ mV)\approx 54$ steps to cover the entire output swing, thus requiring 6 bits to encode all the states. Therefore, in this design, we employ a total of 63 states, one for no offset correction, and 31 for each of the positive and negative offset corrections.

Fig. 6 depicts the state evolution of the amplifier. The states can be divided into three categories—S_0, $S_{\rm p,i}$, and $S_{\rm m,i}$, $i\in\{1,\ldots,31\}$—according to the polarities of the correction to be introduced to $V_{\rm out}$: the state S_0, indicating that $V_{\rm out,eff}$ still remains within $\pm V_{\rm thr}$, introduces no correction to $V_{\rm out}$; the state $S_{\rm p,i}$, indicating that $V_{\rm out,eff}$ is higher than $V_{\rm thr}$, introduces $-iV_{\rm step}$ to keep $V_{\rm out}$ within $\pm V_{\rm thr}$; the state $S_{\rm m,i}$, indicating that $V_{\rm out,eff}$ is lower than $-V_{\rm thr}$, introduces $iV_{\rm step}$ to keep $V_{\rm out}$ within $\pm V_{\rm thr}$.

Upon reset, the amplifier enters the state S_0 in which all of the offset capacitors are connected to $V_{\rm CM}$ such that no correction voltage is to be introduced to $V_{\rm out}$ in the next amplifying phase. To move from one state to the next requires two input signals, UP and DN. The signal UP, derived from UP = (Dir = 1) & (thresh_cross=1) and indicating that $V_{\rm out}$ has exceeded $+V_{\rm thr}$, instructs the state to move "up"—to change from S_0 to $S_{\rm p,1}$ (or

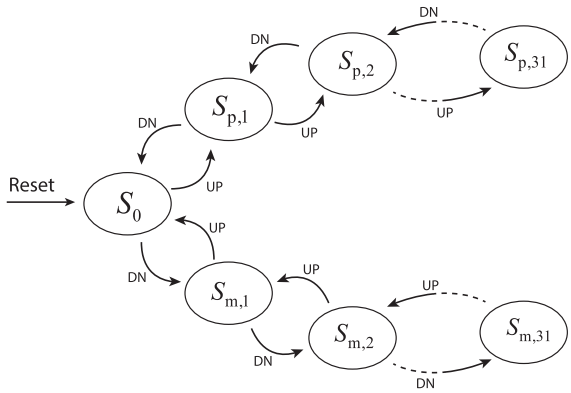

Fig. 6. Diagram showing the state evolution of the proposed amplifier.

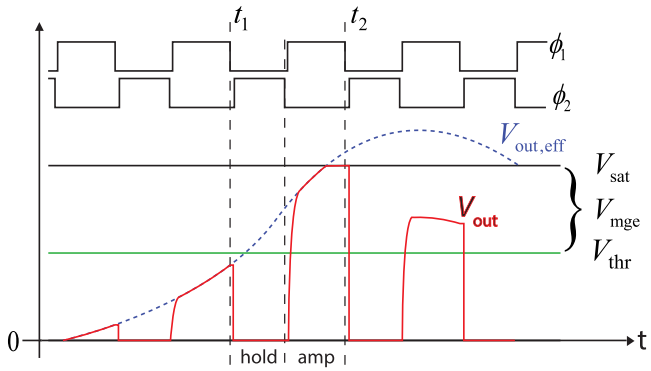

Fig. 7. A graph showing the saturation of $V_{\rm out}$ due to fast input.

from $S_{\rm p,i}$ to $S_{\rm p,i+1}$)—to subtract one additional $V_{\rm step}$ from $V_{\rm out}$ in the next amplifying phase. Conversely, the DN signal, derived from DN = (Dir = 0) & thresh_cross = 1 and indicating that $V_{\rm out}$ drops below $-V_{\rm thr}$, instructs the state to move "down"—to change from S_0 to $S_{\rm m,1}$ (or from $S_{\rm m,i}$ to $S_{\rm m,i+1}$)—to add one additional $V_{\rm step}$ to $V_{\rm out}$ in the next amplifying phase.

D. Maximum Amplitude vs. Frequency of the Input Signal

Since the amplitude sensing circuit monitors the threshold crossing in a discrete-time manner, it is possible for the amplifier's output to saturate, especially when the input changes very rapidly. Illustrated in Fig. 7 is an example of such a scenario for a positive output. At t_1, the amplitude sensing circuit determines that $V_{\rm out}$ is still below $V_{\rm thr}$; hence it does not flag the control logic to introduce a correction voltage for the next amplifying phase. Unfortunately, the input $V_{\rm in}$ changes so rapidly during t_1 and t_2 such that $V_{\rm out,eff}$ exceeds the saturation level $V_{\rm sat}$ of the amplifier's output stage. As a result, $V_{\rm out}$ could no longer track $V_{\rm out,eff}$ in the next amplifying phase and becomes clipped before the next threshold crossing check at t_2. If the ADC samples the amplifier's output right before t_2, information of $V_{\rm out,eff}$ will be lost, leading to increased distortion of the reconstructed output signal.

To avoid such scenario, we must ensure that the period between two consecutive threshold crossing checks, $T_{\rm clk} = t_2 - t_1$, must be short enough for $V_{\rm out,eff}$ not to traverse the entire margin of error, $V_{\rm mge} = V_{\rm sat} - V_{\rm thr}$. In other words, we have to enforce the condition:

$$\max\left(\Delta V_{\rm out,eff}\right) \approx \max\left(\left|\frac{dV_{\rm out,eff}}{dt}\right|\right) \cdot T_{\rm clk} < V_{\rm mge}. \quad (5)$$

Assuming a sinusoidal input into the amplifier of the form $V_{\rm in}(t) = V_{\rm p}\sin(2\pi f_{\rm in}t)$ and the amplifier's gain of $A_{\rm c} = C_{\rm in}/C_{\rm f}$, we have $\max(|\, dV_{\rm out,eff}\,/\,dt\,|) = A_{\rm c}V_{\rm p}2\pi f_{\rm in}$. Substituting this value into (5) and solving for the input amplitude, $V_{\rm p}$, we obtain

$$V_{\rm p} < \frac{V_{\rm mge}f_{\rm clk}}{2\pi A_{\rm c}} \cdot \frac{1}{f_{\rm in}}, \quad (6)$$

where $f_{\rm clk} = 1/T_{\rm clk}$ is the frequency of the clock signals ϕ_1 and ϕ_2.

The relationship in (6) suggests that the maximum input amplitude to guarantee no output clipping is inversely proportional to the frequency of the input signal $f_{\rm in}$, with the proportionality constant a function of $V_{\rm mge}$, $f_{\rm clk}$, and $A_{\rm c}$. Thus, to maximize $V_{\rm p}$ for given values of $f_{\rm in}$, $f_{\rm clk}$, and $A_{\rm c}$, we have to maximize $V_{\rm mge}$. This can be achieved by using an opamp whose open-loop gain remains high even when its output swings close to the supply rails such that the closed-loop gain of the amplifier remains relatively constant regardless of the output level. In this design with $V_{\rm mge} \approx 0.6$ V ($\approx V_{\rm DD} - V_{\rm thr}$) and the nominal $A_{\rm c}$ of 16 V/V, we use $f_{\rm clk} = 16$ kHz to allow the maximum input amplitude into the proposed amplifier of as large as 1.6 $\rm V_{pp}$ for the 60-Hz differential-mode mains interference without saturating the amplifier's output. This input amplitude is equivalent to 16 $\rm mV_{pp}$ when referred to the input of the ECG acquisition system if an AFE with a gain of 40 dB precedes the proposed amplifier. This level of tolerance to differential-mode mains interference should be adequate for most well designed ECG acquisition systems with proper grounding and low-to-moderate electrode impedance (< 10 MΩ). For motion artifact, whose frequency contents are normally well below 5 Hz, (6) indicates that a motion artifact of larger than 18 $V_{\rm pp}$ at the amplifier's input is required to saturate the output. Hence, the chosen $f_{\rm clk}$ of 16 kHz allows the amplifier to handle motion artifacts of any size provided that the output of the AFE preceding the proposed amplifier does not saturate.

It is worth mentioning that, in deriving (6), we assume a zero offset voltage for the comparator CMP2 in the amplitude sensing circuit (Fig. 5(a)). Even though the offset voltage of CMP2 does not affect the accuracy of the proposed amplifier—as the amount of the offset voltage introduced into $V_{\rm out}$ is independent of the characteristics of CMP2—it can affect the value of the margin of error $V_{\rm mge}$, and thus altering the achievable value of $V_{\rm p}$. Supposedly, if CMP2 has an offset voltage of $V_{\rm off}$ which reduces the margin of error to $V_{\rm mge} - V_{\rm off}$, the maximum achievable $V_{\rm p}$ then becomes a factor of $(1 - V_{\rm off}/V_{\rm mge})$ of its nominal value. For $V_{\rm off} = 50$ mV and $V_{\rm mge} = 0.6$ V, the reduction in $V_{\rm p}$ then amounts to a decrease in the SNDR of around 0.75 dB, which is negligible for our application. Besides, since the proposed amplifier employs a switched-capacitor input network, it presents an effective load resistance to the preceding AFE. Nevertheless,

the chosen frequency of $f_{\rm clk} = 16$ kHz and the input capacitance of $C_{\rm in} = 2$ pF results in the load resistance of around 31 MΩ on each side of the AFE's output. This level of load resistance is deemed high enough to not degrade the open-loop gain of the preceding AFE with μA-level bias current.

E. Notes on the Similarities to Other ADC/Frontend Architectures

At this point, some keen readers may have noticed that the proposed signal-folding scheme to prevent output saturation may look similar to the operation of a multiplying digital-to-analog converter (MDAC) in algorithmic or pipelined ADCs [25]. Besides, the use of capacitive feedback to subtract from the input a voltage proportional to the output may look similar to some of the $\Delta\Sigma$-based AFEs [27], [28]. The MDAC checks the input or, in later iterations, the output of the multiply-by-2 ($\times 2$) circuit and compares it to a reference voltage to perform appropriate level shifting such that the output of the $\times 2$ circuit stays within the rails in the next iteration. This process is performed iteratively until the least-significant-bit (LSB) is determined. What differentiates our proposed amplifier from the MDAC is that it uses a high-gain switched-capacitor amplifier to amplify the input signal only once, while having a signal-folding scheme to prevent the output from exceeding the rails. Compared to the MDAC, our proposed amplifier is more prone to output saturation when present with a large high-frequency interferences.

Nevertheless, there are certain advantages to our approach which makes it more amenable to low-power ECG acquisition systems compared to the MDAC. First, in the ECG acquisition system, the interferences (from MA and the mains) may be large but often slowly-varying. Since our signal-folding feedback only needs to correct for these large-but-low-frequency interferences, there is little risk of signal saturation, provided that the output of the preceding AFE does not saturate (see Section V-D). Second, since our high-gain amplifier amplifies the signal only once, there is no iterative addition of noise into the signal. For the MDAC, the use of low-gain amplification in each iteration results in the iterative addition of the $\times 2$ circuit's noise into the signal, resulting in an increased input-referred noise of the ADC to around twice the noise floor (in power units) of the $\times 2$ circuit. As a result, to achieve the same noise floor in a given bandwidth, our proposed amplifier can be designed with less stringent noise requirement, thus leading to power saving.

In the $\Delta\Sigma$-based AFEs, to prevent output saturation due to the large input offset voltage, the scheme in [27], [28] employs an integrator in the feedback path such that the output of the system represents the differentiation of the input, thus free of the input offset voltage. The output can then be reconstructed by integration. In our view, this $\Delta\Sigma$ approach relies on the conventional feedback concept by forcing the feedback signal to mimic the input as closely as possible to minimize error. To achieve this, $\Delta\Sigma$ amplifiers rely on oversampling—usually with an oversampling ratio (OSR) of 1,000—and noise shaping to overcome the ADC's quantization noise. Such high oversampling ratio can lead to high power consumption in the $\Delta\Sigma$ amplifiers and the clock generation circuitry. On the contrary, the signal-folding scheme in our proposed amplifier only tries to subtract a crude estimate from the input to keep the output within the rails, with the crude estimate normally determined by the large but slowly-varying interferences into the amplifier. As long as the input signal of interest is small, and the overall output is kept within the rails by the signal-folding scheme, the signal of interest can be amplified with a switched-capacitor amplifier without the need of a very high OSR. Thus, compared to the $\Delta\Sigma$ approach, our proposed amplifier only needs to operate at a much lower frequency, making it more amenable for low-power implementation.

TABLE I
TRANSISTORS' SIZES AND THE DC-OPERATING-POINT PARAMETERS OF THE OPAMP IN FIG. 8

Transistors	Aspect Ratio (μm/μm)	$g_{\rm m}$ (μA/V)	$r_{\rm o}$ (MΩ)
M_1, M_2	32/1	14.5	5.8
M_3, M_4	32/1	11.5	22.3
M_5, M_6	32/1	11.4	11.1
M_7, M_8	32/1	10.9	13.6
M_9, M_{10}	8/4	10.4	18
M_{11}, M_{12}	16/1	5.3	102.8
M_{13}, M_{14}	4/4	5.1	34.8
$M_{\rm b1}$, $M_{\rm b2}$	8/12	8.83	24.23
$M_{\rm b3}$, $M_{\rm b4}$	4/1	1.14	274

F. Opamp Design

We have seen from Section III that, during the hold phase, the opamp is connected in the unity-feedback configuration, resulting in the opamp's differential output being reset to zero; hence, it requires that the opamp be unity-gain stable. Besides, the proposed amplifier must also drive a sizable load capacitance—i.e., the input capacitance of the next-stage ADC. Thus, it must exhibit a sufficient slew rate for its output to reach the final value within half of $T_{\rm clk}$ once the amplifier re-enters the amplifying phase (31.25 μs in this design). Also, to maximize the input amplitude by maximizing $V_{\rm mge}$ as discussed in Section III-D, the opamp must exhibit a high open-loop gain even at large output swing. Besides being unity-gain stable, fast, and exhibiting high open-loop gain, the opamp must also consume low power to minimize the overall power consumption of the ECG acquisition system.

To meet all these requirements, we employ a fully-differential two-stage opamp shown in Fig. 8 with all the devices' sizes listed in Table I, along with their transconductances and output resistances from the DC operating point simulation. The transistors M_1-M_6 form the first gain stage while M_7-M_{14} form a class-AB output stage to provide a high driving strength while minimizing the overall quiescent current of the opamp. Since the opamp operates in a switched-capacitor fashion, we employ switched-capacitor common-mode feedback [29] circuits to generate $V_{\rm cmfb1}$ and $V_{\rm cmfb2}$ to set the common-mode outputs of the first and the second stages, respectively, without consuming static bias current. With the expected load capacitance of $C_{\rm L} \approx 5$ pF and $f_{\rm clk}$ of 16 kHz, we allocate in each branch the bias current labeled in Fig. 8 for the amplifier to function properly with

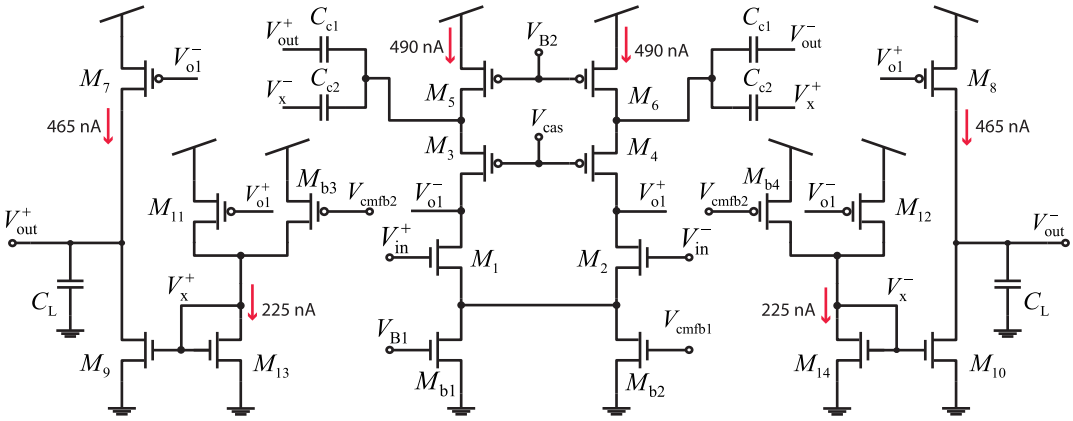

Fig. 8. Schematic of the opamp used in the proposed amplifier.

the expected ranges of input's frequency and amplitude. Due to the low bias current of the first stage, the pole formed by the source resistance of $M_{3,4}$ and the compensation capacitors situates at low frequency, thus requiring the use of a nested Miller compensation to achieve the settling time requirement. To avoid the use of zero-nulling resistors which may increase the chip area, we make the Miller compensation indirect by feeding capacitive feedback currents through the compensation capacitors $C_{c1} = 3$ pF and $C_{c2} = 1$ pF to the source nodes of M_3 and M_4. Through this design, with $C_L = 5$ pF, simulations show that the opamp achieves the low-frequency open-loop gain of 87 dB, the unity-gain frequency of 600 kHz, the phase margin of 46°, and the 0.1% settling time of 13 μs when the amplifier's output changes by 700 mV.

IV. Noise Analysis

The sampling nature of the proposed amplifier inevitably causes an increase of in-band noise due to aliasing. In this section, we consider the important determining factors of the amplifier's noise performance to pinpoint the control knobs for keeping the noise within our specification.

A. Noise From the Sampling Switches

All the sampling switches, when closed, exhibit finite resistances and hence thermal noise. Such thermal noise affects the amount of charge to be sampled onto the capacitor connected to each switch. To simplify our calculation, let us assume that the opamp is ideal with infinite gain and bandwidth. Such assumption leads to the upper bound for the calculation of the input-referred noise due to the sampling switches: the ideal opamp results in the true virtual ground condition at the opamp's inputs and, consequently, the maximum amount of noise sampled onto each capacitor.

Figure 9(a) and 9(b) show the half-circuit models for analyzing the amplifier's noise in the hold and the amplifying phases, respectively. The resistances $R_{\mathrm{sw,in}}$, $R_{\mathrm{sw,o}}$, and $R_{\mathrm{sw,f}}$ are the ON resistances of the switches connected to C_{in}, each of C_{o}, and C_{f}, respectively, while the thermal noise voltages associated

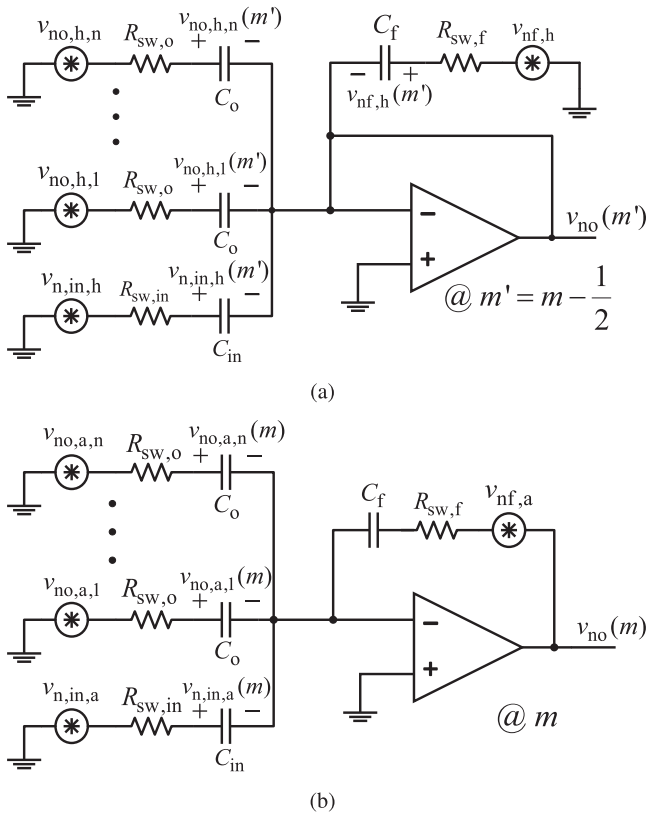

Fig. 9. Equivalent circuits for calculating the proposed amplifier's noise due to the sampling switches in: (a) hold phase (b) amplifying phase.

with these switches are denoted as the noise generators $v_{\mathrm{n,in,h}}$, $v_{\mathrm{no,h,i}}$ ($i \in \{1, \ldots, n\}$), and $v_{\mathrm{nf,h}}$. In the amplifying phase, each capacitor is connected to a different switch, whose noise is uncorrelated to that of the switch in the hold phase. Therefore, we denote the noise in the amplifying phase with a subscript "a" instead of "h"—e.g., the noise associated with the switch's resistance $R_{\mathrm{sw,in}}$ that is sampled onto C_{in} in the amplifying phase is denoted as $v_{\mathrm{n,in,a}}(m)$, and so on.

To find the total input-referred noise due to all the switches, we first write the total charges in all the capacitors at the end of the hold phase and the end of the amplifying phase:

$$Q_{\rm tot}\left(m-\frac{1}{2}\right)=C_{\rm in}v_{\rm n,in,h}\left(m-\frac{1}{2}\right)+\sum_{\rm i=1}^{n}C_{\rm o}v_{\rm no,h,i}\left(m-\frac{1}{2}\right)+C_{\rm f}v_{\rm nf,h}\left(m-\frac{1}{2}\right) \quad (7)$$

and

$$Q_{\rm tot}(m)=C_{\rm in}v_{\rm n,in,a}(m)+\sum_{\rm i=1}^{n}C_{\rm o}v_{\rm no,a,i}(m)+C_{\rm f}\left(v_{\rm no}(m)+v_{\rm nf,a}(m)\right). \quad (8)$$

From charge conservation, we can equate (7) to (8) and solve for $v_{\rm no}(m)$. We then use the fact that noises from different switches associated with the same capacitor are uncorrelated but exhibit the same spectrum, and that we have to double the noise power as we have two sets of these switches in our differential implementation. We can then express the output noise spectrum of the amplifier due to all the sampling switches as

$$\overline{V_{\rm no}^2}(f)=4\left(\frac{C_{\rm in}}{C_{\rm f}}\right)^2\overline{V_{\rm n,in,a}^2}(f)+4n\left(\frac{C_{\rm o}}{C_{\rm f}}\right)^2\overline{V_{\rm no,a,1}^2}(f)+4\overline{V_{\rm nf,a}^2}(f), \quad (9)$$

where we have assumed that $\overline{V_{\rm no,a,1}^2}(f)=\overline{V_{\rm no,a,i}^2}(f)$ for all i.

Note that each term of the noise spectrum on the right-hand-side of (9) represents the power spectral density (PSD) of a sampled switch's noise. Since an ON switch carries no DC current, thus exhibiting no 1/f noise, we only need to consider its thermal-noise contribution. For a particular switch with an ON resistance R connected to a capacitance C, the continuous-time spectrum of the switch's noise sampled onto C is a two-sided spectrum with a height of $2kTR$ and a noise bandwidth of $1/4RC$. This noise voltage across the capacitor is then sampled by the ADC's sampling rate, $f_{\rm s}$—$f_{\rm s}$ is normally several times lower than $f_{\rm clk}$ used in the switched-capacitor operation of the amplifier. Since $f_{\rm s}$ is normally much lower than the noise bandwidth, $1/4RC$, aliasing results in noise folding, which elevates the spectrum of the sampled noise to $kT/(f_{\rm s}C)$ [30]; this sampled noise's spectrum is periodic in the frequency domain with a periodicity of $f_{\rm s}$ such that we can regard its bandwidth to be $\pm f_{\rm s}/2$. Therefore, we can substitute $\overline{V_{\rm n,in,a}^2}(f)=kT/(C_{\rm in}f_{\rm s})$, $\overline{V_{\rm no,a,1}^2}(f)=kT/(C_{\rm o}f_{\rm s})$, $\overline{V_{\rm nf,a}^2}(f)=kT/(C_{\rm f}f_{\rm s})$, and divide the result by the square of the amplifier's gain, $(C_{\rm in}/C_{\rm f})^2$, to obtain the input-referred noise spectrum due to all the sampling switches as

$$\overline{V_{\rm ni,samp}^2}(f)=\frac{4kT}{C_{\rm in}}\left(1+\frac{nC_{\rm o}+C_{\rm f}}{C_{\rm in}}\right)\frac{1}{f_{\rm s}}. \quad (10)$$

B. Noise Due to the Opamp

Next, let us consider the noise contribution from the opamp itself. Fig. 10(a) and Fig 10(b) show the equivalent circuits for computing the noise of the opamp in the hold and the amplifying phases, respectively, in which $v_{\rm nA}$ represents the input-referred noise of the opamp. To simplify our analysis, let us assume that all the switches' ON resistances are zero, which represents the worst-case scenario for the opamp's noise contribution. Such assumption results in the sampled noise onto all the capacitors to be bandlimited by the opamp's transfer function and not by the wider bandwidth of the RC networks formed by the sampling switches and capacitors. Also, let us assume a first-order opamp's transfer function of the form $A(s)=\omega_{\rm c}/s$, where $\omega_{\rm c}$ is the unity-gain bandwidth of the opamp.

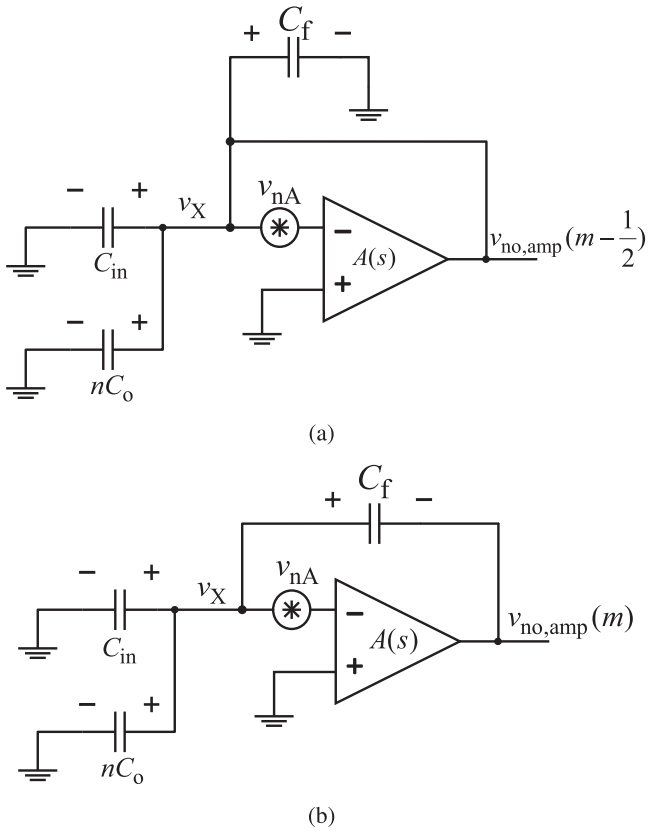

Fig. 10. Equivalent circuits for calculating the input-referred noise of the proposed amplifier due to the opamp: (a) hold phase (b) amplifying phase.

During the hold phase shown in Fig. 10(a)), $v_{\rm nA}$ is filtered by the opamp connected in the unity-gain configuration to produce the voltage $v_{\rm x}$ on the top plates of all the capacitors, producing, at the end of the hold phase ($t=m-1/2$), the total charge on all the capacitors of

$$Q_{\rm tot}\left(m-\frac{1}{2}\right)=(C_{\rm in}+nC_{\rm o}+C_{\rm f})v_{\rm x}\left(m-\frac{1}{2}\right). \quad (11)$$

In the amplifying phase, $C_{\rm f}$ is connected as feedback around the opamp as shown in Fig. 10(b). We can then write the total charge in all the capacitors at the end of the amplifying phase ($t=m$) as

$$Q_{\rm tot}(m)=(C_{\rm in}+nC_{\rm o})v_{\rm x}(m)+C_{\rm f}(v_{\rm x}(m)-v_{\rm no,amp}(m)). \quad (12)$$

Equating (12) to (11), we can solve for $v_{\mathrm{no,amp}}$ as

$$v_{\mathrm{no,amp}}(m) = \left(1 + \frac{C_{\mathrm{in}} + nC_{\mathrm{o}}}{C_{\mathrm{f}}}\right)\left(v_{\mathrm{x}}(m) - v_{\mathrm{x}}\left(m - \frac{1}{2}\right)\right). \tag{13}$$

Then, taking the z-transform of (13) with $z = e^{j2\pi f/f_{\mathrm{s}}}$ and computing the noise spectrum, we obtain

$$\overline{V^2_{\mathrm{no,amp}}}(f) = 4\left(1 + \frac{C_{\mathrm{in}} + nC_{\mathrm{o}}}{C_{\mathrm{f}}}\right)^2 \sin^2\left(\pi\frac{f}{2f_{\mathrm{s}}}\right)\overline{V^2_{\mathrm{x}}}(f). \tag{14}$$

Note that $\overline{V^2_{\mathrm{x}}}(f)$ in (14) is the discrete-time spectrum of the sampled noise voltage v_{x}. To compute $\overline{V^2_{\mathrm{x}}}(f)$, we first recognize that the continuous-time transfer functions from v_{nA} to v_{x} in the hold and the amplifying phases are given by $(V_{\mathrm{x}}/V_{\mathrm{nA}})_{\mathrm{hold}}(s) = -1/(1 + s/\omega_{\mathrm{c}})$ and $(V_{\mathrm{x}}/V_{\mathrm{nA}})_{\mathrm{amp}}(s) = -1/(1 + s/\omega'_{\mathrm{c}})$, respectively, where ω_{c} is the unity-gain frequency of the opamp and $\omega'_{\mathrm{c}} = \omega_{\mathrm{c}}C_{\mathrm{f}}/(C_{\mathrm{in}} + C_{\mathrm{f}} + nC_{\mathrm{o}})$. Since the amplifying phase experiences a smaller filtering bandwidth than the hold phase's, we can again simplify our analysis by assuming the worst-case scenario: that both phases experience a wider bandwidth of ω_{c}. Hence, we can write the continuous-time spectrum, $\overline{V^2_{\mathrm{x,c}}}(f)$, of the noise voltage at V_{x} as

$$\overline{V^2_{\mathrm{x,c}}}(f) = \overline{V^2_{\mathrm{nA}}}(f) \cdot \frac{1}{1 + f^2/f_{\mathrm{c}}^2}, \tag{15}$$

where $f_{\mathrm{c}} = \omega_{\mathrm{c}}/2\pi$.

To account for both the thermal and 1/f noise components of $\overline{V^2_{\mathrm{nA}}}$, let $\overline{V^2_{\mathrm{n,th}}}$ represent its thermal noise component and f_{fn} its $1/f$ noise corner such that we can represent the opamp's input-referred noise as $\overline{V^2_{\mathrm{nA}}}(f) = \overline{V^2_{\mathrm{n,th}}}(1 + f_{\mathrm{fn}}/f)$, thus allowing us to rewrite (15) as

$$\overline{V^2_{\mathrm{x,c}}}(f) = \overline{V^2_{\mathrm{n,th}}}\left(1 + \frac{f_{\mathrm{fn}}}{f}\right)\frac{1}{1 + f^2/f_{\mathrm{c}}^2}. \tag{16}$$

Recognizing that $\overline{V^2_{\mathrm{x}}}(f)$ is the aliased version of $\overline{V^2_{\mathrm{x,c}}}(f)$, which is given by $\overline{V^2_{\mathrm{x}}}(f) = \Sigma_{k=0}^{\infty}\overline{V^2_{\mathrm{x,c}}}(f - kf_{\mathrm{s}})$, we can then write $\overline{V^2_{\mathrm{x}}}(f)$ using (16) as

$$\overline{V^2_{\mathrm{x}}}(f) = \overline{V^2_{\mathrm{n,th}}}\sum_{k=0}^{\infty}\left(\left(1 + \frac{f_{\mathrm{fn}}}{|f - kf_{\mathrm{s}}|}\right)\cdot\frac{1}{1 + \frac{(f-kf_{\mathrm{s}})^2}{f_{\mathrm{c}}^2}}\right). \tag{17}$$

Finally, substituting (17) into (14) and dividing the result by the square of the amplifier's gain, we obtain the input-referred noise component of the amplifier due to the opamp's noise as

$$\overline{V^2_{\mathrm{ni,amp}}}(f) = 4\overline{V^2_{\mathrm{n,th}}}\left(1 + \frac{C_{\mathrm{f}} + nC_{\mathrm{o}}}{C_{\mathrm{in}}}\right)^2 \sin^2\left(\pi\frac{f}{2f_{\mathrm{s}}}\right) \cdot\sum_{k=0}^{\infty}\left(\left(1 + \frac{f_{\mathrm{fn}}}{|f - kf_{\mathrm{s}}|}\right)\cdot\frac{1}{1 + \frac{(f-kf_{\mathrm{s}})^2}{f_{\mathrm{c}}^2}}\right). \tag{18}$$

As will be seen in Section V-B, the noise due to the opamp in (18) is the dominant noise source of the proposed amplifier. We can also notice from (18) that, besides the thermal noise $\overline{V^2_{\mathrm{n,th}}}$, the 1/f noise corner, f_{fn}, of the opamp plays an important role in determining the overall input-referred noise of the amplifier, even though the noise at low frequency is attenuated by the highpass transfer function $\sin^2(\pi f/2f_{\mathrm{s}})$. In this design, we size the transistors such that the settling time in the amplifying phase is well below 31.25 μs while ensuring a low enough 1/f noise corner to yield the amplifier's input-referred noise of around 150 $\mu\mathrm{V_{rms}}$. If a lower input-referred noise for the amplifier is desired, given the achieved settling time of only 13 μs in the amplifying phase as discussed in Section III-F, we could trade the settling time with the opamp's 1/f noise—i.e., by increasing the transistors' sizes of the opamp.

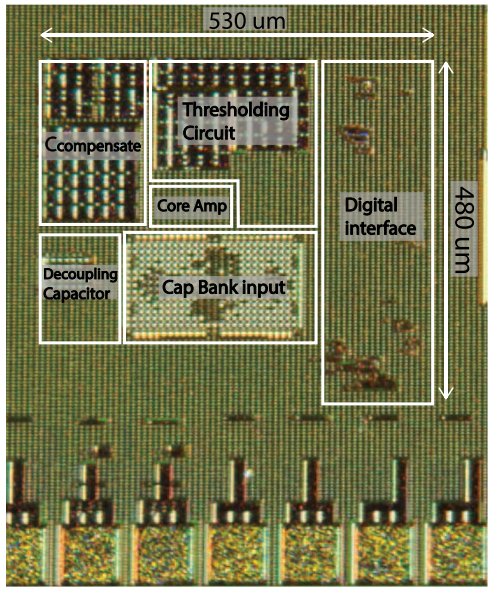

Fig. 11. Chip micrograph of the proposed amplifier.

V. Experimental Results

The proposed amplifier with the micrograph shown in Fig 11, was fabricated in a 0.18-μm CMOS process from United Microelectronics Corp. The amplifier occupies the total area of 0.254 mm^2 (530 $\mu\mathrm{m} \times 480\ \mu\mathrm{m}$), with 14.65% of the total area attributed to the input capacitor banks and 12% to the opamp's compensation capacitors. Operating from a 1.2 V supply, the amplifier consumes 2.64 μW of total power when amplifying a rail-to-rail (2.4 $\mathrm{V_{pp}}$) 32-Hz sinusoidal input to drive a capacitive load of 5 pF. The overall gain of the amplifier is measured to be 17.8 V/V, instead of the nominal value of 16 V/V. Such gain error is attributed to inaccuracy in the layout modeling as the error is observed across many chips.

A. Reconstruction

Due to the folding operation, the physical output of the amplifier (V_{out}) must be reconstructed to recover the effective output ($V_{\mathrm{out,eff}}$). Since the state kept by the control logic contains information on the correction voltage introduced into $V_{\mathrm{out,eff}}$ to create V_{out}, we can use such information to easily reconstruct $V_{\mathrm{out,eff}}$ from V_{out}. For example, if a particular sample of V_{out} corresponds to the state $S_{\mathrm{p,i}}$, $i \in \{1, \ldots, 31\}$, indicating that

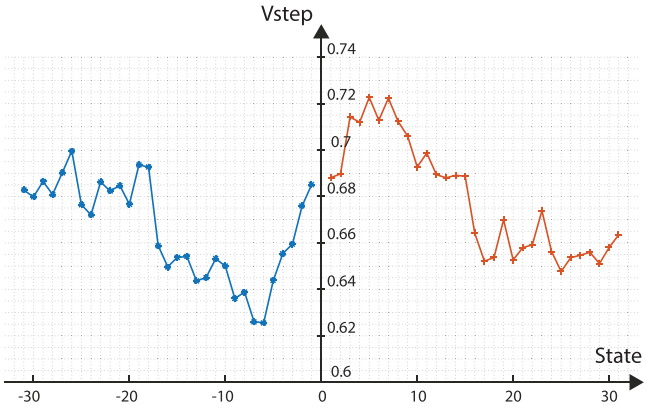

Fig. 12. Distribution of V_{step} as a function of the amplifier's state.

the sampled V_{out} has been effectively created by substracting $i \cdot V_{\text{step}}$ from $V_{\text{out,eff}}$, we can reconstruct $V_{\text{out,eff}}$ using

$$V_{\text{out,eff}} = V_{\text{out}} + i \cdot V_{\text{step}}(S), \tag{19}$$

where S is the amplifier's state corresponding to the sampled V_{out}. Note that we write V_{step} in (19) as a function of the state S because, due to process variations affecting the sizes of the unit capacitors, V_{step} is not constant but a function of the amplifier's state. To minimize distortion in the reconstructed $V_{\text{out,eff}}$, we recommend that initially V_{step}'s be determined for all the states S and stored in a memory in the digital backend such that they can be readily employed in the reconstruction process. Determining all the V_{step}'s can be easily achieved by feeding a slow ramp into the input of the amplifier—such that all the amplifier's states are utilized—while recording V_{out}. In this work, we fed a 1-Hz 2.4-V_{pp} ramp (sawtooth) signal into the input of the amplifier to cover its entire input range while recording V_{out}. We then plotted V_{out} in MATLAB and noted the discontinuities resulted from the signal folding operation as the amplifier transitioned from one state to the next. Each discontinuity was then taken as V_{step} of the state into which the amplifier just transitioned.

Fig. 12 shows the resulting V_{step} as a function of the amplifier's state. Marked on the x-axis, states $+i$ and $-i$ correspond to the states $S_{\text{p,i}}$ and $S_{\text{m,i}}$, respectively. The distribution of V_{step} shows a spread of around 100 mV, possibly due to process variations affecting the values of the unit capacitors C_{o}'s and the feedback capacitors C_{f}'s. Achieving a narrower spread in V_{step} can be achieved by increasing the unit sizes of C_{o}'s and C_{f}'s but at the expense of a larger area. Nevertheless, as long as the amplifier is calibrated once to obtain the values of V_{step} for all the states, V_{out} can be later reconstructed with high linearity. It is also worth noting that the reconstruction process recommended here aims to achieve maximum linearity despite the inherent nonlinearities in the circuit. If we opt for an easier reconstruction process, we may as well use just one value of V_{step} instead of a dedicated value for each of the amplifier's state, at the expense of lower linearity.

To test the effectiveness of the mentioned reconstruction process, we time-multiplexed two sinusoidal inputs into the amplifier, one with the frequency of 30 Hz and the amplitude of 2.4 V_{pp}, and the other with the frequency of 40 Hz and the

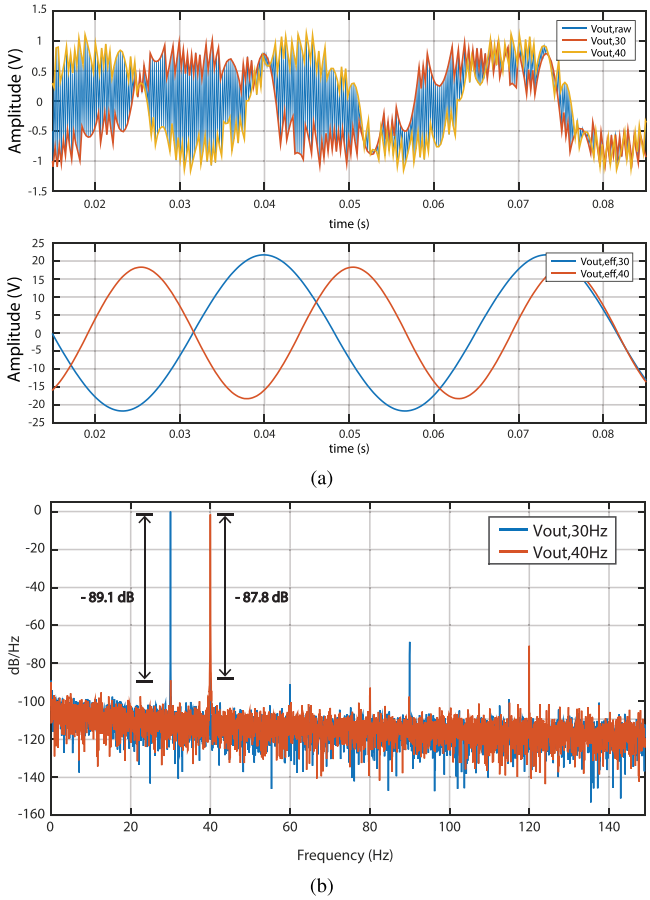

Fig. 13. (a) Raw output of the amplifier in response to 30-Hz and 40-Hz sinusoidal inputs. (b) Spectrum of the reconstructed 30-Hz and 40-Hz outputs showing the crosstalks of −87.8 dB from the 30-Hz into the 40-Hz signals and −89.1 dB from the 40-Hz into the 30-Hz signals.

amplitude of 2 V_{pp}. In the top panel of Fig. 13(a), the trace $V_{\text{out,raw}}$ represents the raw output of the proposed amplifier, while the traces $V_{\text{out,30}}$ and $V_{\text{out,40}}$ represent the digitized physical outputs of the amplifier corresponding to the 30-Hz and 40-Hz input signals, respectively, each sampled by an on-chip ADC with a 9-bit ENOB (in the bandwidth from DC to 150 Hz) at a rate of 4.096 kS/s. The bottom panel of Fig. 13(a) shows the effective outputs—$V_{\text{out,eff,30}}$ and $V_{\text{out,eff,40}}$—corresponding to the two input signals after reconstruction. The amplitudes of the 30-Hz and 40-Hz output signals are 42.6 and 35.5 V_{pp}, respectively, indicating an overall gain of 17.75 V/V (24.98 dB). From visual inspection, we notice negligible crosstalk between the two output signals. Fig. 13(b) shows the PSD of $V_{\text{out,eff,30}}$ and $V_{\text{out,eff,40}}$ with the fundamentals normalized to 0 dB. Note that the crosstalk from the 30-Hz to 40-Hz signals and from the 40-Hz to 30-Hz signals are −87.8 and −89.1 dB, respectively, thus suggesting that the proposed amplifier is suitable for amplifying two input signals with negligible crosstalk to permit area saving in multi-channel applications.

B. Linearity and Noise

The principal aim of the proposed amplifier is to allow accurate recording of ECG for a wide range of interference's

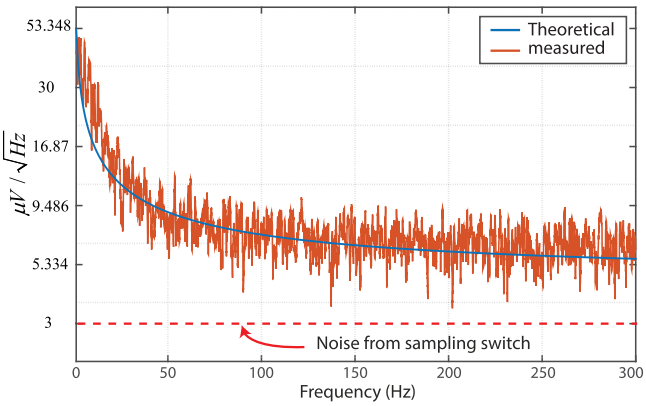

Fig. 14. Measured input-referred noise PSD of the proposed amplifier compared to the theoretical prediction. The total integrated input-referred noise is 143.6 μV_{rms}.

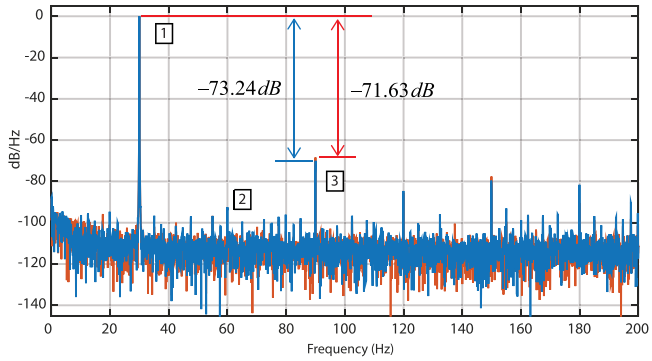

Fig. 15. Spectrums of the reconstructed output in response to a 30-Hz rail-to-rail input signal from the two reconstruction methods: (i) V_{step}-distribution method (blue trace) and (ii) fixed V_{step} method (red trace).

amplitude, without the need for an automatic gain control scheme. With small interference, the amplifier's intrinsic noise may degrade the SNR unless the gain of the preceding AFE is sufficiently large. With large interference, the amplifier's nonlinearity may introduce unwanted spectral contents into the desired ECG, thus limiting the system's ability for discerning tiny ECG from the interference. In this section, we explore the proposed amplifier's noise and nonlinearity to understand its limitation in preserving the SNDR of the desired signal.

1) Noise: To measure the intrinsic noise of the proposed amplifier, we grounded its input and sampled its output at 4.096 kS/s with the same on-chip ADC as in Section V-A. We then computed the power spectral density of these output samples and normalized the result by the overall gain of the amplifier to get the input-referred noise. Fig. 14 shows the resulting input-referred noise spectrum of the amplifier (red trace) in the frequency range from DC to 300 Hz along with the theoretical fit (blue trace) obtained from the sum of the switches' and opamp's noises in (10) and (18), respectively. For the opamp's noise, we use $\sqrt{\overline{V_{n,th}^2}}$=52.21 nV/$\sqrt{\text{Hz}}$, $f_{fn} = 80$ kHz, $f_c = 46$ kHz, and $f_s = 4.096$ kHz. The input-referred thermal noise $\overline{V_{n,th}^2}$ is obtained from the theoretical calculation—$\overline{i_n^2} = 4kT\gamma g_m$, where $\overline{i_n^2}$ is the power spectral density of the thermal noise current of a particular transistor, k the Boltzman's constant, T the absolute temperature, and g_m the small-signal transconductance of the transistor—with g_m's from Table I and $\gamma = 2/3$ as typical for long-channel devices; the crossover frequency f_c is obtained from AC simulation, while the 1/f noise corner f_{fn} is empirically adjusted for the theoretical plot to fit the measured result. A good fit between theory and the measured result indicates that our analysis in Section IV explains the noise behavior of the proposed amplifier with reasonable accuracy. Integrating the measured noise spectrum from DC to 150 Hz gives the total input-referred noise of 143.6 μV_{rms}.

Note that due to its fully-differential nature, the proposed amplifier is immune to noise on the V_{CM} line into the switch networks (see Fig. 2). However, it can be seen from (2) that the offset voltage added to $V_{in}(m)$ to properly fold the input signal directly depends on the value of V_{DD} (with respect to V_{SS})—with a gain of iC_o/C_f. Referred to the input of the proposed amplifier, the noise on this V_{DD} line experiences a gain of iC_o/C_{in}. To avoid degrading the input-referred noise and the power-supply-rejection-ratio (PSRR), we thus recommend that the V_{DD} line into the switch networks of Fig. 2 be separated from the main V_{DD} of the amplifier and properly lowpass filtered. Nevertheless, since the proposed amplifier is intended for use as a second-stage amplifier, the noise requirement of the quiet V_{DD} line is alleviated by the gain of the AFE. For the 150-μV_{rms} specification of the proposed amplifier, it follows that, in the worst case of offset voltage addition ($i = n = 31$), the total integrated noise on the quiet V_{DD} line should be less than 40 μV_{rms} for this noise to account for less than 10% of the overall noise power. Provided that the overall recording system is battery-powered such that the main V_{DD} contains negligible mains interference, the quiet V_{DD} line with such relaxed noise requirement can be easily achieved through filtering the main V_{DD} by an off-chip filtering network.

2) Linearity: To assess its linearity, we fed a rail-to-rail (2.4-V_{pp}) 30-Hz sinusoidal signal into the input of the amplifier and sampled its output with the same on-chip ADC as discussed in Section V-A. Due to the large input amplitude, the sampled output signal must first be reconstructed, as explained in Section V-A. To achieve maximum linearity, we can use the reconstruction method with one specific value of V_{step} for each of the amplifier's state discussed in Section V-A. However, one may choose to minimize the complexity of the reconstruction circuit in the digital backend by using just one value of V_{step} for the whole reconstruction process. This value of V_{step} may be chosen to be the median of the V_{step} distribution obtained during calibration—e.g., the median of the distribution in Fig. 12. Fig. 15 compares the spectrums of the amplifier's output, with the fundamentals normalized to 0 dB, as reconstructed from the two methods: i) using V_{step} distribution in Fig. 12 (blue trace) and ii) using $V_{step} = 0.674$ V (red trace). Within the 150-Hz bandwidth, the amplifier's nonlinearity is dominated by the 3rd harmonic, which is 73.2 dB and 71.6 dB below the fundamental for the V_{step}-distribution method and the fixed V_{step} method, respectively. Calculation of the SNDRs within this bandwidth yields 71 dB and 70.13 dB for the V_{step}-distribution method

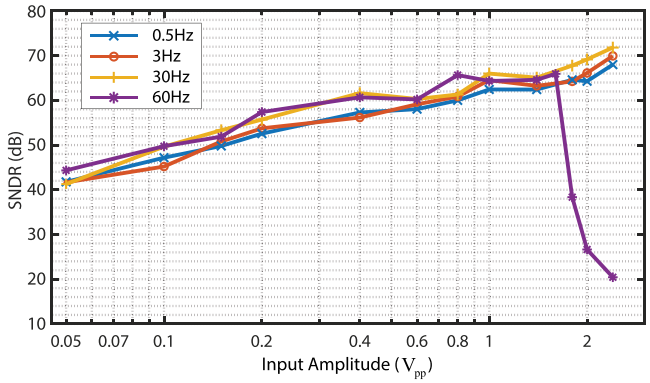

Fig. 16. SNDR vs. input amplitude at various frequencies of the input.

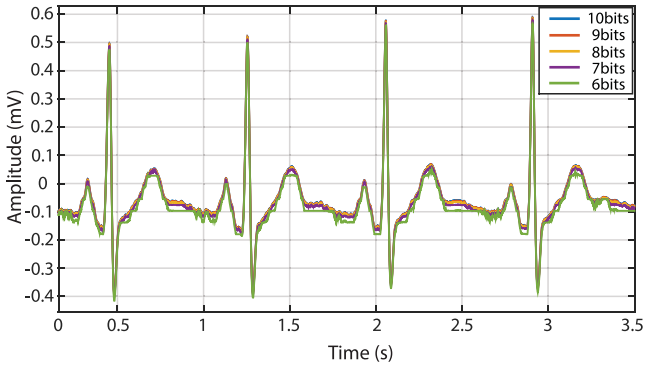

Fig. 17. Plot of the ECG waveforms as digitized by an ADC at various resolutions.

and the fixed $V_{\rm step}$ method, respectively, implying that the 3rd harmonic is indeed the dominant source of the amplifier's nonlinearity. For the proposed $V_{\rm step}$-distribution method, the SNDR of 71 dB amounts to an input-referred noise-plus-distortion of 213 $\mu{\rm V_{rms}}$. Removing the 3rd harmonic results in the SNR of 75 dB, which amounts to an integrated input-referred noise of 150 $\mu{\rm V_{rms}}$; this value agrees reasonably well with the measured input-referred noise of 143.6 $\mu{\rm V_{rms}}$ discussed earlier.

Since the frequency of the large interference stressing the proposed amplifier may vary—the interference can be either a low-frequency MA or a 60-Hz mains interference—it is instructive to assess the amplifier's nonlinearity at various input frequencies and amplitudes. Fig. 16 shows the SNDRs of the proposed amplifier as a function of the input amplitude for the input frequencies of 0.5, 3, 30, and 60 Hz. At low input frequencies (0.5, 3, and 30 Hz), the SNDR is approximately a linear function of the logarithm of the input amplitude for the entire amplifier's input range, reaching around 68–71 dB at the maximum input amplitude (2.4 ${\rm V_{pp}}$). Unlike [15] and [16] in which the SNDRs at high input amplitudes saturate at much lower values due to errors from the reconstruction processes, our proposed amplifier suffers no such reconstruction error, and thus achieves high SNDRs even at a very high input amplitude. Such SNDR performance indicates that the proposed amplifier is highly-tolerant to large low-frequency interferences such as the electrode offset or MA. For the 60-Hz interference, the SNDR drops appreciably once the input amplitude exceeds 1.6 ${\rm V_{pp}}$ due to saturation of the physical output as discussed in III-D. Hence, with a 40-dB gain AFE preceding the amplifier, the maximum tolerable amplitude for the 60-Hz mains interference into the input of the acquisition system amounts to around 16 ${\rm mV_{pp}}$. Keeping the differential mains interference below such level can be achieved through careful control of the common-mode interference [5], a proper grounding scheme [31], and the use of an AFE with high-enough common-mode input impedances to reduce the effect of the electrode-impedance mismatch.

From these measured results, we can thus see that the use of a reasonably high-gain AFE ($>$ 40dB) can help keep the amplifier's noise and noise-plus-distortion referred to the input of the acquisition system well below our targeted 3 $\mu{\rm V_{rms}}$ as discussed in Section II.

C. Reduction of the Required ADC's Resolution

The main benefit of the proposed amplifier is to allow the use of a very high gain in the amplification stage without the worry of output saturation even in the presence of large input interferences. Such high gain helps relax the ADC resolution requirement, which, consequently, helps reduce power consumption and the design complexity of the ADC.

To illustrate the concept discussed above, we recorded an ECG from standard Ag-AgCl electrodes placed in the lead-II configuration using our on-chip ECG acquisition system [18]. The acquisition system consists of an on-chip AFE—with a gain of 200 V/V and an input-referred noise of around 2.5 $\mu{\rm V_{rms}}$—followed by the proposed amplifier. The amplifier's output was then digitized with the same on-chip 10-bit ADC discussed earlier. To emulate the digitization by lower-resolution ADCs, we just discarded specific numbers of the LSBs from each sample. For instance, to emulate the digitization by a 6-bit ADC, we discard 4 LSBs, and so on. Fig. 17 shows the recorded ECG referred to the input of the ECG acquisition system for the digitization at 6 to 10 bits of resolution. We can see that the ECG waveforms from the digitization at higher than 7 bits are nearly indistinguishable from each other, indicating that increasing the resolution beyond 7 bits provides negligible SNR improvement.

D. Tolerance to Motion Artifacts and Mains Interference

In this part, we investigate the proposed amplifier's tolerance to large MA and mains interference. To test the tolerance to MA, we emulated the input into the amplifier by superimposing a 1.6-${\rm V_{pp}}$ 0.5-Hz sinusoidal signal as MA—which is large enough to saturate the amplifier's output—on top of a pre-processed ECG whose amplitude is around 100 ${\rm mV_{pp}}$ (assuming that the ECG has been amplified by an AFE with a 40-dB gain). The combined input was then fed into the amplifier whose output was digitized by an 8-bit ADC—i.e., by the same 10-bit ADC with two LSBs discarded. Fig. 18 (blue trace) illustrates the digitized output of the proposed amplifier after reconstruction—normalized by a gain of 1,780 V/V to refer to the input of the ECG acquisition system. We can see that even when stressed by such large MA, the amplifier's output is not saturated, thus permitting the recovery of the ECG in the digital backend. To

TABLE II
PERFORMANCE SUMMARY AND COMPARISON TO PREVIOUS WORKS

Parameters	[15] **TCAS1'09**	[16] **TBCAS'14**	[11] **JSSC'11**	[14] **JSSC'15**	[32] **TCAS2'18**	**This work**
Tech.	0.35 μm	0.18 μm	0.5 μm	0.18 μm	0.13 μm	0.18 μm
Supply	3 V	1 V	2 V	1.2 V	1.8 V	1.2 V
Gain Scheme	signal-folding	signal-folding	PGA	PGA	fixed	signal-folding
ADC Res.	16 bits	8 bits	11 bits	13.5 bits	-	7 bits [(3)]
Samp. Rate	5 kS/s	20 kS/s	64 S/s 1.024 kS/s	500 S/s	-	4.096 kS/s
Gain (V/V)	400	512	3, 5, 9, 13	1, 2, 4	53.7	17.8
THD (3 harmonics)	0.7%@ 20 mV_p, 20 Hz 0.9%@ 1 mV_p, 20 Hz	0.2%@ 2 mV_{pp}, 3 Hz	- -	- -	0.06%@ 5.5 mV_{pp}, 12 Hz 0.7%@ 22 mV_{pp}, 12 Hz	0.022%@ 1.2 V_p 0.5-32 Hz
DR	96 dB	66 dB	-	84.8 dB	68 dB	75 dB
SNDR	43 dB[(1)]	32 dB@ 2.2 mV_{pp}, 10 Hz 26 dB@ 2.2 mV_{pp}, 30 Hz	-	-	55.7 dB@ 5.5 mV_{pp} 37 dB@ 22 mV_{pp}	**71 dB**
Area	0.08 mm^2	0.124 mm^2	-	7 mm^2[(2)]	0.24 mm^2	0.25 mm^2
Power	180 μW	2.52 μW	125 nW	12 μW	1.8 μW	2.64 μW

[(1)]Calculated from 0.7% THD @ 20 mV_p input.
[(2)]Estimated area of the PGA.
[(3)]Only 7-bit resolution is used to achieve the stated DR and SNDR performances.

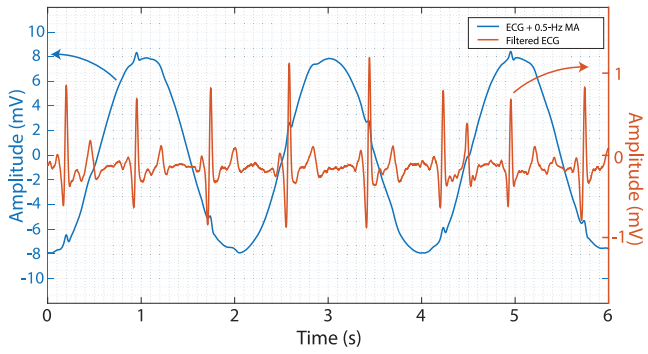

Fig. 18. Recording of an ECG corrupted by a very large MA.

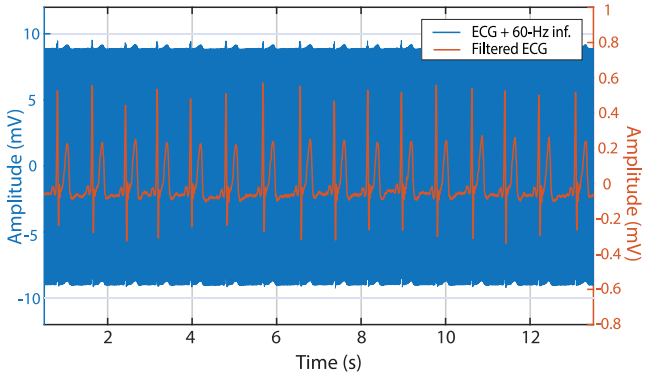

Fig. 19. Recording of an ECG corrupted by a very large mains interference.

illustrate this point, we applied a simple adaptive noise canceling technique using the generated MA as a reference to extract the clean ECG from the amplifier's output. The result is shown as the red trace in Fig. 18. We can see that even though the shapes of the P and T waves are affected by the filtering, the QRS complex is still clearly evident. It is worth noting that the quality of the filtered ECG depends much on the applied filtering algorithm, and not on the proposed amplifier as it only provides faithful ECG recording with minimal distortion to the ECG waveforms.

To test the tolerance of the proposed amplifier to mains interference, we emulated its input by superimposing a 1.6-V_{pp} 60-Hz sinusoidal signal as mains interference on top of a pre-processed ECG whose amplitude is around 100 mV_{pp}. Following the same procedure as in the MA case, we obtained the reconstructed output of the amplifier referred to the ECG acquisition system's input, as shown in Fig. 19 (blue trace). Not surprisingly, the amplifier's output exhibits no saturation, thus allowing us to recover the ECG from the recorded signal. Fig. 19 (red trace) shows the recovered ECG after the amplifier's output has been processed in MATLAB—by passing it through a 4th-order Butterworth notch filter centered at 60 Hz and then bandlimiting the result from DC to 150 Hz with a 4th-order Butterworth lowpass filter. Notice that, even when corrupted by a large 60-Hz interference, the features of the ECG waveforms are still quite well preserved, thanks to the excellent linearity of our proposed amplifier.

VI. CONCLUSION

This paper demonstrates a discrete-time amplifier that utilizes a signal-folding scheme to maximize its linearity even when the input is rail-to-rail. The proposed amplifier is suitable for use in place of PGAs to help eliminate the need for an automatic gain-control circuitry deemed necessary in most practical programmable-gain ECG acquisition systems. Also, the amplifier's high gain and excellent linearity help maximize the total gain of the amplification stage, thus allowing for the reduction of the ADC's resolution. Table II summarizes the performance of the proposed amplifier compared to previous works—including

previous signal-folding amplifiers [15], [16], PGAs in state-of-the-art ECG acquisition systems [11], [14], and a highly-linear AFE [32]. Note that, in Table II, the gains of the proposed work, [11], and [14] refer to the 2nd-stage amplifier's gain while the gains of [15], [16], and [32] refer to that of the entire AFE. It is also worth noting that our proposed amplifier achieves a very high SNDR of 71 dB while consuming only 2.64 μW of power from a 1.2-V supply. Such low-power consumption and high SNDR thus make the proposed amplifier attractive for ECG recording amid large differential interferences—e.g., in systems that use dry or non-contact electrodes.

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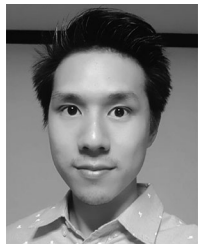

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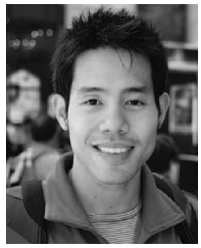

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