สกว
TRF

รายงานวิจัยฉบับสมบูรณ์

โครงการ : การวิจัยวงจรรวมและเทคนิคการออกแบบวงจรสำหรับการประมวลผลสัญญาณ

โดย ศ.ดร.วัลลภ สุระกำพลธร และคณะ

14 สิงหาคม 2546

รายงานวิจัยฉบับสมบูรณ์

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คณะผู้วิจัย		สังกัด
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2. รศ.บุญรักษ์	จิปิภพ	มหาวิทยาลัยพระจอมเกล้าธนบุรี
3. ผศ.ดร.เกียรติศักดิ์	คมวัชระ	สถาบันเทคโนโลยีพระจอมเกล้าเจ้าคุณทหารลาดกระบัง
4. ผศ.วรพงศ์	ตั้งศรีรัตน์	สถาบันเทคโนโลยีพระจอมเกล้าเจ้าคุณทหารลาดกระบัง
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7. น.ส.ขนิษฐา	แก้วแดง	สถาบันเทคโนโลยีพระจอมเกล้าเจ้าคุณทหารลาดกระบัง
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10.นายมนูญ	สันถวะคุปต์	สถาบันเทคโนโลยีพระจอมเกล้าเจ้าคุณทหารลาดกระบัง
11. นายอดุลย์	ขันติชนะกุล	สถาบันเทคโนโลยีพระจอมเกล้าเจ้าคุณทหารลาดกระบัง
12. น.ส.ภัทรา	เพียรชอบ	สถาบันเทคโนโลยีพระจอมเกล้าเจ้าคุณทหารลาดกระบัง
13. น.ส.ทิพย์สุคนธ์	อุ่นอบ	สถาบันเทคโนโลยีพระจอมเกล้าเจ้าคุณทหารลาดกระบัง

สนับสนุนโดย สำนักงานกองทุนสนับสนุนการวิจัย

ชุดโครงการ เมธีวิจัยอาวุโส

บทคัดย่อ

(Abstract)

บทคัดย่อ

โครงการวิจัย "การวิจัยวงจรรวมและเทคนิคการออกแบบวงจรสำหรับประมวลผลสัญญาณ" เป็นการดำเนินการวิจัยเพื่อค้นคว้า คิดค้นและเสนอแนวคิดใหม่ในการออกแบบวงจรอนาลอก (Analog) และดิจิตัล (Digital) สำหรับระบบประมวลผลสัญญาณ โดยเน้นการสร้างเป็นวงจรรวมหรือวงจรไอซี (Integrated Circuit) เป็นการดำเนินการวิจัยที่พยายามผลักดันให้ผลงานมีคุณภาพสูง โดยเฉพาะสามารถตีพิมพ์เผยแพร่ในวารสารระดับนานาชาติที่มีมาตรฐานสูงได้ นอกจากนี้ยังเป็นการสร้างกลุ่มวิจัยทางด้านการออกแบบวงจรรวม และส่งเสริมให้เกิดความเชื่อมโยงของงานวิจัยที่สามารถนำไปใช้ในอุตสาหกรรมไมโครอิเล็กทรอนิกส์ได้ การวิจัยจะจำกัดเฉพาะวงจรรวมที่สร้างเป็น ไบโพลาร์เทคโนโลยี (bipolar technology) มอสเทคโนโลยี (MOS technology) และแกเลียมอาเซไนด์เทคโนโลยี (GaAs or gallium arsenide technology)

สำหรับวงจรประมวลผลสัญญาณอนาลอก งานวิจัยเน้นการค้นคว้าและออกแบบวงจรรวมพื้นฐาน(circuit building blocks) ในเทคโนโลยีแบบต่าง ๆ เป็นหลักและการนำเอาวงจรพื้นฐานเหล่านี้มาประยุกต์ใช้งานในการออกแบบวงจรประมวลผลสัญญาณ โดยหัวข้อวิจัยที่ได้ดำเนินการวิจัยและสามารถตีพิมพ์เผยแพร่ในวารสารวิจัยและการประชุมวิชาการระดับนานาชาติ เช่น การออกแบบวงจร Four Terminal Floating Nullor (FTFN) การออกแบบวงจรแปลงศักย์ไฟฟ้าอาร์เอ็มเอสเป็นศักย์ดีซีที่เหมาะกับการสร้างด้วยซีมอสเทคโนโลยี การออกแบบ วงจรคูณ/หารสัญญาณเชิงอนาลอก วงจรกำเนิดสัญญาณและวงจรเรียงกระแสโดยใช้เทคโนโลยีแบบซีมอสและไบโพลาร์ การสังเคราะห์วงจรกรองโหมดกระแสหลายฟังก์ชันโดยใช้อุปกรณ์แอกทีฟแบบต่าง ๆ เช่น Current Differencing Buffered Amplifier : CDBA, Operational Transconductance Amplifier : OTA , FTFN และSecond Generation Current Conveyor: CCII การออกแบบวงจรทวีความถี่และวงจรเรียงกระแสในโหมดกระแสด้วย OTA หรือ CCII ส่วนวงจรประมวลผลสัญญาณดิจิตอล มีการพัฒนาออกแบบวงจรดิจิตอลซึ่งพัฒนาขึ้นโดยใช้อุปกรณ์ Field Programmable Gate Array (FPGA) โดยเน้นวงจรกรองแบบโครงสร้างเลขคณิตแจกแจง (distributed arithmetic) และในขณะเดียวกันสามารถลดทอนสัญญาณรบกวนจากการคำนวณ (round-off noise) ด้วย

ผลงานวิจัยของโครงการนี้ ได้สรุปเป็นบทความวิจัยพิมพ์ในวารสารวิชาการระดับนานาชาติแล้วจำนวน 2 เรื่อง เสนอในวารสารระดับชาติ จำนวน 2 เรื่อง การประชุมวิชาการระดับนานาชาติจำนวน 33 เรื่อง และอยู่ในระหว่างการพิจารณาของวารสารระดับนานาชาติอีก 4 บทความ รวมทั้งได้มีการนำเอาวงจรที่ออกแบบขึ้นมาสร้างเป็นวงจรรวมต้นแบบโดยเป็นการร่วมมือกับ NECTEC และบริษัทซิลิกอนคราฟท์ จำกัด รวมทั้งหมด 5 วงจร การสร้างทีมวิจัยประกอบด้วยนักวิจัยที่สำเร็จการศึกษาระดับปริญญาเอก 2 คน และระดับปริญญาโท 5 คน เป็นนักศึกษาระดับบัณฑิตศึกษา 1 คน และมีนักวิจัยรุ่นใหม่ที่ร่วมโครงการจากสถาบันเดียวกัน 3 คน และจากต่างสถาบัน 1 คน

Abstract

This project, the Research on Integrated Circuits and Design Techniques for Signal Processing, is researching in the areas of analog and digital signal processing with mainly emphasis in integrated circuit (IC) design. The objectives are to produce high quality research papers in international journals, to produce human resources (under graduate and postgraduate students) in the area of integrated circuit design, to form a forum in IC design, to promote research work that can be related with the Microelectronics industry and to upgrade the human resource for the Microelectronics industry. The circuit designs that can be fabricated in three technologies, i.e. bi-polar technology, MOS technology and GaAs technology, are investigated.

For analog integrated circuits, we focus on the research and design of analog circuit building blocks, sine they are the basic units for signal processing systems. The research works that can be published in the international journal and international conferences are as follows; the design of Four Terminal Floating Nullor (FTFN), the realization of RMS through DC converter suitable for CMOS technology, wide-band analog multiplier and divider, oscillator and rectifier circuits based on CMOS and bipolar technologies, the realization of multifunctional current mode filter by using active circuits such as CDBA (Current Differencing Buffered Amplifier), OTA (Operational Transconductance Amplifier), FTFNs and CCII (Second Generation Current Conveyor), and the design of frequency doubler and rectifier circuits by using active circuit such as OTA and CCII. For digital signal processing, we focus on the implementation of distributed arithmetic structure digital filter using Field Programmable Gate Array (FPGA), where a method for the reduction of round-off noise is also included.

The outputs from this research project are as follows. We can publish 2 articles in international journal and 2 national journals. Thirty three (33) technical papers have been presented in international conferences. Four (4) research articles are submitted for possible publication. Furthermore, five (5) analog building block IC prototypes have been under fabrication, with the cooperation from NECTEC and Silicon Craft Co., Ltd. For the research staff, two (2) doctoral degree and 5 master degree students are graduated under the support of this project. Moreover, we can produce 3 new researchers in the same institute and 1 new researcher from the other institute.

หน้าสรุปโครงการ

(Executive Summary)

หน้าสรุปโครงการ (EXECUTIVE SUMMARY)
ทุนเมธีวิจัยอาวุโส สกว. (ทุนส่งเสริมกลุ่มวิจัย)

1. ชื่อโครงการ (ภาษาไทย) การวิจัยวงจรรวมและเทคนิคการออกแบบวงจรสำหรับการประมวลผลสัญญาณ

   (ภาษาอังกฤษ) **RESEARCH ON INTEGRATED CIRCUITS AND DESIGN TECHNIQUES FOR SIGNAL PROCESSING**

2. **ชื่อหัวหน้าโครงการ หน่วยงานที่สังกัด ที่อยู่และหมายเลขโทรศัพท์ โทรสาร และ E-mail**

ศาสตราจารย์ ดร.วัลลภ สุระกำพลธร
ภาควิชาอิเล็กทรอนิกส์
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3. **สาขาที่ทำการวิจัย** วิศวกรรมไฟฟ้า ด้าน Analog Integrated Circuit Design, Current-Mode Circuit, Mixed Signal VLSI Signal Processing

7. ปัญหาที่ทำการวิจัย และความสำคัญของปัญหา

In the field of digital signal processing, from the last 10 years, the technology on the design of integrated circuit, particularly VLSI technology, has been rapidly developed. We can implement a very high-complicated circuit such as, for examples, a Personal Computer (PC) or a communication system, into a very small size silicon chip. This cause the electronic equipment in the future gets smaller and smaller but with cheaper price, high reliability, and with highly sophisticated functions. It is well accepted that the IC design and fabrication technology is the infrastructure and contributes greatly to the development of science and technology, the advancement of the electronic industry, and also the development of information technology (IT). Today we utilize a lot of electronic products and our daily activities are influence by electronic equipment, since most of the today consumer products are well equipped with electronic circuits and components. The IC technology is also very important for the Thai economy and Thai industry. This is due to that we export quite a large number of electronic products. For example, for the year 1994/1995, the electronics industry exports about Bht. 200,000 million, which is about 10% of the export of the country, and keeps growing rapidly every year. However, we can gain only 5% of that amount, which is for the labor-intensive cost, since most of these products are imported. In order to gain more benefit, we must have our own technology for the design and production of electronic product, with highly competitive and low price. This means we need to have, apart from the local microelectronic industry, a large number of high-educated researcher and engineer for this area. In order that in the future, we will have many design houses that are to specialize in intellectual properties and in developing news design. And these engineers can do the IC design that matched with the set of design rules and device-characteristics provided by the Foundry Company.

It should be noted that, the research and development in VLSI design requires a lot of investment on the software design tools and fabrication facilities. In the other hand, the software design tools and fabrication facilities are very expensive and most of the universities can not effort to have their own design tools and fabrication facilities. This is the main reason that the research activity in IC design has been limited to the study level of senior projects. In order to stimulate the VLSI design and research activities in Thailand, in 1989, the National Electronics and Computer center (NECTEC) has launched a project on Microelectronic design by joining the ASEAN-Australian project. From this project, many integrated circuits were sent for fabrication. The ASIC chip development project, which aimed to design the VLSI for telecommunication, micro-controller core and digital signal processing (DSP) core, are created [1]. Also the Thailand Microelectronic center, which equipped with IC fabrication facilities and IC software design tool, will be established. However the research activities and the number of researcher in this area until now is quite limited (not more than 15). In addition, unlike other major industry, the microelectronics industry relies heavily on research and development (R&D). Thus, for an advanced IC company that will be installed in Thailand in the future, high quality manpower is the key of success.

For the research in analog signal processing, there are three main technologies that have been usually employed to design the analog integrated circuits, namely, Bipolar technology, MOS technology and GaAs (gallium arsenide) technology [2-5]. The brief background on the development of these technologies is as follows. Since the early of 1960, the designs for most of analog integrated circuits have been dominated by the bipolar technology. While for the MOS technology, with its superior device density, was used mostly for digital logic and memory applications. Later on, in the early of 1970, there has been strong motivation to develop a novel MOS circuit that can perform an analog function. This is due to the rapid progress in MOS technology which made it possible to design analog circuits by utilizing standard digital MOS technology, and can also be placed in the same chip with digital circuitry. However, both the bipolar and MOS technologies circuits are appropriate for the frequency range lower than the GHz band. Therefore, for the very high frequency applications or the high speed analog circuits, the GaAs technology will offers unique and significant advantages [6]. The term analog IC design will generally refer to the circuit designs based on the use of analog active circuit building blocks, such as for example, a current mirror, a differential amplifier, a differential amplifier with active load, an operational amplifier (op-amp), an operational transconductance amplifier (OTA), a current conveyor (CCII), and an four terminal floating nollor (FTFN). This also includes the use of analog active building blocks to realize system transfer function such as voltage-mode and current-mode filter functions [7].

Comparing with analog discrete circuits, the main limitations for the analog IC design are due to the inherent limitations of monolithic device structures such as lack of monolithic inductors, limited choice of components values, poor absolute value tolerances and large temperature coefficients. But, on the other hand, the IC technologies provides some powerful advantages such as the availability of large number of active devices, good matching and good thermal tracking of component values. Therefore, the design approaches for analog IC circuit, functions, and building blocks will mainly based on the advantages offered the monolithic integrated circuit. It should be emphasized that for the analog integrated circuit, there is no general design method that can be applied to the design of IC circuit in all the IC technology, i.e. bipolar, MOS or GaAs technology. Difference technology will require difference design approach. In addition, even in the same technology but with difference transistor size, the design approach will be also quite different. This means that, to design an analog integrated circuit with low price, high efficiency and reliability, and matched with the technology, we need to have the researcher and engineer with high experience and close in touch with the development in analog IC design and technology.

Therefore, this project, which under the Thailand Research Fund (TRF) senior research scholarship and has the objective to form and upgrade the forum for IC design, will not only help in stimulating the research in this area, but also promoting the collaborative research with the researchers in the universities and the microelectronic center. In addition, this project will also help in preparing and upgrading the human resource for the microelectronic industry, which is one of the major exporting industries of Thailand, in the near future.

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8. วัตถุประสงค์ของโครงการ

8.1 To conduct research in the areas of analog and digital (mixed) signal processing with mainly emphasis in VLSI integrated circuit design

8.2 To produce high quality technical research papers in international journals such as the Institute of Electrical and Electronics Engineers (IEEE) transactions, and the Institution of Electrical Engineers (IEE) journals.

8.3 To form a forum in IC design and conduct joint collaborative research with the researches in the other universities.

8.4 To promote research work that can be related with the Microelectronics industry and to upgrade the human resource for the Microelectronics industry.

9. ระเบียบวิธีวิจัย

The research will be conducted in 4 areas, with two subjects in each area, where the activities can be described step by step as follows:

9.1 The design of analog circuit building blocks in bipolar and MOS technology

9.1.1 The realization of translinear four terminal floating nullor (FTFN)

a. Literature review

b. Design the bipolar-based FTFN circuits

c. Circuit simulation using PSPICE to evaluate the circuit performance

d. Comparing with the exiting circuit, if the performance of the circuit is not excellent enough then go back to step b

e. Complete circuit diagram for the final integrable translinear based FTFN

f. Work out for the circuit characteristic and applications

g. Prepare for the report and publication

9.1.2 The Design of CMOS-based true RMS-to-DC Converter

a. Literature review

b. Design the CMOS circuits

c. Circuit simulation using PSPICE to evaluate the circuit performance

d. Comparing with the exiting circuit, if the performance of the circuit is not excellent enough then go back to step b

e. Circuit diagram for the integrable CMOS-based RMS-to-DC converter

f. Design the circuit layout using L-Edit

g. Design and modify the layout of the RMS-to-DC using CADENCE

h. Layout prototype for the CMOS circuit and evaluate the circuit performance by simulation using CADENCE

i. Prepare and sent for fabrication

j. Performance test

k. Prepare for report and publication

9.2 The realization of integrable current-mode transfer functions

9.2.1 On the realization of current-mode multifunctional filters using OTAs

a. Literature review

b. Investigate, realize and develop current-mode filters that using OTAs and grounded capacitors

c. Simulate the filters response using PSPICE

d. Optimize and design the filter that provides low sensitivity and that can be electronically tuned

e. Work out for the filter characteristic and applications

f. Prepare for the report and publication

9.2.2 Realization of current-mode FTFN-based filters and inverse filters

a. Literature review

b. Study on the network transformation using nullor model, RC:CR transformation and dual transformation

c. Develop the systematically transformation procedure to transform the op-amp-based filters to stable current-mode FTFN-based filters with preserve the filter response

d. Develop the systematically transformation procedure to transform the FTFN-based filters to stable current-mode inverse FTFN-based filters with preserve the filter response

e. Simulate and test for the filters characteristics

f. Prepare for the report and publication

9.3 Integrable GaAs-based high frequency circuit design

9.3.1 GaAs-based second-generation current conveyor (CCII)

a. Literature review

b. Design the GaAs-based CCII circuits

c. Circuit simulation using PSPICE and GaAs transistor model to evaluate the circuit performance

d. Comparing with the exiting circuit, if the performance of the circuit is not excellent enough then go back to step b

e. Design the final integrable GaAs-based CCII

f. Work out for the circuit characteristic and applications

g. Prepare for the report and publication

9.3.2 GaAs-based voltage-to-current (V/I) converter

a. Literature review

b. Design the GaAs-based V/I circuits

c. Circuit simulation using PSPICE and GaAs transistor model to evaluate the circuit performance

d. Comparing with the exiting circuit,If the performance of the circuit is not excellent enough then go back to step b

e. Design the final integrable GaAs-based V/I

f. Work out for the circuit characteristic and applications

g. Prepare for the report and publication

9.4 Integrable circuit design for digital signal processing

9.4.1 FPGA realization of recursive digital filter

a. Literature review

b. Study on the realization of recursive digital filters using FPGAs

c. Filter simulation using ASIC design tool and evaluate the filter performance using XACT or MAX-plusII

d. Go back to step b and develop the filters until get the filter with expectable response

e. Implement the FPGA-based filter using FPGA chip such as Xilinx XC3000

f. Work out for the circuit characteristic and applications

g. Prepare for the report and publication

9.4.2 VLSI implementation of logarithmic A/D converter

a. Literature review

b. Study and investigation of logarithmic A/D

c. Circuit simulation using HSPICE to evaluate the circuit performance

d. Comparing with the exiting circuit, if the performance of the circuit is not excellent enough then go back to step b

e. Circuit diagram for the integrable CMOS-based V/I converter

f. Design of the layout using CADENCE Layout prototype for the CMOS circuit

g. Performance test

h. Prepare for report and publication

10. จำนวนโครงการที่คณะผู้วิจัยกำลังดำเนินอยู่

10.1 <u>สำหรับหัวหน้าโครงการ</u>

ชื่อโครงการ : ห้องปฏิบัติการวิจัย MVLSI Signal Processing Research and Development Laboratory

ระยะเวลาของโครงการ 5 ปี ตั้งแต่ พ.ศ. 2539 ถึง พ.ศ. 2543

แหล่งทุนที่ให้การสนับสนุน เป็นความช่วยเหลือที่ทางรัฐบาลญี่ปุ่นให้กับ สถาบันเทคโนโลยีพระจอมเกล้าเจ้าคุณทหารลาดกระบัง ที่จะเสริมสร้างความสามารถทางด้านวิจัยของสถาบัน

งบประมาณที่ได้รับ เป็นการช่วยเหลือด้านเครื่องมือและอุปกรณ์วิจัย รวมถึงผู้เชี่ยวชาญจากมหาวิทยาลัยของประเทศญี่ปุ่น

สถานะของหัวหน้าโครงการ ☑ หัวหน้าโครงการ

☐ ผู้ร่วมโครงการ

เวลาที่ใช้ทำวิจัยในโครงการนี้มีกี่ชั่วโมงต่อสัปดาห์ 8 ชั่วโมงต่อสัปดาห์

10.2 <u>สำหรับนักวิจัยในโครงการ</u>

ชื่อโครงการ : ห้องปฏิบัติการวิจัย MVLSI Signal Processing Research and Development Laboratory

ระยะเวลาของโครงการ 5 ปี ตั้งแต่ พ.ศ. 2539 ถึง พ.ศ. 2543

แหล่งทุนที่ให้การสนับสนุน เป็นความช่วยเหลือที่ทางรัฐบาลญี่ปุ่นให้กับ สถาบันเทคโนโลยีพระจอมเกล้าเจ้าคุณทหารลาดกระบัง ที่จะเสริมสร้างความสามารถทางด้านวิจัยของสถาบัน

งบประมาณที่ได้รับ เป็นการช่วยเหลือด้านเครื่องมือและอุปกรณ์วิจัย รวมถึงผู้เชี่ยวชาญจากมหาวิทยาลัยของประเทศญี่ปุ่น

สถานะของหัวหน้าโครงการ ☐ หัวหน้าโครงการ

☑ ผู้ร่วมโครงการ

เวลาที่ใช้ทำวิจัยในโครงการนี้มีกี่ชั่วโมงต่อสัปดาห์ 8 ชั่วโมงต่อสัปดาห์

เนื้อหางานวิจัย
และผลที่ได้จากโครงการ

สัญญาเลขที่ RTA/04/2543

โครงการ : การวิจัยวงจรรวมและเทคนิคการออกแบบวงจรสำหรับการประมวลผลสัญญาณ

รายงานฉบับสมบูรณ์

ชื่อหัวหน้าโครงการ ศาสตราจารย์ ดร.วัลลภ สุระกำพลธร

รายงานในช่วงตั้งแต่วันที่ 15 สิงหาคม 2543 **ถึงวันที่** 14 สิงหาคม 2546

1. กิจกรรมที่ได้ดำเนินการ

ทุนวิจัยประเภททุนส่งเสริมกลุ่มวิจัยในโครงการ **การวิจัยวงจรรวมและเทคนิคการออกแบบวงจรสำหรับการประมวลผลสัญญาณ** (Research on Integrated Circuits and Design Techniques for Signal Processing) ได้เสนอการดำเนินการวิจัยไว้ใน 4 ด้านหลักนั้น ในช่วงวันที่ 15 สิงหาคม 2543 ถึงวันที่ 14 สิงหาคม 2546 โดยสรุปทางโครงการได้ดำเนินการวิจัยสำเร็จในระดับหนึ่งได้ใน 3 ด้านหลักด้วยกัน ส่วนในอีก 1 ด้านนั้นผลงานเริ่มพัฒนาและได้รับการยอมรับให้นำเสนอในการประชุมวิชาการระดับชาติและระดับนานาชาติ ส่วนอีก 1 ด้านยังไม่ได้ดำเนินการ เนื่องจากว่าในแต่ละด้านมีรายละเอียดที่ค่อนข้างมาก รายละเอียดเหล่านี้ได้สรุปไว้เป็นอย่างดีในบทความวิจัย ซึ่งได้แนบบทความเหล่านี้ไว้ในภาคผนวกแล้ว ดังนั้นผลงานวิจัยต่างๆจึงขอกล่าวถึงอย่างกว้างๆ

เนื่องจากการประชุมทางวิชาการ โดยเฉพาะทางด้านวิศวกรรมไฟฟ้ามีอยู่มาก และระดับคุณภาพโดยเฉพาะการประชุมวิชาการที่มีผู้เข้าร่วมประชุมมาก จะมีการคัดเลือกบทความ (peer review) อย่างเข้มข้นจากนักวิจัยทั่วโลกอย่างน้อยบทความละ 3 คน และบทความวิจัยที่ได้รับการคัดเลือกให้เสนอผลงานก็จะปรากฏในฐานข้อมูล เช่น ฐานข้อมูลของ The Institute of Electrical and Electronics Engineers (IEEE) Xplore ด้วย ดังนั้นในรายงานนี้ได้จำแนกบทความวิจัยที่เสนอในการประชุมวิชาการระดับนานาชาติไว้เป็น 2 ประเภท คือ การประชุมวิชาการนานาชาติที่อยู่ในฐานข้อมูล IEEE Xplore และ การประชุมวิชาการระดับนานาชาติทั่วไป ซึ่งมีการคัดเลือกบทความไม่เข้มข้นนัก นอกจากนี้ทางโครงการได้ทำการพัฒนาวงจรรวมต้นแบบและจัดสร้างเป็นวงจรไอซี โดยการจัดสร้างบางส่วนได้รับความร่วมมือจาก ศูนย์เทคโนโลยีอิเล็กทรอนิกส์และคอมพิวเตอร์แห่งชาติ (NECTEC) และบริษัทซิลิคอนคราฟท์ จำกัด ตามรายละเอียดของการดำเนินการวิจัยของโครงการมีดังต่อไปนี้

1.1 การวิจัยและพัฒนาเพื่อศึกษา ค้นคว้า ออกแบบ และคิดค้นวงจรที่จะเป็นวงจรพื้นฐาน (The Design of Analog Integrated Circuit Building Blocks in Bipolar and MOS Technology) ซึ่งจะเป็นอุปกรณ์หลักสำหรับที่จะนำไปใช้ในการออกแบบระบบวงจรประมวลผลสัญญาณที่สร้างด้วย ไบโพลาร์เทคโนโลยี และ มอสเทคโนโลยี ด้านนี้มีผู้ร่วมดำเนินการวิจัยคือ รศ.บุญรักษ์ จิปิภพ ผศ.ดร.เกียรติศักดิ์ คมวัชระ ผศ. วรพงศ์ ตั้งศรีรัตน์ อ.บุญชัย บุญชู นายเฉลิมภัณฑ์ ฟองสมุทร นายอมร จิรเสรีอมรกุล ศ.วัลลภ สุระกำพลธร และ น.ส.ขนิษฐา แก้วแดง โดยได้ทำการวิจัยต่อเนื่องใน 3 หัวข้อวิจัยย่อย รายละเอียดของผลงานวิจัยในหัวข้อย่อยสามารถสรุปดังนี้

1.1.1 การออกแบบวงจร Four Terminal Floating Nullor (FTFN) โดยอาศัยหลักการของวงจรทรานลิเนียร์ (The Realization of Translinear Four Terminal Floating Nullor) เป็นการศึกษาเพื่อ พัฒนาและออกแบบวงจร FTFN ซึ่งเป็นอุปกรณ์วงจรพื้นฐานที่สำคัญอุปกรณ์หนึ่ง ให้มีประสิทธิภาพความแม่นยำดียิ่งขึ้นโดยเฉพาะกับการสร้างเป็นมอสเทคโนโลยี นอกจากนี้ยังมีการขยายคุณสมบัติของ FTFN ให้สามารถประยุกต์ได้อย่างกว้างขวางมากขึ้น โดยดำเนินการวิจัยเป็นไปตารางที่ 1.1.1 ในโครงการนี้ได้เสนอทำการออกแบบให้ FTFN มีหลายจุดสัญญาณออก (multi-output FTFN)

และแสดงให้เห็นว่า จากการที่มีหลายจุดสัญญาณออกเมื่อนำไปประยุกต์ใช้จะทำให้จำนวนอุปกรณ์ FTFN ที่ต้องใช้ลดน้อยลง นอกจากนี้ยังเสนอการออกแบบให้ FTFN มีคุณสมบัติแบบที่ปรับค่าขยายด้วยวิธีอิเล็กทรอนิกส์ (electronically tunable FTFN) และ แสดงการประยุกต์ใช้ในการสร้างเป็นวงจรกรองโหมดกระแส (current-mode FTFN-based filters) ที่สามารถปรับความถี่ตัด (cut-off frequency) โดยวิธีอิเล็กทรอนิกส์ได้ ผลงานนี้รวมถึงรายละเอียดการออกแบบและการประยุกต์ใช้ได้สรุปเขียนในบทความวิจัยซึ่งนำเสนอในการประชุมวิชาการระดับนานาชาติจำนวน 9 บทความ ตามเอกสารในภาคผนวก ก และ ภาคผนวก ง นอกจากนี้ยังได้ออกแบบวงจรรวมต้นแบบของ FTFN แบบหลายจุดสัญญาณออกที่อยู่ในกระบวนการสร้างเป็นไอซี 1 วงจร บทความที่ได้จากการวิจัยในหัวข้อวิจัยนี้มีดังต่อไปนี้

การประชุมวิชาการนานาชาติที่อยู่ในฐานข้อมูล IEEE XPlore

1). A. Jiraseri-amornkun, B. Chipipop and W. Surakampontorn, "Novel Translinear-Based Multioutput FTFN," *Proc. 2001 IEEE International Symposium on Circuits and Systems*, Sydney, Australia, May 6-9, 2001, pp.180-183. (เอกสารหมายเลข ก.6)

การประชุมวิชาการนานาชาติ

2). A. Jiraseri-amornkun, W. Tangsrirat and W. Surakampontorn, "CMOS Multi-Output FTFN: A Translinear Approach," *Proc. 2001 IEEJ International Symposium on Analog VLSI*, Bangkok, Thailand, May 14-15, 2001, pp. 62-67. (เอกสารหมายเลข ก.12)

3). W. Tangsrirat, A. Jiraseri-amornkun and W. Surakampontorn, "Tunable FTFN and Its Application," *International Symposium on Communications and Information Technology,* Chiang Mai, Thailand, November 14-16, 2001, pp.489-492. (เอกสารหมายเลข ก.15)

4) B. Chipipop and W. Surakampontorn, "Realization of Current-Mode FTFN-Based Lowpass Filter From the Optimal Sallen and key Lowpass filter (Saraga Design) Using Driving Point Impedance and Signal-Flow Graph (DPI/SFG) Method to Preserve the Sensitivities of the Original Circuit, *International Symposium on Communications and Information Technology,* Chiang Mai, Thailand, November 14-16, 2001, pp.183-186. (เอกสารหมายเลข ก.16)

5) B. Chipipop and W. Surakampontorn, "Realization of Current-Mode FTFN-Based Lowpass Filter and Its Inverse Filter from the Optimal Sallen and Key Lowpass filter (Saraga Design) Using RC:CR Dual Transformation to Preserve the sensitivities of the Original Circuit, *International Symposium on Communications and Information Technology,* Chiang Mai, Thailand, November 14-16, 2001, pp.497-499. (เอกสารหมายเลข ก.19)

6) A. Jiraseree-amornkun and W. Surakampontorn, "Constant-gm Rail-to-Rail CMOS Multi-Output FTFN", *The 2002 International Technical Conference On Circuits/Systems,Computers and Communications,* Phuket, Thailand, July 16-19, 2002, pp.333-336.(เอกสารหมายเลข ก.24)

7) A. Jiraseree-amornkun and W. Surakampontorn, "Dual Translinear loop Multi-Output FTFN", *The 2002 IEEJ International Analog VLSI Workshop*, Singapore, September 11-12, 2002, pp.94-98. (เอกสารหมายเลข ก.29)

8) W. Tangsrirat, T. Dumawipata, S. Unhavanich and W. Surakampontorn, "On the Realization of FTFN with a Variable Voltage and Current Gains", *The 2003 International Technical Conference On*

Circuits/Systems,Computers and Communications, Kang Won Do, Korea, July 7-9, 2003, pp.884-887. (เอกสารหมายเลข ก.32)

<u>วงจรรวมต้นแบบที่อยู่ในระหว่างการสร้างเป็นวงรวม</u> จำนวน 1 วงจรคือ

9) A. Jiraseri-Amornkun and W.Surakampontorn, "Multi-Output FTFN" (เอกสารหมายเลข ง.1)

ตารางที่ 1.1.1

Item	Activity	Year 1		Year 2		Year 3	
		1 - 6	7 - 12	1 - 6	7 - 12	1 - 6	7 - 12
1.1.1	**The Realization of Translinear Four Terminal Floating Nullor (FTFN)**						
a.	Literature review	——					
b.	Design the bipolar-based/CMOS based FTFN	——					
c.	Circuit simulation using PSPICE/CADENCE Spectre to evaluate the circuit performance	——					
d.	Go back to step b	——	——	——			
e.	Complete circuit diagram for the final integrable translinear based FTFN						
f.	Work out for the circuit characteristic and applications		——	——		——	——
g.	Layout prototype for the CMOS circuit						——
h.	Prepare and sent for fabrication						——
i	Performance test						
j.	Prepare for the report and publication				——	——	——

1.1.2 การออกแบบวงจรแปลงศักย์ไฟฟ้าอาร์เอ็มเอสเป็นศักย์ดีซีที่เหมาะกับการสร้างด้วยซีมอสเทคโนโลยี (The Design of CMOS-Based True RMS-to-DC Converter) ในหัวข้อย่อยนี้ได้ทำการศึกษาและออกแบบวงจรแปลงศักย์ไฟฟ้าอาร์เอ็มเอสเป็นศักย์ดีซี โดยทำการปรับปรุงจากงานวิจัยเดิมที่เคยนำเสนอไว้ที่ออกแบบให้เหมาะกับการสร้างในไบโพลาร์เทคโนโลยี (Bipolar-Based RMS-to-DC Converter) เพื่อให้เหมาะสมกับการสร้างเป็นซีมอสเทคโนโลยีได้ โดยมีแผนการปฏิบัติงานตามที่ได้แสดงไว้ในตารางที่ 1.1.2 รายละเอียดของการวิจัยได้สรุปเป็นบทความวิจัยเสนอในการประชุมวิชาการระดับนานาชาติ 2 บทความ และเป็นบทความเป็นบทความที่อยู่ระหว่างการพิจารณาตีพิมพ์ในวารสารระดับนานาชาติ 1 บทความ ทางโครงการยังเกิดแนวความคิดใหม่ ในการออกแบบวงจรแปลงศักย์ไฟฟ้าอาร์เอ็มเอสเป็นศักย์ดีซีแบบไบโพลาร์เทคเทคโนโลยีโดยใช้ทรานซิสเตอร์แบบ npn (npn transistors) เพียงอย่างเดียว ซึ่งมีจุดเด่นคือกินไฟน้อยและสามารถทำงานในย่านความถี่สูงได้ หลักการที่พัฒนาขึ้นได้สรุปนำเสนอเป็นบทความนำเสนอ เป็นบทความที่อยู่ระหว่างการพิจารณาตีพิมพ์ในวารสารระดับนานาชาติอีก 1 บทความ และ นอกจากนี้ยังออกแบบเพื่อสร้างเป็นวงจรรวมต้นแบบที่อยู่ในกระบวนการสร้าง 1 วงจร ดังนี้

<u>วารสารวิจัยระดับนานาชาติ</u>

1). K.Kaewdang, K.Kumwachara and W.Surakampontorn," A Simple Wide Band CMOS Based True RMS to DC Converter", *International Journals of Electronics* (Submitted) (เอกสารหมายเลข ค.2)

2). C. Jongkunstidchai, C. Fongsamut, K. Kumwachara and W. Surakampontorn," A Traslinear-Based True RMS-to-DC Converter Using Only npn BJTs", *IEEE Trans. Instrmentation and Measurements.* (Submitted) (เอกสารหมายเลข ค.4)

<u>การประชุมวิชาการระดับนานาชาติ</u>

3). K. Kaewdang, K. Kumwachara, A. Jiraseri-amornkun and W. Surakampontorn, "An Integrable CMOS-Based Grounded-Capacitor True RMS-to-DC Converter," *Proc. 2001 IEEJ International Symposium on Analog VLSI*, Bangkok, Thailand, May 14-15, 2001, pp. 167-172. (เอกสารหมายเลข ก.13)

4). K. Kaewdang, K. Kumwachara, C. Fongsamut and W. Surakampontorn, "An Integrable CMOS-Based True RMS-to-DC Converter Using Class AB Amplifier," *International Symposium on Communications and Information Technology*, Chiang Mai, Thailand, November 14-16, 2001, pp.606-619. (เอกสารหมายเลข ก.17)

<u>วงจรรวมต้นแบบที่อยู่ในระหว่างการสร้างเป็นวงจรรวม</u> จำนวน 1 วงจรคือ

5) K. Kaewdang, K. Kumwachara and W. Surakampontorn, "True RMS to DC Converter" (เอกสารหมายเลข ง.3)

ตารางที่ 1.1.2

Item	Activity	Year 1		Year 2		Year 3	
		1 - 6	7 - 12	1 - 6	7 - 12	1 - 6	7 - 12
1.1.2	**The Design of CMOS-based true RMS-to-DC Converter.**						
a.	Literature review	—					
b.	Design the CMOS circuits	—					
c.	Circuit simulation using PSPICE/CADENCE Spectre to evaluate the circuit performance	—	—	—	—	—	—
d.	Go back to the step b.	—	—	—			
e.	Circuit diagram for the integrable CMOS-based RMS-to-DC converter	—	—	—			
f.	Design the circuit layout using L-Edit		—	—			
g.	Design of the layout using CADENCE		—	—			
h	Layout prototype for the CMOS circuit						
i.	Prepare and sent for fabrication				—	—	—
j.	Performance test				—	—	—
k.	Prepare for report and publication				—	—	—

1.1.3 การออกแบบ วงจรคูณ/หารสัญญาณเชิงอนาลอก วงจรกำเนิดสัญญาณ และวงจรเรียงกระแส (On the Design of Analog Multiplier, Divider, Squarer, Oscillator and Rectifier Circuits) ในหัวข้อวิจัยนี้มีการค้นคว้า คิดค้น และเสนอแนวทางการออกแบบวงจรคูณและหารสัญญาณ วงจรยกกำลังสองและเรียงกระแส และวงจรกำเนิดสัญญาณ โดยเน้นคุณสมบัติที่ทำงานในโหมดกระแส กินไฟต่ำ และทำงานในย่านความถี่สูง ได้ทำการดัดแปลง ปรับปรุง พัฒนา แก้ไขให้มีคุณสมบัติดีขึ้นตามตารางที่ 1.1.3 แล้วสรุปผลเป็นบทความวิจัยนำเสนอในการประชุมวิชาการ จำนวน 8 บทความ ดังนี้

<u>การประชุมวิชาการนานาชาติที่อยู่ในฐานข้อมูล IEEE XPlore</u>

1) B. Boonchu and W. Surakampontorn, "A CMOS Current-Mode Squarer/Rectifier Circuit", *The 2003 IEEE International Symposium on Circuits and Systems*, Thailand, May 25-28, 2003. , pp.405-408. (เอกสารหมายเลข ก.10)

2). K. Kaewdang, C. Fongsamut and W. Surakampontorn, "A Wide-Band Current-Mode OTA-Based Analog Multiplier-Divider", *The 2003 IEEE International Symposium on Circuits and Systems,* Thailand, May 25-28, 2003 ,pp.349-352. (เอกสารหมายเลข ก.9)

<u>การประชุมวิชาการระดับนานาชาติ</u>

3). B. Boonchu, P. Phadungkul and W. Surakampontorn, "A 100-MHz 1.5-mW Quarter-Square Four-Quadrant Analog Multiplier," *Proc. 2001 IEEJ International Symposium on Analog VLSI*, Bangkok, Thailand, May 14-15, 2001, pp.68-71. (เอกสารหมายเลข ก.18)

4). B. Srisuchinwong, I. Seedadan and W. Surakampontorn, "Fully differential sinusoidal oscillator using current-tunable phase-lead all-pass filters", *Proc. 2001 IEEJ International Symposium on Analog VLSI*, Bangkok, Thailand, May 14-15, 2001, pp. 62-67. (เอกสารหมายเลข ก.14)

5). B. Boonchu, P. Phadungkul and W. Surakampontorn, "Low Voltage Current Multiplier Using Linear MOS Resistors," *International Symposium on Communications and Information Technology,* Chiang Mai, Thailand, November 14-16, 2001, pp.179-182. (เอกสารหมายเลข ก.20)

6). W. Surakampontorn, K. Kaewdang and C. Fongsamut, "A Simple Current-Mode Analog Multiplier-Divider Circuit Using OTAs", *The 2002 International Technical Conference On Circuits/Systems,Computers and Communications*, Phuket, Thailand, July 16-19, 2002, pp.658-661. (เอกสารหมายเลข ก.25)

7). B. Boonchu and W. Surakampontorn,"Voltage-Mode CMOS Squarer/Multiplier Circuit", *The 2002 International Technical Conference On Circuits/Systems,Computers and Communications*, Phuket, Thailand, July 16-19, 2002, pp.646-649. (เอกสารหมายเลข ก.26)

8). K. Kaewdang, C. Fongsamut and W. Surakampontorn," A Wide-Band Current-Mode Analog Multiplier-Divider Using OTAs", *The 2002 IEEJ International Analog VLSI Workshop*, Singapore, September 11-12, 2002, pp.90-93. (เอกสารหมายเลข ก.30)

ตาราง 1.1.3

Item	Activity	Year 1		Year 2		Year 3	
		1 - 6	7 - 12	1 - 6	7 - 12	1 - 6	7 - 12
1.1.3	**On the Design of Analog Multiplier -Divider, Squarer and Rectifier Circuits**	—	—				
a.	Literature review	—	—	—			
b.	Design the CMOS circuits	—		—			
c.	Circuit simulation using using PSPICE/CADENCE		—				
	Spectre to evaluate the circuit performance	—				—	
d.	Go back to the step b.						
e.	Circuit diagram for the Analog Multiplier-		—				
	Divider, Squarer and Rectifier Circuits		—	—			
f.	Design the circuit layout using L-Edit						
g.	Design of the layout using CADENCE						
h	Layout prototype for the CMOS circuit						
i.	Prepare and sent for fabrication						
j.	Performance test					—	—
k.	Prepare for report and publication				—	—	—

1.2 การวิจัยเพื่อคิดค้น เทคนิคการสังเคราะห์และสร้างเป็นวงจรรวมของฟังก์ชันแบบโหมดกระแส (On the Realization of Integrable Current-Mode Transfer Function) ซึ่งในหัวข้อนี้เป็นการคิดค้นและออกแบบวงจรรวมของการประมวลสัญญาณอนาลอกขนาดเล็ก โดยเป็นการสังเคราะห์ฟังก์ชันที่ใช้การประมวลสัญญาณในโหมดกระแสเป็นหลัก มีผู้ร่วมดำเนินการวิจัยคือ รศ.ดร.เกียรติศักดิ์ คมวัชระ ผศ.ดร. วรพงศ์ ตั้งศรีรัตน์ ดร.คงศักดิ์ อนันตหิรัญรัตน์ นายเฉลิมพันธ์ ฟองสมุทร นายอมร จิรเสรีอมรกุล และ น.ส.เกษสุดา กล้าหาญ การวิจัยได้ดำเนินการใน 2 หัวข้อย่อย ดังนี้

1.2.1 การสังเคราะห์ตัวกรองโหมดกระแสหลายฟังก์ชันโดยใช้อุปกรณ์แอคทีฟแบบ OTA, FTFN, CCII หรือ CDBA (On the Realization of Current-Mode Multifunctional Filter Using OTA, FTFN CCII or CDBA) งานวิจัยนี้เป็นความพยายามในการออกแบบวงจรกรอง เพื่อให้ได้วงจรกรองที่มีความสามารถในการสังเคราะห์ฟังก์ชันถ่ายโอนได้หลายฟังก์ชันภายในวงจรเดียวกัน โดยที่ใช้อุปกรณ์แอคทีฟน้อย การปรับแต่งวงจรง่าย และมีความเป็นเชิงเส้นสูง โดยการออกแบบเป็นการประยุกต์ใช้อุปกรณ์พื้นฐาน เช่น อุปกรณ์ CDBA, อุปกรณ์ CCII, อุปกรณ์ OTA และ อุปกรณ์ FTFN จากการดำเนินการวิจัยตามตารางที่ 1.2.1 สามารถมีบทความตีพิมพ์ในวารสารนานาชาติ 1 บทความ บทความพิมพ์ในวารสารระดับชาติ 2 บทความ บทความนำเสนอในการประชุมวิชาการระดับนานาชาติ 11 บทความ และวงจรต้นแบบที่อยู่ในระหว่างจัดสร้าง 1 วงจร คือ

<u>วารสารวิชาการระดับนานาชาติ</u>

1) W. Tangsrirat, W. Surakampontorn and N. Fujii, "Realization of Leapfrog Filters using Current Differential Buffered Amplifiers", *The IEICE Trans on Fundamental, Special Section on Analog Circuits and Related Topics,* February 2003, Vol. E86-A, No.2, pp.318-326. impact factor 0.27 (เอกสารหมายเลข ก.1)

<u>วารสารวิชาการระดับชาติ</u>

2) I. Seedadan and W. Surakampontorn and B. Srisuchinwong "A Fully Balanced Wide-Frequency Current-Tunable Phase-Lead All-Pass Filter ", *KMUTT Research and Development Journal,* Vol. 24, January-April 2002, pp. 31-41. (เอกสารหมายเลข ก.2)

3) K. Klahan, W. Tangsrirat, W. Surakampontorn and T. Dumawipata "Current-Mode Integrator using OA and OTAs and Its Applications", *Thammasat International Journal on Science and Technology*, Vol.8, No. 2, 2003, pp. 26-32. (เอกสารหมายเลข ก.3)

<u>การประชุมวิชาการนานาชาติที่อยู่ในฐานข้อมูล IEEE XPlore</u>

4). W. Tangsrirat, S. Unhavanich, T. Dumawipata and W. Surakampontorn, "A Realization of Current-Mode Biquadratic Filters Using Multiple-Output FTFNs, " *Proc. 2000 IEEE Asia Pacific Conference on Circuits and Systems*, Tianjin, China, Dec. 4-6, 2000. , pp. 571-574. (เอกสารหมายเลข ก.4)

5). W. Tangsrirat, N. Fujii and W. Surakampontorn," Current-Mode Leapfrog Ladder Filters Using CDBAs", *The 2002 IEEE International Sympusium on Circuits and Systems*, USA, May 26-29, 2002, vol.5 , pp.V-57 -V-60. (เอกสารหมายเลข ก.7)

6). A. Jiraseri-amornkun, N. Fujii and W. Surakampontorn, "Realization of Electronically Tunable Ladder filters using Multi-Output Current Controlled Conveyors", *The 2003 IEEE International Symposium on Circuits and Systems,* Thailand, May 25-28, 2003., pp.180-183. (เอกสารหมายเลข ก.11)

7). W. Tangsrirat, S. Unhavanich, T. Dumawipata and W. Surakampontorn, "Single-Input and Three-Output Current-Mode Biquadratic Filters Using Multiple Output OMAs", *Asia Pacific Conference on Circuits and System 2002,* Indonesia, October 28-31, 2002, pp.399-404. (เอกสารหมายเลข ก.8)

<u>**การประชุมวิชาการระดับนานาชาติ**</u>

8). K. Klahan, W. Tangsrirat and W. Surakampontorn, "An Active-Only Current-Mode Differentiator and Its Applications," *International Symposium on Communication and Information Technology,* Chiang Mai, Thailand, November 14-16, 2001, pp.79-82. (เอกสารหมายเลข ก.21)

9). K. Klahan, W. Tangsrirat, T. Dumawipata and W. Surakampontorn, "Current-Mode Integrator Using OA and OTAs and Its Applications", *The 2002 International Technical Conference On Circuits/Systems,Computers and Communications*, Phuket, Thailand, July 16-19, 2002, pp.747-750. (เอกสารหมายเลข ก.27)

10). S. Prakobnoppakao, B. Chipipop, W. Surakampontorn and K. Watanabe, "Design of a Current-Mode CCII-Based Bandpass Filter from Immittance Function Simulator Using Commercial Available CCII (AD844)" , *The 2002 International Technical Conference On Circuits/Systems,Computers and Communications*, Phuket, Thailand, July 16-19, 2002, pp.743-746. (เอกสารหมายเลข ก.28)

11). W. Tangsrirat, S. Unhavanich, T. Dumawipata and W. Surakampontorn, "Electronically Tunable Voltage-Mode and Current-Mode Biquadratic Filter without External Passive Elements", *The 2002 International Symposium on Nonlinear theory and its Applications,* China, October 7-11,2002., pp.727-730. (เอกสารหมายเลข ก.31)

12). W. Tangsrirat, T.Dumawipata, S. Unhavanich and W. Surakampontorn, "Realization of Lowpass and Bandpass Leapfrog Filters Using OA and OTAs", *The 2003 Society of Instrument and Control Engineer Annual Conference*, August 4-6, 2003, Fukui, Japan , pp.1046-1051. (เอกสารหมายเลข ก.32)

13). K. Klahan, W. Tangsrirat and W. Surakampontorn, " Current-mode Universal Biquadratic Filter Using Current Differencing Buffered Amplifiers ", *International Symposium on Communication and Information Technology*, September 3-5, Songkhla, Thailand, 2003, Vol.1, pp.110-113. (เอกสารหมายเลข ก.34)

14). W. Tangsrirat, K. Klahan, K.Kaewdang, and W. Surakampontorn, " Low-Voltage CMOS Current Differencing Buffered Amplifier and Its Application ", *International Symposium on Communication and Information Technology*, September 3-5, Songkhla, Thailand, 2003, Vol.2, pp.795-798. (เอกสารหมายเลข ก.35)

<u>**วงจรรวมต้นแบบที่อยู่ในระหว่างการสร้างเป็นวงรวม**</u> จำนวน 1 วงจรคือ

15) K. Klahan, W. Tangsrirat and W. Surakampontorn, "Low-Voltage CMOS CDBA" (เอกสารหมายเลข ง.2)

ตาราง **1.2.1**

Item	Activity	Year 1		Year 2		Year 3	
		1 - 6	7 - 12	1 - 6	7 - 12	1 - 6	7 - 12
1.2.1	**On the Realization of Current-Mode Multifunctional Filters using FTFN, CCII, CDBA and OTA**						
a.	Literature review	—					
b.	Investigate, realize and develop current-mode filters that using FTFN, CCII, CDBA, and OTA	—					
c.	Simulate the filters response using PSPICE/CADENCE Spectre		—		—		—
d.	Optimize and design the filter that provides low sensitivity and that can be electronically tuned	—	—		—	—	
e.	Work out for the filter characteristics and applications				—	—	—
f.	Layout prototype for the CMOS circuit						—
g.	Prepare and sent for fabrication						—
h.	Performance test						
i.	Prepare for the report and publication		—		—	—	—

1.2.2 การออกแบบสังเคราะห์วงจรทวีความถี่และวงจรเรียงกระแสในแบบโหมดกระแส (On the Realization of Sinusoidal Frequency Doubler and Full-Wave Rectifier Circuits) หัวข้อย่อยนี้เป็นการเสนอแนวคิดในการออกแบบวงจรทวีความถี่และวงจรเรียงกระแส ซึ่งเป็นวงจรการประมวลผลสัญญาณที่สำคัญ โดยการออกแบบเป็นการอาศัยคุณสมบัติภายในของอุปกรณ์แอคทีฟที่มีชื่อเรียกว่า Translinear Current Controlled Conveyor หรือเรียกย่อว่า CCCII และอุปกรณ์ OTA การดำเนินการตามตารางที่ 1.2. โดยมีผลงานวิจัยที่ได้รับการยอมรับให้ตีพิมพ์ในวารสารวิชาการระดับนานาชาติจำนวน 1 บทความ และได้พิมพ์เป็นบทความที่เสนอในวารสารวิชาการระดับนานาชาติ 2 บทความ (อยู่ในระหว่างแก้ไข 1 บทความและอยู่ระหว่างพิจารณา 1 บทความ) นำเสนอในการประชุมวิชาการระดับนานาชาติ 3 บทความ และมีวงจรต้นแบบที่อยู่ในระหว่างจัดสร้างอีก 2 วงจร ดังนี้

<u>**วารสารวิชาการระดับนานาชาติ**</u>

1). Kiattisak Kumwachara and Wanlop Surakampontorn, "An Integrable Temperature-Insensitive g_m-RC Quadrature Oscillator, *International Journals of Electronics.* (Accepted) (เอกสารหมายเลข ข.1)

2). K. Anuntahirunrat, W. Tangsrirat, V. Riewruja and W. Surakampontorn, "Sinusoidal Frequency Doubler and Full-Wave Rectifier Using Translinear Current Controlled Conveyor," *International Journals of Electronics.* (Revised) (เอกสารหมายเลข ค.1)

3). C. Fongsamut, K. Kumwachara and W. Surakampontorn, "Full-wave Rectifier Based on Operational Transconductance Amplifiers", *International Journal of Electronics.* (Submitted) (เอกสารหมายเลข ค.3)

<u>**การประชุมวิชาการนานาชาติที่อยู่ในฐานข้อมูล IEEE XPlore**</u>

4). K. Anuntahirunrat, W. Tangsrirat, V.Riewruja and W. Surakampontorn, "Sinusoidal Frequency Doubler and Full-Wave Rectifier Using Translinear Current Controlled Conveyor," *Proc. 2000 IEEE Asia Pacific Conference on Circuits and Systems*, Tianjin, China, pp. 166-169, Dec. 4-6, 2000. (เอกสารหมายเลข ก.5)

<u>การประชุมวิชาการระดับนานาชาติ</u>

5). P. Nipathahathapong, K. Kumwachara and W. Surakampontorn, "OTA-Based Temperature-Insensitive Sinusoidal N-Times Frequency Multiplier," *International Symposium on Communications and Information Technology,* Chiang Mai, Thailand, November 14-16, 2001, pp.163-166. (เอกสารหมายเลข ก.22)

6). C. Fongsamut, K. Kumwachara and W. Surakampontorn, " The Implementation of OTA-Based Full-Wave Rectifiers" *International Symposium on Communications and Information Technology,* Chiang Mai, Thailand, November 14-16, 2001, pp.171-174. (เอกสารหมายเลข ก.23)

<u>วงจรรวมต้นแบบที่อยู่ในระหว่างการสร้างเป็นวงรวม</u> จำนวน 2 วงจรคือ

7) K. Kaewdang, K. Kumwachara and W. Surakampontorn, "Positive Current Conveyor" (เอกสารหมายเลข ง.4)

8) K. Kaewdang, K. Kumwachara and W. Surakampontorn, "Negative Current Conveyor" (เอกสารหมายเลข ง.5)

ตาราง 1.2.2

Item	Activity	Year 1		Year 2		Year 3	
		1 - 6	7 - 12	1 - 6	7 - 12	1 - 6	7 - 12
1.2.2	**Sinusoidal Frequency Doubler and Full-Wave Rectifier Using Second-Generation Current Conveyors (CCIIs) and OTA**						
a.	Literature review	—					
b.	Investigate, realize and develop translinear based sinusoidal frequency doubler and full-wave rectifier circuits	—					
c.	Simulate the filters response using PSPICE	—	—				
d.	Optimize and design the proposed sinusoidal frequency doubler and full-wave rectifier circuits	—	—	—		—	
e.	Work out for the circuit characteristics	—	—	—		—	—
f.	Prepare for the report and publication			—		—	—

1.3 การออกแบบวงจรรวมย่านความถี่สูงด้วยแกเลี่ยมอาร์เซไนด์เทคโนโลยี (Integrable GaAs-Based High Frequency Integrated Circuit Design) ในหัวข้อนี้ยังไม่ได้ทำการวิจัย ถึงแม้ทางโครงการจะมีประสบการณ์การวิจัยในสาขาวิชานี้อยู่บ้าง แต่การวิจัยในหัวข้อนี้จำเป็นต้องใช้พื้นฐานความรู้ที่ลึกซึ้ง โดยเฉพาะยังไม่สามารถหานักวิจัยที่มีความรู้พื้นฐานเพียงพอ และงานวิจัยในหัวข้อต่างๆที่ดำเนินการอยู่ก็มีประเด็นการวิจัยที่มากพอสมควรอยู่แล้ว ดังนั้นทางโครงการจึงตัดสินใจไม่ดำเนินการวิจัยในหัวข้อนี้

1.4 การออกแบบวงจรรวมสำหรับระบบประมวลผลสัญญาณเชิงตัวเลข (Integrable Circuit Design for Digital Signal Processing) โดยเฉพาะมุ่งเน้นการออกแบบที่สามารถสร้างและพัฒนาเป็นวงจรรวมแบบที่สร้างด้วยอุปกรณ์ FPGA (Field Programmable Gate Array) หรือ ที่สร้างเป็นวงจรรวมขนาดใหญ่ (VLSI) มีผู้ร่วมดำเนินการวิจัยคือ ศ.ดร.วัลลภ สุระกำพลธร นายเฉลิมภัณฑ์ ฟองสมุทร นายมนูญ สันถวะคุปต์ และ นายอดุลย์ ขันติชนะกุล โดยทางโครงการได้เสนอที่จะดำเนินการวิจัยไว้ 2 ด้าน แต่เนื่องจากไม่สามารถหานักวิจัยและผู้ช่วยนักวิจัยที่มีความรู้พื้นฐานดีได้ครบตามที่ตั้งเป้าหมายไว้ จึงมีการดำเนินการเพียง 1 ด้าน คือ

1.4.1 การสังเคราะห์วงจรกรองป้อนกลับเชิงเลขด้วย FPGA (On the FPGA Realization of Recursive Digital Filter) การวิจัยในด้านนี้อยู่ในขั้นตอนตามที่ได้แสดงไว้ในตารางที่ 1.4.1 ซึ่งเป็นการศึกษาเพื่อสร้างวงจรกรองเชิงเลข (digital filter) บน semi-custom IC ที่มีชื่อเรียกว่า FPGA (Field Programmable Gate Array) โดยให้ใช้เนื้อที่น้อยที่สุด มีความเร็วในการประมวลผลสูง และสามารถลดทอนสัญญาณรบกวนได้ โดยการศึกษาจะเน้นโครงสร้างวงจรกรองแบบเลขคณิตแจกแจง (distributed arithmetic) เป็นหลักเนื่องจากเป็นโครงสร้างแบบที่ไม่ต้องใช้ วงจรคูณ (multiplier) ผลงานวิจัยได้นำเสนอเป็นบทความทางวิชาการในการประชุมวิชาการระดับนานาชาติ 1 บทความ นอกจากนี้ยังได้มีการพัฒนาวิทยุติดตามตัว (paging) ระบบ POGSAG (Post Office Code Standardization Advisory Group) ที่สร้างลงบน FPGA ไว้ด้วย ผลงานนี้ได้เสนอในการประชุมวิชาการระดับชาติ 1 บทความ

การประชุมวิชาการระดับนานาชาติ

1). M.Santawakoop, C.Fongsamut, A.Kantichanakul and W. Surakampontorn, " A Programmable FPGA-based Distributed Arithmetic Digital Filter", *International Symposium on Communication and Information Technology*, September 3-5, Songkhla, Thailand, 2003, Vol.2, pp.813-817. (เอกสารหมายเลข ก.36)

การประชุมวิชาการระดับชาติ

2). อดุลย์ ขันติชนะกุล เฉลิมภัณฑ์ ฟองสมุทร และวัลลภ สุระกำพลธร,"การพัฒนาวิทยุติดตามตัวในระบบ POCSAG โดยใช้เอฟพีจีเอ (On the Implementation of Pocsag Paging Using FPGA)", *การประชุมวิชาการทางวิศวกรรมไฟฟ้า ครั้งที่ 25*, มหาวิทยาลัยสงขลานครินทร์, 21-22 พฤศจิกายน 2545, หน้า 119-123. (เอกสารหมายเลข ก.37)

ตารางที่ 1.4.1

Item	Activity	Year 1		Year 2		Year 3	
		1 - 6	6 - 12	1 - 6	7 - 12	1 - 6	7 - 12
1.4.1	**FPGA Realization of Recursive Digital Filter**						
a.	Literature review	—	—				
b.	Study on the realization of recursive digital filters using FPGAs	—	—	—			
c.	Filter simulation using ASIC design tool and evaluate the filter performance using XACT or MAX-plus II			—			
d.	Go back to step b and develop the filter until get the filter with expectable response				—		
e.	Implement the FPGA-based filter using FPGA chip such as Xilinx XC3000				—		—
f.	Work out for the circuit characteristic and applications				—		—
g.	Prepare for the report and publication				—	—	—

1.4.2 การสร้างวงจรแปลงสัญญาณอนาลอกเป็นดิจิตอลด้วยไอซีแบบวีแอลเอสไอ (VLSI Implemen -tation of Logarithmic A/D Converter) หัวข้อย่อยการวิจัยนี้ไม่ได้มีการดำเนินการ เนื่องจากไม่สามารถหานักวิจัยที่สนใจงานวิจัยด้านนี้ได้

2. ผลงาน

2.1 นักวิจัยของโครงการ

ตารางที่ 2.1

ที่	นักวิจัยของโครงการ		ปีที่ 1		ปีที่ 2		ปีที่ 3	
	ผู้วิจัย	นักวิจัยเต็มโครงการ	1-6	7-12	1-6	7-12	1-6	7-12
1.	หัวหน้าโครงการ	1	1	1	1	1	1	1
2.	นักวิจัย	3	3	3	3	3	3	3
3.	นักศึกษาปริญญาเอก	5	2	3	3	5	4	4
4.	นักศึกษาปริญญาโท	5	3	4	3	1	3	2
5.	ผู้ช่วยนักวิจัย	1	1	1	1	1	1	1
6.	เจ้าหน้าที่ธุรการ/เลขานุการ	1	1	1	1	1	1	1
	รวม	16	11	13	12	12	13	14

หมายเหตุ : มีนักศึกษาระดับปริญญาเอกของโครงการ RTA/04/2543 ลาออก เนื่องจากได้รับทุนอุดหนุนการศึกษาและวิจัยจากโครงการปริญญาเอกกาญจนาภิเษก สำนักงานกองทุนสนับสนุนการวิจัย จำนวน 2 ราย คือ

1. นายอมร จิรเสรีอมรกุล นักศึกษาระดับปริญญาเอก สาขาวิศวกรรมไฟฟ้า ลาออกเมื่อ 31 พฤษภาคม 2545
2. นายเฉลิมภัณฑ์ ฟองสมุทร นักศึกษาระดับปริญญาเอก สาขาวิศวกรรมไฟฟ้า ลาออกเมื่อ 31 พฤษภาคม 2545

: มีการรับนักศึกษาระดับปริญญาเอก 1 ราย และนักศึกษาระดับปริญญาโท 1 ราย เข้าร่วมในโครงการ คือ

1. นายชัยวัฒน์ จงกุลสถิตชัย นักศึกษาระดับปริญญาเอก สาขาวิศวกรรมไฟฟ้า เมื่อ 16 สิงหาคม 2545
2. น.ส.ภัทรา เพียรชอบ นักศึกษาระดับปริญญาโท สาขาวิศวกรรมอิเล็กทรอนิกส์ เมื่อ 16 สิงหาคม 2545

2.2 ปัจจุบันมีผลงานจากการดำเนินการวิจัย ที่สามารถสรุปดังได้แสดงไว้ใน ตารางที่ 2.2 คือ

ตารางที่ 2.2

	ผลงาน	ปีที่ 1		ปีที่ 2		ปีที่ 3		รวม
1.	ผลงานพิมพ์ในวารสารวิชาการนานาชาติ	-	-	-	-	-	2	2
2.	ผลงานในการประชุมวิชาการนานาชาติ IEEE Xplore	2	1	-	2	-	3	8
3.	ผลงานเสนอในการประชุมวิชาการนานาชาติ	-	4	8	8	-	5	25
4.	ผลงานพิมพ์ในวารสารวิชาการระดับชาติ	-	1	-	-	-	1	2
5.	ผลงานเสนอในการประชุมวิชาการนานาชาติ	-	-	-	-	-	1	1
6.	จำนวนหนังสือ	-	-	-	-	-	-	-
7.	จำนวนผลงานการจดสิทธิบัตร	-	-	-	-	-	-	-
8.	จำนวนนักวิจัยรุ่นใหม่ที่สร้างจากโครงการ							
	7.1 สถาบันเดียวกัน	-	2	-	1	2	1	6
	7.2 ต่างสถาบัน	-	-	-	-	-	1	1
9.	นักวิจัย/นักศึกษาจบการศึกษาระดับปริญญาเอก	-	-	-	1	-	1	2

	ผลงาน	ปีที่ 1		ปีที่ 2		ปีที่ 3		รวม
10.	จำนวนนักศึกษาระดับปริญญาโท	-	-	2	1	2	-	5
11.	ผลงานอยู่ระหว่างการพิจารณาของวารสารนานาชาติ	-	-	-	-	-	7	7
12.	วงจรรวมต้นแบบที่อยู่ในระหว่างจัดสร้าง	-	-	-	-	-	5	5

หมายเหตุ : (ก) มีนักศึกษาจบการศึกษาระดับปริญญาโท ภายใต้การสนับสนุนของโครงการคือ

1. นายอมร จิรเสรีอมรกุล วิทยานิพนธ์เรื่อง "การออกแบบและการประยุกต์ใช้งานวงจรนูลเลอร์สี่ขั้วแบบลอยตัวที่มีโครงสร้างแบบทรานส์ลิเนียร์" วิทยานิพนธ์ปริญญาวิศวกรรมศาสตรมหาบัณฑิต, สาขาวิศวกรรมไฟฟ้า, สถาบันเทคโนโลยีพระจอมเกล้าเจ้าคุณทหารลาดกระบัง, พ.ศ.2543.
2. นางสาวพัชราภรณ์ นิปัทธหัตถพงศ์ วิทยานิพนธ์เรื่อง "วงจรทวีความถี่ 3 เท่าโดยใช้ OTA ที่มีการชดเชยผลของอุณหภูมิ" วิทยานิพนธ์ปริญญาวิศวกรรมศาสตรมหาบัณฑิต, สาขาวิศวกรรมไฟฟ้า, สถาบันเทคโนโลยีพระจอมเกล้าเจ้าคุณทหารลาดกระบัง, พ.ศ.2544.
3. นางสาวเกษสุดา กล้าหาญ วิทยานิพนธ์เรื่อง "การออกแบบวงจรดิฟเฟอเรนทิเอเตอร์และวงจรอินทิเกรเตอร์โดยใช้อุปกรณ์แอคทีฟออปแอมป์และโอทีเอเป็นอุปกรณ์หลักและการประยุกต์ใช้งาน" วุฒิปริญญาโท วิศวกรรมศาสตรมหาบัณฑิต, สาขาอิเล็กทรอนิกส์, สถาบันเทคโนโลยีพระจอมเกล้าเจ้าคุณทหารลาดกระบัง, พ.ศ.2545.
4. นางสาวขนิษฐา แก้วแดง วิทยานิพนธ์เรื่อง "การออกแบบวงจรแปลงสัญญาณ RMS เป็นสัญญาณไฟฟ้ากระแสตรงแบบเทคโนโลยีซีมอสที่มีการประยุกต์ใช้วงจรคูณค่าตัวเก็บประจุ" วุฒิปริญญาโท วิศวกรรมศาสตรมหาบัณฑิต, สาขาอิเล็กทรอนิกส์, สถาบันเทคโนโลยีพระจอมเกล้าเจ้าคุณทหารลาดกระบัง, พ.ศ.2545.
5. นายอดุลย์ ขันติชนะกุล วิทยานิพนธ์เรื่อง "การพัฒนาตัวถอดรหัสในระบบ POCSAG สำหรับวิทยุติดตามตัวโดยใช้ FPGA" วุฒิปริญญาโท วิศวกรรมศาสตรมหาบัณฑิต, สาขาอิเล็กทรอนิกส์, สถาบันเทคโนโลยีพระจอมเกล้าเจ้าคุณทหารลาดกระบัง, พ.ศ.2546.

(ข) มีนักวิจัยภายใต้ทุนสนับสนุนบางส่วนจากโครงการ จบการศึกษาระดับปริญญาเอก คือ

1. นายคงศักดิ์ อนันตหิรัญรัตน์ วิทยานิพนธ์เรื่อง "วงจรฟังก์ชันอนาลอกชนิดทรานลิเนียร์คลาส AB" วุฒิปริญญาเอก วิศวกรรมศาสตรดุษฎีบัณฑิต, สาขาวิศวกรรมไฟฟ้า, สถาบันเทคโนโลยีพระจอมเกล้าเจ้าคุณทหารลาดกระบัง, พ.ศ.2545.
2. นายวรพงศ์ ตั้งศรีรัตน์ วิทยานิพนธ์เรื่อง "บล็อกวงจรรวมแอคทีฟสำหรับการสังเคราะห์อนาลอกฟังก์ชันเชิงระบบทำงานในโหมดกระแส" วุฒิปริญญาเอก วิศวกรรมศาสตรดุษฎีบัณฑิต, สาขาวิศวกรรมไฟฟ้า, สถาบันเทคโนโลยีพระจอมเกล้าเจ้าคุณทหารลาดกระบัง, พ.ศ.2545.

2.3 บทความวิจัยที่เสนอในบทความวิจัยและการประชุมวิชาการระดับนานาชาติและในประเทศ ในช่วงวันที่ 15 สิงหาคม 2543 ถึงวันที่ 14 สิงหาคม 2546 จำนวน 37 บทความ ดังนี้ คือ

2.3.1 <u>วารสารวิชาการระดับนานาชาติ</u>

1) W. Tangsrirat, W. Surakampontorn and N. Fujii, "Realization of Leapfrog Filters Using Current Differential Buffered Amplifiers", *The IEICE Trans on Fundamental, Special Section on Analog Circuits and Related Topics,* February 2003, Vol. E 86-A, No.2, pp.318-326. (เอกสารหมายเลข ก.1)

2.3.2 <u>วารสารระดับชาติ</u>

1) I. Seedadan and W. Surakampontorn and B. Srisuchinwong "A Fully Balanced Widde-Frequency Current-Tunable Phase-Lead All-Pass Filter ", *KMUTT Research and Development Journal,* Vol. 24, No. 1, January-April 2001, pp. 31-41. (เอกสารหมายเลข ก.2)

2) K. Klahan, W. Tangsrirat, W. Surakampontorn and T. Dumawipata "Current-Mode Integrator Using OA and OTAs and Its Applications", *Thammasat International Journal on Science and Technology*, Vol.8, No. 2, 2003, pp. 26-32. (เอกสารหมายเลข ก.3)

2.3.3 <u>การประชุมวิชาการระดับนานาชาติที่อยู่ในฐานข้อมูล IEEE Xplore</u>

1) W. Tangsrirat, S. Unhavanich, T. Dumawipata and W. Surakampontorn, "A Realization of Current-Mode Biquadratic Filters Using Multiple-Output FTFNs," *Proc. 2000 IEEE Asia Pacific Conference on Circuits and Systems*, Tianjin, China, Dec. 4-6, 2000. , pp. 571-574 (เอกสารหมายเลข ก.4)

2) K. Anuntahirunrat, W. Tangsrirat, V.Riewruja and W. Surakampontorn, "Sinusoidal Frequency Doubler and Full-Wave Rectifier Using Translinear Current Controlled Conveyor," *Proc. 2000 IEEE Asia Pacific Conference on Circuits and Systems*, Tianjin, China, pp. 166-169, Dec. 4-6, 2000. (เอกสารหมายเลข ก.5)

3). A. Jiraseri-amornkun, B. Chipipop and W. Surakampontorn, "Novel Translinear-Based Multi-Output FTFN," *Proc. 2001 IEEE International Symposium on Circuits and Systems*, Sydney, Australia, May 6-9, 2001. , pp.180-183. (เอกสารหมายเลข ก.6)

4) W. Tangsrirat, N. Fujii and W. Surakampontorn," Current-Mode Leapfrog Ladder Filters Using CDBAs", *The 2002 IEEE International Symposium on Circuits and Systems*, May 26-29, USA, 2002, vol.5 , pp.V-57 -V-60. (เอกสารหมายเลข ก.7)

5) W. Tangsrirat, S. Unhavanich, T. Dumawipata and W. Surakampontorn, "Single-Input and Three-Output Current-Mode Biquadratic Filters Using Multiple output OMAs", *Asia Pacific Conference on Circuits and System 2002,* Indonesia, October 28-31, 2002., pp.399-404. (เอกสารหมายเลข ก.8)

6) K. Kaewdang, C. Fongsamut and W. Surakampontorn, "A Wide-Band Current-Mode OTA-Based Analog Multiplier-Divider", *The 2003 IEEE International Symposium on Circuits and Systems,* Thailand, May 25-28, 2003, pp.349-352. (เอกสารหมายเลข ก.9)

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3. ความเห็นของผู้วิจัย

3.1 ความก้าวหน้าของงานวิจัยในส่วนที่นำเสนอไว้

(ก) จากรายงานผลการดำเนินการวิจัยในหัวข้อ 2 จะเห็นว่าโครงการวิจัยย่อยที่เสนอไว้ มีความก้าวหน้า มีแนวคิดในการพัฒนาและออกแบบงานวิจัยมีแนวโน้มที่ดี อย่างไรก็ตามงานวิจัยเหล่านี้จำเป็นต้องมีการพัฒนา ปรับปรุง เพิ่มเติม วิเคราะห์ และสรุปรวม เพื่อเสนอเป็นบทความวิจัยที่พิมพ์เผยแพร่ในวารสารระดับนานาชาติที่มี impact factor ให้ได้ ซึ่งจนถึงปัจจุบันได้รับการตอบรับให้ตีพิมพ์เผยแพร่ในวารสารวิจัยระดับนานาชาติ 1 บทความ และเผยแพร่ในการประชุมวิชาการนานาชาติที่อยู่ในฐานข้อมูล IEEE Xplore 8 บทความ

(ข) นอกจากนี้ยังเน้นการพัฒนาให้นักวิจัยมีความสามารถในการออกแบบเป็นวงจรไอซีต้นแบบได้ด้วย ซึ่งเป็นงานใหม่ที่โครงการยังไม่เคยมีประสบการณ์มาก่อน จึงต้องใช้เวลาในการเรียนรู้มาก อย่างไรก็ตามในที่สุดทางโครงการสามารถที่จะออกแบบวงจรรวมต้นแบบและอยู่ในระหว่างการจัดสร้างถึง 5 วงจร ซึ่งวงจรรวมต้นแบบนี้ถ้าหากไม่มีข้อผิดพลาดใดๆก็จะใช้เป็นอุปกรณ์สำหรับการวิจัยและพัฒนาต่อไป

3.2 นักศึกษาของโครงการวิจัย เนื่องจากงานวิจัยในสาขาวิชานี้ มีนักศึกษาและมีการเรียนการสอนในระดับปริญญาตรีตามมหาวิทยาลัยหรือสถาบันทั่วไปอยู่น้อยมาก ดังนั้นนักวิจัยและนักศึกษาของโครงการจึงเสมือนกับเป็นการเริ่มต้นงานวิจัยใหม่ จึงต้องการการเรียนรู้ที่เกี่ยวข้องกับการวิจัยอยู่มาก โดยเฉพาะแนวความคิดในการพัฒนาและออกแบบวงจรใหม่ ๆ นอกจากนี้ยังจำเป็นต้องมีกระบวนการฝึกการเขียนบทความทางวิชาการด้วย อย่างไรก็ตามเมื่อสิ้นสุดโครงการ นักวิจัยเหล่านี้ได้เข้าศึกษาในระดับปริญญาเอก หรือจบการศึกษาระดับปริญญาเอกโดยมีผลงานที่มีคุณภาพสูงได้

3.3 การสามารถเข้าร่วมประชุมวิชาการระดับนานาชาติ จากการที่ได้รับการสนับสนุนจากทาง สกว. และทางโครงการเห็นความสำคัญได้จัดให้มีงบประมาณสำหรับการเข้าร่วมประชุมและเสนอผลงานวิจัยด้วยนั้น ทำให้นักวิจัยได้มีโอกาสแลกเปลี่ยนประสบการณ์การวิจัยกับนักวิจัยจากนานาชาติ และเกิดความมั่นใจในงานวิจัยที่ดำเนินการอยู่ ทั้งยังได้พบปะกับนักวิจัยที่มีความเชี่ยวชาญ ทำให้งานวิจัยมีความก้าวหน้ามากยิ่งขึ้น ซึ่งตามที่ได้เขียนไว้ในรายงานแล้วว่า มีผลงานวิจัยที่ได้รับการยอมรับให้นำเสนอในวารสารระดับนานาชาติ *The 2002 IEICE Transactions on Fundamentals of Electronics Communications and Computer Sciences* และการประชุมวิชาการระดับนานาชาติ *2003 IEEE International Symposium on Circuits and Systems* ซึ่งเป็นการประชุมวิชาการที่สำคัญทางด้านวิศวกรรมไฟฟ้า และมีนักวิจัยเสนอผลงานวิจัยจำนวนมาก และมีการตรวจคัดงานวิจัยอย่างเคร่งครัด และนอกจากนี้ยังมีผลงานที่ได้รับการยอมรับให้ตีพิมพ์ในวารสารวิชาการ *International Journals of Electronics (IJE)* อีกด้วย

4. ภาคผนวก

4.1 ภาคผนวก ก บทความวิจัยในวารสารและในการประชุมวิชาการ

4.2 ภาคผนวก ข บทความวิจัยที่ได้รับการยอมรับให้ตีพิมพ์ในวารสารวิชาการ

4.3 ภาคผนวก ค บทความวิจัยที่อยู่ในระหว่างการพิจารณา

4.4 ภาคผนวก ง วงจรรวมต้นแบบที่อยู่ในระหว่างจัดสร้าง

4.5 ภาคผนวก จ สรุปการประชุมประจำปี

4.6 ภาคผนวก ฉ ข้อมูลและประวัติย่อของผู้ได้รับทุนวิจัยระดับปริญญาโท/เอก จากโครงการ

(ศาสตราจารย์ ดร.วัลลภ สุระกำพลธร)

หัวหน้าโครงการ

ภาคผนวก

ภาคผนวก ก

บทความวิจัยในวารสารและในการประชุมวิชาการ

เอกสารหมายเลข ก.1

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CONTENTS

PAPER *Special Section on Analog Circuit Techniques and Related Topics*

Realization of Leapfrog Filters Using Current Differential Buffered Amplifiers

Worapong TANGSRIRAT[†a)], *Nonmember*, Wanlop SURAKAMPONTORN[†], *Regular Member*, *and* Nobuo FUJII[††b)], *Fellow*

SUMMARY In this paper, is shown an approach to realize leapfrog structures obtained from proto-type passive RLC ladder filters using current differencing buffered amplifiers (CDBA) as active elements. The use of the CDBA's provides advantages that the realization procedure is simplified and the number of active components required is reduced. The approach is quite suitable for the realization of band-pass ladder filters, which generally requires a complicated structure to simulate LC series and/or parallel resonant branches by the conventional opamp-based leapfrog filters. A simple circuit configuration of the CDBA suitable for high frequency and low power supply voltage applications is also presented. As design examples, a fifth-order Butterworth low-pass ladder filter and a sixth-order Chebyshev bandpass ladder filter are designed. The effectiveness and the correctness of the proposed approach and the characteristics of the proposed filters are verified and examined through computer simulation.

key words: current differencing buffered amplifier, CDBA, low-voltage circuit, leapfrog filter, active filter

1. Introduction

Recent advanced technologies of integrated circuits make devices in an IC so small that the internal electric field may become extremely high, thus the power supply voltage of circuits must be restricted to a low value. In addition, with the popularization of portable equipments, single battery operation of equipments is now most essential. High frequency operation of circuits is also a key word today. In these respects, realization of low-voltage high-frequency active filters is one of the most attractive and important issues in many signal processing fields.

Active RC filter is one of the candidates of filters that may have possibilities of integration and high frequency and low voltage operation. Leapfrog structure that simulates doubly terminated LC filters has been highly appreciated since it inherits the low sensitivity natures of the proto-type LC filters [1]. Active RC filters including the leapfrog filters require active building blocks such as operational amplifiers, transconductance amplifies, etc. From the view points of high frequency and low voltage application of the filters, low gain amplifiers such as unity gain voltage buffer and unity gain current buffer would be the most reasonable active blocks that could have a wide gain bandwidth and operate at a low power supply voltage. Current conveyor (CC) is a building block that only consists of a unity gain current buffer and a unity gain voltage buffer and many realization of active filters using CC's have been proposed [2], [3].

Recently, a new active building block, current differencing buffered amplifier (CDBA), has been proposed [4], [5]. The CDBA is a kind of extended CC and composed of a unity gain current differential amplifier and a unity gain voltage buffer. Acar and Ozoguz showed a realization of filters using the CDBAs that is based on the signal flow graph representation of transfer functions [6]. As this method only realizes the given transfer function, the filters have no direct relation to low sensitivity LCR filters, thus the sensitivity may not be necessarily low.

In this paper, an extension of the method to the leapfrog simulation is shown. Using the CDBA's, the signal flow graph of leapfrog filters can be simply realized and each element of the proposed filters corresponds to an element of the prototype LCR filters one by one, thus the low sensitivity nature can be guaranteed. Especially, the structure is quite suitable for the realization of bandpass filters that generally require a complicated feedback and feedforward paths and one by one correspondence between the elements will not be guaranteed by the conventional leapfrog realizations. Together with the filter realization, a bipolar transistor realization of the CDBA is also presented. The circuit can operate at a low power supply voltage of 2.0 V and has a wide frequency bandwidth of over hundreds MHz. As design examples, a 5th order lowpass and a 6th order bandpass filters are simulated by SPICE to show the availability of the realization.

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2. CDBA-Based Leapfrog Structure

2.1 Leapfrog Realization of Ladder Structures by CDBA's

Figure 1(a) shows the symbol of the CDBA, which has four terminals. The current and voltage relations between these terminals are defined by [4],

$$v_p = 0, \quad v_n = 0, \quad i_z = i_p - i_n \quad \text{and} \quad v_w = v_z \qquad (1)$$

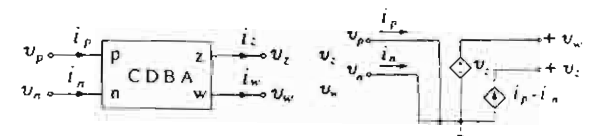
From Eq. (1), we can obtain the equivalent representation of the CDBA shown in Fig. 1(b) that consists of a unity gain differential current amplifier and a unity gain voltage buffer. It must be noted that the input impedances of the terminals p and n are zero. The differential input current $i_p - i_n$ is converted to the output voltage v_w through an impedance connected at the terminal z. A realization of a wide band and low voltage CDBA will be presented in Sect. 3.

To illustrate the leapfrog realization based on the CDBA, let us consider the ladder structure circuit of Fig. 2. Here we concentrate the discussion on the realization of doubly terminated LC filters and thus two resistors, R_S and R_L, are connected at the input and output terminals, however, these two elements can be arbitrary for general cases. This structure is characterized by the following expressions:

$$\begin{aligned} I_1 &= I_S - \frac{V_1}{R_S} - I_2, \\ V_1 &= Z_1 I_1, \\ I_2 &= Y_2(V_1 - V_3), \\ V_3 &= Z_3(I_2 - I_4), \\ I_{2n} &= Y_{2n}(V_{2n-1} - V_{2n+1}), \\ &\vdots \end{aligned}$$

and

$$V_{2n+1} = Z_{2n+1}(I_{2n} - I_o). \qquad (2)$$



(a) (b)

Fig. 1 (a) Symbolof CDBA. (b) Equivalent circuit of CDBA

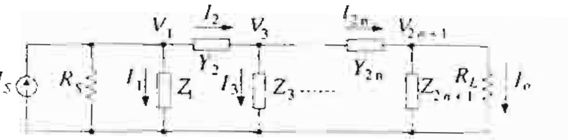


Fig. 2 Doubly terminated ladder network.

where Z_i and Y_i are the impedance and admittance of the elements, respectively.

Using the above expressions, the current and voltage relations of the ladder network can be represented by a block diagram shown in Fig. 3. Figure 3 indicates that the circuit repeatedly uses two basic structures shown in Figs. 4(a) and 4(c). Using the current and voltage relations of the CDBA given by Eq. (1), we easily find that these two basic structures can be realized using CDBA by the circuits shown Figs. 4(b) and 4(d), respectively, where R is a resistor having an arbitrary value.

To illustrate the method, a fifth-order LC ladder low-pass filter shown in Fig. 5 is employed as an example. The resulting CDBA-RC structure of the filter is shown in Fig. 6, where $C_{Li} = L_i/R^2$. The inductors in the prototype LCR filter are converted to capacitors through the CDBA of Fig. 4(d).

2.2 Effects Caused by Non-ideal Characteristics of CDBA

There are some non-ideal characteristics in the parameters of CDBA. One of them is the gain of amplifiers. CDBA consists of a current differential amplifier and a

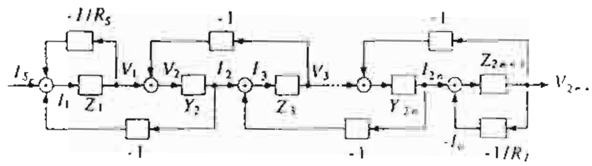


Fig. 3 Block diagram representation of leapfrog structure.

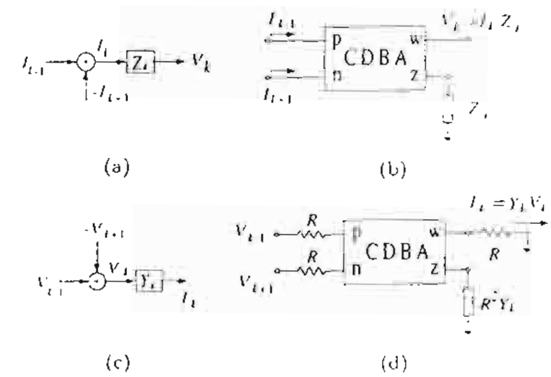


Fig. 4 Sub-circuits and their realization using CDBAs.

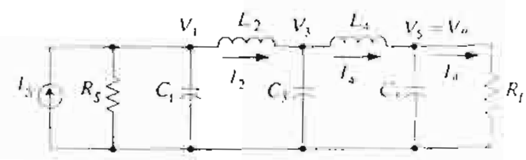


Fig. 5 Fifth-order LC ladder lowpass filter

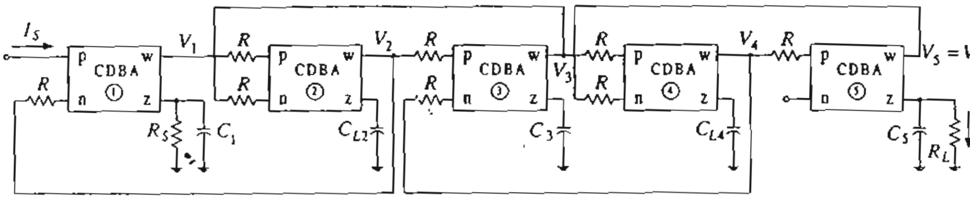


Fig. 6 CDBA-based leapfrog realization of Fig. 5.

voltage buffer which should have unity gain. However, in general case, the gain is not necessarily unity due to parasitic elements and non-ideal characteristics of active devices. If the gain is not unity, the output current and voltage of CDBA are written as,

$$i_z = k_i(i_p - i_n) \tag{3}$$

and

$$v_w = k_v v_z, \tag{4}$$

where k_i and k_v are the gains of the current differential buffer and the voltage buffer, respectively. Substituting Eqs. (3) and (4) into the output current and voltage of Fig. 4, we can easily find that the gain errors of k_i and k_v change the values of Z_i or Y_i, which correspond to the change of element values of the filter. Since the change in the reactance values of doubly terminated LCR filters will not much affect the filter characteristics in the passband, the errors of the gains will not be a serious problem.

Another non-ideal effects should be resulted from the errors of the value R in Fig. 4(d). The errors of the conversion factor R^2 of the impedance R^2Y_k at the terminal z and the value of the resistor R connected to the terminal w lead to a change of the value of the inductor in the prototype LCR filters, thus the effects caused by these errors would be small in the passband. However, the matching between the two resistors in the input terminals p and n must be accurate enough.

The input impedances at the terminal p and n can be included in the resistors R connected in series to the terminals. The output impedances at the terminal w and z become a loss of the impedances connected to the terminals, thus the output impedance of the terminal w must be small enough and that of z must be large enough compared to the impedances connected to the terminals.

2.3 Bandpass Filter Realization

In this section, the proposed technique will be extended to realize LC bandpass filters. In the case of bandpass filters, parallel and series LC resonant branches are fundamental as shown in Fig. 7. We cannot directly apply the structures of Fig. 4 to these braches, since the elements connected to the terminal z may not be realized without inductors. The parallel and series resonant branches of Figs. 8(a) and 8(c) are characterized by the following equations:

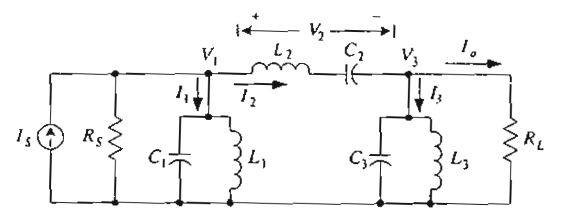


Fig. 7 Sixth-order LC ladder bandpass filter.

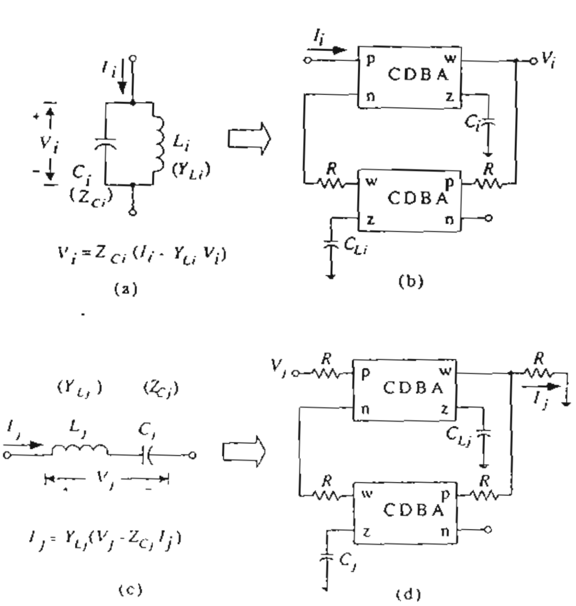


Fig. 8 Realization of resonant branches by CDBAs.

$$V_i = Z_{Ci}(I_i - Y_{Li}V_i) = \frac{1}{sC_i}\left(I_i - \frac{V_i}{sL_i}\right) \tag{5}$$
$$i = 1, 3, 5, \cdots, 2n+1$$

$$I_j = Y_{Lj}(V_j - Z_{Cj}I_j) = \frac{1}{sL_j}\left(V_j - \frac{I_j}{sC_j}\right) \tag{6}$$
$$j = 2, 4, 6, \cdots, 2n.$$

The second terms in the parenthesis must be converted again using an additional CDBA as shown in Figs. 8(b) and 8(d). Thus, the doubly terminated LC bandpass filter of Fig. 7 can be simulated as shown in Fig. 9 using Figs. 8(b) and 8(d). The proposed method is quite suitable for the realization of bandpass filters. All the elements of the filter correspond to the elements of the

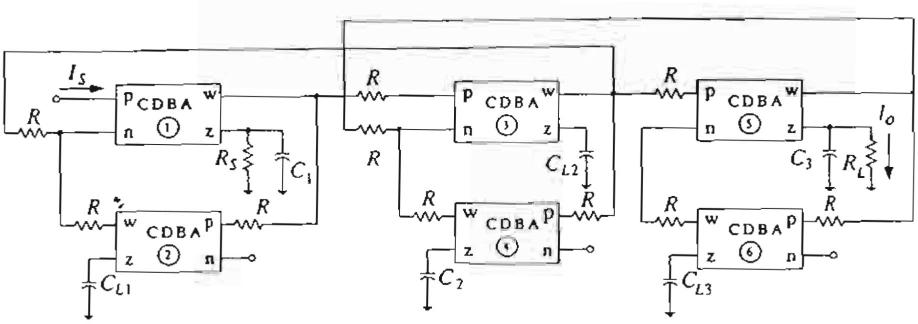


Fig. 9 The sixth-order bandpass filter using CDBAs.

prototype LC filter, thus we can expect low sensitivity natures in the passband.

3. Realization of Low-Voltage Wide-Bandwidth CDBA

In this section, is discussed a realization of the CDBA using bipolar transistors that has a wide frequency bandwidth and can operate at a low power supply voltage. CDBA basically consists of two building blocks; a unity gain current differential amplifier (unity gain current subtractor) and a voltage follower.

3.1 Low-Input Impedance Current Subtractor

Figure 10 shows a low-input resistance input stage of the current subtractor [7], where V_{B1} and I_{B1} are the bias voltage and current, respectively. Assuming that all transistors have a same size and ignoring the base current, we obtain the following relations;

$$i_{in} = i_e + \beta_2 i_e, \tag{7}$$

and

$$v_{in} = r_{e1} i_e. \tag{8}$$

where β_2 is the current gain of the transistor Q_2. From these relations, we obtain the input impedance given by,

$$r_{in} = \frac{v_{in}}{i_{in}} \cong \frac{r_{e1}}{\beta_2}. \tag{9}$$

where r_{e1} is the small signal emitter resistance which is given by $r_{e1} = \frac{V_T}{I_{B1}}$ and V_T is the thermal voltage. Equation (9) shows that the circuit has a low input impedance.

The unity gain current amplifier based on the above input stage is shown in Fig. 11. A biasing circuit composed of the transistor Q_6 and the bias current source I_{B2} are added to provide the bias voltage V_{B1}. The current mirror transistors Q_3 and Q_5 provide the output current i_{out} which is given by,

$$i_{out} = -\beta_2 i_e = -\frac{\beta_2}{\beta_2 + 1} i_{in} \cong -i_{in} \tag{10}$$

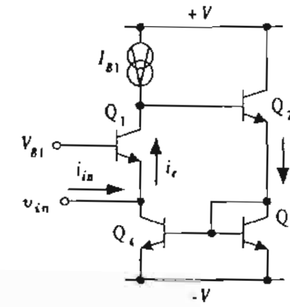


Fig. 10 Low-input resistance input stage.

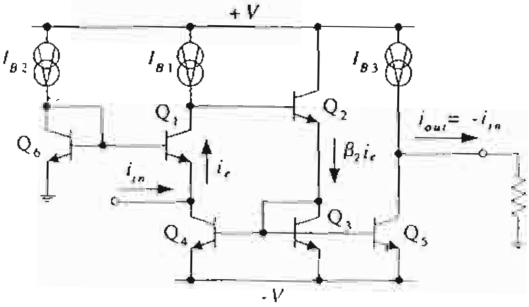


Fig. 11 Unity gain current amplifier.

Figure 12 shows the current subtractor circuit, which consists of two unity gain current amplifiers:$Q_1 - Q_5$ and $Q_7 - Q_{11}$, and a current mirror of Q_{12} and Q_{13} that provides the output with a difference of the two output currents of the current amplifiers. Thus the output current of the circuit can now be expressed as

$$i_{out} = i_p - i_n. \tag{11}$$

3.2 Voltage Buffer

The high-input impedance voltage buffer based on a simple emitter follower is presented in Fig. 13, where a complementary pair of two-stage emitter follower is utilized to maintain a high input impedance. The input impedance at the terminal z is approximately given by,

$$r_z \cong \beta_n \beta_p \left(\frac{r_e}{2} + R_w\right). \tag{12}$$

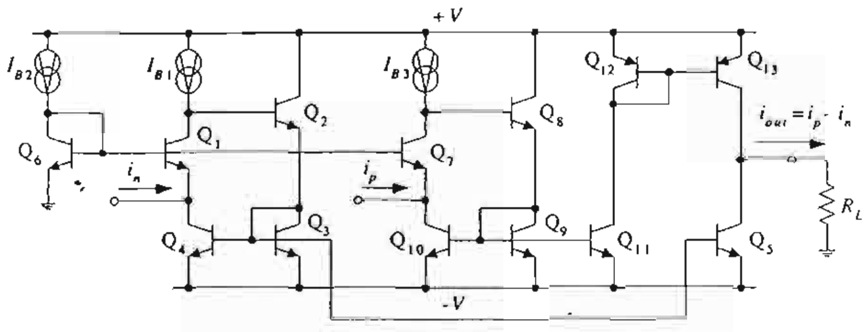


Fig. 12 Current subtractor.

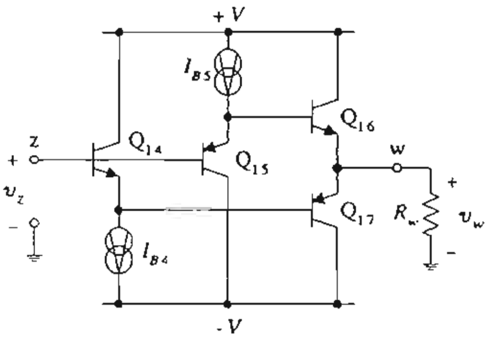


Fig. 13 Unity gain voltage amplifier.

where $\beta_n = \beta_{14} \cong \beta_{16} \gg 1.0$, $\beta_p = \beta_{15} \cong \beta_{17} \gg 1.0$, $r_e = r_{e14} = r_{e15} \cong r_{e16} = r_{e17}$, and R_w is a load resistance connected to the terminal w. The output impedance at the terminal w is low and given by

$$r_w \cong \frac{r_e}{2} + \frac{R_z}{\beta_n \beta_p}. \tag{13}$$

where R_z is a converting resistor connected to the terminal z. For example, if $R_z = 1\,\mathrm{k}\Omega$, $R_w = 10\,\mathrm{k}\Omega$, V_T $26\,\mathrm{mV}$, $I_{B4} = I_{B5} = 100\,\mu\mathrm{A}$ and $\beta_n = \beta_p = 100$, then r_z and r_w are approximately equal to $10.1\,\mathrm{M}\Omega$ and $130\,\Omega$, respectively.

3.3 Low-Voltage CDBA

The hole circuit of the low-voltage CDBA is shown in Fig. 14, which consists of a current subtractor of Fig. 12 and a voltage buffer of Fig. 13. All bias current sources of the circuit are realized by current mirror circuits and set to be equal to I_B. Since the circuit uses only two transistors and two bias current sources between the positive and the negative supply voltages, this circuit can operate at a low power supply voltage of $2(V_{BE} + V_{CEsat})$, where V_{BE} and V_{CEsat} are the base-emitter voltage and collector-emitter saturation voltage of transistors, respectively.

Assuming all the transistors have the same parameters, the current differential gain of Fig. 14 can be approximately expressed by.

$$\frac{i_z}{i_p - i_n} = \frac{H}{(1 + a_1 s)(1 + a_2 s + a_3 s^2)}, \tag{14}$$

where

$$H = \frac{g_{mp} g_{mn}}{(g_{mp} + 2g_{\pi p})\left[g_{mn}^2 + g_{\pi n}(g_{mn} + g_{\pi n})\right]},$$

$$a_1 = \frac{2C_{\pi p} + C_{\mu p}}{g_{mp} + 2g_{\pi p}},$$

$$a_2 = \frac{(2C_{\pi n}+C_{\mu n})g_{\pi n}+(C_{\pi n}+2C_{\mu n})(g_{mn}+2g_{\pi n})}{g_{mn}(g_{mn}+g_{\pi n})},$$

and

$$a_3 = \frac{(2C_{\pi n} + C_{\mu n})(C_{\pi n} + 2C_{\mu n})}{g_{mn}(g_{mn} + 2g_{\pi n})}. \tag{15}$$

In the above expressions, $g_{mn}(g_{mp})$ and $g_{\pi n}(g_{\pi p})$ denote the transconductance and the conductance between the base and the emitter of npn (pnp) transistors and $C_{\pi n}(C_{\pi p})$ and $C_{\mu n}(C_{\mu p})$ denote the emitter-base and the collector-base capacitances of npn (pnp) transistors, respectively. The denominator of Eq. (14) has three poles and can be expressed as

$$D_1(s) = \left(1 - \frac{s}{p_1}\right)\left[1 - s\left(\frac{1}{p_2} + \frac{1}{p_3}\right) + \frac{s^2}{p_2 p_3}\right] \tag{16}$$

where p_i is the pole of Eq. (14). Usually the poles p_2 and p_3 are widely separated and if we assume $p_3 \gg p_2$, Eq. (16) becomes as

$$D_1(s) \cong \left(1 - \frac{s}{p_1}\right)\left[1 - \frac{s}{p_2} + \frac{s^2}{p_2 p_3}\right]. \tag{17}$$

By equating the coefficients of Eq. (17) with those of Eq. (14), the poles can be obtained as follows:

$$p_1 = -\frac{g_{mp} + 2g_{\pi p}}{2C_{\pi p} + C_{\mu p}}, \tag{18}$$

$$p_2 = \frac{-(g_{mn} + g_{\pi n})}{(2C_{\pi n}+C_{\mu n})\left(\frac{g_{\pi n}}{g_{mn}}\right) + (C_{\pi n} + 2C_{\mu n})\left(1 + \frac{g_{\pi n}}{g_{mn}}\right)}, \tag{19}$$

and

$$p_3 = -\left(\frac{g_{\pi n}}{C_{\pi n} + 2C_{\mu n}} + \frac{g_{mn} + 2g_{\pi n}}{2C_{\pi n} + C_{\mu n}}\right). \tag{20}$$

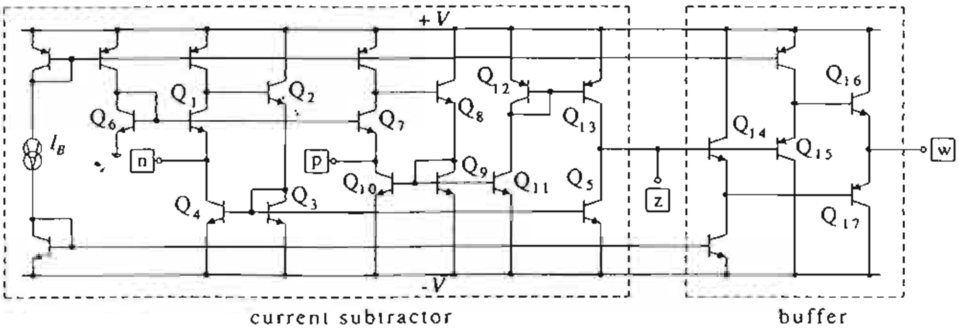


Fig. 14 Circuit diagram of the proposed low-voltage CDBA.

The gain of the voltage buffer with a load of R_w can be approximately given by,

$$\frac{v_w}{v_z} \cong \frac{H\,N(s)}{1+b_1 s+b_2 s^2}, \tag{21}$$

where

$$H = \frac{g_n g_p}{(G_w+g_p)g_n+G_w g_{\pi p})},$$

$$N(s) = \left(1+\frac{C_{\pi n}}{g_n}s\right)\left(1+\frac{C_{\pi p}}{g_p}s\right),$$

$$b_1 = \frac{(G_w+g_p)C_{\pi n}+(G_w+g_n)C_{\pi p}}{(G_w+g_p)g_n+G_w g_{\pi p}},$$

and

$$b_2 = \frac{C_{\pi n}C_{\pi p}}{(G_w+g_p)g_n+G_w g_{\pi p}}.$$

In the above expressions, $g_p = g_{mp}+g_{\pi p}$, $g_n = g_{mn}+g_{\pi n}$, and $G_w = 1/R_w$.

The denominator of Eq. (21) can be rewritten as

$$\begin{aligned} D_2(s) &= 1-s\left(\frac{1}{p_4}+\frac{1}{p_5}\right)+\frac{s^2}{p_4 p_5} \\ &\cong 1-\frac{s}{p_4}+\frac{s^2}{p_4 p_5}, \end{aligned} \tag{22}$$

where we assumed that $p_5 \gg p_4$. The poles p_4 and p_5 can now be obtained by comparing the coefficients of Eqs. (21) and (22). Thus we have:

$$p_4 = -\frac{(G_w+g_p)g_n+G_w g_{\pi p}}{(G_w+g_p)C_{\pi n}+(G_w+g_n)C_{\pi p}} \tag{23}$$

and

$$p_5 = -\left(\frac{G_w+g_n}{C_{\pi n}}+\frac{G_w+g_p}{C_{\pi p}}\right). \tag{24}$$

In order to figure out the high frequency limitation, let us assume that $C_{\pi n} = 8.25\times10^{-14}$ F, $C_{\pi p} = 8.98\times10^{-14}$ F, $C_{\mu n} = 4.14\times10^{-14}$ F, and $C_{\mu p} = 4.22\times10^{-14}$ F. The poles p_3 and p_6 are non-dominant and can be neglected in the calculation. The poles p_1, p_2 and p_4 approximately locate at 1.50, 2.67, and 2.14 GHz, respectively. Thus the high frequency limitation of the circuit is due to the lowest pole p_1 that is determined by the parameters of the pnp transistors consisting of the current mirror, $Q_{12}-Q_{13}$. The pole p_1 locates at a high frequency, though, for higher frequency applications of the filters, these pnp transistors must have smaller parasitic capacitors.

H of Eqs. (14) and (21) gives the DC gain of the amplifiers, and if the transconductances g_{mn} and g_{mp} are not large enough compared with $g_{\pi n}$ and $g_{\pi p}$, there may be errors in the gains of amplifiers. The current gain of current differential amplifier and voltage gain of the buffer at DC are given by,

$$\frac{i_z}{i_p-i_n} = \frac{1}{1+\varepsilon_i}, \tag{25}$$

and

$$\frac{v_w}{v_z} = \frac{1}{1+\varepsilon_v}, \tag{26}$$

where ε_i and ε_v are the gain errors of current and voltage amplifiers, respectively. ε_i and ε_v are derived from Eqs. (14) and (21) as,

$$\varepsilon_i \cong \frac{g_{mp}+2g_{\pi p}}{g_{mp}g_{mn}}\left[g_{mn}+g_{\pi n}\left(1+\frac{2g_{\pi n}}{g_{mn}}\right)\right]-1, \tag{27}$$

and

$$\varepsilon_v \cong \frac{G_w(g_{mn}+g_{\pi n}+g_{\pi p})}{(g_{mn}+g_{\pi n})(g_{mp}+g_{\pi p})}. \tag{28}$$

When 0.7 μm BiCMOS process parameters are employed under the bias current $I_B = 100\,\mu$A, $g_{mn} = 2.23\times10^{-3}$ A/V, $g_{mp} = 2.14\times10^{-3}$ A/V, $g_{\pi n} = 4.17\times10^{-5}$ A/V and $g_{\pi p} = 4.38\times10^{-5}$ A/V. ε_i of about 6.12% is expected and ε_v under a load resistance R_w of 10 kΩ is approximately 4.65%. As mentioned in 2.2, these errors directly affect the values of capacitances of the filter, however, the change of transfer characteristics in the passband remains small due to the low sensitivity nature of the prototype doubly terminated LCR filters.

The performances of the CDBA of Fig. 14 were simulated using PSPICE with 0.7 μm BiCMOS process

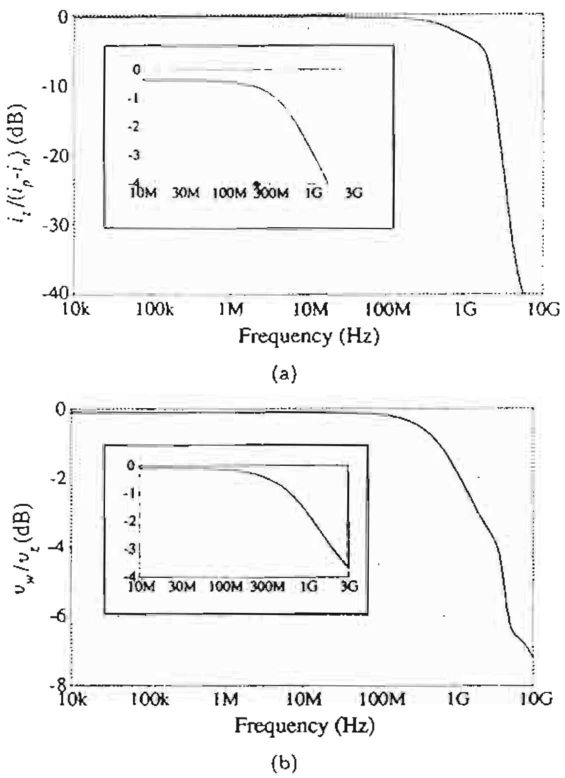


Fig. 15 Frequency responses of the gains of CDBA. (a) Current gain, (b) voltage gain.

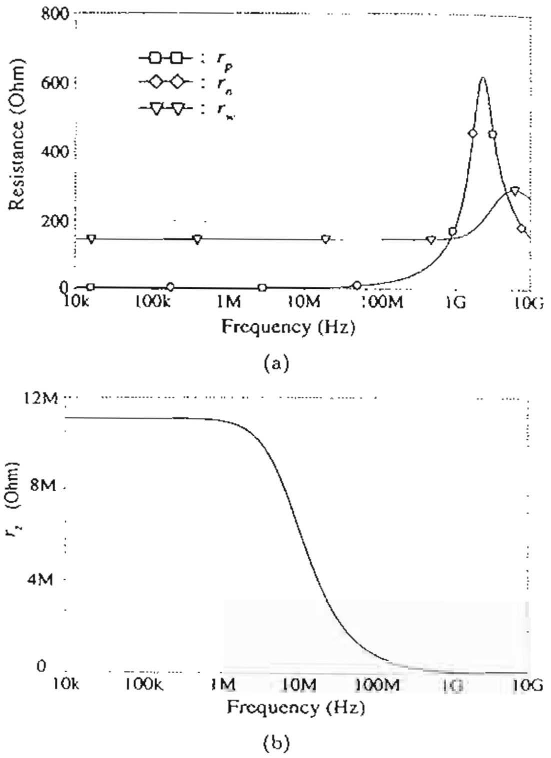


Fig. 16 Frequency characteristics of impedances of ports. (a) r_p, r_n, and r_w, (b) r_z.

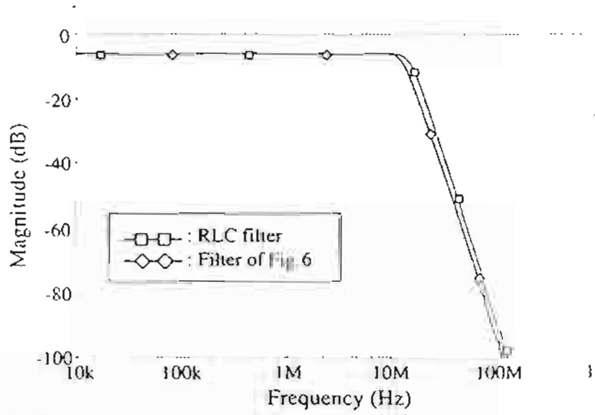


Fig. 17 Frequency responses of the fifth-order lowpass filter.

parameters. The power supply voltage is ±1 V and the bias current I_B is 100 μA. Figure 15 shows the simulated gain-frequency characteristics of the CDBA. It is clearly seen from the figures that the gain bandwidth is wide and reaches around 1 GHz. The frequency dependencies of the impedances r_p, r_n, and r_z at the terminals p, n, and z are shown in Fig. 16. The impedances begin to change at about 1 MHz, however, they still have satisfactorily good values at the frequencies of 100 MHz. The DC offset current at the port z with a load of $R_z = 1\,\mathrm{k\Omega}$ was 3.23 μA and the DC offset voltage at the terminal w with a load of $R_w = 10\,\mathrm{k\Omega}$ was 1.98 mV. The total power consumption was 1.84 mW.

4. Design Examples and Computer Simulation

To illustrate the effectiveness of the method, two examples, 5th order lowpass and 6th order bandpass filters were designed using the CDBA's. The CDBA-based filter of Fig. 6 that simulates the 5th order filter shown in Fig. 5 was designed at the −3 dB frequency of $\omega_{-3\,\mathrm{dB}} = 100$ Mrad/s (15.9 MHz). Selecting $R_S = R_L = R = 1\,\mathrm{k\Omega}$, we obtain the passive element values as: $C_1 = C_5 = 6.18$ pF, $C_{L2} = C_{L4} = 16.18$ pF, and $C_3 = 20$ pF. The simulated responses of the filter are shown in Fig. 17.

Sixth-order Chebyshev bandpass filter of Fig. 9 was also designed to have the center frequency of 100 Mrad/s (15.9 MHz), the bandwidth ratio of 0.45, and the passband ripple of 0.1 dB. Selecting $R_S = R_L = R = 1\,\mathrm{k\Omega}$, we obtain; $C_1 = C_3 = 22.9$ pF, $C_2 = 3.92$ pF, $C_{L1} = C_{L3} = 4.36$ pF, and $C_{L2} = 25.5$ pF. The simulated responses of the bandpass filter together with the prototype LCR filter responses are shown in Fig. 18.

Both simulation results reveal that the frequency of the filters shifts about 10%. This is resulted from the errors of the amplifier gains that change the values of capacitances of the filters. The capacitance value

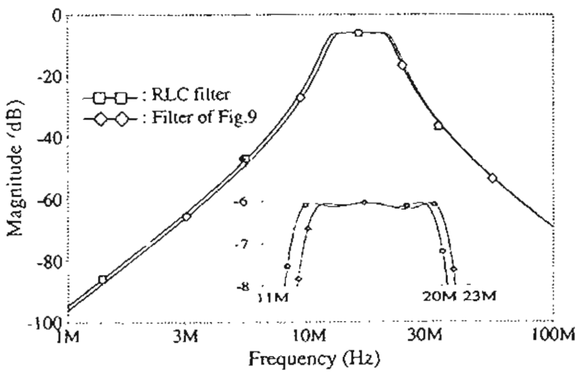


Fig. 18 Frequency responses of the sixth-order bandpass filter.

changes correspond the value changes of the reactance elements of the prototype LCR filters resulting in the shift of the frequency and not in the gain change in the passband. Therefore, we cannot observe gain errors in the passband as shown in Figs. 17 and 18.

5. Conclusions

A realization of leapfrog ladder filters using current differencing buffered amplifiers (CDBA) has been shown. CDBA basically consists of a unity gain current differential amplifier and a unity gain voltage buffer and does not require high gain amplifiers, thus high frequency performances can be expected. CDBA is quite suitable for the realization of filters with a leapfrog structure, especially bandpass filters that contain parallel and series LC resonant branches can be well simulated with a simple configuration. Since each element of the CDBA based filters corresponds to a reactance element of the prototype LCR filters, the sensitivities in the passband become quite low. Two examples of CDBA based filters simulated by PSPICE showed a small error only in the filter cutoff or center frequency, even though the amplifiers in the CDBA have errors of several percents.

The method proposed in this paper requires n CDBA's to realize an n-th order filter. We need to consider how to reduce the number of CDBA's without loosing the features of the CDBA based filters. The CDBA used in this paper can operates at a power supply voltage of 2.0 V (± 1 V) that is limited by the number of transistors between the power supply and the ground. We may need to consider the operation of circuits at a lower voltage than 1.0 V for some applications. These will be our futures works.

Acknowledgment

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1. Introduction

All-pass filters are utilised in many applications such as in sinusoidal quadrature oscillators in an integrated receiver. It is usually desirable that the architecture of such devices is fully balanced with differential signals so as to enable, for example, accurate quadrature outputs with maximum symmetry over a wide tunable-frequency sweep range. There are other significant, well understood advantages in employing a fully balanced realisation [1]. However several techniques of all-pass filters have not been fully balanced [2]-[4]. Recently, a fully balanced wide-frequency current-tunable phase-lag all-pass filter has been reported with the maximum useful frequency of approximately 112 MHz [5]-[7].

In this paper, an integrable fully balanced wide-frequency current-tunable phase-lead all-pass filter is presented. The architecture of the circuit is relatively simple and symmetry with differential signals. The frequency ω_0 where the magnitude and phase shift of the transfer function are approximately 0 dB and +90 degrees, respectively, is linearly current-tunable using a tunable r_e network where r_e is the small-signal dynamic resistance of a forward biased base-emitter junction of a bipolar transistor. The maximum useful frequency is approximately 220 MHz.

2. Circuit Descriptions

Fig. 1 shows the basic circuit configuration of the fully balanced current-tunable phase-lead all-pass filter consisting of ten matched npn transistors Q1 to Q10, a capacitor C and current sinks I_1 and I_f. The differential, small-signal, input voltage V_{in} is applied to the bases of two differential pairs (Q1-Q2) and (Q3-Q4), between nodes A and B. The resulting differential, small-signal, output voltage V_o is taken across the emitters of Q9 and Q10, between nodes G and F.

The current sinks I_1 and I_f may be implemented through the conventional Wilson current mirrors. Current $I_1/2$ biases the (Q3, Q9) and the (Q4, Q10) branches, whilst a frequency setting current I_f biases the (Q1, Q8, Q7) and the (Q2, Q5 and Q6) branches. It can be seen from Fig. 1 that the architecture of the circuit is symmetry and fully-balanced. The circuit is also relatively simple and is "integrable" as all active devices can be fabricated on-chip.

3. Ideal Analysis

Referring to Fig. 1, assuming that the bases of Q9 and Q10 at nodes D′ and E′ are temporarily disconnected with nodes D and E, and as a result the bases of Q9 and Q10 at D′ and E′ are then temporarily connected together with an appropriate bias voltage say V_{bias}. Such a temporary case is illustrated in Fig. 2 and 3, where the resulting differential, small-signal, output voltage across nodes D and E be V_{o1}, as shown in Fig. 2, and that across nodes F and G be V_{o2}, respectively. The differential, small-signal, input voltage V_{in} results in a differential output current i_{d1} as shown in Fig. 2 and therefore

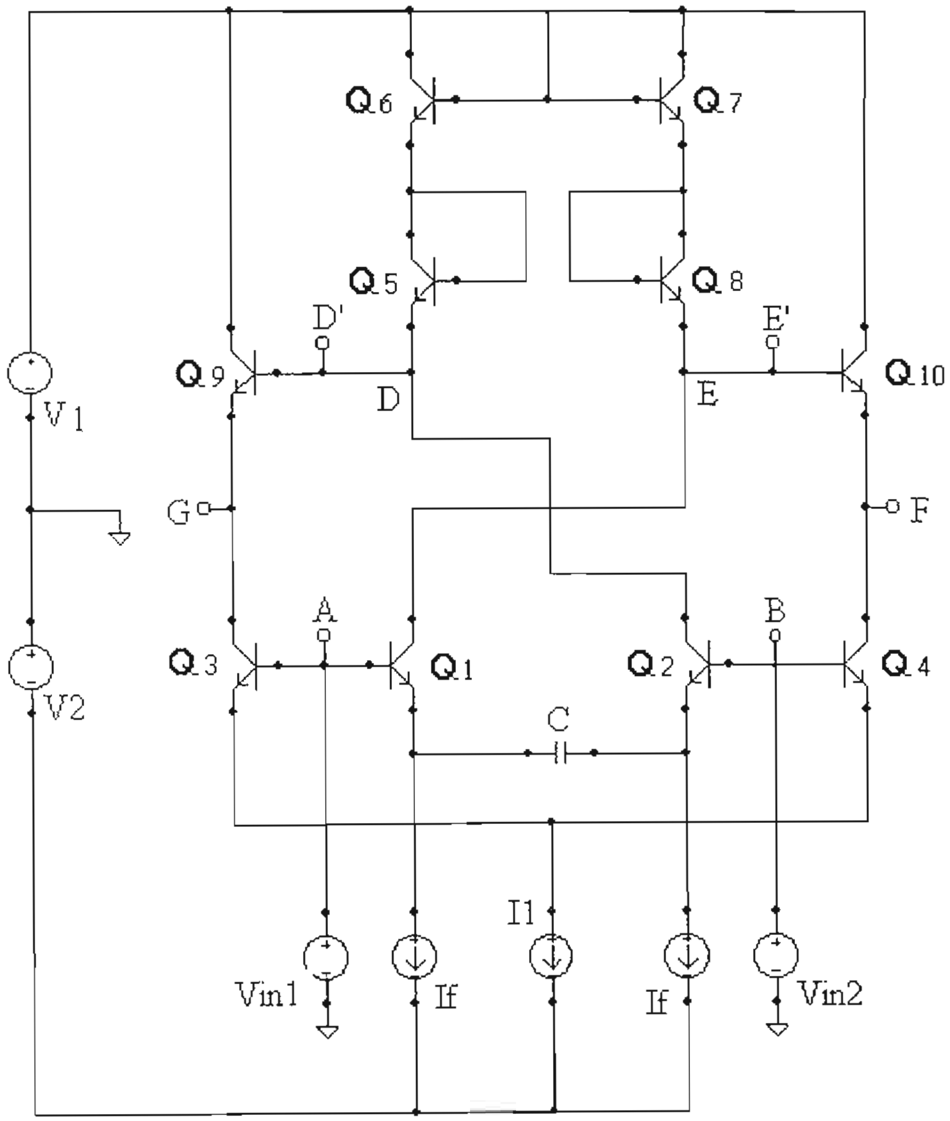

Fig. 1 Schematic diagram of the fully-balanced wide-frequency current-tunable phase-lead all-pass filter.

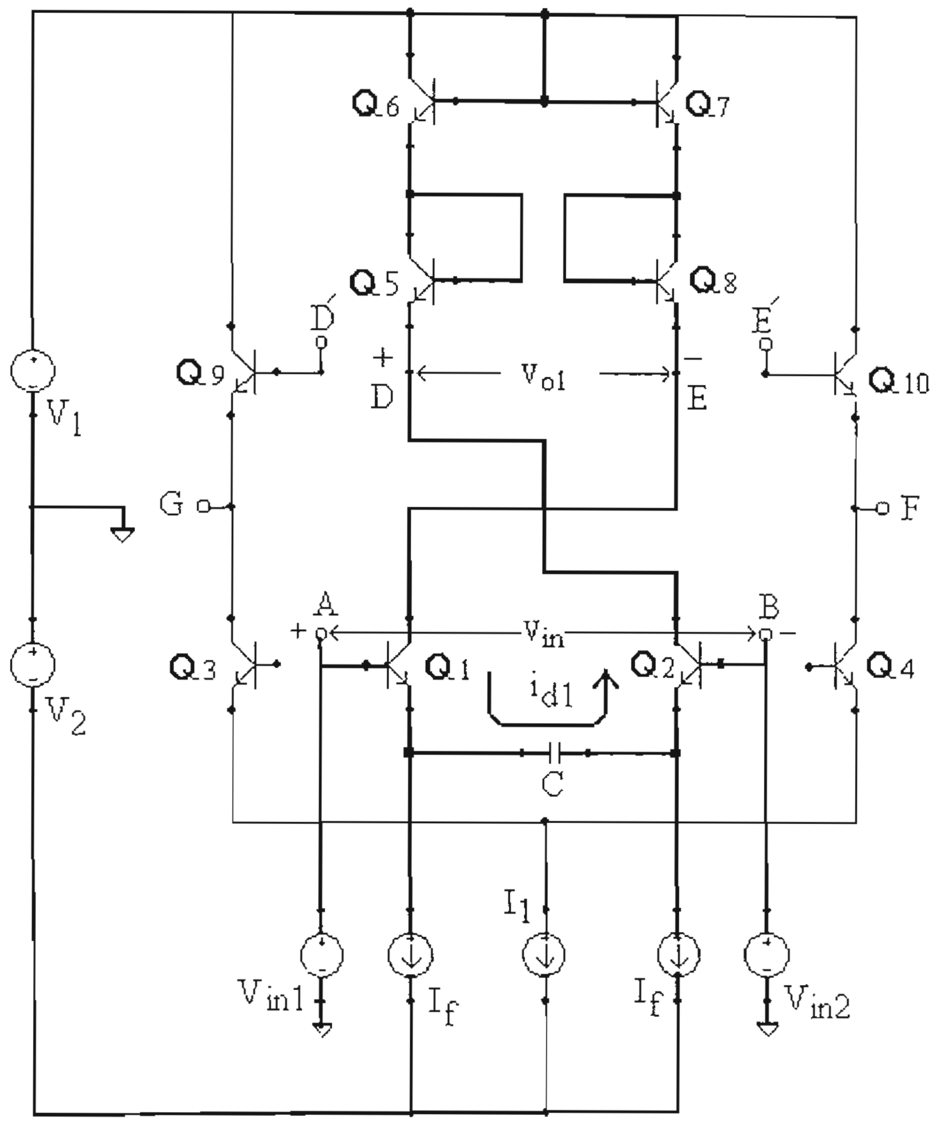

Fig. 2 Differential output current i_{d1} resulting from V_{in}.

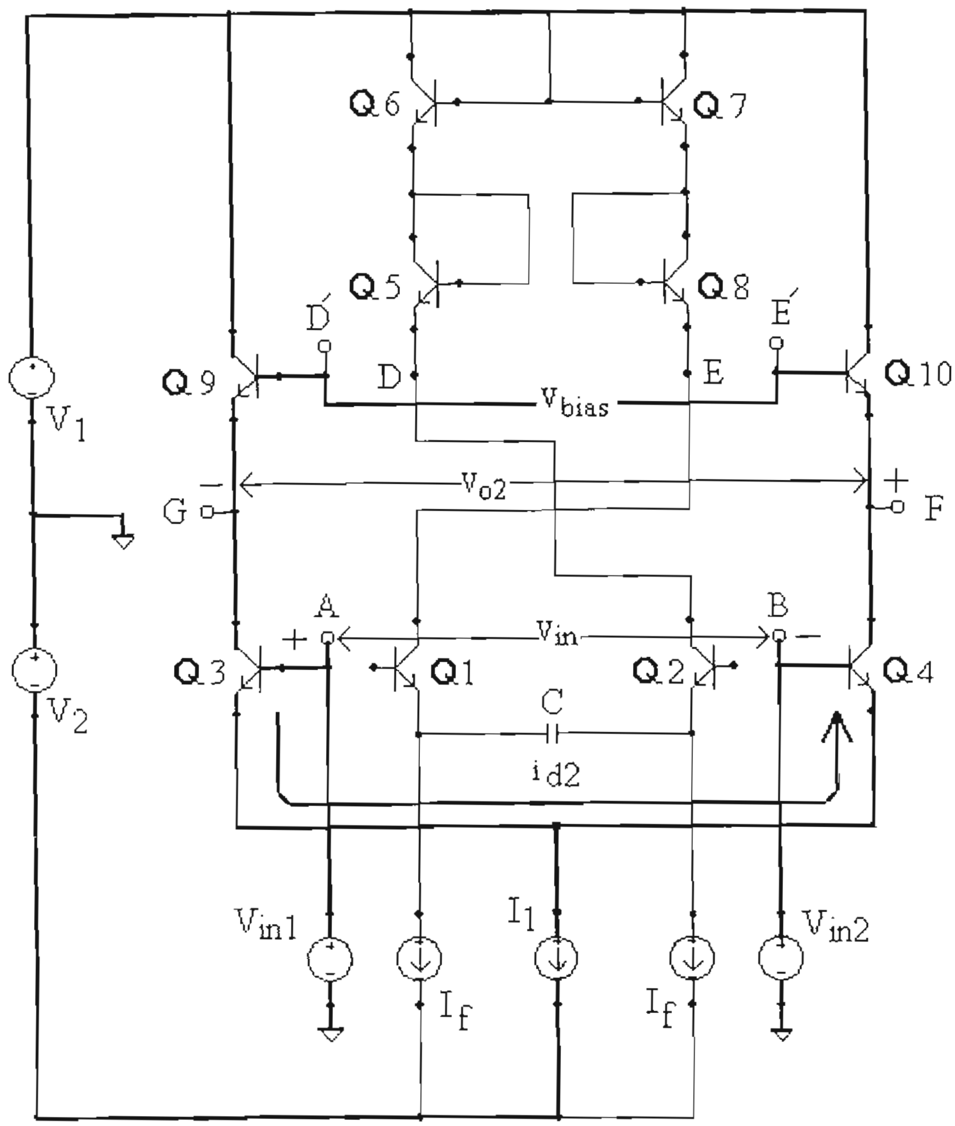

Fig. 3 Differential output current i_{d2} resulting from V_{in}.

$$i_{d1} = \frac{Cs}{1+s\tau} V_{in} \tag{1}$$

$$\tau = 2r_{e1}C = \frac{2V_T C}{I_f} \tag{2}$$

V_T is the usual thermal voltage associated with a pn junction and is approximately equal to 25 mV at room temperature. As shown in Fig. 2, the current i_{d1} passes through the loading resistance $4r_{e1}=4V_T/I_f$ formed by Q5, Q6, Q7 and Q8 between nodes D and E. The output voltage $V_{o1}=(i_{d1})(4r_{e1})$. The 1st-order transfer function V_{o1}/V_{in} therefore represents a high-pass filter of the form

$$\frac{V_{o1}}{V_{in}}=\frac{2s\tau}{1+s\tau} \tag{3}$$

In addition, V_{in} also results in a differential output current i_{d2} as shown in Fig. 3 and therefore

$$i_{d2}=\frac{V_{in}}{2r_{e2}}=\frac{V_{in}}{2V_T}\left(\frac{I_1}{2}\right) \tag{4}$$

As shown in Fig. 3, the current i_{d2} passes through the loading resistance $2r_{e2}=2V_T(2/I_1)$ formed by Q9 and Q10 between nodes F and G. The output voltage $V_{o2}=(i_{d2})(2r_{e2})$. The transfer function V_{o2}/V_{in} therefore represents a buffer of the form

$$\frac{V_{o2}}{V_{in}}=1 \tag{5}$$

By reconnecting the bases of Q9 and Q10 with nodes D and E (as shown in Fig. 1), the resulting differential, small-signal, output voltage V_o, taken across nodes G and F, is obtained through superposition and therefore $V_o=V_{o1}-V_{o2}$. Consequently, the transfer function V_o/V_{in} is of the form

$$\frac{V_o}{V_{in}}=-\left[\frac{1-s\tau}{1+s\tau}\right] \tag{6}$$

It can be seen that equation (6) represents the transfer function of a phase-lead all-pass filter [8]. The frequency ω_0 of the phase-lead all-pass filter where the magnitude and phase shift of the transfer function V_o/V_{in} are approximately 0 dB and +90 degrees, respectively, is of the form

$$\omega_0=\frac{1}{\tau}=\frac{I_f}{2CV_T} \tag{7}$$

It can be seen from equation (7) that the frequency ω_0 is tunable through the bias current I_f and hence the name "current-tunable phase-lead all-pass filter".

4. Simulation Results

The performance of the circuit shown in Fig. 1 has been simulated using PSpice. The npn transistors are modeled by Q2N3904, where the transition frequency f_T is at 300 MHz. [9]. Fig. 4 illustrates magnitude (dB) and phase shift (degree) of V_o/V_{in} versus frequency (Hz) obtained from the simulation using, as an example, capacitor C = 0.01 μF, I_1 = 200 μA, I_f = 40 μA, 200 μA, 1mA and 5 mA. It can be seen from Fig. 4 that, for the phase shift at +90 degrees, the corresponding frequencies $f_0 = \omega_0/2\pi$ for individual values of I_f are at 12.7 kHz, 65 kHz, 320 kHz and 1.6 MHz, respectively, with the corresponding magnitude of approximately 0 dB.

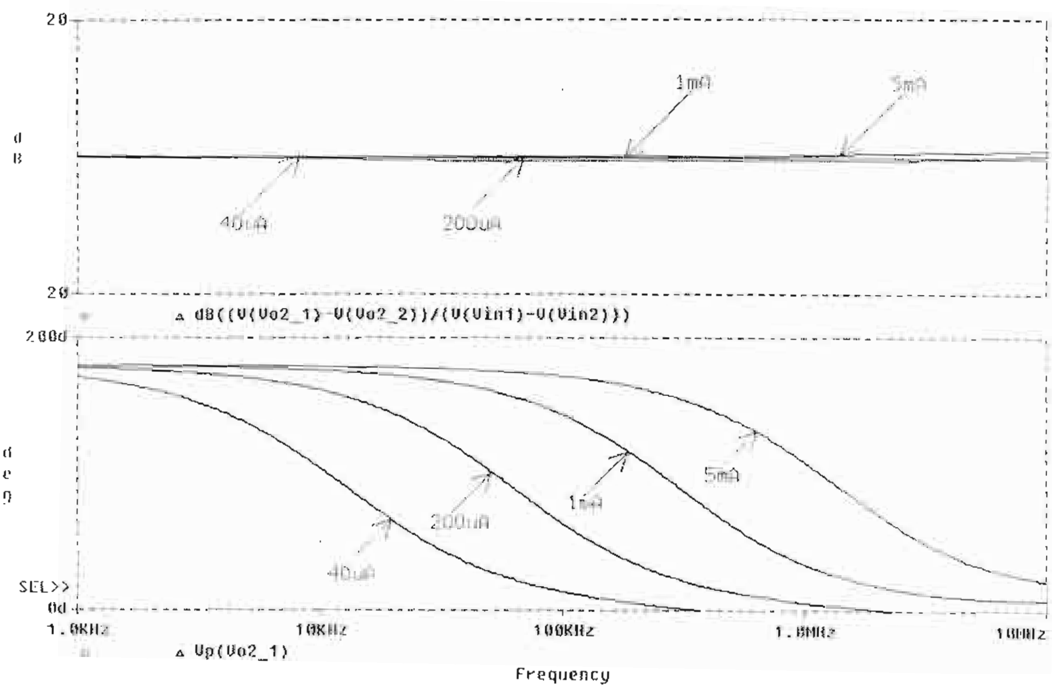

Fig. 4 Magnitude (dB) and phase shift (degree) of V_o/V_{in} versus frequency (Hz) using the capacitance C = 0.01 μF, I_1 = 200 μA and I_f = 40 μA, 200 μA, 1 mA, and 5 mA.

Fig. 5 depicts the simulation results of both the frequency $f_0 = \omega_0 / 2\pi$ and the corresponding magnitude (dB) of V_o / V_{in} , at the phase shift of +90 degrees, versus the bias current I_f using capacitor C = 0.01 μF and I_1 = 200 μA. For purposes of comparison, the expected (ideal) results are also included. It can be seen from Fig. 5 that both the expected and the simulated results are consistent, and the frequency f_0 is linearly current-tunable over a "wide-frequency" sweep range of approximately three orders of magnitude.

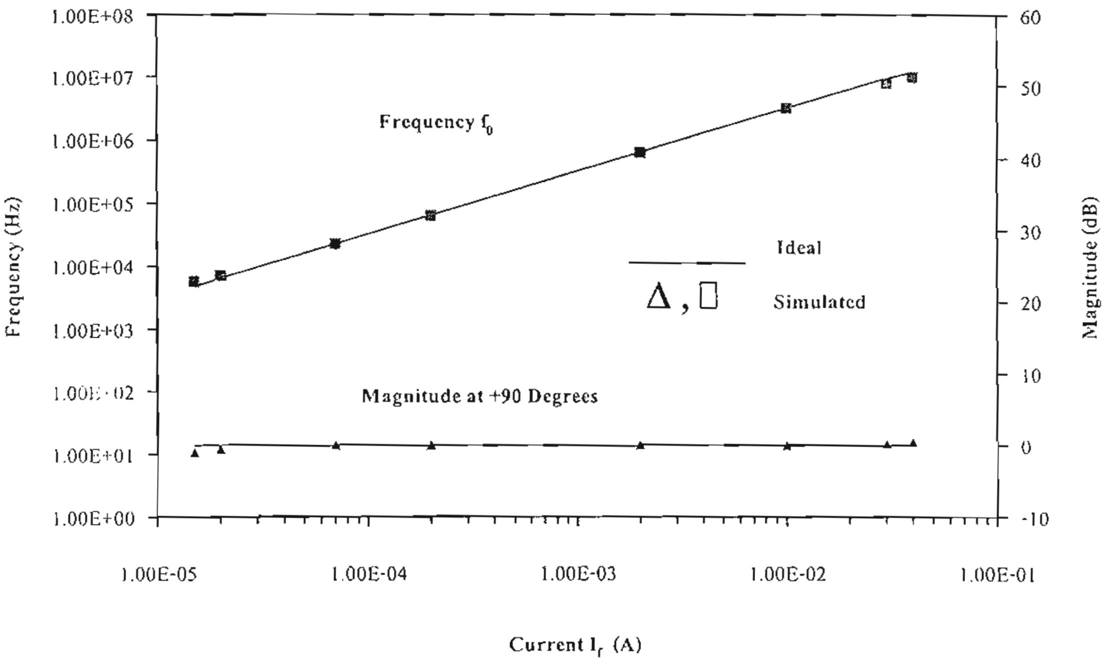

Fig. 5 Frequency f_0 and the corresponding magnitude (dB) of V_o/V_{in}, for the phase shift at +90 degrees versus the bias current I_f (A) , using a capacitance C = 0.01 μF and I_1 = 200 μA.

Fig. 6 shows the simulation results of both the frequency $f_0 = \omega_0 / 2\pi$ and the corresponding magnitude (dB) of V_o / V_{in} , at the phase shift of +90 degrees, versus the capacitance C, using bias current I_f = 4 mA and I_1 = 200 μA. For purposes of comparison, the expected (ideal) results are also included. It can be seen from Fig. 6 that both the expected and the simulated results are linear and consistent. By using a minimum frequency setting capacitance of 20 pF, the upper frequency f_0 can be expected at 220 MHz.

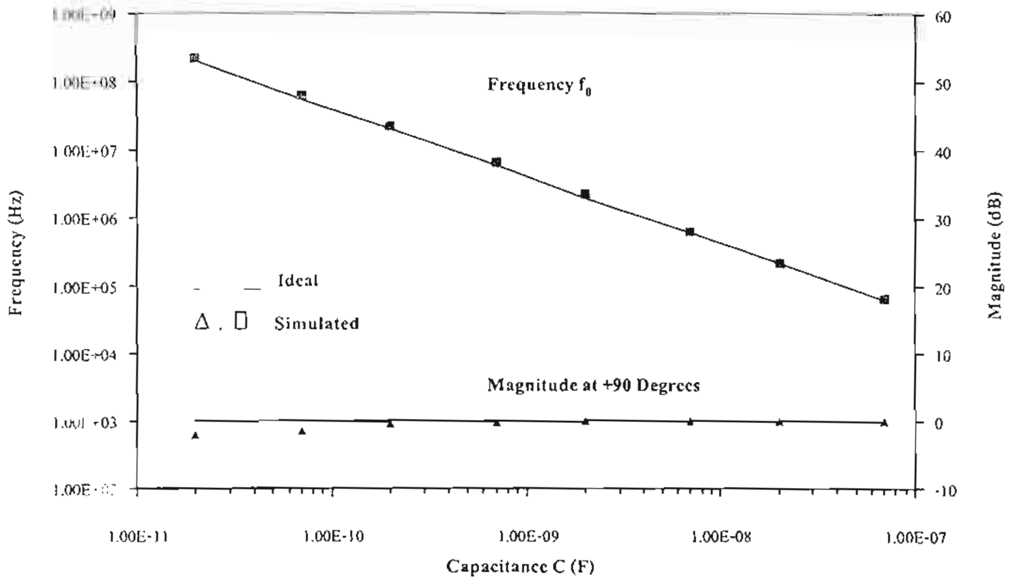

Fig. 6 Frequency f_0 and the corresponding magnitude (dB) of V_o/V_{in}, for the phase shift at +90 degrees, versus the capacitance C (F), using a bias current I_f = 4 mA and I_1 = 200 μA.

5. Discussion and Conclusions

A new integrable fully-balanced wide-frequency current-tunable phase-lead all-pass filter has been presented. The architecture of the circuit is symmetry with differential signals. The circuit is also relatively simple and integrable on-chip. Both simulated and expected results are consistent. The frequency f_0 where the magnitude and phase shift of the transfer function are approximately 0 dB and +90 degrees, respectively, is linearly current-tunable over a wide-frequency sweep range of approximately three orders of magnitude. The maximum useful frequency f_0 is approximately 220 MHz. Eq. (7) suggests that if much smaller value of C (e.g. using stray capacitance) and better transistors of much higher f_T (e.g. in the region of several GHz) are used, then much higher and more useful frequency f_0 could be expected.

Acknowledgements

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CONTENTS

Current-Mode Integrator using OA and OTAs and Its Applications

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Abstract

A circuit building block for realizing a continuous-time active-only current-mode integrator is presented. The proposed integrator is composed only of an internally compensated type operational amplifier (OA) and operational transconductance amplifiers (OTAs). The integrator is suitable for integrated circuit implementation in either bipolar or CMOS technologies, since it does not require any external passive elements. Moreover, the integrator gain can be tuned through the transconductance gains of the OTAs. Some application examples in the realization of current-mode network functions using the proposed current-mode integrator as an active element are also given

Keywords: current-mode integrator, driving-point impedance functions, current-mode filters

1. Introduction

In the last decade, the realizations of various active circuits by utilizing the operational amplifier (OA) pole have received considerable attention for their potential advantages, such as being attractive for monolithic IC integration, ease to design, and suitability for high frequency operation [1-2]. Several OA-based active-R capacitor-less circuits for realizing analog transfer functions have been reported [3-4]. Presently, there is a strong motivation to design resistor-less and capacitor-less filter circuits utilizing the finite and complex gain natures of internally compensated OAs and OTAs. Due to its active only nature, the resistor-less and capacitor-less active filter would be attractive for its programmability and wide frequency range of operation. Many implementations of active-only filter designs are available in the literature [5-7].

An integrator is an important circuit building block, which is widely used in analog signal processing applications, such as, filter design, waveform shaping, process controller design, and calibration circuits, etc. However, the implementation of a continuous-time current-mode integrator that employs only active elements has not yet been reported. Therefore, a circuit configuration for realizing active-only current-mode integrator is proposed in this paper. The proposed integrator consists of one OA and two OTAs. Moreover, it can be implemented in integrated circuit form in both bipolar and CMOS technologies. The integrator gain can be electronically tuned by adjusting the transconductance gains of the OTAs. Various accomplishment active-only analog signal processing circuits employing the proposed integrator will also be presented. Finally, the workabilities of the proposed integrator and its applications have been simulated based upon an LM741 type IC OA and a CA3080 type IC OTA.

Fig. 1 : The proposed active-only current-mode integrator
(a) circuit implementation (b) circuit representation

2. Circuit Description

The proposed active-only dual-output current-mode integrator and its representation are shown in Fig. 1. The integrator consists only of an OA and OTAs, where the dual-output-currents are implemented by using single-ended output OTAs in parallel connection [8]. If ω_a is the 3-dB bandwidth of the OA and by considering the OA for the frequencies $\omega >> \omega_a$, the open-loop gain $A_{OA}(s)$ of the OA can be approximately given by

$$A_{OA}(s) = \frac{A_o\omega_a}{s+\omega_a} \cong \frac{B}{s} \qquad (1)$$

where B represents the gain-bandwidth product (GBP) of the OA, which is the product of the dc gain A_o and the 3-dB bandwidth ω_a, assuming that g_{m1} and g_{m2} denote the transconductance gains of the OTA1 and OTA2, respectively. Then the current transfer function of the current-mode integrator can be expressed as:

$$\frac{I_o(s)}{I_{in}(s)} = \frac{B}{s}\left[\frac{g_{m2}}{g_{m1}}\right] = \frac{B}{s}A_G \qquad (2)$$

where A_G is the ratio between g_{m2} and g_{m1} and denotes the integrator gain. Eqn. (2) indicates that the relationship of the currents I_o and I_{in} is in the form of the integrating action. It should be noted that for ordinary bipolar OTAs, $g_{m1} = I_{B1}/2V_T$ and $g_{m2} = I_{B2}/2V_T$, where V_T is the thermal voltage and I_{B1} and I_{B2} are the bias currents of the OTA1 and OTA2, respectively. Thus, eqn. (2) becomes

$$\frac{I_o(s)}{I_{in}(s)} = \frac{B}{s}\left[\frac{I_{B2}}{I_{B1}}\right] = \frac{B}{s}A_G \qquad (3)$$

A_G is the current gain, that is the current ratio between the bias current I_{B2} and I_{B1}. In this case, the temperature dependence of the transconductance gains g_{m1} and g_{m2} of the bipolar OTAs are compensated.

Deviation from the ideal performance predicted from eqn.(2) is due to parasitic effects of the non-ideality characteristics of the OA and OTAs. If the second dominant pole ω_b of the OA is taken for consideration, the OA open-loop gain $A_{OA}(s)$ can be rewritten as

$$A_{OA}(s) = \frac{B}{s}\frac{\omega_b}{(s+\omega_b)} = \frac{B}{s}\frac{1}{(1+\tau_b s)} \qquad (4)$$

where $\tau_b = 1/\omega_b$. For the OTAs, let $\omega_c = 1/\tau_c$ represent the effective transconductance internal-pole of the OTA and g_{m0} is the low frequency transconductance gain. The OTA open-loop gain $g_m(s)$ for the general case can be described by

$$g_m(s) = \frac{g_{m0}}{\left(1+\frac{s}{\omega_c}\right)} \cong g_{m0}\left(1-\frac{s}{\omega_c}\right) \qquad (5)$$

Therefore, the frequency response of the current-mode integrator in Fig. 1 (including the second dominant pole of the OA) and the transconductance internal-poles of the OTAs can now be given by

$$\frac{I_o(s)}{I_{in}(s)} = \left[\frac{B}{s}\right]\left[\frac{1}{1+\tau_b s}\right]\left[\frac{g_{m02}}{g_{m01}}\right]\left[\frac{\omega_{c2}-s}{\omega_{c2}}\right]\left[\frac{\omega_{c1}}{\omega_{c1}-s}\right] \qquad (6)$$

where ω_{c1} and ω_{c2} are the effective transconductance internal-poles of OTA1 and OTA2, respectively. It can be seen that if the conditions $\omega_{c1} \cong \omega_{c2}$ and $\omega_{c1} >> \omega$, $\omega_{c2} >> \omega$ are satisfied, then eqn. (6) becomes frequency independent. As a result, if we define $A_{G0} = g_{m02}/g_{m01}$, eqn. (6) can be reasonably reduced to

$$\frac{I_O(s)}{I_{in}(s)} = \left[\frac{A_{G0}B}{s}\right]\left[\frac{1}{1+\tau_b s}\right] \qquad (7)$$

One can see that the frequency characteristic of the proposed current-mode integrator has a dc current gain equal to eqn. (2) and a high frequency dominant pole located at ω_b. Hence, the OA pole ω_b should be the major high-frequency limitation of the proposed current-mode integrator. For example, the commercially available LF356N OA has the gain-bandwidth product $B = 2\pi(4.5)\times10^6$ rad/s and its second dominant pole is $\omega_b = 2\pi(9)\times10^6$ rad/s [9]. Hence, the major high-frequency limitation of the proposed integrator is approximately located at 9 MHz.

3. Application Examples

The following sections will concentrate on the usefulness of the proposed current-mode integrator. Some application examples to realize driving-point impedance functions and current-mode biquadratic filters will be considered.

3.1. Driving-point impedance functions

3.1.1. Inductance simulations

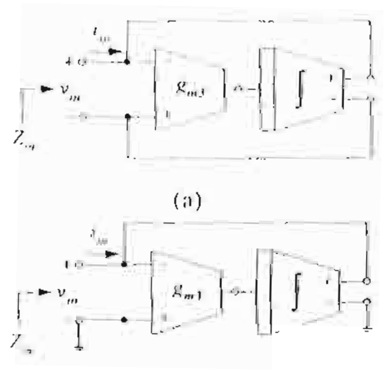

Fig. 2 : Active-only inductance simulations

Fig. 2(a) and Fig. 2(b) show the circuit diagram of a tunable floating and a grounded inductance simulations, respectively. From the circuits, it can easily be shown that the value of the simulated inductance is

$$L_{eq} = \left[\frac{1}{g_{m3}A_G B}\right] \qquad (8)$$

It should be noted that the equivalent inductance L_{eq} can properly be tuned by electronic means through the current ratio A_G and/or the transconductance gain g_{m3}.

3.1.2. Capacitance simulations

An application of the proposed current-mode integrator to simulate an electronically tunable capacitance simulation circuit is shown in Fig.3. In this case, the magnitude of the simulated capacitance can be given by

$$C_{eq} = \left[\frac{g_{m4}g_{m5}}{g_{m3}A_G B}\right] \qquad (9)$$

Since A_G and g_{mi} (i = 3, 4, 5) can be electronically variable, the magnitude of the simulated capacitance can also be electronically variable. In the same manner, the grounded capacitance multiplier of Fig. 3 can be conveniently converted into a corresponding floating capacitance by adding an additional dual-current output OTA.

3.1.3. Frequency-dependent negative resistance (FDNR)

The scheme for simulating a frequency-dependent negative resistance (FDNR) element is shown in Fig. 4. Also, note that the circuit behaves as a grounded FDNR element with

$$D = \left[\frac{g_{m6}g_{m7}}{g_{m5}A_{G1}A_{G2}B_1B_2}\right] \qquad (10)$$

where A_{Gi} and B_i are the gain and the OA's GBP of the i-th integrator unit (i = 1, 2). In contrast to conventional circuits, this circuit does not require any external passive elements and its characteristic can be electronically tuned.

Fig. 3 : Grounded-capacitance multiplier simulation

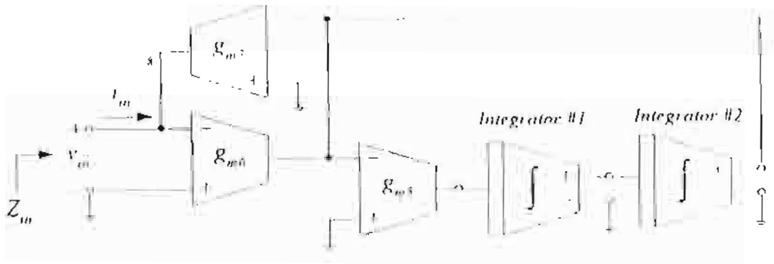

Fig. 4 : An active-only FDNR

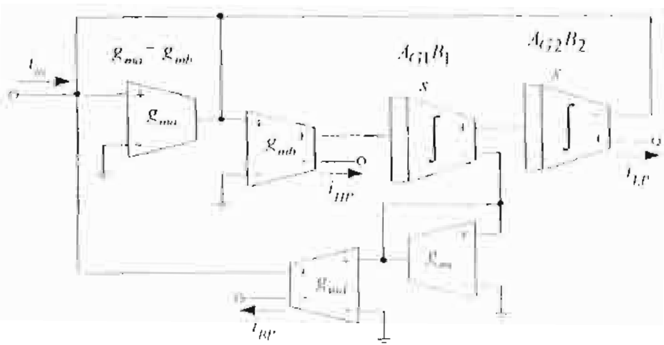

Fig. 5 : Active-only current-mode biquadratic filter

3.2. Electronically tunable active-only current-mode biquadratic filter

Fig. 5 shows the circuit diagram of the tunable current-mode filter based on the proposed current-mode integrator, where i_{LP}, i_{BP}, and i_{HP} are the lowpass, bandpass and highpass current-output terminals, respectively. The circuit parameters ω_o and Q-factor of this filter can be written as

$$\omega_o = \sqrt{A_{G1}A_{G2}B_1B_2} \qquad (11)$$

and

$$Q = \frac{g_{mc}}{g_{md}}\sqrt{\frac{A_{G2}B_2}{A_{G1}B_1}} \qquad (12)$$

One can see that the filter also enjoys orthogonal tuning of ω_o and Q-factor via the transconductance gains of the OTAs and it is also temperature independent.

To discuss the non-ideal effect of the proposed integrator on the filter's frequency characteristics, the parasitic second dominant pole of the OA from equation (7) is taken into account. As a result, the percentage inaccuracies of the ω_o and Q-factor in this case are respectively found to be

$$\frac{\delta\omega_o}{\omega_o}=\left\{\left[1+\left(A_{G1}B_1\tau_{b1}\right)\left(A_{G2}B_2\tau_{b2}-\frac{g_{md}}{g_{mc}}\right)\right]^{\frac{1}{2}}-1\right\}\times 100\% \qquad (13)$$

and

$$\frac{\delta Q}{Q}=\frac{\left[1-\left(\frac{g_{mc}A_{G2}B_2}{g_{md}}\right)\left(\tau_{b1}+\tau_{b2}\right)\right]-\left[1+\left(A_{G1}B_1\tau_{b1}\right)\left(A_{G2}B_2\tau_{b2}-\frac{g_{md}}{g_{mc}}\right)\right]^{\frac{1}{2}}}{\left[1+\left(A_{G1}B_1\tau_{b1}\right)\left(A_{G2}B_2\tau_{b2}-\frac{g_{md}}{g_{mc}}\right)\right]^{\frac{1}{2}}}\times 100\% \qquad (14)$$

where $\omega_{b1}=1/\tau_{b1}$, $\omega_{b2}=1/\tau_{b2}$ and ω_{b1} and ω_{b2} are the second dominant poles of the OA1 and OA2, respectively. It is found that undesirable factors, which are yielded by the parasitic effects of OAs, can be made negligible if such factors are considered as the condition:

$$1>>\left(\frac{g_{mc}A_{G2}B_2}{g_{md}}\right)\left(\tau_{b1}+\tau_{b2}\right) \qquad (15)$$

4. Design Examples And Simulation Results

In order to verify the theoretical study of the proposed current-mode integrator, PSPICE simulation results are included. In this simulation, the OTA is modeled by employing a CA3080 type OTA with a macro model [8] and an LM741 type OA with the gain-bandwidth product $B = 2\pi\times10^6$ rad/s. Fig. 6 shows the simulated frequency responses of the proposed current-mode integrator. The results show that the circuit acts as an integrating function with a slope -20 dB per decade for the frequency range from 10 Hz to 1 MHz and has less than 10% phase error in the frequency range of 30 Hz to 500 kHz.

The performance of the floating inductance circuit of Fig. 2(a) is demonstrated through the use of an electronically tunable active RL low-pass filter in Fig. 7(a) with the external resistor R_1 = 1 kΩ. The bias current ratio $A_G = I_{B2}/I_{B1}$ ($= g_{m2}/g_{m1}$) is set to 0.5, 1 and 2, while g_{m1} and g_{m3} are respectively set to 1 mS and 0.4 mS ; thus the cut-off frequencies f_C are approximately equal to 200 kHz, 400 kHz and 800 kHz, respectively. The frequency responses of the low-pass filter are shown in Fig. 7(b).

Fig. 8 shows simulated responses of the tunable current-mode multifunctional filter of Fig. 5, when $A_{G1} = A_{G2} = 0.05$ and $g_{mc}/g_{md} = 0.1$. This filter is designed for $\omega_o/2\pi$ = 50 kHz at the unity Q-factor. All the simulated results shown above imply that the proposed integrator exhibits reasonably good agreement with the predicted values.

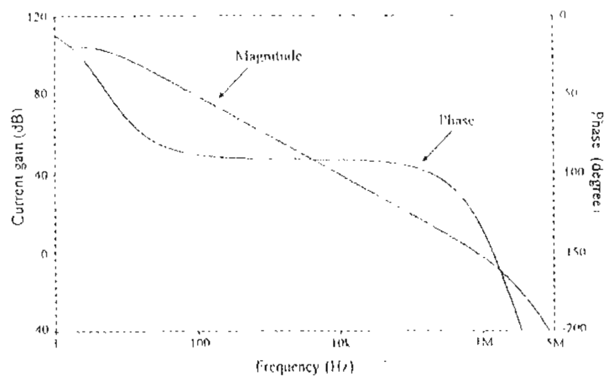

Fig. 6 : Frequency responses of the proposed integrator

A Realization of Current-Mode Biquadratic Filters Using Multiple-Output FTFNs

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ract

A configuration for realizing current-mode second-r multifunctional filter using four terminal floating ors (FTFNs) is presented in this paper. The proposed consists of three multiple output FTFNs and passive nded elements. The circuit can simultaneously ze the highpass, bandpass and lowpass current sfer functions from the same configuration, logonal control of the natural angular frequency ω_o the quality factor Q and low active and passive itivities. PSPICE simulation results are employed to fy the circuit performance.

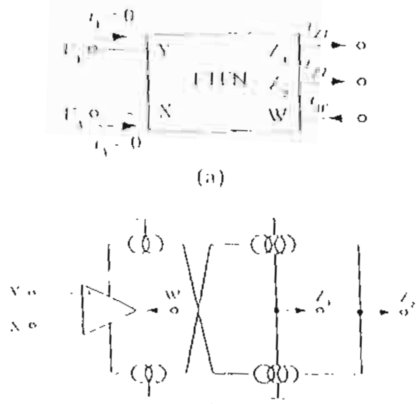
I. Introduction

It is well known that current-mode circuits have n receiving significant attention owing to its advantage r the voltage-mode, particularly for higher frequency operation and simpler filtering structure [1]. Recently, applications and advantages in the realization of nsfer functions using four-terminal floating nullors ve received considerably attention. The design of rent-mode circuits employing FTFN as an active vices such as amplifiers [2], current-mode filters [3-5], nusoidal oscillators [6] and floating inmittances [7], has en developed in the literature. Some previously reports ve been demonstrated that an FTFN is a more flexible d versatile building block than an operational amplifier a current conveyor [4-5]. There are several techniques r realizing current-mode biquadratic filters using FTFNs -5] but there are no FTFN-based circuits that can multaneously realize three types of current-mode ltering function, namely, lowpass, bandpass and ghpass, in the same configuration without changing rcuit topology and elements and provide its parameters ω_o and Q-factor independently tuned.

Therefore, the purpose of this paper is to describe a ealization scheme for generating current-mode FTFN-ased filter configuration. The proposed circuit mplemented from multiple-output FTFNs can realize the second-order highpass, bandpass and lowpass current transfer functions simultaneously from the same circuit. Moreover, the natural angular frequency ω_o and the quality factor Q of the circuit can be orthogonally tuned and both its active and passive sensitivities are quite small. PSPICE simulation results, which are confirmed the theoretical analysis, are obtained.

(a) (b)

Figure 1. Nullor model of the FTFN



(a)

(b)

Figure 2. Multiple-output FTFN (a) symbol for the multiple-output FTFN (b) possible implementation of the multiple-output FTFN

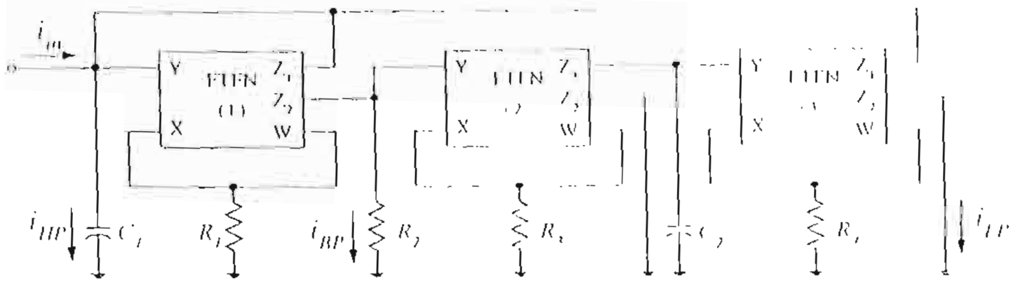


Figure 3 : Proposed circuit configuration for realizing current-mode biquadratic filters

II. Nullor model of FTFN

The FTFN is equivalent to an ideal nullor as shown in Fig.1(a), where the port characteristics can be described by the following equations : [2-7]

$$V_X = V_Y \quad , \quad i_Y = i_X = 0 \quad \text{and} \quad i_Z = i_W \qquad (1)$$

Although the output impedance of the W- and Z-ports of an FTFN are arbitrary, in this paper an FTFN of the type shown in Fig.1(b) is employed where the output impedance of the W-port is very low and that of the Z-port is very high. For the realization scheme proposed here, the multiple-output FTFN can easily be modified from the available FTFN implementation, shown in Fig.1 (b), by adding a another output current mirror terminal as shown in Fig.2. Therefore, the resulting building block becomes the multiple output FTFN or the five terminals FTFN, which can be characterized by the following port relations

$$V_X = V_Y \quad , \quad i_Y = i_X = 0 \quad \text{and} \quad i_{Z1} = i_{Z2} = i_W \qquad (2)$$

III. Proposed circuit

The realization scheme of the proposed filter configuration using multiple-output FTFNs is shown in Fig.3, advantageously has all passive components really grounded, and generates the following current transfer functions yielded by routine circuit analysis

$$T_{HP}(s) = \frac{I_{HP}(s)}{I_{in}(s)} = \frac{s^2}{D(s)} \qquad (3)$$

$$T_{BP}(s) = \frac{I_{BP}(s)}{I_{in}(s)} = \frac{s\left(\frac{1}{R_1C_1}\right)}{D(s)} \qquad (4)$$

$$T_{LP}(s) = \frac{I_{LP}(s)}{I_{in}(s)} = \frac{\left(\frac{R_2}{R_1R_3R_4C_1C_2}\right)}{D(s)} \qquad (5)$$

and $$D(s) = s^2 + s\left(\frac{1}{R_1C_1}\right) + \left(\frac{R_2}{R_1R_3R_4C_1C_2}\right)$$

where $T_{HP}(s)$, $T_{BP}(s)$, $T_{LP}(s)$ are the highpass, bandpass and lowpass current transfer functions, respectively. More importantly these transfer functions can be simultaneously obtained from the same circuit without changing circuit configuration and elements. The natural angular frequency ω_o and the Q factor of this configuration can be given by

$$\omega_o = \sqrt{\frac{R_2}{R_1R_3R_4C_1C_2}} \quad , \qquad (6)$$

and $$Q = \sqrt{\frac{R_1R_2C_1}{R_3R_4C_2}} \qquad (7)$$

According to eqns. (6) and (7), if we set $R_2 = R_3 = R_4 = R_B$ and $C_1 = C_2 = C$, then ω_o and Q-factor of this filter can be rewritten as

$$\omega_o = \frac{1}{R_BC} \qquad (8)$$

and $$Q = \frac{R_1}{R_B} \qquad (9)$$

It is clearly seen from eqn.(8) that the natural angular frequency ω_o can be tuned by adjusting the value of resistors R_B and/or the capacitors C, whereas eqn.(9) shows that Q factor can be orthogonally controlled by varying R_1. The passive sensitivities of ω_o and Q factor of the universal current-mode filter are

$$S^{\omega_o}_{R_B} = S^{\omega_o}_{C} = -1 \tag{10}$$

$$S^{Q}_{R_A} = -S^{Q}_{R_B} = 1 \tag{11}$$

Observing that all of the sensitivities are small.

IV. Effects of the FTFN non-idealities

Assuming that the port relations of the non-ideal performance of the FTFN are considered by $V_X = \beta V_Y$, $i_{Z1} = i_{Z2} = \alpha i_W$, where $\beta = 1 - \varepsilon$, ($|\varepsilon| << 1$), denotes the voltage tracking error and $\alpha = 1 - \delta$, ($|\delta| << 1$), represents the current tracking error of the FTFN. Therefore, from a routine circuit analysis of circuit as shown in Fig.3 yields the current transfer functions rewritten by

$$THP(s) = \frac{I_{HP}(s)}{I_{in}(s)} = \frac{s^2}{D_n(s)} \tag{12}$$

$$TBP(s) = \frac{I_{BP}(s)}{I_{in}(s)} = \frac{s\left(\frac{\beta_1\alpha_1}{R_1C_1}\right)}{D_n(s)} \tag{13}$$

$$TLP(s) = \frac{I_{LP}(s)}{I_{in}(s)} = \frac{\left(\frac{\beta_1\beta_2\beta_3\alpha_1\alpha_2\alpha_3R_2}{R_1R_3R_4C_1C_2}\right)}{D_n(s)} \tag{14}$$

and $$D_n(s) = s^2 + s\left(\frac{\beta_1\alpha_1}{R_1C_1}\right) + \left(\frac{\beta_1\beta_2\beta_3\alpha_1\alpha_2\alpha_3R_2}{R_1R_3R_4C_1C_2}\right)$$

where β_i and α_i, ($i = 1, 2, 3$), are the voltage- and the current tracking errors of the i-th FTFN. As the same condition mentioned-above, the parameters ω_{on} and Q_n factor for the non ideal case can be given by

$$\omega_{on} = \frac{1}{R_BC}\sqrt{\beta_1\beta_2\beta_3\alpha_1\alpha_2\alpha_3} \tag{15}$$

$$Q_n = \frac{R_A}{R_B}\sqrt{\frac{\beta_2\beta_3\alpha_2\alpha_3}{\beta_1\alpha_1}} \tag{16}$$

It can be found that the active sensitivities for this case are

$$S^{\omega_{on}}_{\beta_1,\beta_2,\beta_3} = S^{\omega_{on}}_{\alpha_1,\alpha_2,\alpha_3} = \frac{1}{2} \tag{17}$$

$$S^{Q_n}_{\beta_1} = S^{Q_n}_{\alpha_1} = -\frac{1}{2} \tag{18}$$

and $$S^{Q_n}_{\beta_2,\beta_3} = S^{Q_n}_{\alpha_2,\alpha_3} = \frac{1}{2} \tag{19}$$

The fact that all of the calculated active sensitivities from eqns. (17)-(19) are quite small.

V. Simulation results

The characteristic of the proposed circuit of the Fig.3 has been confirmed by PSPICE simulation results. Although several techniques to implement an FTFN have been presented [2,3,8], the simulation results were obtained by using the possible realization of the multiple-output FTFN shown in Fig.4. The FTFN was constructed with an operational amplifier AD704 from Analog Device [9] and the power-supply current-sensing technique [10] using bipolar transistors of 2N2907A and 2N2222 for pnp and npn transistors, respectively. The circuit was tested under the supply voltages ±15V and the grounded capacitor values are $C_1 = C_2 =$ [illegible]

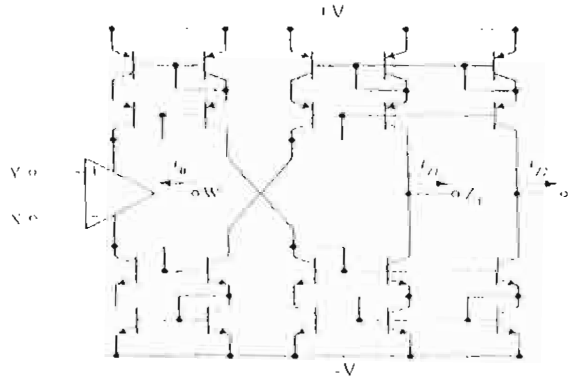


Figure 4. A realization of the multiple-output FTFN using the power supply current sensing technique

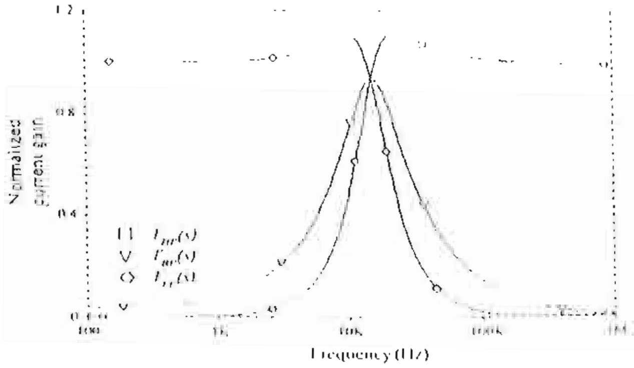


Figure 5. Simulated filter characteristics of the proposed filter with $R_A = R_B = 10$ kΩ and $C_1 = C_2 =$ [illegible]

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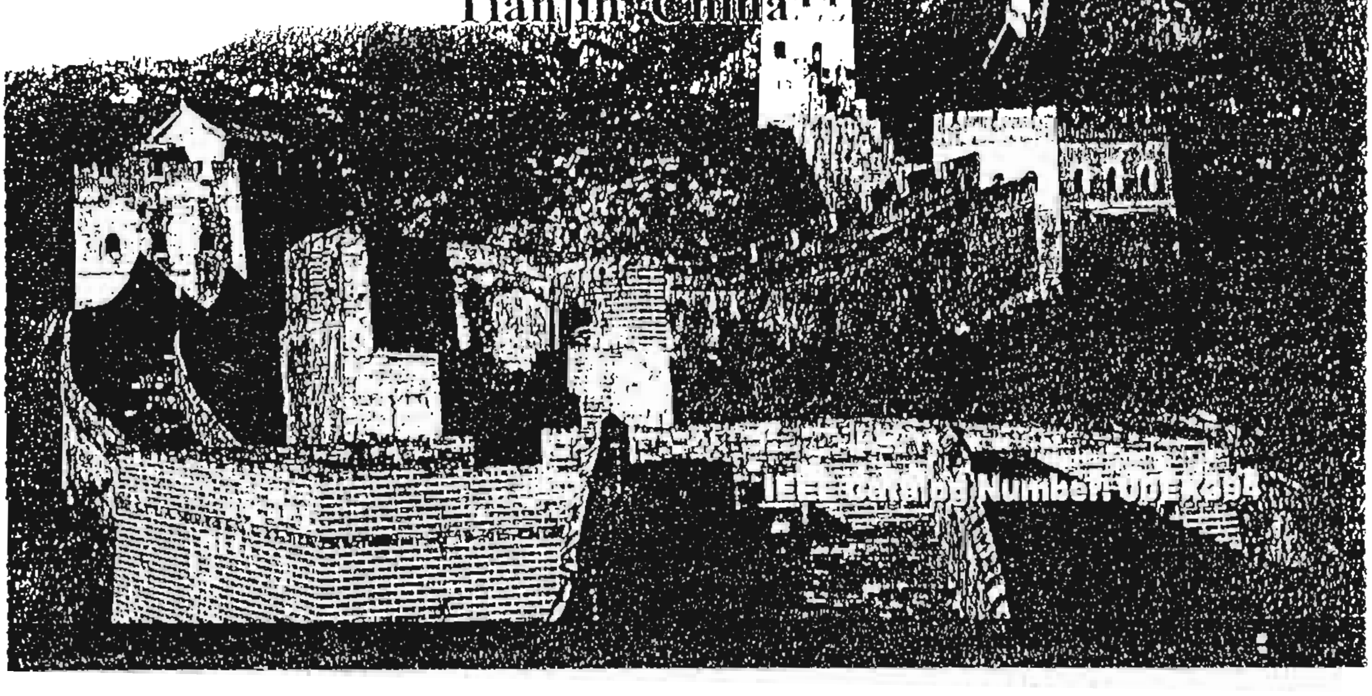

Sinusoidal Frequency Doubler and Full-wave Rectifier Using Translinear Current Controlled Conveyors

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Abstract

An alternative technique for realizing both a sinusoidal frequency doubler and a full-wave rectifier, using translinear current controlled conveyors as active circuit elements, is presented. The frequency doubling and the rectifying action are exploited from the translinear characteristic of the current conveyor. Simulation results are given to confirm the theoretical predictions.

I. Introduction

Sinusoidal frequency doubler and full-wave rectifier find a wide range of applications in instrumentation and communication systems. It has been demonstrated that a dual translinear loop, which works as a class AB amplifier, can be used to implement both a sinusoidal frequency doubler and full-wave rectifier [1]. In recent years, a translinear current controlled conveyor (CCCII) has received much attention in the design and implementation of current-mode function circuits with electronically tunable characteristic such as oscillators, multipliers and filters [2]-[5]. Due to the dual translinear characteristic of bipolar junction transistors associated within the current conveyor, it has also been recently demonstrated that a translinear current controlled conveyor incorporates both a sinusoidal frequency doubler and full-wave rectifier functions [6]. However, the circuit requires the external current mirrors. Therefore, the purpose of this article is to propose a frequency doubler and full-wave rectifier circuit that employing only three CCCIIs and external resistors.

II. Circuit description

A. Basic principle

The schematic diagram of the translinear-based second-generation current-controlled conveyor is shown in Fig. 1, where groups of transistors Q_1-Q_4 constitute a dual translinear input cell, i_{in} is the input current at port X and I_1 is the DC bias current. Assuming that the transistor's common-emitter current gain $\beta >> 1$, the expression for the currents I_2 and I_3 can be stated as [7]-[8]

$$I_2 = \frac{\left(i_{in}^2 + 4I_1^2\right)^{1/2} - i_{in}}{2} \qquad (1a)$$

$$I_3 = \frac{\left(i_{in}^2 + 4I_1^2\right)^{1/2} + i_{in}}{2} \qquad (1b)$$

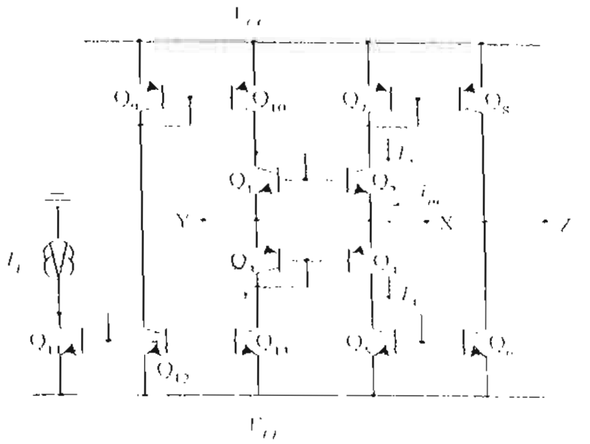

Fig. 1 Schematic diagram of the translinear current controlled conveyor

The proposed sinusoidal frequency doubler and full wave rectifier employing CCCII which corresponds to the circuit diagram of the translinear conveyor in Fig. 1, are shown in Fig. 2. The currents I_{S1} and I_{S2} denote respective the positive-supply current and the negative supply current of the conveyor CCCII$_A$. I_{2A} and I_{3A} represent respective the currents I_2 and I_3 of the conveyor CCCII$_A$. Thus, the expressions for I_{S1} and I_{S2} are

$$I_{S1} = 2I_1 + 2I_{2A} \qquad (2a)$$

and

$$I_{S2} = 3I_1 + 2I_{3A} \qquad (2b)$$

In this scheme, the converting resistor R_{x1} converts the input signal voltage v_{in} to an input signal current i_{in}, i.e. $i_{in} = i_{x1}$. According to equation (1), the current I_{2A} and I_{3A} can be given by

$$I_{2A} = \frac{\left(i_{x1}^2 + 4I_1^2\right)^{1/2} + i_{x1}}{2} \qquad (3a)$$

$$I_{3A} = \frac{\left(i_{x1}^2 + 4I_1^2\right)^{1/2} - i_{x1}}{2} \qquad (3b)$$

The supply currents I_{S1} and I_{S2} are sensed by resistors R_{S1}

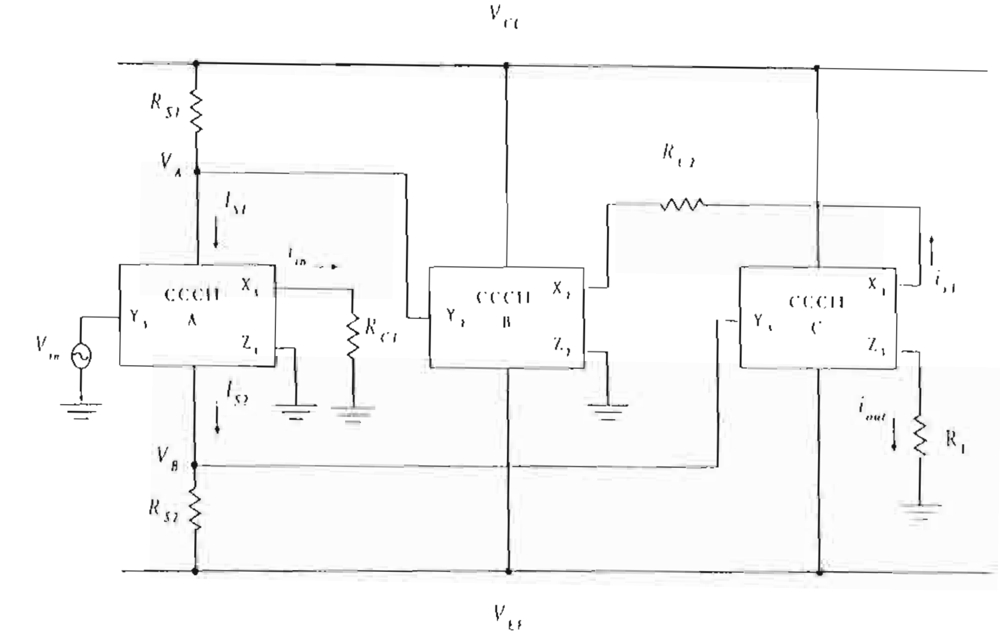

Fig. 2. The proposed sinusoidal frequency double and full-wave rectifier.

d R_{S2}, respectively. The voltage dropped across the sistors that are delivered to input terminal Y_2 and Y_3 that equal potential will appear on the input terminal X_2 and X_3 of the $CCCII_B$ and $CCCII_C$, respectively. Then, the expressions for V_A and V_B are

$$V_A = V_{CC} - (2I_1 + 2I_{2A})R_{S1} \tag{4a}$$

$$V_B = -V_{EE} + (3I_1 + 2I_{3A})R_{S2} \tag{4b}$$

nd

$$V_{R_{C2}} = V_A - V_B \tag{5}$$

$R_{S1} = R_{S2} = R_S$, $R_{x2} = R_{x3} = R_x = \frac{V_T}{2I_1}$, where R_x is the input impedance at terminal X of the CCCIIs and V_T is the thermal voltage at room temperature (approximately 26 mV). The signal current i_{c3} will be conveyed to the output terminal Z_3 such that terminal Z_3 has the characteristics of a current source, of value $i_{c3} = -\frac{V_A - V_B}{R_{C2} + 2R_x}$, with high output impedance, then the output current i_{out} of the $CCCII_C$ are

$$i_{out} = -\frac{V_A - V_B}{R_{C2} + 2R_x} \tag{6}$$

$$i_{out} = 2k_1V_{CC} + 5k_1I_1R_S - 2k_1R_S\left(4I_1^2 + i_{in}^2\right)^{1/2} \tag{7}$$

Where $k_1 = \frac{1}{R_{C2} + 2R_X}$ and V_{CC} is the power supply voltage. From equation (7), it is clearly seen that the third term is in the form of a root-sum of a square relation. It is this term that perform the frequency doubling action

B. Sinusoidal frequency doubler

For a sinusoidal input signal voltage $v_{in} = V_m \sin \omega t$, the input signal current i_{in} is equated to $i_{in} = I_m \sin \omega t$, where $I_m = \frac{V_m}{R_{C1}}$. If we select the signal amplitude such that $|i_{in}| < 4I_1$, $k_2 = -2k_1V_{CC} + 5k_1I_1R_S$, then the equation (7) becomes

$$i_{out} = k_2 - 4I_1k_1R_S\left(1 + k_3 \sin \omega t\right)^{1/2} \tag{8}$$

where $k_3 = \frac{I_m^2}{(2I_1)^2}$ If the power series of the form $\sqrt{(1+x)} = 1 + \left(\frac{1}{2}\right)x - \left(\frac{1}{8}\right)x^2 + \ldots$ are employed, then the equation (7) can be rewritten as

$$i_{out} = k_2 - 4I_1k_1R_S\left(I_{DC} + I_{2\omega}\cos 2\omega t + I_{4\omega}\cos 4\omega t + \ldots\right) \tag{9}$$

CCCIIs is presented. The frequency doubling and the rectifying action are exploited by employing the translinear characteristic associated within the current conveyor, where this characteristic has been monitored from supply-line currents. PSPICE simulation results have been used to verify the performance of the proposed circuit and have been demonstrated to agree very well with the theoretical predictions.

V. Acknowledgement

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NOVEL TRANSLINEAR-BASED MULTI-OUTPUT FTFN

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ABSTRACT

A novel circuit configuration for realizing multi-output four-terminal floating nullor in bipolar monolithic integrated circuit form is described. The circuit is simple and based on the use of an improved translinear cell type circuit, which provide wide bandwidth and dynamic range. The characteristics of this circuit are confirmed by HSPICE simulation results. The performance of the FTFN-based current-mode and inverse filters are also included.

1. INTRODUCTION

At present, current-mode circuits have drawn a considerable attention due to their definite advantages, which are elementary wide bandwidth, wider dynamic range, simpler circuitry and low power consumption [1]. Recently, active devices widely used in current-mode circuit are usually a second-generation current conveyor (CCII), a current feedback op-amp (CFOA), a four-terminal floating nullor (FTFN) and an operational transconductance amplifier (OTA). However, it has been shown that the FTFN is more flexible and versatile building block than other active devices [2][3]. Interest in using FTFNs to design current-mode circuits has increased recently; for example, filters, gyrators, simulated floating impedances and sinusoidal oscillators based on these elements have been reported [3][4]. This is due to the fact that the FTFN-based structures provide a number of potential advantages such as: complete absence of passive component-matching requirement, minimum number of employed passive elements and improvement of high frequency characteristic. Although, in general, FTFN-based and CCII-based current-mode circuits can simply be designed through a systematic transformation, based on the use of a nullor which consist of a nullator and a norator, from a regular RC active circuit. However, it owe to the fact that when using the transformed nullor equivalent circuit the nullator/norator pair can simple be replaced by an FTFN without imposing any restrictions. In addition, by designing through a dual transform technique, the transformed current-mode FTFN-based circuit requires a high output impedance source, for which a current source is suitable. This also enables the circuit to be used in cascade form.

At first, many FTFN realization schemes are based on the use of the conventional op-amps as the major active element [3][5]. These realization schemes are less appropriate for high frequency applications and are uneconomical for applying to an integrated circuit form, since each op-amp will require a substantial chip area by itself. On the other hand, the realization schemes suitable for implementing in monolithic integrated form have been available [6][7] [8] but even so they are too complicated. This paper shows an alternative form for realizing a monolithically integrable multiple-output FTFN, which affords higher gain and wider dynamic range. The proposed scheme is based on the use of an improved bipolar translinear cell [9]. In addition, the number of output ports can be additionally expanded to support the designer applications. For example, recently, there are some interests on realizing FTFN, which has extended more than four terminals such as the so called a five terminal floating nullor (FiTFN) [10]. Therefore, the realization of the FiTFN and its applications will also be discussed. The current-mode filter and inverse filter transformed from Sallen-Key filter [3], are adopted for illustrating the performance of the proposed circuit.

2. CIRCUIT DESCRIPTION

Generally, FTFN is a high gain transconductance amplifier with floating input and output terminals or can be called as an operational floating amplifiers (OFAs) [7]. Fig. 1(a) shows a nullor model of a FTFN, which is equivalent to an ideal nullor. The port relations of the FTFN can be characterized as

$$V_1 = V_2 \qquad I_1 = I_2 = 0 \qquad I_{o1} = -I_{o2} \tag{1}$$

where, it should be noted that the output impedance of the W and Z ports are generally arbitrary. However, most of the FTFNs are traditionally realized from the basic type shown in Fig. 1(b), where the output impedance of the W-port is very low while the impedance of the Z-port is very high. This type of FTFN is also called as operational mirrored amplifiers (OMAs) [6].

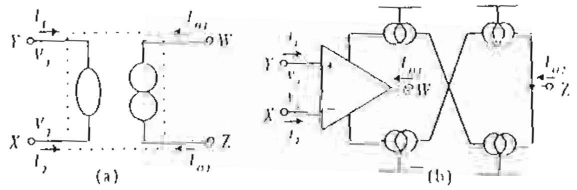

Figure 1. Model of a FTFN (a) An ideal nullor model. (b) Traditional implementation model.

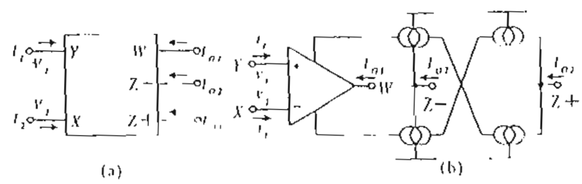

Figure 2. (a) Symbol of multi-output FTFN. (b) Possible implementation of multi-output FTFN.

4. SIMULATION RESULTS

The performance of the proposed circuit in Fig. 3 is verified by HSPICE analogue circuit simulation program. All NPN and PNP bipolar transistors are ALA400's NX1 and PX1, respectively, obtained for AT&T's CBIC-R process [11]. The bias currents are set to I_{B1} = 2 mA, $I_{B2} = I_{B3}$ = 50 μA and the power supply voltages are taken as V_{CC} = +5V and V_{EE} = -5V. The simulated D.C. offset voltage between port X and port Y is approximately 200 μV, the output offset currents at port Z- and port Z+ are about 3 μA and 13 μA, respectively. The output impedances at ports W, Z- and Z+ are 10.7 kΩ, 1.4 MΩ and 1.13 MΩ, respectively. The simulated current following operation of the Fig. 6 shows that the circuit can exhibit the linear response over a very wide current range. Fig. 7 shows the characteristic of the open loop transconductance gain of the proposed circuit. The transconductance gain of about 1.8 A/V is achieved, where this value is much greater than the transconductance gains of the circuits in [6], [7] and [8]. This is owing to the advantage of the high current gain of bipolar transistor. From the response it can be estimated the -3 dB bandwidth in a very high frequency as nearly as 2.8 MHz.

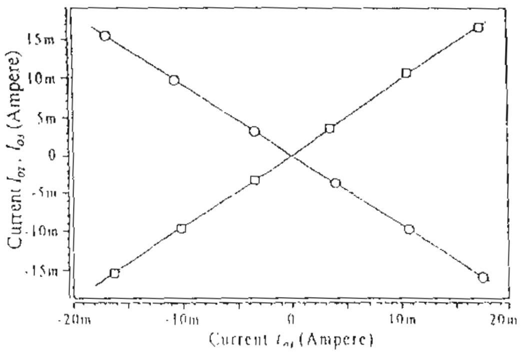

Figure 6. Current following operation at the output port.
-□- Current I_{O2} from port Z-
-○- Current I_{O3} from port Z+

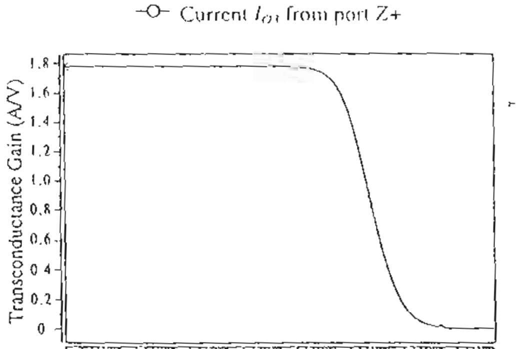

Figure 7. Simulated open loop transconductance gain.

The voltage and current transfer characteristic of the CCIIs are chosen as examples to denote the performance of the active devices presented in Fig. 5. Fig. 8(a) shows the voltage transfer characteristic from port Y to port X whereas Fig. 8(b) shows the current transfer characteristic from port X to port Z. Noting that only the characteristics of the Fig. 8(a) and Fig. 8(b) are demonstrated. It can be expected that the other active devices are also giving a good achievement.

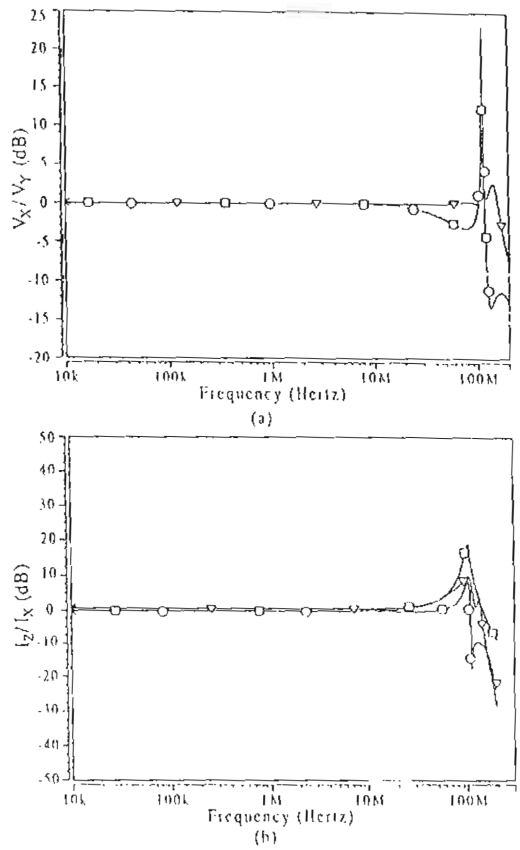

Figure 8. (a) Voltage transfer characteristic from port Y to port X. (b) Current transfer characteristic from port X to port Z.
-○- CCII+ from Fig. 5(b)
-□- CCII- from Fig 5(c)
-▽- CCII- from Fig. 5(d)

In the Leuciuc's work [12], it has been specified that an inappropriate implementation of the nullors can lead to errors in the realization of inverse circuit. Therefore, a current-mode inverse filter is a good example to demonstrate the correctness and the usefulness of the proposed circuit. The FTFN-based current-mode filter and its inverse filter, transformed from the Sallen-Key voltage-mode 2nd order low-pass filter through the using RC:CR dual transformation technique [3], are shown in Fig. 9(a) and Fig. 9(b), respectively. The transfer function of the current-mode Sallen-key low-pass filter and the current-mode Sallen-Key inverse low-pass filter are:

$$\frac{i_{out}}{i_{in}} = \frac{k\left[\dfrac{1}{R_1R_2C_1C_2}\right]}{s^2 + s\left[\dfrac{1}{R_1C_1} + \dfrac{1}{R_1C_2} + \dfrac{1-k}{R_2C_2}\right] + \left[\dfrac{1}{R_1R_2C_1C_2}\right]} \qquad (3)$$

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Paper: 2924
Session: Current-Mode Circuits
Time: Wednesday, May 29, 2:30:00 PM - 2:45:00 PM
Presentation: Lecture
Topic: Analog Circuits: Analog Signal Processing and Filtering

Title: CURRENT-MODE LEAPFROG LADDER FILTERS USING CDBAs

Authors: Worapong TANGSRIRAT
Nobuo FUJII
Wanlop SURAKAMPONTORN

Abstract: In this paper, a possible realization of a current differencing buffered amplifier (CDBA) in the low-voltage operation is proposed. A leapfrog simulation of the current-mode ladder network using the CDBA as active circuit building blocks is then introduced. In order to demonstrate that the CDBA considerably simplifies the leapfrog structure of the current-mode ladder filters, a fifth-order Butterworth low-pass filter and a sixth-order Chebyshev bandpass filter which require a minimum of active components will be presented. PSPICE simulation results are employed to verify the correctness of the realization procedure.

CURRENT-MODE LEAPFROG LADDER FILTERS USING CDBAs

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ABSTRACT

In this paper, a possible realization of a current differencing buffered amplifier (CDBA) in the low-voltage operation is proposed. A leapfrog simulation of the current-mode ladder network using the CDBA as active circuit building blocks is then introduced. In order to demonstrate that the CDBA considerably simplifies the leapfrog structure of the current-mode ladder filters, a fifth-order Butterworth low-pass filter and a sixth-order Chebyshev bandpass filter which require a minimum of active components will be presented. PSPICE simulation results are employed to verify the correctness of the realization procedure.

1. INTRODUCTION

During the past few years, comparing with voltage-mode techniques, current-mode signal processing techniques have been received a wide attention due to its wide bandwidth, low-voltage operation and simple implementation of signal operations such as addition and subtraction [1]. At present, a number of current-mode circuit techniques, such as second-generation current conveyors (CCIIs), current feedback amplifiers (CFAs) and current mirror-based circuits, have been developed. Among these topologies, the CCII has been proved to be a flexible and versatile current-mode building block, which can be widely found in many realizations of the active network synthesis. However, CCII-based circuits in voltage-mode designs require some additional devices when they are used for cascading sections due to the high-output impedance of its output port [7]. Also note that it may require a large number of active components in some circuit implementations.

Recently, a current differencing buffered amplifier (CDBA) has been first proposed [2], which is particularly suitable for the current-mode operation and realization of continuous-time filters. The CDBA can offer such as high-slew rate, wide bandwidth and simple implementation [3]. Therefore, the goal of this paper is to propose a simple design procedure for the implementation of the general current-mode ladder filters, widely used in analog signal processing systems, by using CDBAs. The realization is derived based on the use of leapfrog simulation corresponding to the passive RLC ladder prototypes. The presented method shows that the CDBA-based leapfrog simulation is simple and suitable for realizing of the current-mode ladder filters. Most importantly, current-mode ladder filters with CDBAs employ less active components than compare with CCIIs-based ladder filter implementations.

2. CIRCUIT DESCRIPTION

The circuit representation of the CDBA is shown in Fig.1 and its current and voltage characteristics can be described by the following relations [2-3]:

$$v_p = 0 \ , \ v_n = 0 \ , \ i_z = i_p - i_n \ \text{ and } \ v_w = v_z \qquad (1)$$

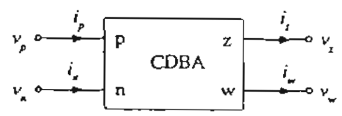

Fig.1 : CDBA circuit representation

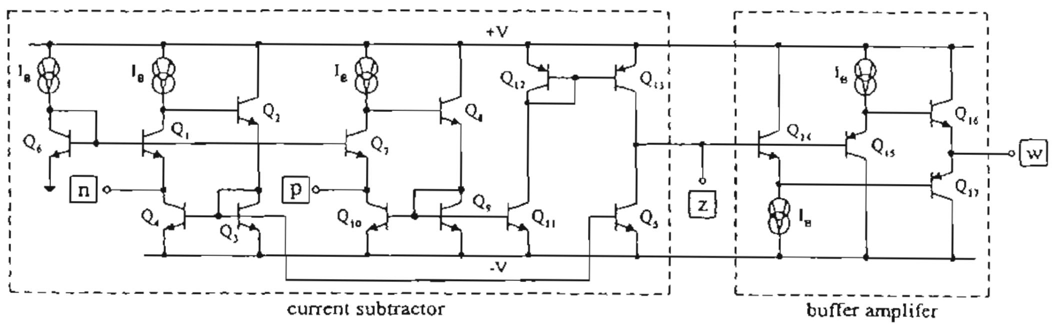

Fig.2 : Proposed realization of CDBA in the low-voltage operation

It should be noted from the above expression that the differential input current i_p-i_n is converted to the output voltage v_w through an impedance connected at the port z. Thus the CDBA basically consists of two blocks, current differencing circuit (current subtractor) and voltage follower. The proposed realization of the low-voltage CDBA in bipolar technology is shown in Fig.2, where group of transistors Q_1-Q_4 and Q_7-Q_{10} function as low-input resistance input stages [4], and complementary NPNs and PNPs Q_{14}-Q_{17} form the buffer stage that forces the w terminal to the potential of the z terminal.

3. CURRENT-MODE LEAPFROG LADDER FILTERS USING CDBAs

An approach to derive CDBA-based current-mode ladder filters from passive RLC ladder prototypes is presented in this section. Due to the doubly terminated RLC ladder filters share all the low sensitivity and low component spread of the RLC prototypes [5-6], this configuration has been receiving considerable attention and popular. These active implementations are conventionally designed by based on the representation of signals as voltages. But in the current-mode based implementation, the input, intermediate and output signals are usually represented as electrical currents that seem to be recognized to offer potential advantage for useful both in continuous-time and in sample-data signal processing. To demonstrate the procedure for the design of a CDBA-based current-mode ladder filter by the leapfrog, consider a popular ladder structure that uses to realize the doubly terminated RLC ladder filter shown in Fig.3. This structure can be characterized by the following expression :

$$
\begin{aligned}
I_1 &= I_S - \frac{V_1}{R_S} - I_2 \quad, & V_1 &= I_1 Z_1 \\
V_2 &= V_1 - V_3 \quad, & I_2 &= V_2 Y_2 \\
I_3 &= I_2 - I_4 \quad, & V_3 &= I_3 Z_3 \\
&\vdots \\
V_n &= V_{n-1} - V_{n+1} \quad, & I_n &= V_n Y_n
\end{aligned}
\tag{2}
$$

and

$$
I_n = I_{n-1} - I_{n+1} \quad, \quad V_n = I_n Z_n
$$

As shown in Fig.3, a LC ladder filter structure can be represented by the block diagram of a leapfrog realization as shown in Fig.4. Observe that in this figure the repeated use of two operations of Fig.5(a) and 5(c) makes up the complete circuit. By using these operations, it can easily be realized by the active-RC circuit involving CDBAs. For the CDBA-based realization, it can readily obtain the CDBA-RC circuit by interconnecting the corresponding sub-circuits of Fig.5(b) and 5 (d) according to the overall block diagram representation of Fig.4.

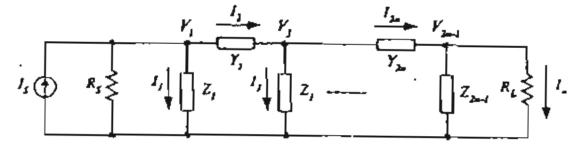

Fig.3 : A general doubly terminated RLC ladder network

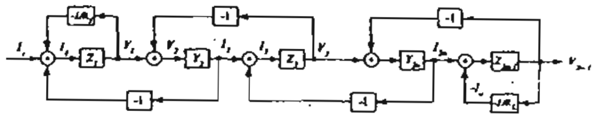

Fig.4 : Block diagram representation of the leapfrog structure

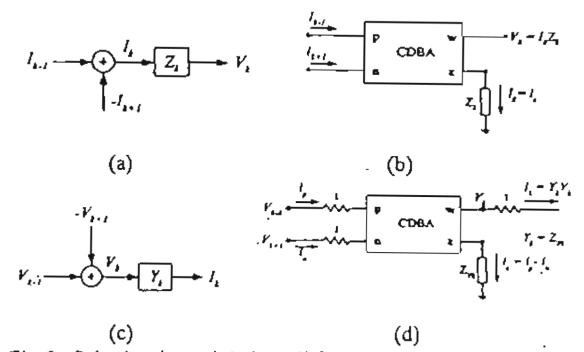

Fig.5 : Sub-circuits and their realizing operation using CDBAs

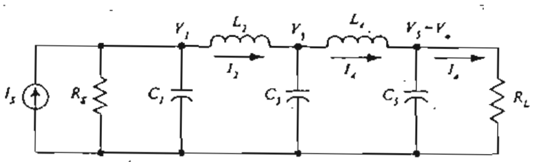

Fig.6 : Current-mode fifth-order Butterworth RLC ladder lowpass filter

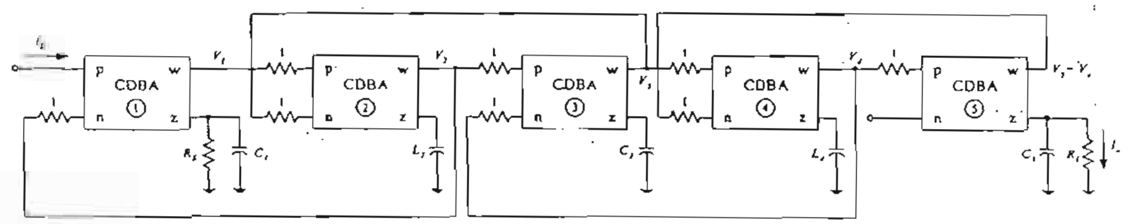

Fig.7 : Current-mode fifth-order Butterworth lowpass filter using CDBAs

As an application of this proposed design procedure, a current-mode fifth-order Butterworth RLC ladder lowpass filter shown in Fig.6 is realized as an example and the resulting circuit is shown in Fig.7. It can be seen that only five CDBAs are employed for implementation of the fifth-order filter. Therefore, in general, n CDBAs are required for realizing of the nth-order filters. This means that the circuits using CDBAs can reduce the number of active components by 50% comparing with the CCII-based circuit implementation [7].

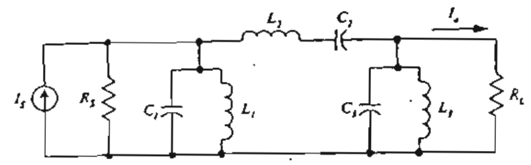

Fig.8 : Current-mode sixth-order RLC bandpass filter

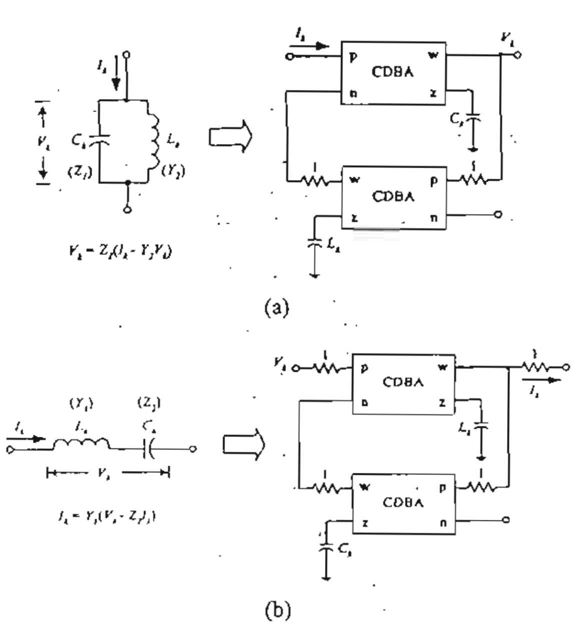

Fig.9 : Sub-circuits of the filter of Fig.8 involving CDBAs

Furthermore, this method can also be used to apply in the design of RLC bandpass filter. Consider a current-mode sixth-order RLC bandpass filter shown in Fig.8. The corresponding sub-circuits of the filter using CDBAs are shown in Fig.9. Based on their realizing operation using CDBAs, the obtained circuit can be shown in Fig.10.

4. SIMULATION RESULTS AND DESIGN EXAMPLES

In order to verify the correctness of the above given filter realization procedure, the low-voltage CDBA of Fig.2 was simulated by PSPICE simulation using the 0.7μm BiCMOS process parameters. The power supply voltage is $\pm V = \pm 1$ volts and all bias currents I_B, which is realized by current mirror circuits, were set to be 200 μA. Fig.11 shows the simulated current and voltage transfer characteristics with R_z = 1 kΩ and R_w = 10 kΩ, which is clearly seen that the cutoff frequencies in the order of a hundred MHz are obtained. The simulated responses demonstrate that the circuit behaves the linear response over a wide operating range.

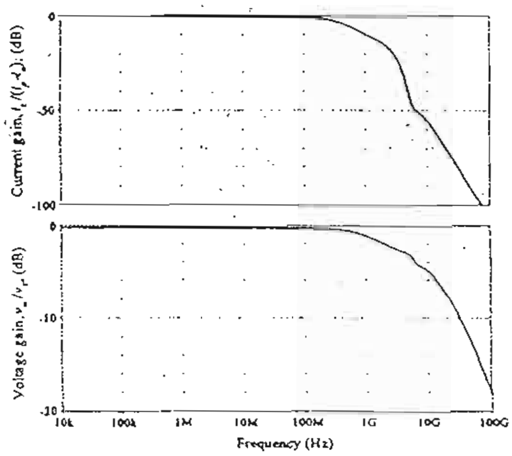

Fig.11 : Simulated frequency responses of the CDBA of Fig.2

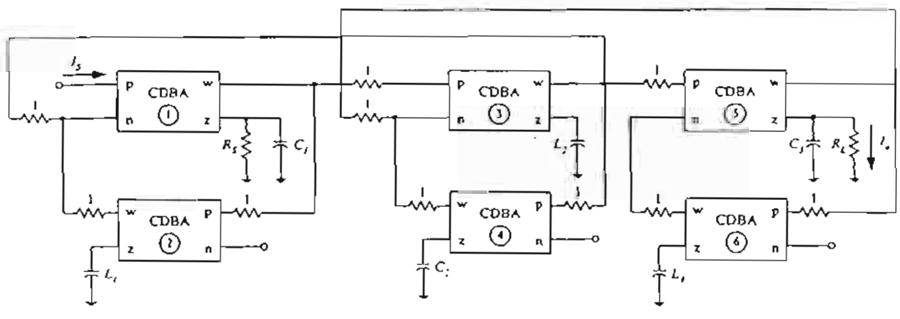

Fig.10 : Current-mode sixth-order bandpass filter using CDBAs

As an illustration of a current-mode fifth-order Butterworth lowpass filter, the filter of Fig.7 with a half-power frequency ω_{3dB} of 100 Mrad/s was designed. This condition leads to the passive element values chosen as follows, $R_S = R_L = R = 1$ kΩ, $C_1 = C_5 = 6.18$ pF, $L_2 = L_4 = 16.18$ pF, $C_3 = 20$ pF. The simulated and theoretical responses are shown in Fig.12.

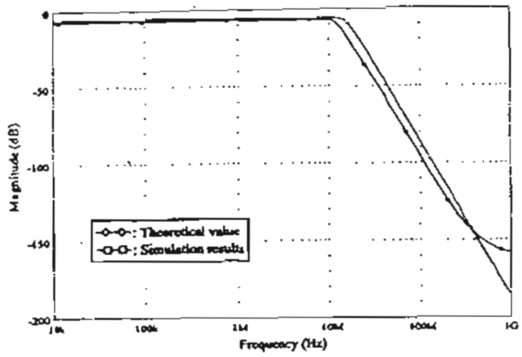

Fig.12 : Simulated response of fifth-order Butterworth lowpass filter of Fig.7

For demonstration purposes a sixth-order Chebyshev bandpass filter according to the circuit configuration shown in Fig.10 was designed with the following specifications : ω_{3dB} = 100 Mrad/s, bandwidth (BW) = 0.45, and ripple width = 0.1 dB. The approximation of this filter resulted in the following components values : $R_S = R_L = R = 1$ kΩ, $C_1 = C_3 = 22.923$ pF, $C_2 = 3.921$ pF, $L_1 = L_3 = 4.362$ pF, $L_2 = 25.498$ pF. The simulated response of the designed filter verifying the theoretical value is shown in Fig.13.

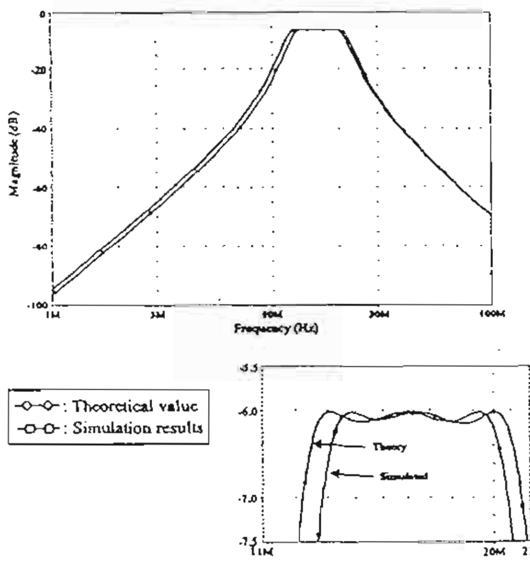

Fig.13 : Simulated response of sixth-order Chebyshev bandpass filter of Fig.10

5. CONCLUSION

A design technique to realize continuous–time current-mode filters employing CDBAs is proposed. Minimum active component counts have been obtained from the simulation of the passive LC ladder network. As an example, a fifth-order Butterworth lowpass filter and a sixth-order Chebyshev bandpass filter are designed and simulated using the PSPICE simulation program. The usefulness and correctness of the proposed design procedures have been confirmed by the simulation results.

6. ACKNOWLEDGMENT

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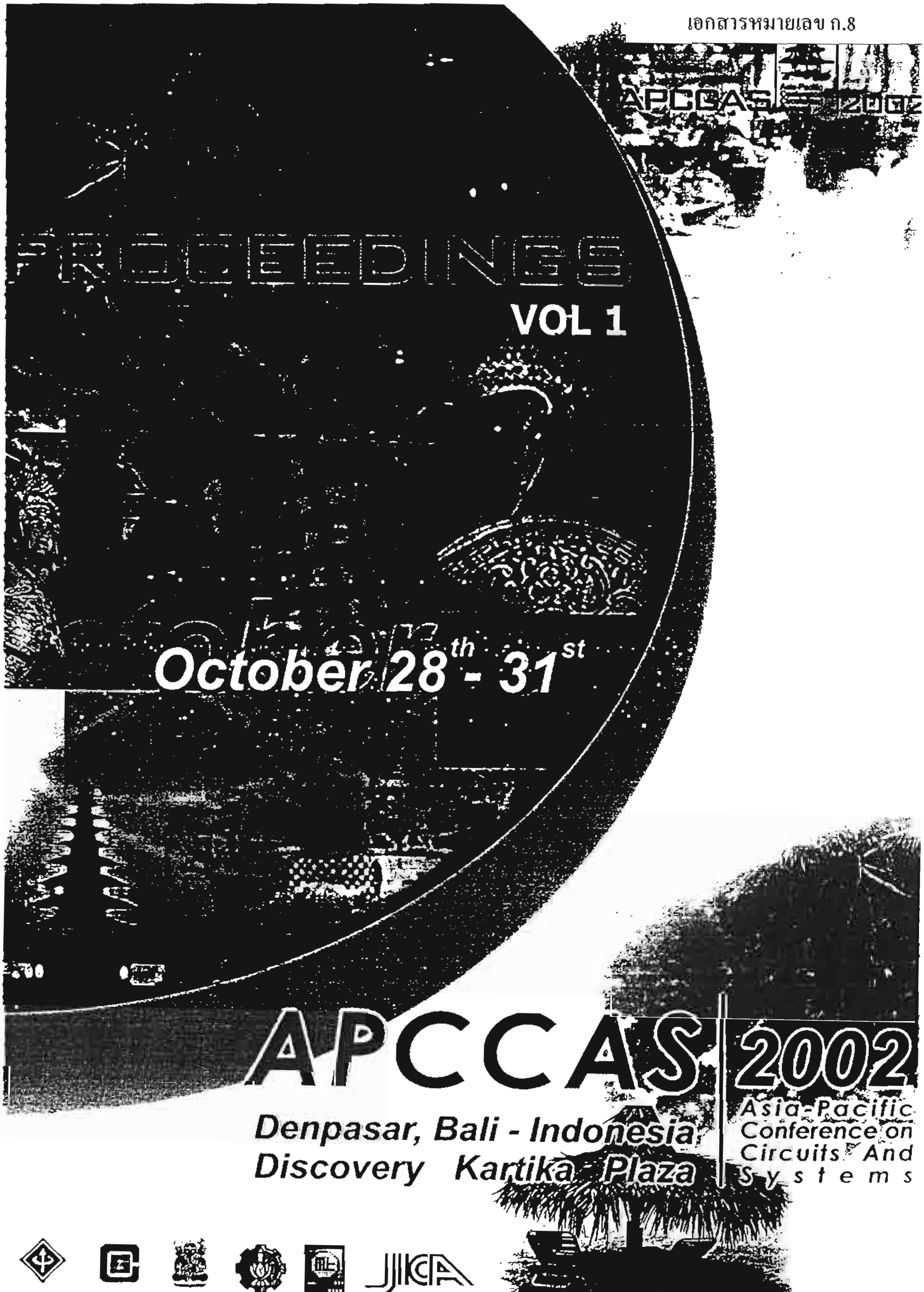

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SINGLE-INPUT AND THREE-OUTPUT CURRENT-MODE BIQUADRATIC FILTERS USING MULTIPLE-OUTPUT OMAs

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ABSTRACT

A novel circuit configuration for the realization of the single-input and three-output (SITO) current-mode biquadratic filters employing only three multiple-output OMAs is presented. The proposed circuit can simultaneously realize lowpass, bandpass and highpass filter functions at three high-impedance outputs without changing the circuit configuration and elements. Moreover, the resultant current-mode filter provides low passive and active sensitivities, uses of only grounded passive elements and can be orthogonal tuned of the parameters ω_o and Q-factor.

1. INTRODUCTION

Owing to the usefulness and advantages of operational mirrored amplifiers (OMAs) and four-terminal floating-nullors (FTFNs) over current conveyors (CCs) [1]-[4], there has been great emphasis in the design and implementation of analog signal processing circuits using OMAs and FTFNs as active elements. In the recent past, several techniques for realizing floating immittances and current-mode filters using OMAs and FTFNs have been described by various authors [1]-[2], [5]-[8]. One of these filters known as a current-mode single-input and three-output (SITO) type multifunction filter which offers particularly attractive features, such as, simultaneously realizes lowpass (LP), bandpass (BP) and highpass (HP) filter characteristics without changing the circuit configuration and elements, provides high-impedance current outputs [9]-[12]. Only SITO current-mode biquadratic filter that obtains the mentioned advantages using OMAs as active elements has been recently presented [12]. However, it requires four OMAs, floating passive elements and, more importantly, its parameters ω_o and Q-factor are interdependent.

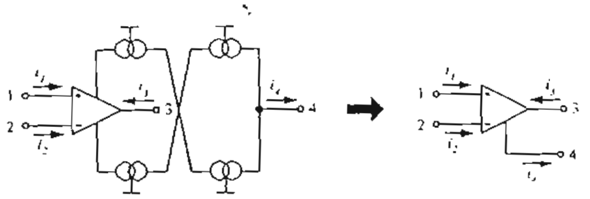
The major goal of this paper is to present the SITO current-mode biquadratic filter employing only three multiple-output OMAs with all grounded elements. The number of active elements proposed here is less than that required by the previous SITO filter proposed in reference [12], when the filter provides three high output impedance current output. The proposed filter realizes three current transfer functions simultaneously and all passive and active sensitivities are quite low. Moreover, it offers the attractive feature of independent grounded-element control of the parameters ω_o and Q-factor

2. PROPOSED CONFIGURATION

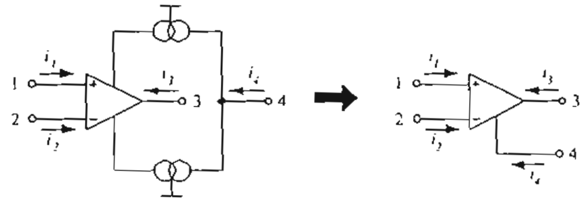
2.1 Operational mirrored amplifiers (OMAs)

Fig.1 shows the circuit implementation and representation of the operational mirrored amplifiers (OMAs). The negative OMA (OMA-), comprising an op-amp and two pairs of current mirrors as shown in Fig.1(a), is a more general and flexible device owing to it can be equivalent to an ideal nullor or FTFN [3],[13]. Whereas the other type of OMA which requires only one pairs of current mirrors is named the positive OMA (OMA+) and is shown in Fig.1(b). Therefore, it can be concluded from the Fig.1 that the port characteristics of the OMA can be characterized as :

$$v_2 = v_1 \quad , \quad i_1 = i_2 = 0 \quad \text{and} \quad i_4 = i_3 \tag{1}$$



(a)



(b)

Figure 1 : Circuit implementation and circuit representation of the OMAs
(a) negative OMA (b) positive OMA

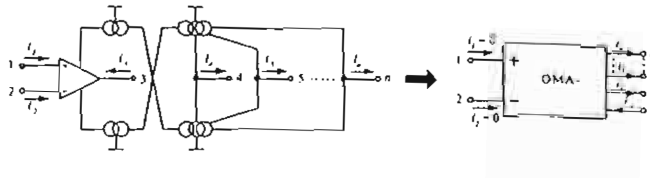
2.2 Multiple-output OMAs

For realizing the multiple-output OMA, it can easily be modified from the conventional OMA realization of the Fig.1 by adding n-output current mirror terminals as shown in Fig.2. Thus, the resulting building blocks become the multiple-output OMAs, which can be described by the following port relations :

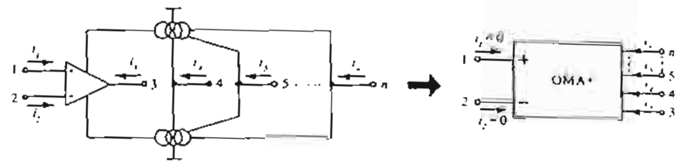
$$v_2 = v_1 \quad , \quad i_1 = i_2 = 0 \quad \text{and} \quad i_n = .. = i_5 = i_4 = i_3 \tag{2}$$

2.3 Proposed SITO current-mode filter

Fig.3 shows the proposed current-mode filter with single-input and three-output terminals using three multiple-output OMAs, four grounded-resistors and two grounded-capacitors. According to the port relations of the multiple-output OMA from equation (2), a elementary circuit analysis shows that the current transfer functions of this circuit can be expressed as .



(a)



(b)

Figure 2 : Multiple-output OMAs
(a) negative multiple-output OMA
(b) positive multiple-output OMA

$$T_{HP}(s) = \frac{I_{o1}(s)}{I_{in}(s)} = \frac{s^2\left(\frac{R_3}{R_4}\right)}{D(s)} \tag{3}$$

$$T_{BP}(s) = \frac{I_{o2}(s)}{I_{in}(s)} = \frac{s\left(\frac{R_2 R_3 C_2}{R_4}\right)}{D(s)} \tag{4}$$

$$T_{LP}(s) = \frac{I_{o3}(s)}{I_{in}(s)} = \frac{\left(\frac{R_3}{R_1 R_2 R_4 C_1 C_2}\right)}{D(s)} \tag{5}$$

where $D(s) = s^2 + s\left(\frac{R_3}{R_1 R_4 C_1}\right) + \left(\frac{R_3}{R_1 R_2 R_4 C_1 C_2}\right)$

The equations (3) to (5) show that this filter can realize the highpass $T_{HP}(s)$, bandpass $T_{BP}(s)$, and lowpass $T_{LP}(s)$, current transfer functions simultaneously without changing the circuit configuration and elements. Moreover, it can also provide a high-impedance output port that is suitable for cascadable systems and it contains only grounded elements. Noting that the advantage for filters that employ grounded capacitors is the case of the integrated circuit implementation [14].

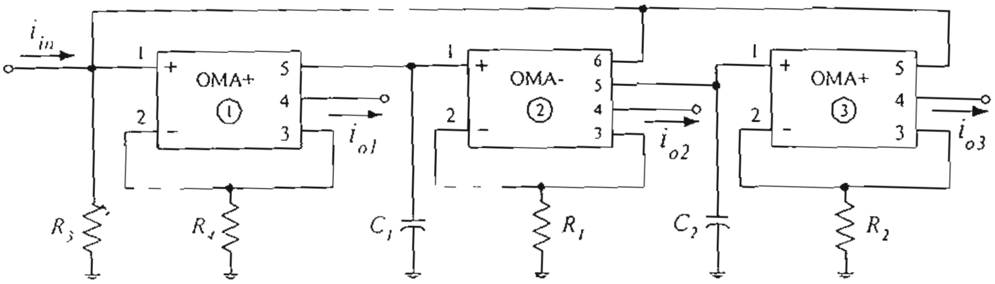


Figure 3 : Proposed SITO current-mode biquadratic filters using multiple-output OMAs

The natural angular frequency ω_o and the Q-factor of this configuration can be given by :

$$\omega_o = \sqrt{\frac{R_3}{R_1 R_2 R_4 C_1 C_2}} \tag{6}$$

and

$$Q = \sqrt{\frac{R_1 R_4 C_1}{R_2 R_3 C_2}} \tag{7}$$

Then the passive sensitivities of ω_o and Q-factor are

$$S^{\omega_o}_{R_1} = S^{\omega_o}_{R_2} = -S^{\omega_o}_{R_3} = S^{\omega_o}_{R_4} = S^{\omega_o}_{C_1} = S^{\omega_o}_{C_2} = -\frac{1}{2} \tag{8}$$

$$S^{Q}_{R_1} = -S^{Q}_{R_2} = -S^{Q}_{R_3} = S^{Q}_{R_4} = S^{Q}_{C_1} = -S^{Q}_{C_2} = \frac{1}{2} \tag{9}$$

It can be found that all of the sensitivities with respect to the passive elements are less than unity.

Furthermore, by setting $R_1 = R_3 = R_A$, $R_2 = R_4 = R_B$ and $C_1 = C_2 = C$, then the parameters ω_o and Q-factor of this filter, from equations (6) and (7), will be rewritten as :

$$\omega_o = \frac{1}{R_A C} \tag{10}$$

and

$$Q = \frac{R_A}{R_B} \tag{11}$$

It is important to noted from equations (10) and (11) that the natural angular frequency ω_o can be varied by tuning the value of the grounded resistor R_A and/or the grounded capacitor C without disturbing the value of Q-factor. Moreover, the Q-factor can be independently controlled through a single grounded resistor R_B. Therefore, the proposed filter provides orthogonal grounded-element control of the parameters ω_o and Q-factor.

3. EFFECTS OF THE NON-IDEALITIES OF THE MULTIPLE-OUTPUT OMAs

By taking into consider the non-ideal performance of the multiple-output OMA, its characteristics can be modeled as $v_2 = \beta . v_1$, $i_n = \ldots = i_5 = i_4 = \alpha . i_3$, where $\beta = 1 - \varepsilon$, ($|\varepsilon| \ll 1$), denotes the input voltage tracking error and $\alpha = 1 - \delta$, ($|\delta| \ll 1$), represents the output current tracking error of the multiple-output OMA. In this case, reanalysis of the configuration in Fig.3 shows that the current transfer functions become :

$$T_{HP}(s) = \frac{I_{o1}(s)}{I_{in}(s)} = \frac{s^2\left(\dfrac{\beta_1 \alpha_1 R_3}{R_4}\right)}{D_n(s)} \tag{12}$$

$$T_{BP}(s) = \frac{I_{o2}(s)}{I_{in}(s)} = \frac{s\left(\dfrac{\beta_1 \beta_2 \alpha_1 \alpha_2 R_3}{R_1 R_4 C_1}\right)}{D_n(s)} \tag{13}$$

$$T_{LP}(s) = \frac{I_{o3}(s)}{I_{in}(s)} = -\frac{\left(\dfrac{\beta_1 \beta_2 \beta_3 \alpha_1 \alpha_2 \alpha_3 R_3}{R_1 R_2 R_4 C_1 C_2}\right)}{D_n(s)} \tag{14}$$

and $\quad D_n(s) = s^2 + s\left(\dfrac{\beta_1 \alpha_1}{R_1 C_1}\right) + \left(\dfrac{\beta_1 \beta_2 \beta_3 \alpha_1 \alpha_2 \alpha_3 R_3}{R_1 R_3 R_4 C_1 C_2}\right)$

where β_i and α_i , (i = 1, 2, 3), are the voltage- and the current-tracking errors of the i-th multiple-output OMA. By using the same condition mentioned above, the parameters ω_{on} and Q_n-factor for the non-ideal cases can be given, respectively, by

$$\omega_{on} = \frac{1}{R_A C}\sqrt{\beta_1\beta_2\beta_3\alpha_1\alpha_2\alpha_3} \qquad (15)$$

$$Q_n = \frac{R_A}{R_B}\sqrt{\frac{\beta_3\alpha_3}{\beta_1\beta_2\alpha_1\alpha_2}} \qquad (16)$$

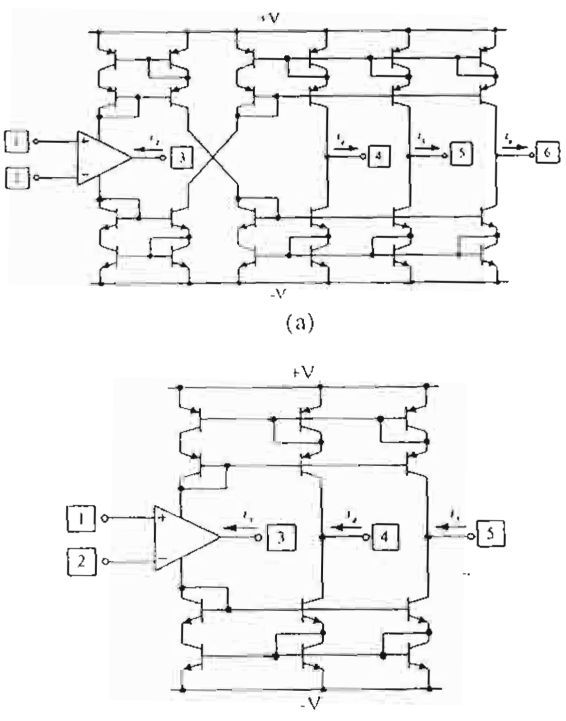
Hence, its active sensitivities for this case are obtained as

$$S^{\omega_{on}}_{\beta_1,\beta_2,\beta_3} = S^{\omega_{on}}_{\alpha_1,\alpha_2,\alpha_3} = \frac{1}{2} \qquad (17)$$

$$S^{Q_n}_{\beta_1,\beta_2} = S^{Q_n}_{\alpha_1,\alpha_2} = -\frac{1}{2} \qquad (18)$$

and $$S^{Q_n}_{\beta_3} = S^{Q_n}_{\alpha_3} = \frac{1}{2} \qquad (19)$$

all of which are equal to 0.5 in magnitude.



(a)

(b)

Figure 4 : Possible realizations of multiple-output OMAs using power-supply current-sensing technique
(a) negative multiple-output OMA
(b) positive multiple-output OMA

4. SIMULATION RESULTS

To verify the validity of the proposed configuration, the filter of Fig.3 has been simulated through the use of a PSPICE simulation program. In the simulation, possible realizations of multiple-output OMAs using power-supply current-sensing technique [15] are shown in Fig.4. The OMAs were built by employing AD704 operational amplifier together with improved Wilson current mirrors composed of *pnp* 2N2907A and *npn* 2N2222A transistors. The biasing power supplies used were taken as $\pm V = \pm 15V$ and the capacitor values were $C_1 = C_2 = 5$ nF.

Fig.5 represents the frequency responses, all the three current functions, obtained with the following values for passive components : $R_A = R_B = 10$ kΩ, designed for $Q = 1$ and $f_o = 3.18$ kHz.

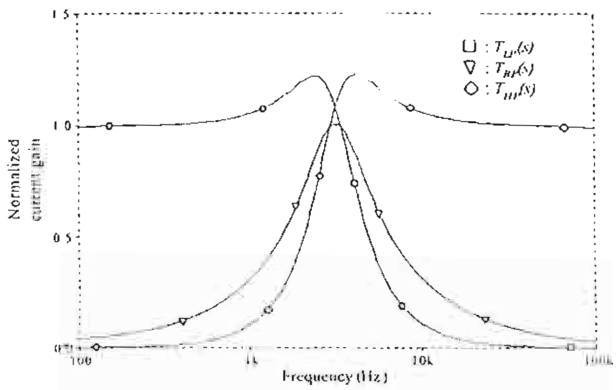


Figure 5 : Frequency responses of LP, BP and HP filters obtained from the circuit of Fig.3 with $R_A = R_B = 10$ kΩ and $C_1 = C_2 = 5$ nF.

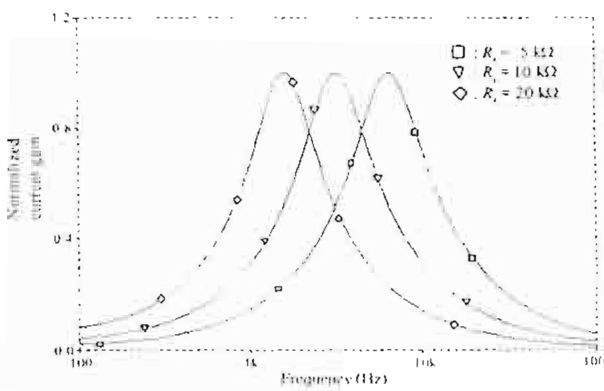


Figure 6 : Simulation results of BP response for various values of ω_o.

As an illustration of the controllability of the natural frequency ω_o, Fig.6 shows bandpass output responses for three different values of $R_i = R_A = R_B$; i.e., $R_i = 5$ kΩ, 10 kΩ and 20 kΩ. The corresponding natural frequency obtained by simulation are 6.45 kHz, 3.23 kHz and 1.62 kHz, respectively, which are in good agreement with theoretical values calculated from equation (10) : 6.36 kHz, 3.18 kHz and 1.59 kHz, respectively.

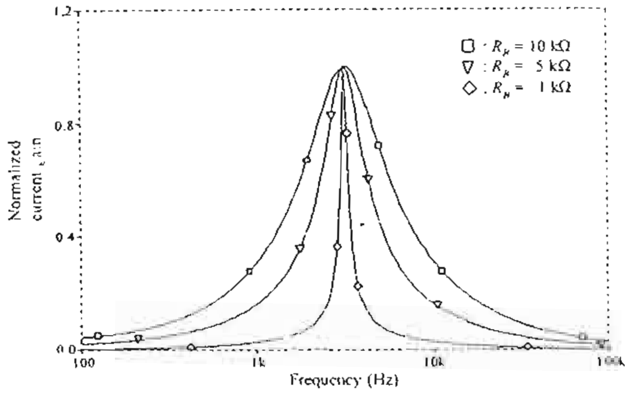


Figure 7 : Simulation results of BP response for various values of Q-factor

The obtained responses of the bandpass output for variable Q-factor (i.e.; Q-factor = 1, 2, 10) are shown in Fig.7, while R_A set to constant at 10 kΩ. This figure shows that the various values of Q-factor can be obtained by varying R_B without disturbing the parameter ω_o. It can be concluded from above mentioned that in both cases the filter characteristics are very close to the theoretical analysis which is deduced from equations (10) and (11).

5. CONCLUSIONS

A variety of new single-input and three-output (SITO) current-mode biquadratic filters using only three multiple-output OMAs has been proposed. The proposed filter provides the following advantages :

(i) simultaneous realization of lowpass, bandpass and highpass current transfer functions without changing the circuit configuration and elements.

(ii) employment of only grounded elements.

(iii) cascadable structure.

(iv) independent control of the parameters ω_o and Q-factor through grounded elements, and

(v) low passive and active sensitivities.

The validity of the proposed filter has been confirmed by the simulation results.

6. ACKNOWLEDGMENT

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A WIDE-BAND CURRENT-MODE OTA-BASED ANALOG MULTIPLIER-DIVIDER

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ABSTRACT

A current-mode analog multiplier-divider circuit that realized through the use of operational transconductance amplifiers (OTAs) is proposed in this paper. The proposed scheme is realized in such a way that employs only OTAs as active circuit elements and does not require external passive circuit elements. The circuit is simple and can be easily constructed from commercially available IC. The circuit is temperature compensated and the circuit bandwidth is approximately close to the bandwidth of pnp current mirrors or $f_{T}/2$. The performance of the multiplier-divider circuit is discussed and confirmed by simulation results.

1. INTRODUCTION

Analog multipliers and dividers are important nonlinear building blocks that have found useful in wide range of applications,particularly,in the fields of control, instrumentation, measurement, signal processing and telecommunication. At present, because of the main featuring of wider bandwidth, greater linearity, wider dynamic range and simple circuitry compared with their voltage-mode counterparts, current-mode circuits have been received growing interest in analog signal processing. Many techniques to design current-mode analog multiplier-divider circuits have been presented in the literatures. For examples, the methods that are suitable for CMOS integrated technology [1-3], and the methods that are implemented through the use of active circuit elements such as, for examples, current feedback amplifiers (CFAs) [4] and second-generation current-controlled current-conveyors (CCCIIs) [5].

It is well accepted that an OTA is one of the essential active building blocks in the design of analog circuits such as, for example, active filters, active networks and oscillators [6,7]. This is due to the fact that an OTA is a low-cost device that has only a single high-impedance node and its transcondeuctance gain g_m can be linearly controlled over more than four decades by means of an external bias current. The implementation of analog circuits in such a way that employs only OTA as standard cells will not only be easily constructed from readily commercial available IC, but also significantly simplified the design. In addition, the OTA-based circuit that requires no external passive element would facilitate its integratability and programmability [8]. Although, in the past, circuit techniques that employ OTAs to implement analog multiplier have been presented [7,9]. However, they are voltage-mode circuits, only multiplication functions are realized, and the circuit bandwidths are only about 2 MHz. In this paper, a current-mode temperature compensated multiplier-divider circuit using only OTAs as active circuit elements has been presented. The realization scheme does not require external passive elements. PSPICE simulation results will be used to demonstrate the performance of the proposed realization scheme.

2. BASIC PRINCIPLE

In this work, a bipolar-based OTA will be employed as an active circuit element, where its schematic diagram is shown in the Fig.1. The commercially available OTAs of this type are such as LM13600 and CA3280. By assuming that the OTAs are operated in the linear range, the OTA transconductance gain is $gm = I_B/2V_T$, which can be tuned by the DC bias current (I_B). The circuit diagram of the proposed current multiplier-divider circuit using OTAs is shows in Fig. 2. The input signal current i_{in1} is injected into the operational transconductance amplifier OTA1, which is connected as a current-controlled grounded resistor. The voltage across the OTA1 is then used as the input voltage for the OTA2 and OTA3. The input signal current i_{in2} is added with the bias current I_{B2} of the OTA2. Let g_{m1}, g_{m2} and g_{m3} be the transconductance gains of the OTA1, OTA2 and OTA3, respectively. Then, from routine circuit analysis, the output currents I_{O2} and I_{O3} of the OTA2 and OTA3, respectively, can be written as

$$I_{o2} = \frac{g_{m2}}{g_{m1}} i_{in1} = \frac{(I_{B2} + i_{in2})}{I_{B1}} i_{in1} \tag{1}$$

and

$$I_{o3} = -\frac{g_{m3}}{g_{m1}} i_{in1} = -\frac{(I_{B3})}{I_{B1}} i_{in1} \tag{2}$$

where $g_{m1} = I_{B1}/2V_T$, $g_{m2} = (I_{B2}+i_{in2})/2V_T$ and $g_{m3} = I_{B3}/2V_T$ and V_T is the usual thermal voltage. If we set the bias current such that $I_{B2} = I_{B3} = I_B$, the output current I_{out} of the circuit, that is the summation of the currents I_{O2} and I_{O3}, can be expressed as

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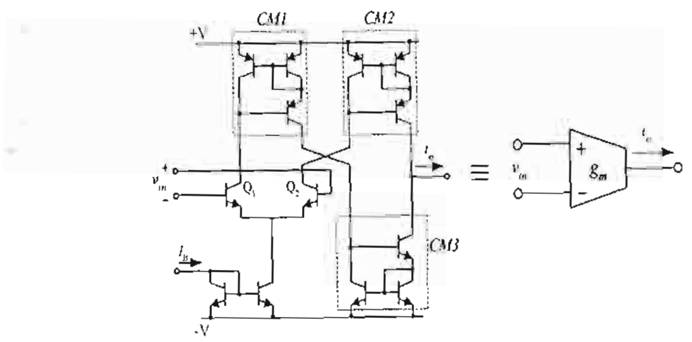

Figure 1. The schematic diagram of the OTA.

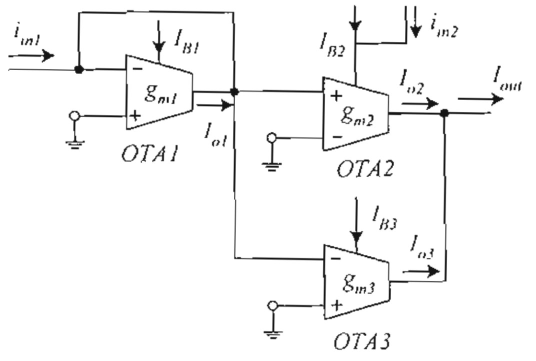

Figure 2. The proposed current-mode multiplier-divider cuicuit using OTAs.

$$I_{out} = I_{o2} + I_{o3} = \frac{i_{in1} i_{in2}}{I_{B1}} \tag{3}$$

which is in the form of a current-mode analog multiplication-division function. The circuit is performed as a four-quadrant multiplier if i_{in1} and i_{in2} are the input current signals. On the other hand, the circuit is performed as a divider circuit if i_{in1} (or i_{in2}) and I_{B1} are the input signal currents. It should be noted from the eqns. (1)-(3) that, since the output current I_{out} is in the form of the ratio of OTAs transconductance gains, therefore, the thermal voltages V_T's of the OTAs are compensated. This means that the output current I_{out} is less sensitive to temperature.

3. CIRCUIT PERFORMANCE

The major factors that contribute to the error and non-linearity in the circuit can be identified as follows. The first factor is due to the offset current at the output port of the OTA1. From eqn. (3), if I_{os} is the offset current at the output port of the OTA1, the output current I_{out} can be rewritten as

$$I_{out} = \frac{(i_{in1} \pm I_{os}) i_{in2}}{I_{B1}} \tag{4}$$

We can see that, apart from the multiplication-division result, this offset current produces a signal current that is proportional to the signal current i_{in2} to leak through the output. This effect can be reduced if $|i_{in1}| >> I_{os}$ and the bias current $I_{B1} >> I_{os}$. While the offset currents at the output ports of the OTA2 and OTA3 are not contribute to the multiplication error, but will produce a DC current at the output of the circuit.

The second factor that causes the non-linearity at the output of the circuit is due to the limited linear range of the input stages of the OTA2 and OTA3, where their input stages are conventional differential pairs. For linear operation, the input differential voltage of the bipolar-based OTA is restricted to be less than 26 mV. Therefore, to minimize this error, the voltage swing across the OTA1 should be kept to be less than 26 mV. On the other hand, it is means that the signal current i_{in1} should be limited to $|i_{in1}| < I_{B1}$.

For the high frequency response, consider the schematic diagram shown in the Fig.1. The OTA is comprised of three major building blocks, the common-base differential pairs (Q_1 and Q_2), the n-p-n current mirror (CM3) and the pnp current mirrors (CM1 and CM2). The bandwidth of the differential pair will be equal to f_α, which is approximately close to f_T of the n-p-n transistor or f_{TN}. For the current mirror, the bandwidth of Wilson's current mirror is approximately equal $f_T/2$. And, usually, the npn transistor f_{TN} is much higher than the lateral pnp transistor f_{TP}. Thus, the limitation to the high frequency performance of the proposed multiplier-divider circuit is mainly due to the bandwidth of the current mirrors CM2 and CM3, which is approximately equal to $f_{TP}/2$.

4. SIMULATION RESULTS

The performance of the proposed multiplier-divider circuit of Fig.2 was verified through the use of SPICE simulation results. All the OTA was simulated by using the bipolar transistor parameters of the 2N3904 and 2N3906 for the npn and pnp transistors, respectively, where $\beta_N = 416$ and $\beta_P = 180$. The transistors f_{TN} and f_{TP} were 400MHz and 300MHz, respectively. Since the DC offset current will distort the output signal, a DC current of about 5μA was injected at the output of the OTA1 to adjust the offset to be less than ±0.1μA. Noting that this offset can be reduced by using transistors with high value of beta, specially pnp transistors. The power supply voltages were set to V_{CC} = 10V and V_{EE} = -10V.

The multiplier function was tested by multiplying two sinusoidal signals. The results obtained are shown in Fig. 3 for i_{in1} = 0.5sin(2π1000t) mA, i_{in2} = 0.5sin(2π30000t) mA and I_{B1} = 1mA. Fig.4 shows the simulated DC transfer characteristics for the multiplier function, where the bias currents were set to $I_{B1} = I_{B2} = I_{B3}$ = 1mA.

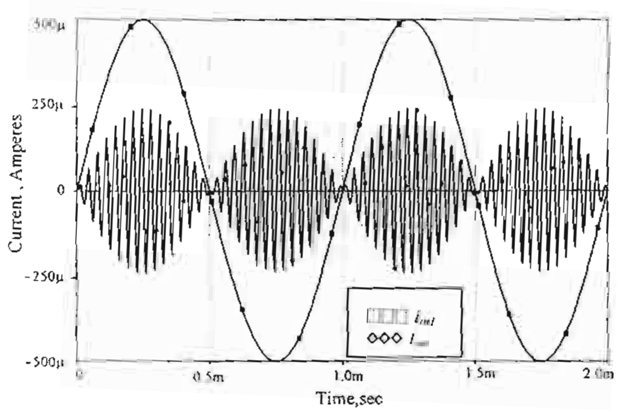

Figure 3. Simulated transient response for the multiplier function.

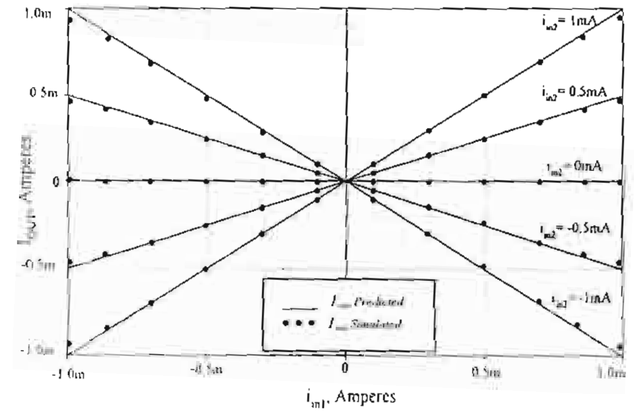

Figure 4. Simulated DC transfer characteristic of the multiplier.

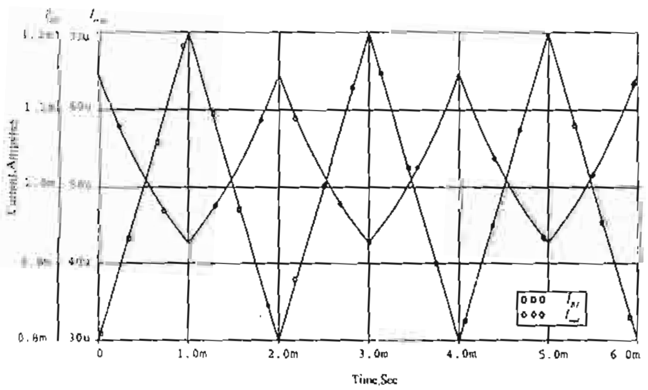

Figure 5. Simulated transient response for the divider function.

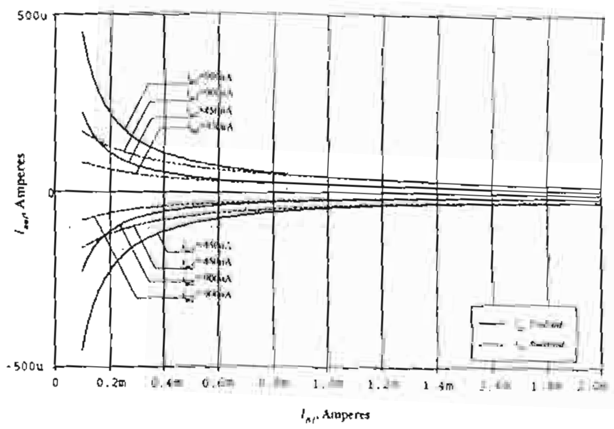

Figure 6. Simulated DC transfer characteristic of the divider.

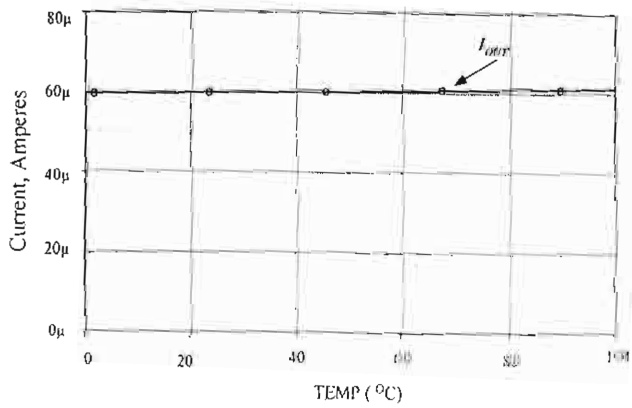

Figure 7. Simulated transient response of I_{out} versus Temperature.

The figure shows the plot of the output current I_{out} against the input signal current i_{in1} from −1mA to 1mA and the input signal current i_{in2} from −1mA to 1mA with 0.5mA per step. The simulation and calculated data are agreed very well over the ±0.8mA input range with error of less than 0.1%. We can see large non-linearity for i_{in1} close 1mA this is due to that the voltage across the OTA1 is closed to the limited linear range. Fig.5 shows the simulated transient response of the circuit that is functioned as a divider. In this case, the output current I_{out} is an inverting function of a triangular wave signal, where i_{in1} and i_{in2} are DC currents, i.e. i_{in1} = 50μA, i_{in2} = 900μA, and I_{B1} is a 500Hz triangular wave with amplitude of 200μA and with DC component of equal to 1mA. To demonstrate the error, Fig.6 shows the comparison of the simulated and the calculated values of the output current I_{out}. The output current I_{out} is ploted against I_{B1} with i_{in2} taking values from −0.9mA to 0.9mA with 0.45mA steps. For i_{in2} is positive, we found that the relative error is decrease if i_{in2} is increase, for examples, for 1mA<I_{B1}<2mA, i_{in2} = 0.3, 0.6 and 0.5mA the error are 7.36, 6.17 and 5.0%, respectively. However for i_{in2} is negative, the relative error is high, such as the error is about 12 % for i_{in2} = -0.9mA, since the bias current of the OTA2 in this case is small (I_{B2}-|i_{in2}|). The linearity of the divider

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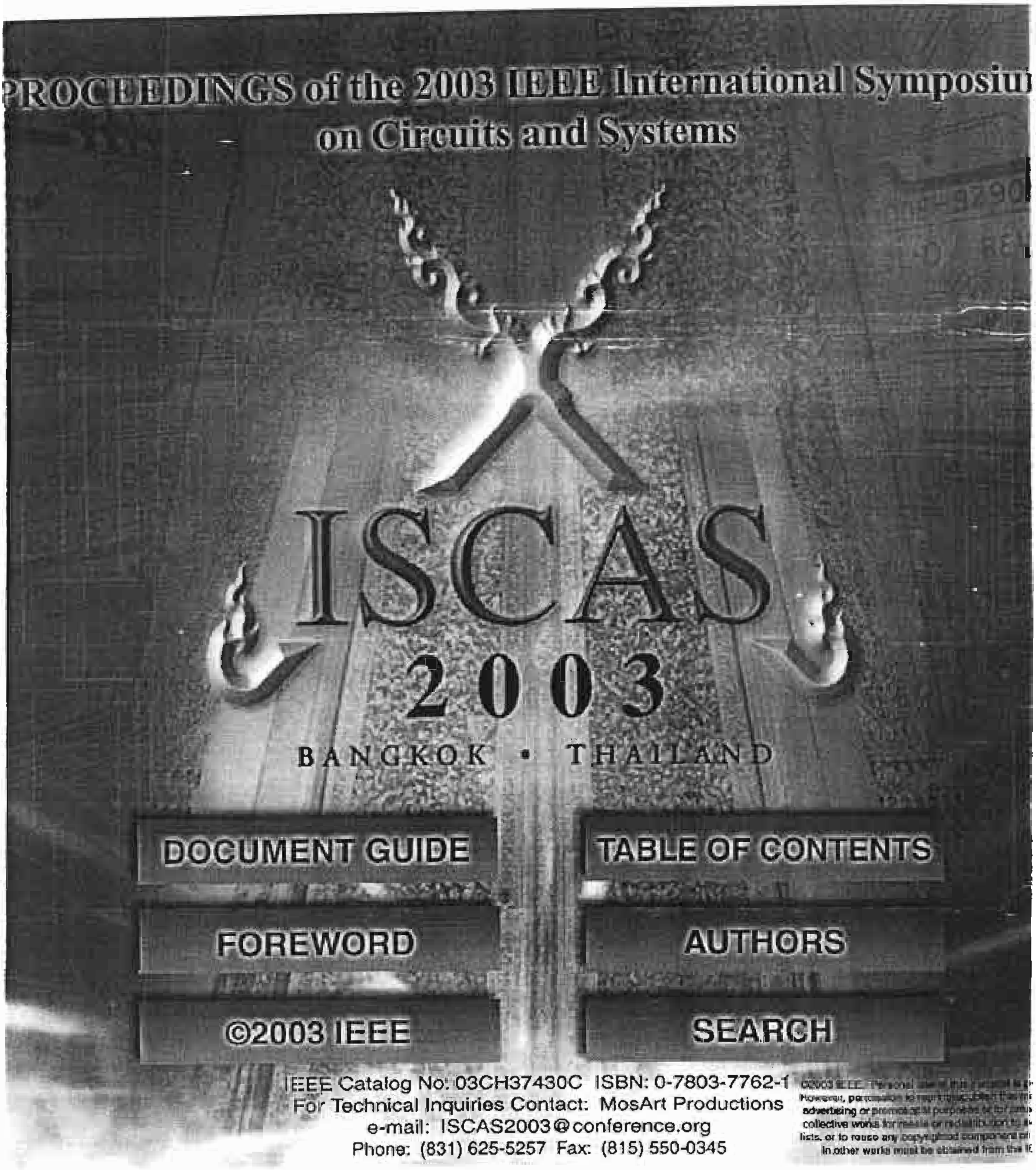

A CMOS CURRENT-MODE SQUARER/RECTIFIER CIRCUIT

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ABSTRACT

In this paper, a new current squarer and precision full-wave rectifier based on a CMOS class AB amplifier that modified to receive a differential input current has been presented. The proposed circuits are simulated with HSPICE level 49. From a ±1.5V supply voltage, the power consumption of the rectifier and the squarer at the quiescent point are about 210nW and 120μW, respectively. The total harmonics distortion of the squarer is less than 1%, with a input signal of 24μA.

1. INTRODUCTION

Squarer and full-wave rectifier are useful importance basic building block for the design of many analog signal processing applications, communications, frequency translation and instrumentation systems.

Usually, a squarer circuit can be realized by through the use of the square-law characteristics of MOS transistor [1][2][3]. For a full-wave rectifier circuit, it can be realized by some arrangement of diode-operational amplifier, diode-current conveyor, CMOS class AB amplifier and translinear current conveyor [8][6][4][5]. The main disadvantages of the mentioned methods are that they require a large power supply voltage, high power dissipation and large circuit implementations. Another problem is the accuracy. For the rectification, an interesting circuit, which is based on the class AB amplifier has been proposed [4], where it needs a large magnitude of the input current supplied by the input voltage and a resistor that cause an error for very low input current.

In this paper, a low voltage, current-mode and compact circuit structure precision squarer/full-wave rectifier have been introduced.

2. CIRCUIT DESCRIPTION

2.1 Class AB Amplifier

Consider a CMOS class AB amplifier formed by transistors M_1, M_2, M_3 and M_4 shown in Fig.1, where the current source I_{DD} provides the bias current for the circuit. Assuming that all transistors M_1, M_2, M_3 and M_4 are matched and are biased in saturation region with individual wells connected to their sources to eliminate the body effect [3]. Connecting the input node Y to a constant voltage and applying the input current I_x, we can express the drain currents of the transistors M_3 and M_4 as [4][7]

$$I_{d3} = \frac{(4I_{DD} - I_x)^2}{16I_{DD}} \quad \text{for } \left| I_x \right| \leq 4I_{DD} \tag{1}$$

$$I_{d4} = \frac{(4I_{DD} + I_x)^2}{16I_{DD}} \quad \text{for } \left| I_x \right| \leq 4I_{DD} \tag{2}$$

The expressions (1)-(2) are valid when the four transistors stay in saturation mode. However, if we apply the magnitude of the input current $|I_x| \geq 4I_{DD}$, the drain current I_{D3} close to zero and the transistor M_3 will be cut off. Then, the input current flows through the transistor M_4. This means that this circuit functions as a half-wave rectifier.

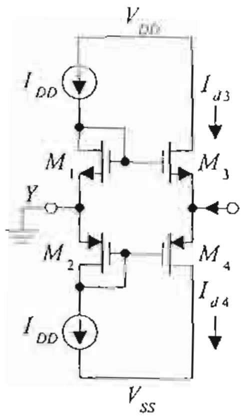

Fig. 1 CMOS class AB amplifier.

2.2 Current-Mode Squarer/Rectifier Circuit

Fig. 2 shows the current squarer/rectifier circuit. The proposed circuit consists of the CMOS class AB amplifier which is modified to receive the differential input current $\pm I_{in}$. The current gain of the p-type current mirror M_7-M_8 is unity. Assuming that the complementary pair of transistors M_1-M_2, M_3-M_4 and M_5-M_6 are identical. Neglecting the body effect and if all of the transistors are biased in saturation region, by applying eqns.(1)-(2), we can express the drain currents I_{d3} and I_{d5} as

$$I_{d3} = I_{DD} - \frac{I_{in}}{2} + \frac{I_{in}^2}{16 I_{DD}} \tag{3}$$

$$I_{d5} = I_{DD} + \frac{I_{in}}{2} + \frac{I_{in}^2}{16 I_{DD}} \tag{4}$$

The summation of the drain currents I_{d3} and I_{d5} is copied by the p-type current mirror M_7 and M_8, then the output current I_o can be written as

$$I_o = (I_{d3} + I_{d5}) - 2I_{DD} \tag{5}$$

$$= \frac{I_{in}^2}{8 I_{DD}} \qquad \text{for } \left| I_{in} \right| \le 4 I_{DD} \tag{6}$$

It is clearly seen that the output current I_o is related to the square of the input current I_{in}, where the squarer factor can be controlled by the bias current I_{DD}, as indicated by eqn.(6).

On the other hand, if we select the bias current $I_{DD} \le I_{in}/4$, then the circuit will operate in class B mode. This means that [4]

$$I_o = I_{D5} = I_{in} \qquad \text{for } I_{in} > 0 \tag{7}$$

$$I_o = I_{D3} = I_{in} \qquad \text{for } I_{in} < 0 \tag{8}$$

Therefore, the output current I_o becomes

$$I_o = \left| I_{in} \right| \tag{9}$$

In this case, the circuit represents a current full-wave rectifier.

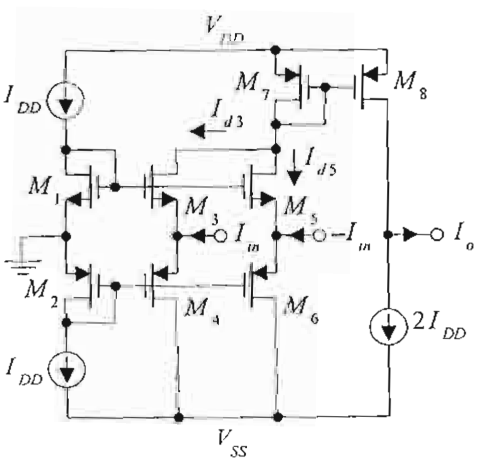

Fig. 2 Current squarer/rectifier circuit.

The complete current-mode squarer and full-wave rectifier circuit is shown in Fig.3. Where, the current sources I_{DD} and $2I_{DD}$ were replaced by the transistors M_8, M_{12} and M_{11}, respectively. The transistors M_{13}-M_{15} and M_7 generate the bias current for the class AB cell M_1-M_6.

From the proposed circuit of Fig.3, the squarer and rectifier functions can be achieved by connecting or by opening the drain-to-source of the transistor M_{15}. If the drain-to-source of M_{15} is not connected together and $(V_{DD}-V_{SS}) \le (V_{TN13} + |V_{TP14}| + |V_{TP15}| + |V_{TP17}|)$, where V_{TN} and V_{TP} are the threshold voltage of NMOS and PMOS transistors, respectively. The circuit works as a full-wave rectifier.

Finally, by connecting the drain-to-source of the transistor M_{15} together, the value of $(V_{DD}-V_{SS}) \le (V_{TN13} + |V_{TP14}| + |V_{TP7}|)$, and all the transistors are biased in saturation region, the proposed circuit becomes a squarer.

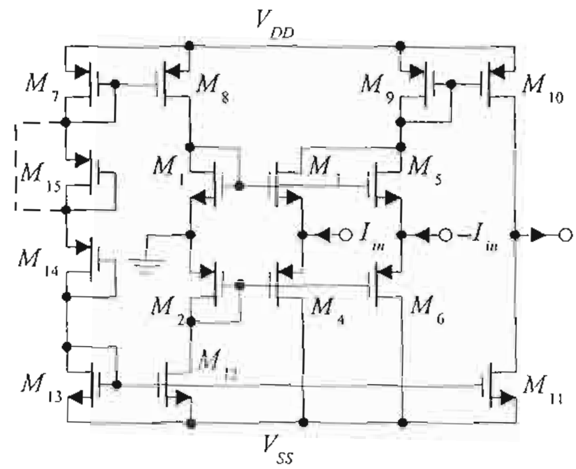

Fig. 3 Complete current squarer/rectifier circuit.

MOS transistor	$W(um)$	$L(um)$
M_1, M_3, M_5	10	5
M_2, M_4, M_6	32	5
$M_7 - M_{10}$	60	5
M_{11}	73	5
M_{12}, M_{13}	40	5
M_{14}, M_{15}	30	5

Table 1. Transistor sizes used in the squarer/rectifier circuit.

3. SIMULATION RESULTS

The proposed squarer/rectifier circuit of Fig.3 was simulated by HSPICE using the model parameter of HP 0.5μm CMOS process level 49. The transistor dimensions are given in Table 1. To cancel out the dc output offset current, the aspect ratio of the transistor M_{11} must be adjusted. The bulks(body) of all transistors are connected to respective power supply V_{DD} and V_{SS}, that is $\pm 1.5V$.

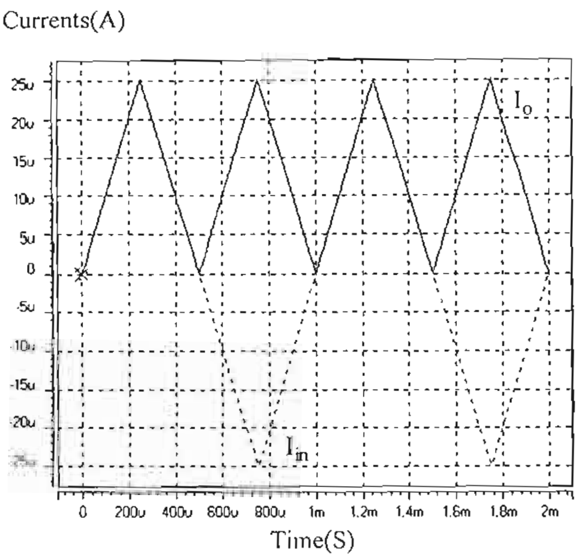

Fig. 4 Triangular differential input current.

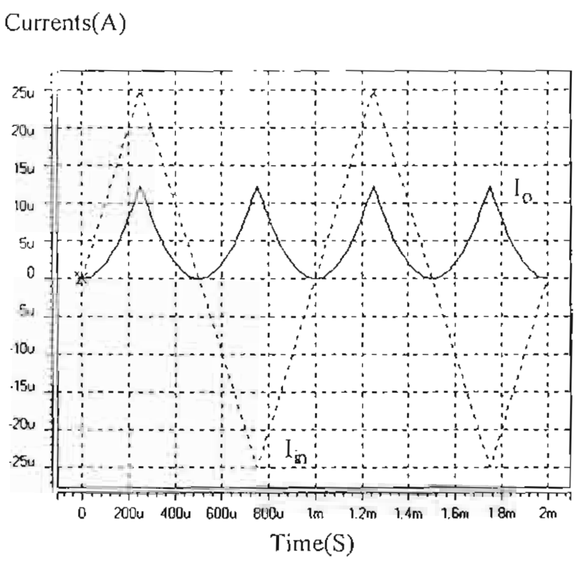

Fig. 5 Simulated current squarer response.

Fig.4 shows the response for the use of rectification function, by applying the triangular differential input current with peak amplitude of 25μA and the frequency is 1kHz, the drain of M_{15} is not connected to source. The bias currents of the transistors M_1-M_6 that the value of 12nA have been measured and the power dissipation at the bias point is about 210nW.

By connecting the drain-to-source of M_{15}, the bias currents of M_1-M_6 is set to 6.6μA and, the power consumption is about 120μW, respectively. Now the circuit works as a squarer and the output current waveform can be observed in Fig.5.

The total harmonics distortion (THD) against a 1kHz input current is shown in Fig.6 and has been calculated as the harmonic content of the fundamental frequency at 2kHz [1]. THD value less than 1% is achieved for the input current <24μA. The THD versus the output frequency with a 24μA input current signal is shown in Fig.7. It is lower than 1.1% up to 1MHz.

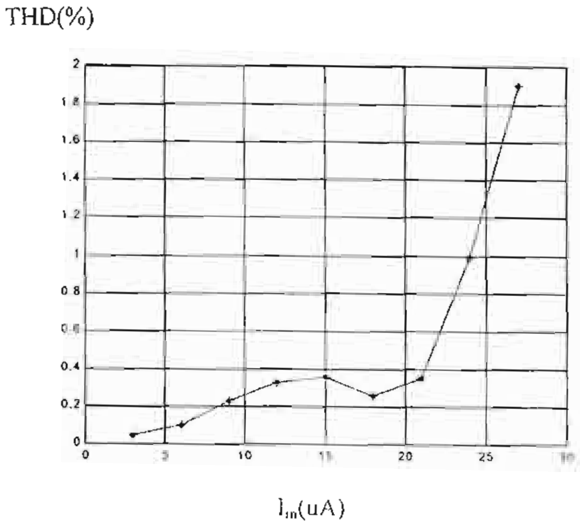

Fig. 6 THD against input current.

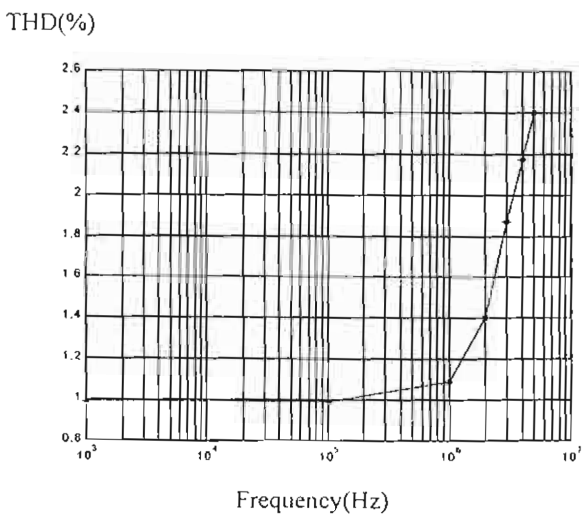

Fig. 7 THD against output frequency.