4. CONCLUSION

The realization of current-mode squarer and full-wave rectifier in the same circuit based on the use of a modified CMOS class AB amplifier has been proposed. Their performances have been demonstrated by the HSPICE program.

ACKNOWLEDGEMENT

This work is partly funded by the Thailand Research Fund (TRF) under the Senior Research Program, grant number RTA/04/2543.

The support provided by the Japan International Cooperation Agency (JICA) is also acknowledged.

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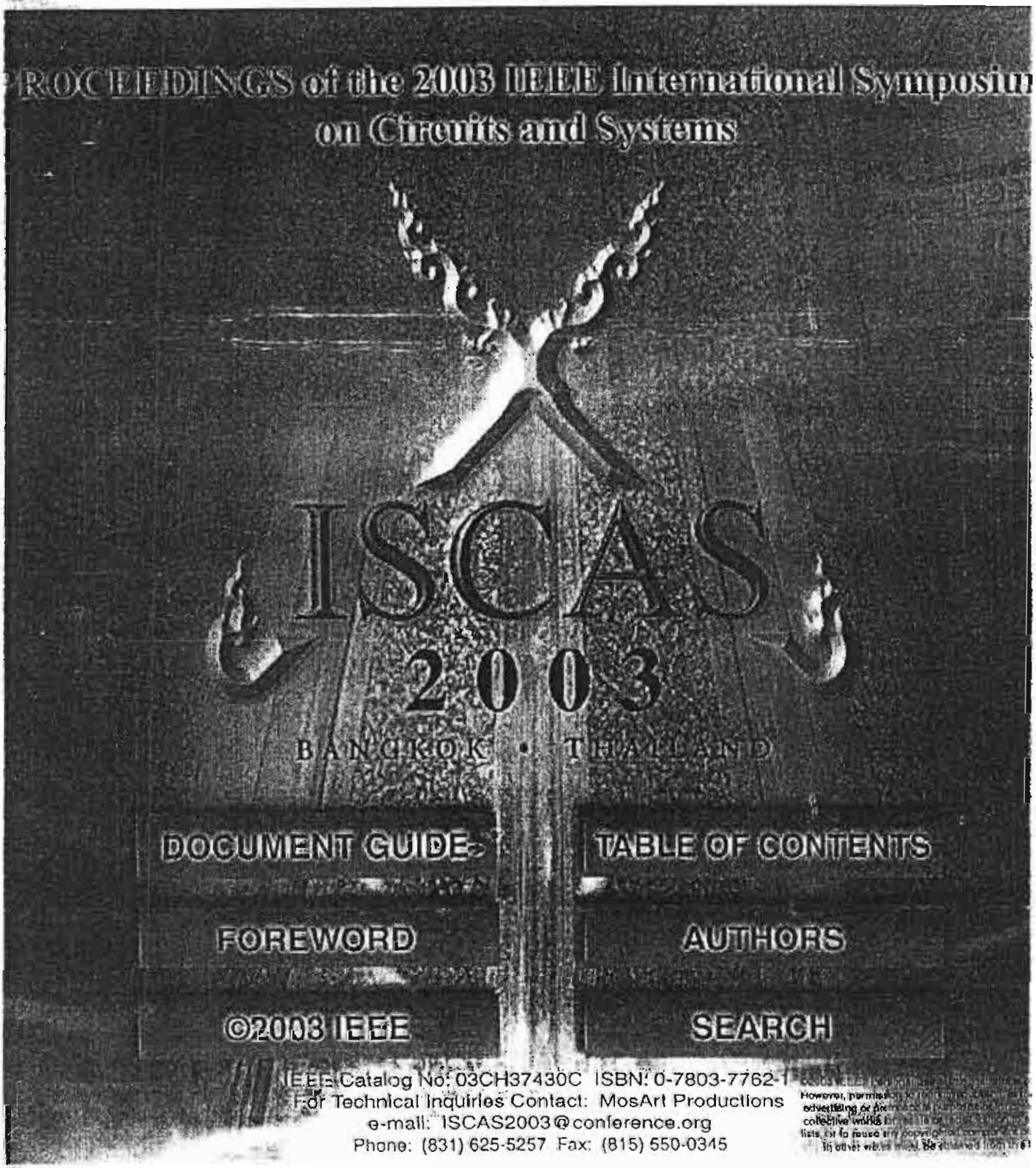

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REALIZATION OF ELECTRONICALLY TUNABLE LADDER FILTERS USING MULTI-OUTPUT CURRENT CONTROLLED CONVEYORS

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ABSTRACT

A systematic realization of continuous-time current-mode ladder filter using multi-output second generation current controlled conveyor (MCCCII) has been presented. The proposed technique is based on leapfrog simulation of RLC ladder filter using only MCCCIIs and capacitors that lead to simple structure, easy to design and suitable for IC fabrication. A fifth-order Butterworth low-pass filter and a sixth-order Chebyshev band-pass filter which retain a minimum requirement of passive elements and have an advantage of electronically tunable will be introduced. The feasibility of realization strategy is confirmed through HSPICE circuit simulations.

1. INTRODUCTION

Double terminated passive RLC ladder filters are well known on having an inherent advantage over active filter in terms of their sensitivity to component tolerances. There are several methods to extract this benefit from the prototype passive filter using the op-amp-based RC-active and OTA-C-based circuits [1]. The leapfrog structure seem to receive more popular due to it share all the low sensitivity characteristic and low component spread of the precedent RLC filter. Traditionally, the simulation is based on modeling all circuit equations as voltage signals [1]. Recently, current-mode signal processing has been received substantial consideration owing to its higher performance properties. Consequently, many suggestions of current-mode leapfrog ladder filter had been published employing OTAs [2] and CCIIs [3] as the active building blocks. However, all of them are established from simulating the operation of the ladder by mean of realizing the transfer function, which require a lot of active and passive elements and sometime the sensitivity may not necessitate being low. In very recent, the implementation of leapfrog filter using current differential buffered amplifies or CDBAs has been proposed [4], which can perform high frequency and low voltage supply operation. This scheme can simplify the signal flow graph of leapfrog filter and then realize each circuit element one by one, hence the low sensitivity basis is promised. Unfortunately, several floating resistors are required for voltage to current conversion and the utilized frequency is exactly fixed by determined passive elements.

This paper follows the idea of realizing the voltage-current relationships of each element corresponding to the prototype RLC filters one by one. Current controlled conveyor is chosen to function as a V-to-I converter cell regenerating all voltage parameter into current form. This proposed scheme possesses many advantages. Firstly, the structure is very simple and easy to design. No any external resister is required, which can safe the area in case of fabricating in a silicon chip. Moreover, the center frequency can be tuned electronically by adjusting the bias current of MCCCIIs. This will be useful in redeeming when the values of passive devices are deviated; including changing the system's characteristic is also very comfortable.

2. CURRENT CONTROLLED CONVEYOR

Second generation current conveyors (CCIIs) have found useful applications especially in current-mode world. Based on a complementary translinear loop, the current conveyor will be possible to operate at high frequency in class AB. In addition, the translinear current conveyor has a structure as simple as basic OTA but take less power consumption [5]. Despite this, it has only one output terminal and a current signal is available only once for each signal feed back. Therefore, in the multi-loop feedback path topology like leapfrog, multi-output characteristic seem to play an important role. The circuit symbol of multi-output current controlled conveyor is shown in figure1, which has both positive output terminal represented by $+Z$ and negative output terminal by $-Z$.

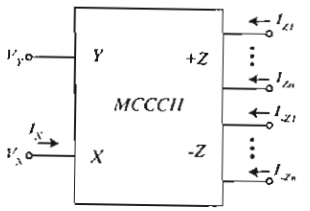

Figure 1. Circuit symbol of MCCCII

The schematic implementation of BiCMOS translinear MCCCII is shown in figure 2, which the ports relation can be described by the following matrix equation:

$$\begin{bmatrix} I_Y \\ V_X \\ I_{+Z} \\ I_{-Z} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 1 & R_X & 0 & 0 \\ 0 & 1 & 0 & 0 \\ 0 & -1 & 0 & 0 \end{bmatrix} \begin{bmatrix} V_Y \\ I_X \\ V_{+Z} \\ V_{-Z} \end{bmatrix} \quad (1)$$

where $R_X = V_T/2I_{B1}$ is an intrinsic small signal resistance of the equivalent voltage follower. It is possible to control R_X by

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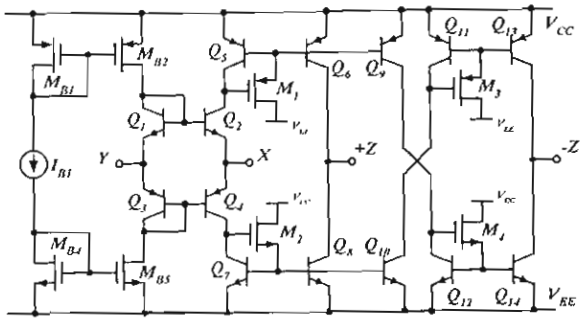

Figure 2. BiCMOS implementation of MCCCII

varying the bias current I_{B1}. Note that since the main contribution in noise is coming from current mirrors, the employment of MOS transistors in the biasing circuit is to minimize noise [5]. The multi-output topology can be easily implemented by adding the further output transistors. MOS transistors, M_1-M_4, are used to supply base current to all output transistors for accurate current transfer.

3. FILTER DESIGN METHODOLOGY

In order to develop the simulation procedure, consider the general ladder structure in figure 3. Here we focus on the realizing of the doubly terminated RLC filter. The characteristic of this structure can be expressed as following:

$$I_1 = I_S - \frac{V_1}{R_S} - I_2,$$

$$V_1 = Z_1 I_1,$$

$$I_2 = Y_2(V_1 - V_3),$$

$$V_3 = Z_3(I_2 - I_4),$$

$$\vdots$$

and

$$I_{n-1} = Y_{n-1}(V_{n-2} - V_n),$$

$$V_n = Z_n(I_{n-1} - I_O) \qquad (2)$$

where Z_i and Y_i stand for the impedance and admittance, respectively. These equations can be represented with block diagram in form of leapfrog structure as shown in figure 4. It can be observed that the diagram comprises of 2 operations, current to voltage and voltage to current conversion, as sketched in figure 5(a) and 5(c). Then if we convert the variables to be processed in only one type, the current variable, the execution would be simpler and ease in design. As seen in figure 5(b) and 5(d), with transforming all voltage to its current counterpart using MCCCIIs, these two operators can then be implemented using the same circuit. It should be noted that R_X is intrinsic resistance at port X of MCCCII introduced in the previous section. Since after the transformation, all variables are related to R_X, altering on R_X can also varying the characteristic of the filter that is the key of electronically tunable property.

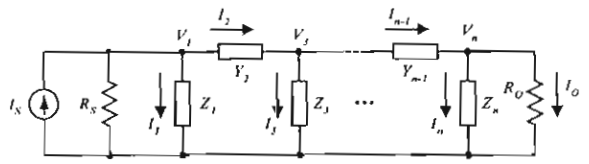

Figure 3. General doubly terminated ladder network

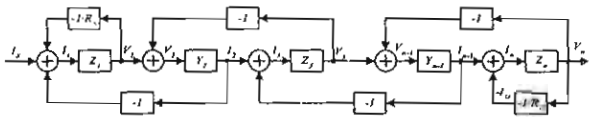

Figure 4. Block diagram redrawn from figure 3

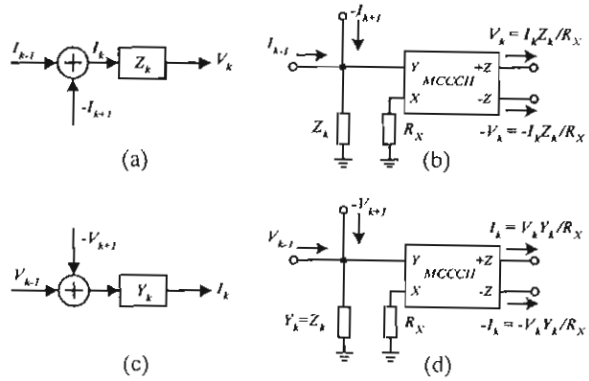

Figure 5. Basic blocks and the realization using MCCCIIs

A current-mode fifth-order Butter-worth low-pass RLC ladder filter shown in figure 6 is adopted as an example and the consequent circuit is shown in figure 7. It comprises of the minimum requirement of MCCCIIs and capacitors. As it is clearly seen that only five MCCCIIs and five capacitors are needed for realizing the fifth-order filter. There is no obligation of any external resistor, even the terminated resistor, R_S and R_O, are also implementing using MCCCIIs. Not only the attempt to eliminate the passive components, it is the necessary for tuning center frequency feature. Then, in general, merely $n+2$ MCCCIIs and n capacitors are required for the n^{th}-order filters implementation. Furthermore, this composition has several high impedance outputs, which allow to be easily cascaded without any additional matching circuits.

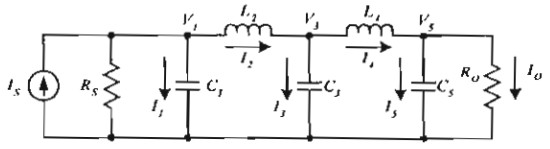

Figure 6. Prototype current-mode fifth-order Butterworth low-pass RLC ladder filter

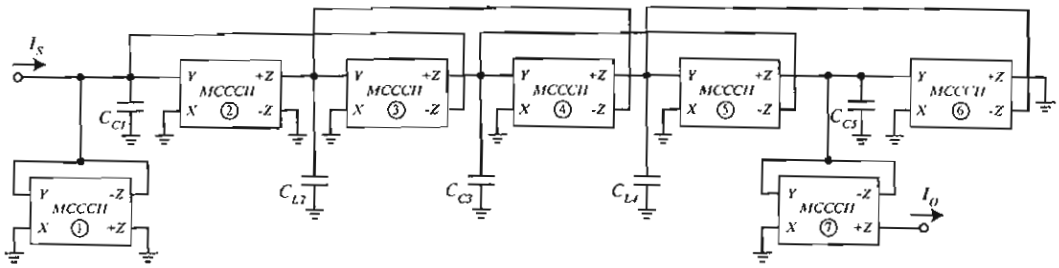

Figure 7. Current-mode tunable fifth-order Butterworth low-pass filter using MCCCIIs

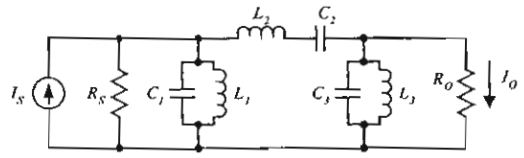

Figure 8. Current-mode sixth-order RLC band-pass filter

In addition, deriving the RLC ladder band-pass filter with this procedure is also possible. Consider a current-mode sixth-order band-pass filter in figure 8. In this case, the parallel and series LC branches can be realized using the basic block as shown in figure 9. And then the full leapfrog filter is obtained as in figure 10.

4. SIMULATION RESULTS AND DESIGN EXAMPLE

The performance of the proposed filter is verified through HSPICE circuit simulation based on 0.8-μm BiCMOS process technology supplied by AMS. The emitter areas for bipolar transistors are all equaled while set the W/L ratio of CMOS bias circuit, M_{b1} - M_{b4}, to 10μm/1μm and current mirror CMOS transistors, M_1 - M_4, to 5μm/1μm. The bias current is set to I_{B1} = 100 μA under the voltage supply of ±V = ±2 V. The basic characteristics of the MCCCII as a transconductance cell are listed in table1.

To picture out the feasibility of the proposed filter technique, a current-mode fifth-order Butterworth low-pass filter has been designed with a half-power frequency ω_{3dB} of 100 Mrad/s (15.9 MHz). The terminated resistances are chosen to 1 Ω in prototype RLC filter. Then after scaling with MCCCII's intrinsic resistance

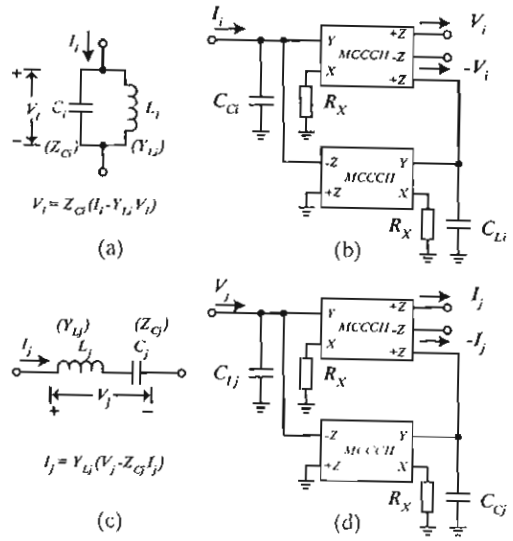

Figure 9. Basic blocks of filter in fig. 8 using MCCCIIs

Table1. Transconductance cell characteristic of MCCCII

Parameter	Simulated val.	Unit
Open loop G_m	5	mA/V
-3 dB Bandwidth	306	MHz
Input resistance	5.72	kΩ
Output resistance	140	kΩ

R_X ($1/G_m$), the capacitances' values are C_{C1} = C_{C5} = 30.9 pF, C_{L2} = C_{L4} = 80.9 pF and C_{C3} = 100 pF. The simulated frequency

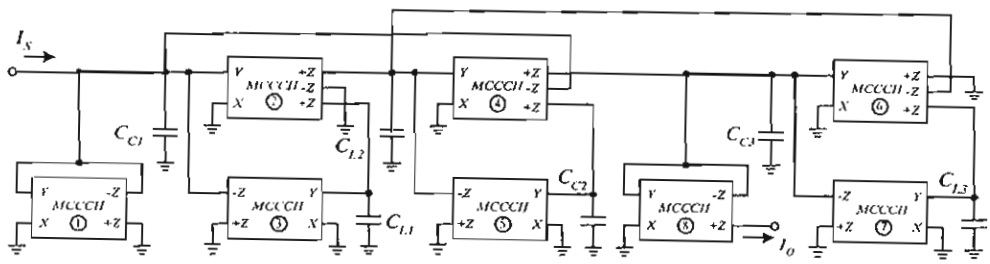

Figure 10. Current-mode sixth-order Chebyshev band-pass filter using MCCCIIs

response of the designed circuit and prototype RLC filter are compared in figure 11. Tuning ability is also simulated and shown in figure 12 by varying bias current to 25 μA and 400 μA.

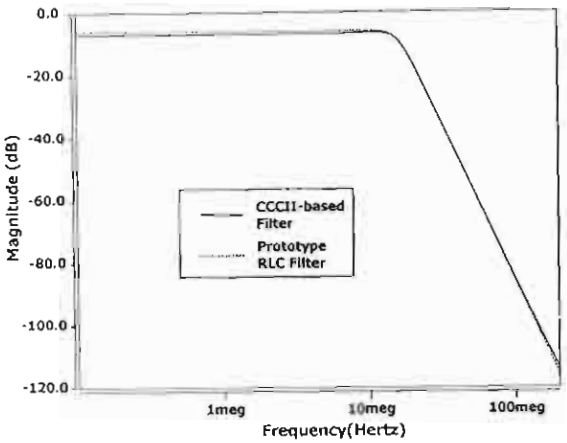

Figure 11. Simulated frequency response of the fifth-order low-pass filter

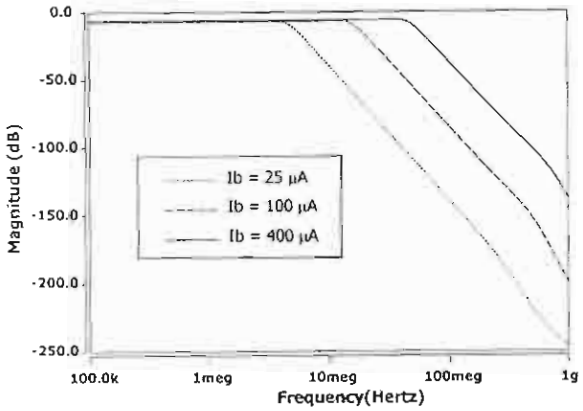

Figure 12. Simulated response of tuning cutoff frequency

A sixth-order Chebyshev band-pass filter deriving from RLC grouping as shown in figure 8 has been designed as well with the center frequency of 100 Mrad/s (15.9 MHz). The passive components are set to $C_{C1} = C_{C3} = 114.5$ pF, $C_{L1} = C_{L3} = 21.8$ pF, $C_{C2} = 19.6$ pF and $C_{L2} = 127.5$ pF. Adjust the bias current to 10 μA and 30 μA as the example of tunable ability. The simulated results are shown in figure 13.

It can be observed the well agreement with the passive prototype in low-pass filter implementation. However, there are some deviations in realizing band-pass filter especially in the higher frequency range. This is due to the conversion resistance R_X is not pure resistance but combined from both RLC, since the simulation using ideal MCCCII with genuine R_X have the exact response to the passive filter one as shown in dash line of figure 13. The high frequency compensation can be worked out to improve the efficiency in the future work.

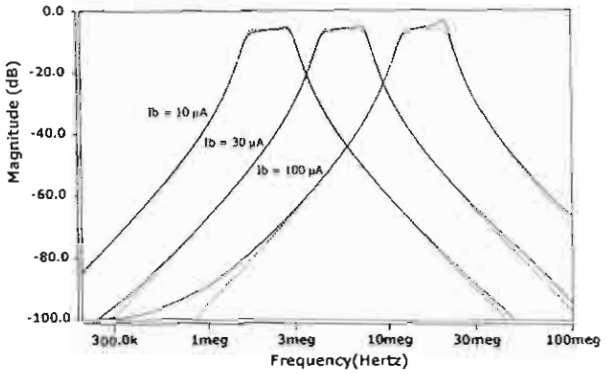

Figure 13. Simulated frequency response of tuning the sixth-order band-pass filter

5. SUMMARY

A realization of leapfrog ladder filter using multi-output current controlled conveyor is proposed. The design strategy is very simple and requires the minimum passive components. The center frequency can be tuned electronically by controlling the bias current of current conveyor, which is very helpful in compensating unmatched components as well as varying the characteristic without changing any device. Fifth-order Butterworth low-pass filter and sixth-order Chebyshev band-pass filter are derived as examples. HSPICE simulation results give a good agreement with the theoretical expectation. Nevertheless, the frequency compensation should be done on implementing current conveyor for serving the filters' responses much more perfect.

6. ACKNOWLEDGEMENT

The first author would like to thank Mr. Worapong Tangsirat for useful discussions on ladder filter design. This work is partly funded by the Thailand Research Fund (TRF) under the Senior Research Scholar Program grant number RTA/04/2543. The support provided by the Japan International Cooperation Agency (JICA) is also acknowledged.

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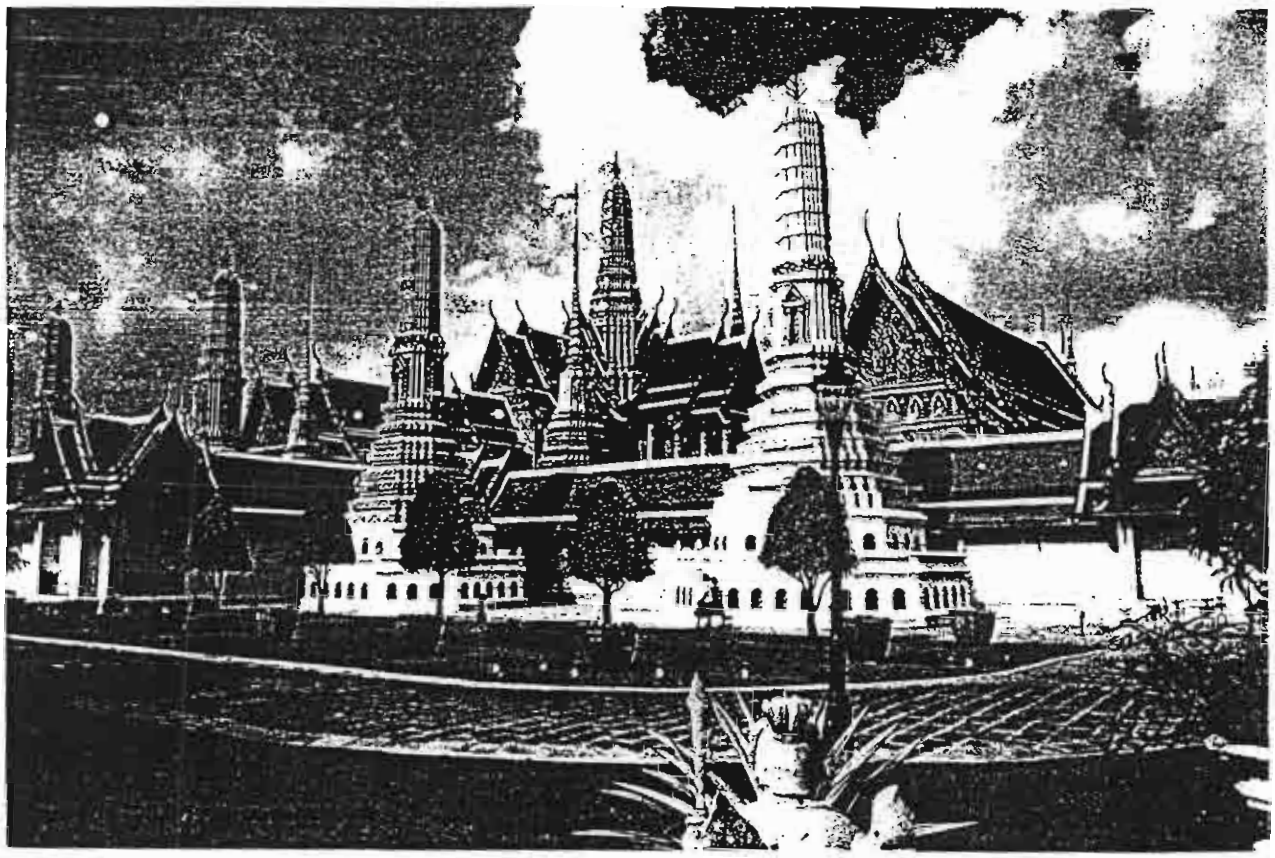

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CMOS Multi-Output FTFN: A Translinear Approach

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Abstract

An alternative CMOS implementation scheme of a multi-output four-terminal floating nullor (MFTFN) is proposed. The presented scheme is based on the advantages of a complementary transconductance amplifier and a class AB translinear cell type circuit that comes up with extremely high gain and wide bandwidth. The MFTFN is a very useful building block that can be used to substitute the other well-known blocks in every application. The characteristics of the proposed universal active circuit element are confirmed through HSPICE simulations. Current-mode band-pass filter and multifunction biquadratic filter are determined to exhibit the potentiality of this proposed scheme.

Keywords: Universal Active element, FTFN, Translinear, CMOS analog circuit, Current-mode filter

1. Introduction

Current-mode circuits have gained essential consideration recently. This arises from their significant advantages over the voltage-mode, especially for higher frequency operation and simpler structure. The regular active devices that have been used in current-mode are a second-generation current conveyor (CCII), a current feedback op-amp (CFOA), an operational transconductance amplifier (OTA) and a four-terminal floating nullor (FTFN). However, it has been recently shown that the FTFN is more flexible and versatile than the other building blocks. These lead up to the increasing interest in using FTFNs to design current-mode circuits: for example, filters, gyrators, simulated floating impedance and sinusoidal oscillator [1-3]. FTFN-based structures provide a number of influential advantages such as minimum number of employed elements, complete absence of passive component-matching requirement and endowing high frequency characteristic. Although FTFN-based and CCII-based current-mode circuits can simply be designed through a systematic transformation, based on the use of a nullor which consist of a nullator and a norator, from a regular RC active circuit. However, the CCII-based implementations are more complex and require the additional number of the active elements. This owes to the fact that when using the transformed nullor equivalent circuit the nullator/norator pair can simple be represented by an FTFN without imposing any restrictions. Moreover, by designing through a dual transform technique, the transformed current-mode FTFN-based circuit furnishes a high output impedance source. This property enables the circuit to be used in cascade form.

There are many FTFN realisations that have been recently reported in literatures [4-5]. However, this paper shows an alternative form to realise an integrable multiple-output port FTFN in CMOS technology, with offers higher gain and bandwidth. The proposed scheme realises through the combination of a complementary transconductance amplifier, a translinear cell and current mirrors. In addition, the number of output ports can easily be expanded to support the designer applications. For example, recently, there are some interests on realising and using the FTFN which has been extended more than four terminal such as the so-called a five-terminal floating nullor (FiTFN) [2, 6], which are good basic applications for our multi-output FTFN idea. The current-mode band-pass filter is adopted to demonstrate the FTFN-based circuit capability. While the universal current-mode biquadratic filter is employed to demonstrate the proposed multiple-output FTFN application example.

2. Basic idea

In general, FTFN is equivalent to an ideal nullor, which can imply to be a high gain transconductance amplifier with independently floating characteristic at

input and output terminals. Fig. 1(a) shows a nullor model of an FTFN that can be described by its port relation characteristics as:

$$v_Y = v_X \qquad i_Y = i_X = 0 \qquad i_Z = -i_W \qquad (1)$$

where it should be noted that the output impedance of the W and Z ports are generally arbitrary. Usually, the realisations of FTFN are based on the use of the conventional op-amps as the basis parts. One of the most famous realisation techniques of the FTFNs is built up from a basic type shown in Fig. 1 (b) [1, 2, 6]. It is using one op-amp and supply current sensing technique, where the output impedance of port W is very low and the impedance of port Z is very high.

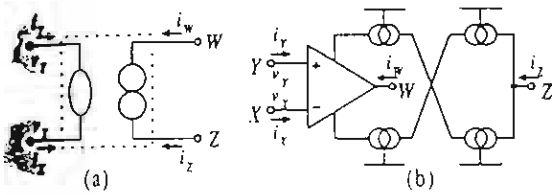


Fig. 1 (a) A nullor model (b) traditional implementation.

Unfortunately, op-amp based realisation schemes are inappropriate for high frequency applications due to frequency limitation of op-amp itself. In addition, in integrated circuit form, each op-amp will require substantial chip area. Another well-known structure is two CCII's, where ports X are connected together [3-4]. Although this configuration affords high accuracy applications, it can not yield the really high requirement. On the other hand, the appropriate topology schemes for implementing in monolithic integrated form have been reported [5-6] but even so they are too complicated.

The modification from the original FTFN to be a MFTFN is done by adding the new output terminals as shown in Fig. 2. Fig. 2 (a) shows the schematic diagram of the MFTFN, where its characteristics can be point out by the following port relations:

$$v_Y = v_X$$

$$i_Y = i_X = 0$$

$$i_{Z1} = i_{Z2} = \cdots = i_{Zn} = -i_{W1} = -i_{W2} = \cdots = -i_{Wn} \qquad (2)$$

where n is number of the output ports. The implementation scheme of the MFTFN will be shown in the section 3 and the application of the MFTFN will be outlined in the section 5.

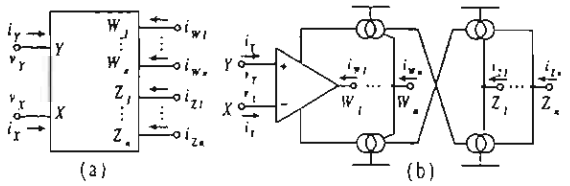


Fig.2 (a) Multi-output FTFN symbol
(b) possible implementation.

3. Circuit description

From the drawback of previous works, there is a motivation to find out a simple realisation structure, which has simultaneously high gain and bandwidth. The circuit diagram of the proposed multi-output FTFN is shown in Fig. 3. This circuit basically comprises of a complementary transconductance amplifier, a basic translinear cell and some of current mirrors. Transistors M_1 to M_4 and the bias current sources I_{B1} and I_{B2} perform a complementary differential amplifier, which

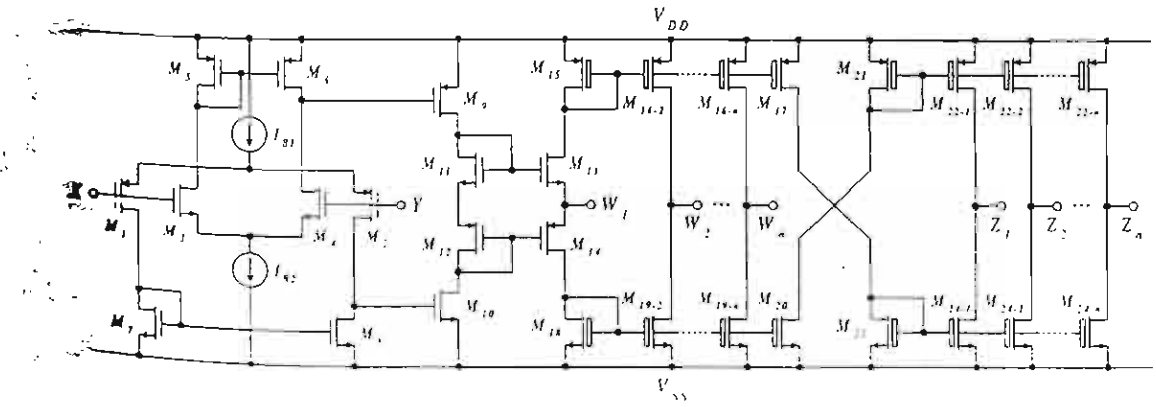


Fig. 3 Schematic diagram of the multi-output FTFN.

are connected with active loads, current mirrors M_5 - M_6 and M_7 - M_8. It should be noted that a P-channel input pair, M_1 – M_2, is employed to be able to reach the negative supply rail while an N-channel input pair, M_3 – M_4, is able to reach the positive supply rail. As a result, the common-mode input range of this circuit extends nearly from rail to rail. This complementary input stage feed a differential output voltage, which is continuously enlarged by the gain stage, transistors M_9 and M_{10}. The converted current signal from the gain stage is injected to the translinear cell, M_{11} – M_{14}, and then summing to be output current at port W_1. This configuration provides very high transconductance gain over a wide frequency range. Ideally, it is required that the pairs of transistors M_{11}, M_{13} and M_{12}, M_{14} are closely matched and all current mirrors have the exact unity gain. This translinear cell act as a current-follower that allows output current i_{W1} to sources and sinks at port W_1 and will be reflected and inverted to be current i_{Z1} at terminal Z_1. With this cross-coupled current mirror technique, it can be easily kept up $i_{Z1} \equiv -i_{W1}$. The transistors having boxes as gates are composite transistors with high output impedance such as normal cascodes, low-voltage cascodes, or regulated cascodes [8]. The multi-output concept can be easily adapted by adding transistors to the output current mirror set. Transistors M_{16-2} – M_{16-n} and M_{19-2} – M_{19-n} are used to perform the output terminals W_2 to W_n, respectively. Similarly, transistors M_{22-2} – M_{22-n} and M_{24-2} – M_{24-n} are used to perform the output terminals Z_2 to Z_n.

4. Simulation results

The performance of the proposed circuit is verified by HSPICE circuit simulation program based on the SCN2 level-2 CMOS model obtained through MOSIS [9]. All transistor dimensions are listed in Table 1,

Table 1 Transistors dimension

Transistors	W (μm)	L (μm)
M_1, M_2	300	2
M_3, M_4	150	2
M_5, M_6, M_{10}	40	2
M_7, M_8	20	2
M_9	80	2
M_{11}, M_{12}	100	2
M_{13}, M_{14}	200	2
M_{15}, M_{16-2} – M_{16-n}, M_{17}, M_{21}, M_{22-1} – M_{22-n}	70	2
M_{18}, M_{19-2} – M_{19-n}, M_{20}, M_{23}, M_{24-1} – M_{24-n}	35	2

where W is channel width and L is channel length. The bias currents are set to $I_{B1} = I_{B2} = 2$mA. Supply voltages are taken as V_{CC} = +5V and V_{EE} = -5V. The simulated characteristic of open loop transconductance gain is given in Fig. 4 showing a significant greater amplification circuits both gain and bandwidth than ever published [4-6].

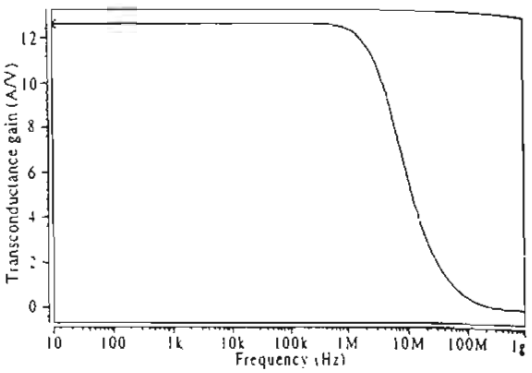


Fig. 4 Simulated open loop transconductance gain.

From the response, it can be estimated the –3 dB bandwidth in a very high frequency as nearly as 5 MHz and the transconductance gain of over 12 A/V is obtained. This gain is exceptionally high especially comparing to the preceding proposed circuit, which have the transconductance gain not exceeding a few hundred of milliampere per volt [4-5]. The simulated DC offset voltage between input port is approximately 90 μV and the offset current of the output port is about 1 μA. The input voltage swing and the output current swing are in the range of ±3.5 V and ±7mA, respectively. The current follower operation proves the linear identity over a very wide current range as shown in Fig. 5 where I_{Wn} and I_{Zn} are the currents from port W_n and Z_n, n=1,2,..., respectively.

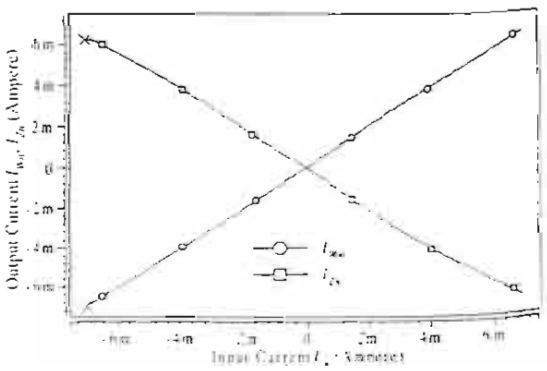


Fig. 5 Current following operation at output port.

ion Examples

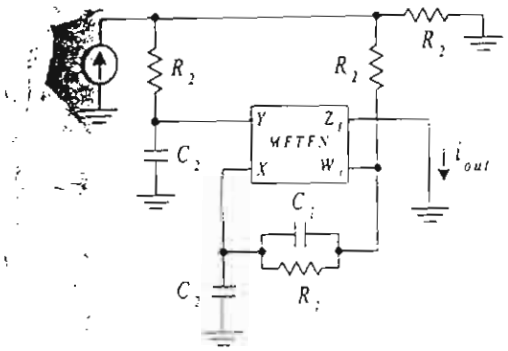
realisation of a current-mode band-pass from reference 4 is chosen as an illustrative the FTFN-based circuit and is shown in Fig. fer function of this filter is:

$$\frac{-s/3C_1R_2}{s^2+s\left(\frac{1}{C_1R_1}+\frac{1}{3C_2R_2}-\frac{1}{3C_1R_2}\right)+\frac{1}{3C_1C_2R_1R_2}} \quad (3)$$

atural angular frequency and quality factor are given by

$$\omega_0=\frac{1}{\sqrt{3C_1C_2R_1R_2}} \quad (4)$$

$$Q=\frac{\sqrt{3C_1C_2R_1R_2}}{3C_2R_2+C_1R_1-C_2R_1} \quad (5)$$



6 FTFN-based current-mode band-pass filter.

nter frequency is set to 100 kHz. Therefore, the components are chosen as R_1 = 3 kΩ, R_2 = 1kΩ = C_2 = 0.5 nF. The simulation result of the filter

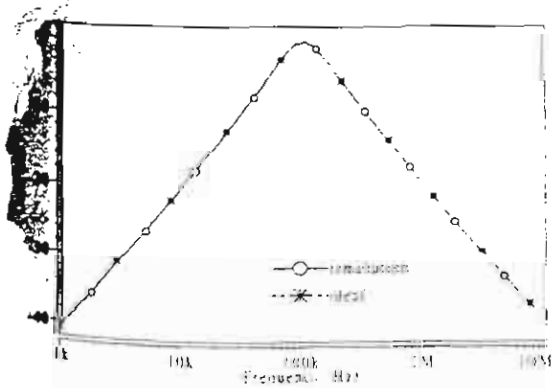


Fig. 7 Simulation result of FTFN-based current-mode band-pass filter and ideal function.

using the proposed multi-output FTFN, function as a traditional FTFN, and using ideal transfer function are compared in Fig. 7. It is clearly seen the perfect match between the two cases over a very wide frequency range. This is due to the truly high gain and wide bandwidth of the proposed device.

The other interesting application that demonstrated the availability of multi-output principle is the current-mode multifunction biquadratic filter. This filter can simultaneously realise three types of current-mode filtering function i.e. low-pass, band-pass and high-pass in the same configuration without changing any circuit topology or elements. Moreover, its primary parameters, the natural angular frequency ω_0 and the quality factor Q, can be orthogonally tuned and both of its active and passive sensitivities are quite small [2].

The accomplishment design of the filter using MFTFNs is shown in Fig. 8. It has all passive components really grounded. By routine circuit analysis, the following current transfer functions yielded

$$T_{HP}(s)=\frac{i_{HP}(s)}{i_{in}(s)}=\frac{s^2}{D(s)} \quad (6)$$

$$T_{BP}(s)=\frac{i_{BP}(s)}{i_{in}(s)}=-\frac{s\left(\frac{1}{C_1R_1}\right)}{D(s)} \quad (7)$$

$$T_{LP}(s)=\frac{i_{LP}(s)}{i_{in}(s)}=-\frac{\left(\frac{R_2}{C_1C_2R_1R_3R_4}\right)}{D(s)} \quad (8)$$

and $$D(s)=s^2+s\left(\frac{1}{C_1R_1}\right)+\left(\frac{R_2}{C_1C_2R_1R_3R_4}\right)$$

where $T_{HP}(s)$, $T_{BP}(s)$ and $T_{LP}(s)$ are the high-pass, band-pass and low-pass current transfer functions, respectively. These transfer functions can be contemporaneously obtained from the original circuit without changing any configuration and elements. The natural angular frequency ω_0 and the Q-factor of this configuration can be given by

$$\omega_0=\sqrt{\frac{R_2}{C_1C_2R_1R_3R_4}} \quad (9)$$

and $$Q=\sqrt{\frac{C_1R_1R_2}{C_2R_3R_4}} \quad (10)$$

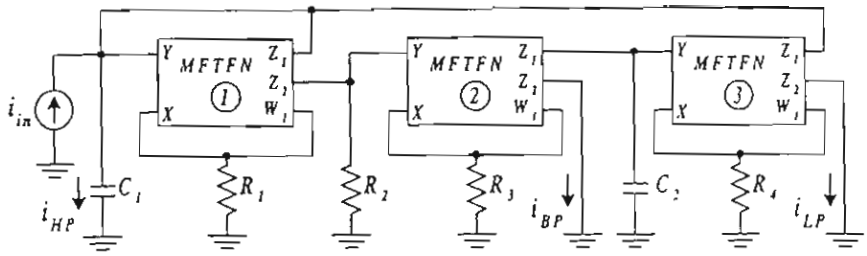


Fig. 8 Current-mode multifunction biquadratic filter using MFTFN.

The grounded resistor values are set to $R_1 = R_2 = R_3 = R_4 = 1\text{k}\Omega$ while the grounded capacitor values are $C_1 = C_2 = 0.1$ nF. The setting was designed to acquire the natural frequency $\omega_0/2\pi = 1.59$ MHz at Q-factor = 1. Fig. 9 shows the simulated frequency responses of the multifunction biquadratic filter using the proposed MFTFN. The simulated natural frequency measured from the HSPICE is approximately equal to 1.55 MHz, which attained to be in a very good agreement with the predicted value.

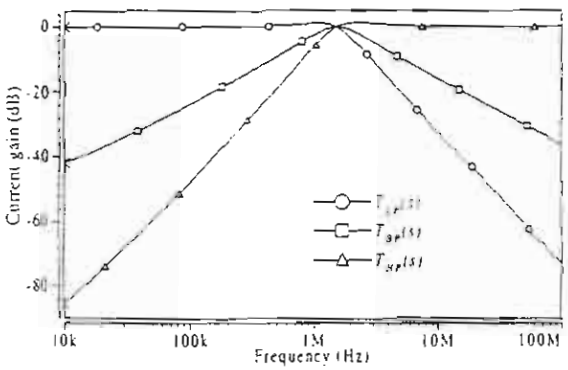


Fig. 9 Simulation result of the current-mode multifunction filter using MFTFN.

6. Summary

We have proposed a simple scheme for implementing FTFN circuit with additional extended output port. The proposed scheme is suitable for CMOS process monolithic integrated circuit form, and has been realised through the use of a complementary transconductance amplifier, a translinear cell and some of current mirrors. Simulation results from HSPICE program are used to confirm the high performance of our presented structure. The current-mode band-pass filter is an example to identify the feasibility of the FTFN-based circuit. The current-mode multifunction biquadratic filter is also used to demonstrate the usefulness of the multi-output topology. Detail analysis of the device and additional useful applications will be the subjects of the further publications.

7. Acknowledgements

This work is partly funded by the Thailand Research Fund (TRF), under the senior Research Scholar Program grant number RTA/04/2543. The support from the Japan International Cooperation Agency (JICA) is also gratefully acknowledged.

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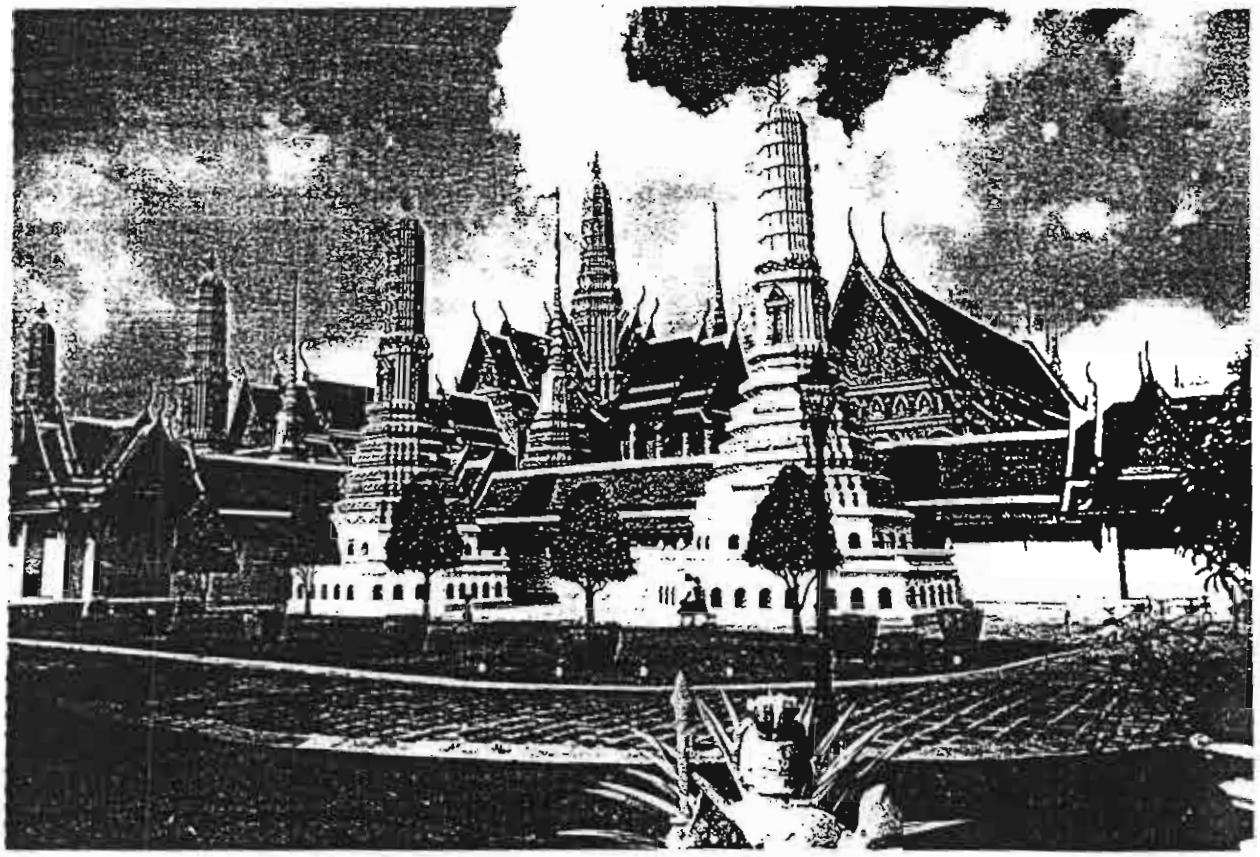

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AN INTEGRABLE CMOS-BASED GROUNDED-CAPACITOR TRUE RMS-TO-DC CONVERTER

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Abstract

A simple integrable CMOS circuit design technique to realize a grounded-capacitor true rms-to-dc converter is described in this paper. The conversion circuit consists of a squarer circuit, a low-pass filter and current mirrors and does not require a full-wave rectifier circuit. In order to reduce the value of the capacitor suitable for monolithic integration, a capacitance multiplier circuit that can multiply the value of the capacitance for the order of 1,000 time is also incorporated. The performance of the proposed circuit is studied through PSPICE and Cadence simulation results.

Keywords: True RMS-to-DC Converter, Capacitance multipliers, Analog VLSI

1. Introduction

It is well accepted that a true rms-to-dc converter, which is used for measuring the average energy content in an electrical signal, is found useful in the fields of instrumentation, communication and display systems. Many true rms-to-dc converters are available. However, these design methods are based on bi-polar integrated circuit technology and the rms-to-dc conversions are performed through the use of a full-wave rectifier and a multiplier/divider circuits employing a log-antilog principle[1-3]. Due to the bandwidth and the slew-rate of the full-wave rectifiers, the useful frequency range of these converters are limited. Although, a design technique for a true rms-to-dc converter based on the use of a dual translinear loop have been proposed recently [4]. However, the implementation scheme is suitable for bipolar technology. As more and more electronic systems are implemented using CMOS technology, the purpose of this paper is to present a CMOS circuit technique for the realization of a true rms-to-dc converter, where a grounded capacitor is used. A full-wave rectifier is not required by the proposed realization scheme. The conversion circuit is simple, suitable for implementing in monolithic integrated form, and can be readily integrated as part of a larger system. The performance of the conversion circuit is studied from PSPICE and Cadence IC circuit design systems simulation results.

2. Conversion Circuit

The proposed grounded-capacitor true rms-to-dc converter is shown in Fig 1. The operation of the circuit is based on the square law characteristic of MOS transistors biased in the strong inversion region [5,6]. Transistors M_1 through M_3 function as a current squarer circuit, where M_4 and M_6 and the current I_O form the current-controlled bias circuit, and the current I_{SA} can be written as

$$I_{SA} = I_{IN}^2 / 8I_O + 2I_O \qquad (1)$$

where the currents I_{IN} and I_O are the input and the bias currents, respectively. Due to we design such that the drain of transistor M_5 sources the current $2I_O$ at point A, then the current I_{SQ} can be expressed as

$$I_{SQ} = I_{IN}^2 / 8I_O \qquad (2)$$

The current I_{SQ} passes through the first-order current-mode low-pass filter, which is consisting of the current mirror (formed by transistors M_7 and M_8) and the grounded capacitor C_{AV} connected parallel to the mirror input. The current I_{O1} can be written as

$$I_{OI} = \frac{1}{8I_O T}\int I_{IN}^2\, dt \qquad (3)$$

where $T = C_{AV}/gm_7$ is the time constant of the filter and gm_7 is the transconductance of the transistor M_7. Due to the unity gain current mirrors of (M_7 and M_8) and of (M_{11} and M_{12}), the bias current I_O is driving by I_{OI} such that

$$I_O = I_{OI} \qquad (4)$$

At the output, since we set the transistor channel widths as $W_{13} = \sqrt{8}\, W_{11}$, this means the output current

$$I_{RMS} = \sqrt{8} I_O \qquad (5)$$

Then, from eqns. (2),(3) and (4) and solving for I_{RMS}, we get

$$I_{RMS} = \sqrt{\frac{1}{T}\int I_{IN}^2\, dt} \qquad (6)$$

It is clearly seen that the output current I_{RMS} is in the form of the root-mean-square value as required. It should be noted that, for a sinusoidal signal, the circuit can be easily modified to also measure the average value of the signal by using the method of the reference 7.

However, in order that the proposed rms-to-dc converter give a good performance in the required frequency range, the value of the capacitor C_{AV} must be chosen such that [4]

$$C_{AV} >> g_{m7(MAX)}/4f_{(MIN)} \qquad (7)$$

where $f_{(MIN)}$ is the lower end of the frequency range of interest. For example, for $K_P = 2.226\times10^{-5}$ A/V, then $gm_{7(MAX)}$ can be given by

$$g_{m7(MAX)} = 29.84\times10^{-3}\sqrt{I_M}\ A/V \qquad (8)$$

where I_M is the peak amplitude of the input signal. In this case C_{AV} must be chosen such that

$$C_{AV} >> (2.37\times10^{-3}\sqrt{I_M})/f_{(MIN)} \qquad (9)$$

If a sinusoidal input signal with I_M = 1 mA and $f_{(MIN)}$ = 100 Hz, the averaging capacitance must be chosen such that $C_{AV} >> 0.75\ \mu$F. For example, $C_{AV} = 7.5\ \mu$F must be employed. It is well accepted that this value of capacitance is not suitable for monolithic integration.

To reduce the size of the capacitor used, a current-controlled C-multiplier as shown in the Fig. 2 is presented, where the current conveyors (CCIIs) that reported in reference 9 have been used. The current-controlled C-multiplier, which is composed of two CCII (CCII+ and CCII-), is similar to the voltage-controlled C-multiplier proposed in the reference 8. But, in this case, the input signal is a current signal that injected into port X_1 and the capacitor C_{AV} is connected at the port Y_1. If we let $n = R_2/R_1$, the value of the capacitance that appeared at the port B to ground or C_{EQV} will be equaled to

$$C_{EQV} = nC_{AV} = (R_2/R_1)C_{AV} \qquad (10)$$

3. Simulation results

The characteristics of the converter were studied through the simulation results using PSPICE [10]. The transistor dimensions of the circuit in Fig.1 are in micron and are listed in the Table 1, where W is channel width and L is channel length, and the dimensions of all the transistor of the circuit in Fig 2 are W=50μm and L=5μm. The simulation was carried out using the transistor parameter of the 0.35-um CMOS TSMC process. Therefore, the simulation results were listed in the Table II. Note that the circuit exhibits the bandwidth of 200 MHz at I_{IN} = 1 mA_{rms}. The maximum conversion nonlinearity, for the input signal in the range from 2 uA_{rms} to 1 mA_{rms}, of about 0.8 % was achieved. The simulation for the frequency response for the sine wave input current signal with the amplitude of 20, 50 and 90 percents of the full scale current ($I_{IN(MAX)}$=1mA) was also carried out. The results show the bandwidth of about 30 MHz, 80 MHz and 100 MHz, respectively. Fig. 3(a) shows the plot of the percent ripple of the I_{RMS} versus frequency. The simulation results demonstrate that the percent ripple is small for high value of C_{AV}, such as, for example, for the case of C_{AV} = 2.5 μF and C_{AV} = 5 μF. Fig. 3(b) shows the plot of the percent ripple of the I_{RMS} versus frequency for the case that C_{AV} has been replaced by the C-multiplier circuit of the Fig.2, where port B is connected to point A of the Fig. 1. In order to compare with the plot in the Fig. 3(a), C_{AV} and R_1 are kept constant at 0.5 nF and 10 Ω, respectively, and n is varied by varying the value of the resistor R_2, for n=100, 500 and 1,000, respectively. From the Fig. 3(b), it is demonstrated that the percent ripple for the case of n=100, 500 and 1000 are quite in good agreement with the percent ripple for the case

C_{AV}=50nF, 250nF, and 500nF, respectively, of the Fig. 3(a). But, however, we found that for larger value of n, the percent ripples for the case of C-multiplier are larger than the percent ripples of the circuit in Fig.1, particularly for the high frequency range. This is due to that for large value of n the offset of the CCIIs have also been multiplied and cause the value of C_{EQV} deviated from the value predicted from the eqn. (10).

However, the simulation performance of the circuit using PSPICE is much depending on the chosen transistor parameters. Therefore, in order to test for the circuit workability, the performance of the rms-to-dc converter circuit and the C-multiplier circuit will be further studied through the layout by using Cadence's IC Circuit Design Systems, which is an integrated circuit design software running on Workstation [11]. The layout in a 0.35 um TSMC CMOS process was drawn by using Virtuoso Layout Editor of Cadence's system. Fig. 4 shows the layout of the C-multiplier circuit. The Diva interactive Electrical Rules Checker program, which is the layout extractor in the Cadence program, was then employed to translate the layout drawing into the SPICE-compatible text file for the simulation. Then the Analog Artist Design Environment is used to simulation the C-multiplier characteristic. Table III shows the effective capacitances of the layout circuit of the Fig. 4, where for n = 1, C_{AV} = 100 pF. Further investigation for the performance of the circuit for a large value of n and also the rms-to-dc converter will be reported.

4. Conclusion

We have developed a simple grounded-capacitor true rms-to-dc conversion circuit.For a more suitable for monolithic integration, the capacitance multiplier circuit has been used in order to reduce the value of the capacitor. The realization scheme is suitable for implemented in a standard CMOS process. The circuit has been fully simulated, through the use of PSPICE simulation program, and the characteristics of the conversion circuit have been reported. The circuit characteristic studied from Cadence IC circuit design systems is also included.

5. Acknowledgments

This work is partly funded by the Thailand Research Fund (TRF), under the senior Research Scholar Program grant number RTA/04/2543. The support of the Cadence IC Circuit Design Systems from the Japan International Co-operation Agency (JICA) is also gratefully acknowledged.

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Table I Transistors dimension

Transistors	W(μm)	L(μm)
M1,M2,M3,M4,M6,M7,M8	40	5
M9,M10,M11,M12	100	5
M5	80	5
M13	283	5

Table II Summary of the characteristics of the circuit of Fig. 1

Parameters	Simulated results
Supply voltage (rated)	$3V$ to $15V$
Input current range(max)	1mA
Gain error	2% Max. nonlinearity, 10μA to 1mA input
Peak amplitude value I_{IN} = 10 μA (1.0% 0f $I_{IN(MAX)}$) I_{IN} = 100 μA (10% 0f $I_{IN(MAX)}$) I_{IN} = 200 μA (20% 0f $I_{IN(MAX)}$) I_{IN} = 500 μA (50% 0f $I_{IN(MAX)}$) I_{IN} = 900 μA (90% 0f $I_{IN(MAX)}$) I_{IN} = 1000 μA (100% 0f $I_{IN(MAX)}$)	-3dB bandwidth 450 kHz 5 MHz 10 MHz 20 MHz 40 MHz 45 MHz

Table III Equivalent Capacitances of the Fig. 4

n	Expected Capacitance (F)	Equivalent Capacitance (F)
1	100pF	96.81pF
10	1nF	0.973nF
100	10nF	9.542nF
1000	100nF	82.25nF

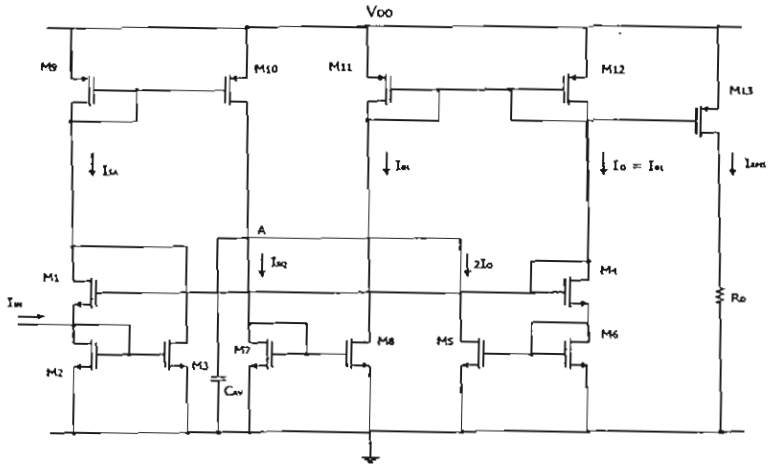

Figure 1. Schematic diagram of the rms-to-dc converter.

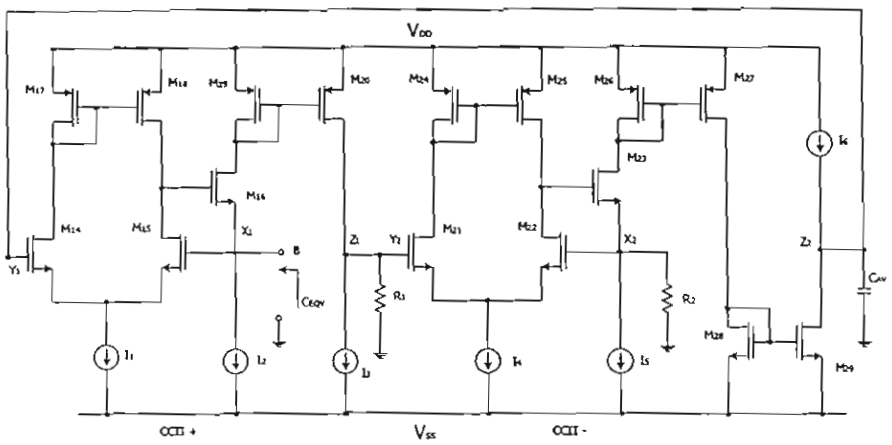

Figure 2. A current-controlled capacitance multiplier circuit.

(a) (b)

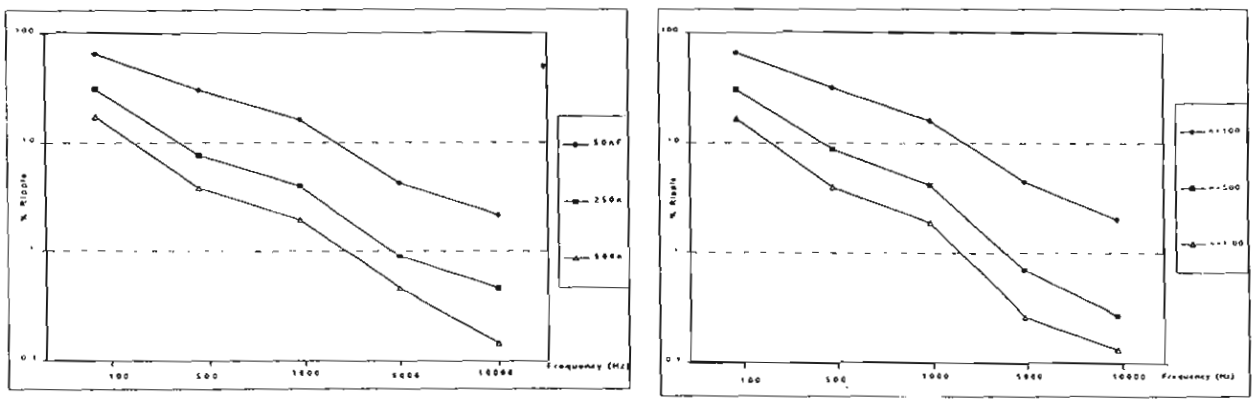

Figure 3. Plots of percent ripple versus frequency for (a) difference values of C_{AV} and (b) difference values of n.

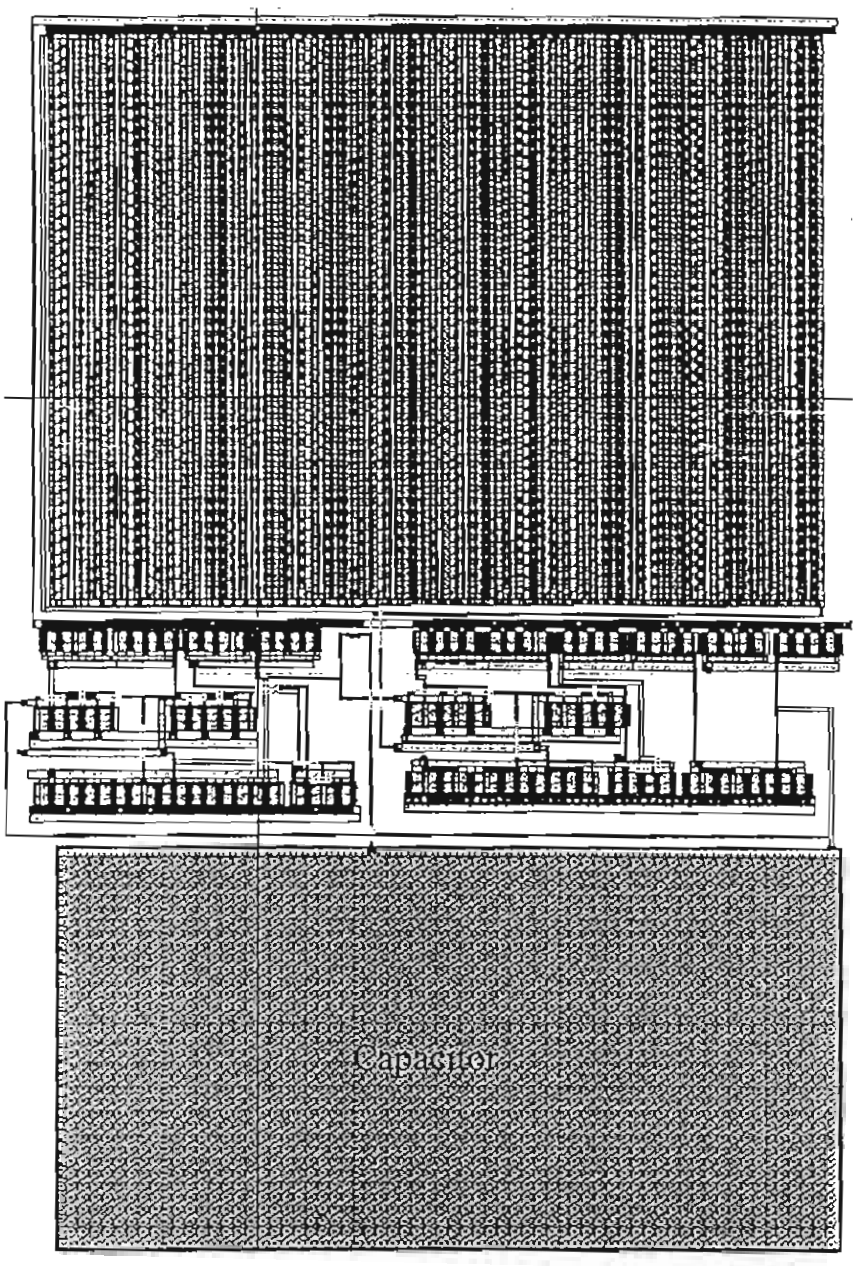

Fig. 4 Layout of the C-multiplier circuit

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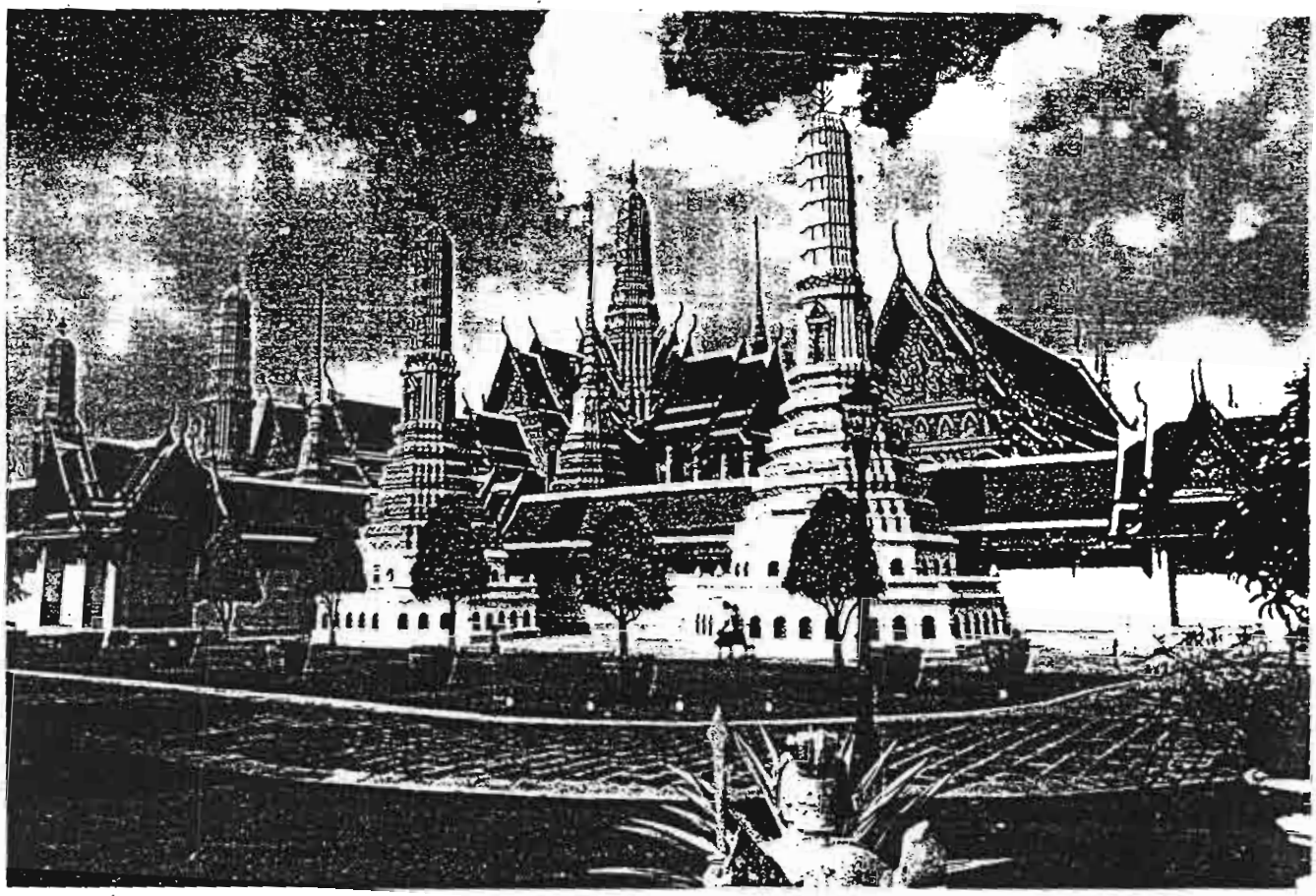

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differential, input voltage V_{AB} is applied to the bases of Q1 and Q2 across nodes A and B, and the small-signal, differential, output voltage V_{GF} is taken across the emitters of Q9 and Q10 between nodes G and F. The current I /2 biases the (Q3, Q9) and the (Q4, Q10) branches, whilst the frequency setting current I_P biases the (Q1, Q8, Q7) and the (Q2, Q5, Q6) branches. The differential pair (Q21 and Q22), functioning as a voltage-to-current converter, constitutes the required loop gain controllable by the loop-gain setting current I_G to initiate and to sustain steady-stead oscillations.

Similarly, for the second stage, the phase-lead all-pass filter is formed by ten matched transistors (Q11 to Q20), a capacitor C and current sinks I and I_P, where the small-signal, differential, input voltage V_{MN} is applied to the bases of Q11 and Q12 across nodes M and N, and the small-signal, differential, output voltage V_{OP} is taken across the emitters of Q19 and Q20 between node O and P. The current I/2 biases the (Q13, Q19) and the (Q14, Q20)branches, whilst the frequency setting current I_P biases the (Q11, Q18, Q17) and the (Q12, Q15, Q16) branches. The differential pair (Q23 and Q24) constitutes the required loop gain controllable by the loop-gain setting current I_G to initiate and to sustain steady-stead oscillations.

The input of the first stage V_{AB}, across nodes A and B, is connected to the output of the second stage $V_{A'B'}$, across nodes A'and B', but they possess the opposite polarities. On the other hand, the input of the second stage V_{MN}, across nodes M and N, is connected to the output of the first stage, and they possess the same polarities. The circuit is fully differential so as to enable accurate quadrature signals with symmetry. There are other significant, well understood, advantages in employing a fully differential realization [17]. The circuit is also relatively simple and integrable as devices can be fabricated on-chip.

3. Ideal analysis

The analysis of Fig. 1 assumes that each transistor acts as an idealized voltage-controlled current source (VCCS), where the collector current is simply equal to the small-signal voltage across the base-emitter nodes divided by r_e, where r_e is the usual ratio of the thermal voltage and the emitter bias current. The common-emitter current gain factors (β's) are also assumed to be infinite. As the two stages of Fig. 1 are identical, only the first stage will be described. For clarity, the phase-lead all-pass filter of the first stage can be described by the isolation from other connections such that the inputs of the phase-lead all-pass filter at nodes A and B are disconnected from the outputs of the second stage at nodes A′ and B′, respectively, and that the outputs of the phase-lead all-pass filter at nodes G and F are disconnected from the inputs of the differential amplifier at nodes G′ and F′, respectively.

For such isolation, it can be assumed for the moment that the bases of Q9 and Q10 at nodes D′ and E′ are temporarily disconnected from nodes D and E, respectively. As a result the bases of Q9 and Q10 at nodes D′ and E′ are then temporarily connected together to appropriate bias voltage say V_{bias}. In such temporary cases, let V_{O1} be the small-signal, differential, output voltage at node D with respect to node E, and V_{O2} be the small-signal, differential, output voltage at node F with respect to node G. The input voltage V_{AB} results in a small-signal, differential, output current $i_{d1} = sCV_{AB} / (1+s\tau)$ passing through nodes D and E and the loading resistance $4r_{e1}$ where $r_{e1} = (V_T / I_P)$ is the emitter resistance of either Q1, Q2, Q5, Q6, Q7 or Q8, V_T is the usual thermal voltage of approximately 25 mV associated with a pn junction at room temperature, and time constant $\tau = 2Cr_{e1}$. Therefore the transfer function $V_{O1} / V_{AB} = 2s\tau / (1+s\tau)$ represents a first-order high-pass filter. In addition, V_{AB} also results in another small-signal, differential, output current $i_{d2} = V_{AB} / 2r_{e2}$ passing through nodes F and G and the loading resistance $2r_{e2}$ where $r_{e2} = (2V_T / I)$ is the emitter resistance of either Q3, Q4, Q9 or Q10. Therefore the transfer function $V_{O2} / V_{AB} = 1$ represents a buffer.

By reconnecting the bases of Q9 and Q10 at nodes D′ and E′ to nodes D and E, respectively (as shown in Fig. 1), the total output voltage V_{GF} at node G with respect to node F, is obtained through superposition, i.e. $V_{GF} = V_{O1} - V_{O2}$ and hence the name 'signal differencing'. Consequently, the transfer function V_{GF} / V_{AB} represents a phase-lead all-pass filter with phase angle θ of the forms

$$\frac{V_{GF}}{V_{AB}} = -\left(\frac{1-s\tau}{1+s\tau}\right) \tag{1}$$

$$\theta = 2\tan^{-1}(\omega\tau) \tag{2}$$

where $\theta = \pi/2$ at $\omega = 1/\tau = I_f / (2CV_T)$.

As mentioned earlier, V_{AB} across nodes A and B and the resulting small-signal, differential, output voltage $V_{A'B'}$ across nodes A′ and B′ possess the opposite polarities. By reconnecting the phase-lead all-pass filter to the original connections as shown in Fig. 1, the relationship between V_{AB} and $V_{A'B'}$ can be written as

$$\frac{V_{A'B'}}{V_{AB}} = -\left[G\left(-\frac{1-s\tau}{1+s\tau}\right)\right]^2 \tag{3}$$

where $G = R / r_{e3}$ is the gain of each differential amplifier and $r_{e3} = (2V_T / I_G)$ is the emitter resistance of either Q21 or Q22 of the first stage, or either Q23 or Q24 of the second stage. For steady-state sinusoidal oscillations to be sustained, the ratio $V_{A'B'} / V_{AB}$ must be unity. Setting (3) to unity and rearranging yields

$$s^2 - s\frac{2}{\tau}\left(\frac{G^2-1}{G^2+1}\right) + \frac{1}{\tau^2} = 0 \qquad (4)$$

Upon substituting s in (4) with $j\omega_0$, and setting the real and the complex parts to zero simultaneously, the required value of G to sustain steady-state sinusoidal oscillations and the angular frequency of oscillations ω_0 can be written as

$$G = \frac{R}{r_{e3}} = R\frac{I_G}{2V_T} \qquad (5)$$

$$\omega_0 = \frac{1}{\tau} = \frac{I_F}{2CV_T} \qquad (6)$$

Equation (5) shows that the required condition for steady-state oscillations can be set by adjustments of I_G. Equation (6) indicates that the frequencies of oscillations are linearly proportional to the bias current I_F and hence the name 'current-tunable'. By substituting (6) in (2) for $\omega = \omega_0$, it follows that the phase angle θ_0 of V_{MN} of the second stage is different from the phase angle θ_1 of V_{AB} of the first stage by $\theta_0 - \theta_1 = \pi/2$. In order words, V_{MN} and V_{AB} provide quadrature oscillation of values $\cos\theta_0$ and $\sin\theta_0$, respectively, and hence the name 'sinusoidal quadrature oscillator'.

4. Simulation results

The performance of the circuit shown in Fig. 1 has been simulated through PSPICE. Q2N3904 and QMPS3640 model the npn and pnp transistors, where the average transition frequencies (f_T) are at 300 and 500 MHz, respectively. As an example, the values of capacitor C is equal to 1000 pF, R = 50 Ω, bias current I and I_G are approximately 200 μA and 1.2 mA, respectively. Figure 2 shows the resulting sine and cosine oscillograms of the quadrature waveforms V_{AB} and V_{MN}, respectively, at I_F = 700 μA where the oscillation frequency is measured to be 2 MHz. Figure 3 illustrates comparisons of the plots of oscillation frequencies and amplitudes versus bias current I_F for cases of ideal analysis and PSPICE analysis. As shown in Fig. 3, the oscillation frequencies are tunable by the bias current I_F over approximately three orders of magnitude. It can be seen from Fig. 3 that the maximum useful frequency of oscillation is approximately 19 MHz.

Figure 4 depicts the amplitude matching (dB) in terms of the ratio V_{AB}/V_{MN}, as well as the phase matching (deg) in terms of [(phase of V_{AB}) – (phase of V_{MN})] of the quadrature signals versus frequency. The amplitude matching is as near as 0.004 dB, whilst the phase matching for 90° is better than 0.17°.

5. Conclusions

A fully-differential current-tunable sinusoidal quadrature oscillator has been presented using r_e tunable phase-lead all-pass filters as the frequency-selective network. The filter is realized through the use of a signal-differencing technique. The oscillation frequency is current-tunable over a wide-frequency sweep range of approximately three orders of magnitude. The amplitude matching and the quadrature phase matching are better than 0.004 dB and 0.17°, respectively. The maximum useful frequency of oscillation is approximately 19 MHz.

6. Acknowledgements

The authors are grateful to Mr. M. Watchakittikorn for his useful suggestion. This work is partly funded by the Thailand Research Fund (TRF) under the Senior Research Scholar Program, grant number RTA/04/2543. The support provided by the Japan International Cooperation Agency (JICA) is also acknowledged.

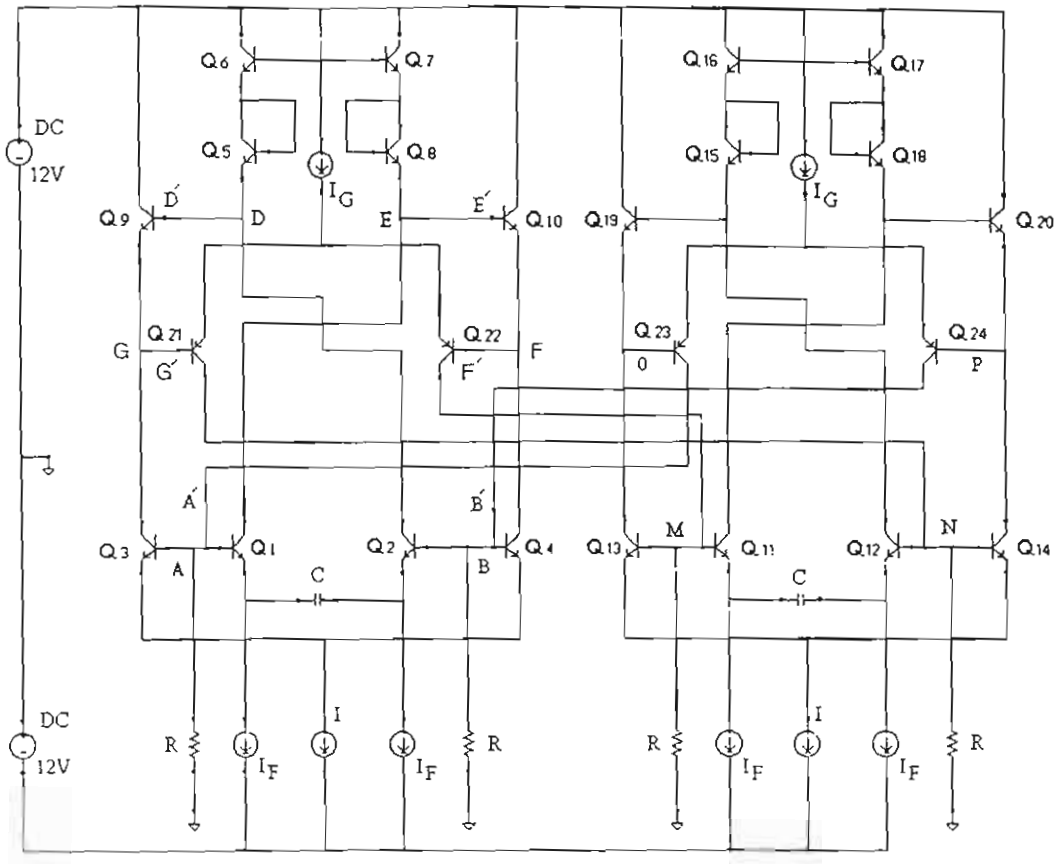

Figure 1. Circuit diagram of the fully balanced high-frequency sinusoidal quadrature oscillator using current-tunable phase-lead all-pass filters

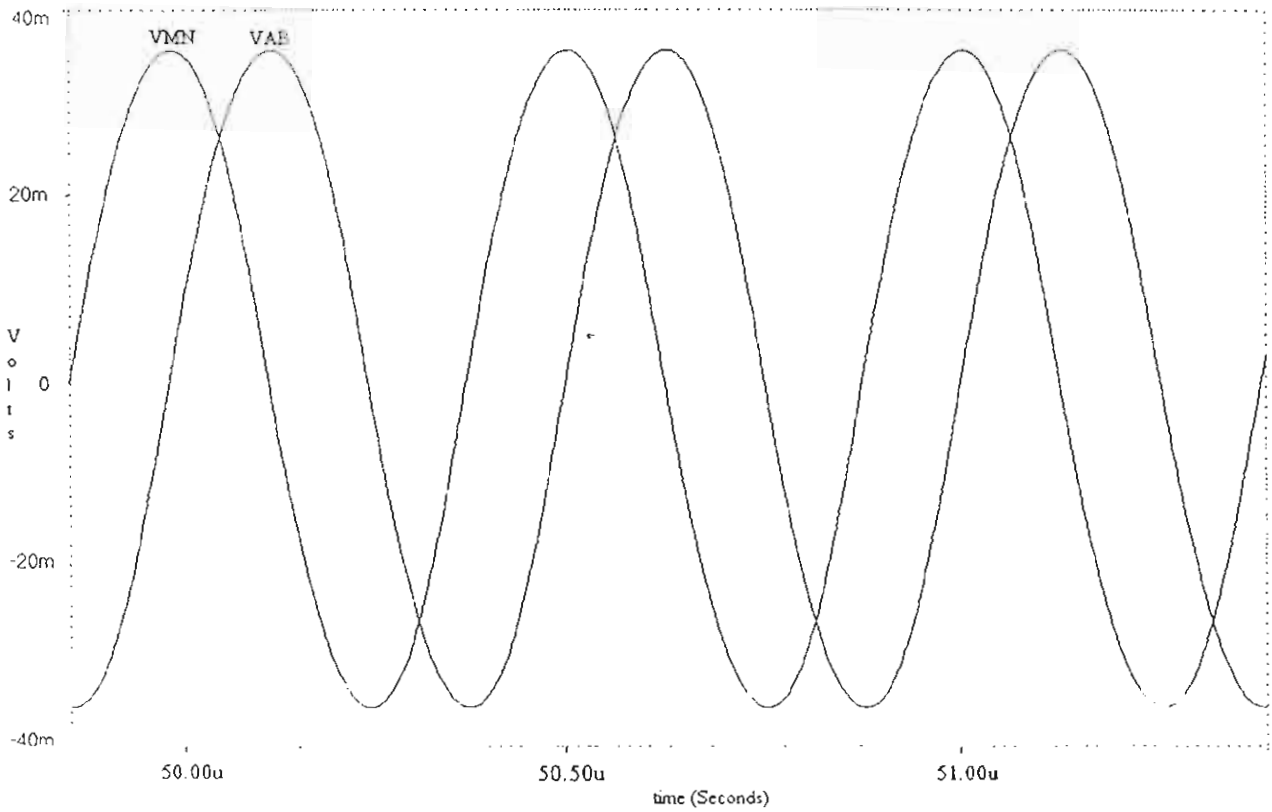

Figure 2. Oscillograms of the quadrature waveforms V_{AB} and V_{MN} at $I_P = 700\ \mu A$

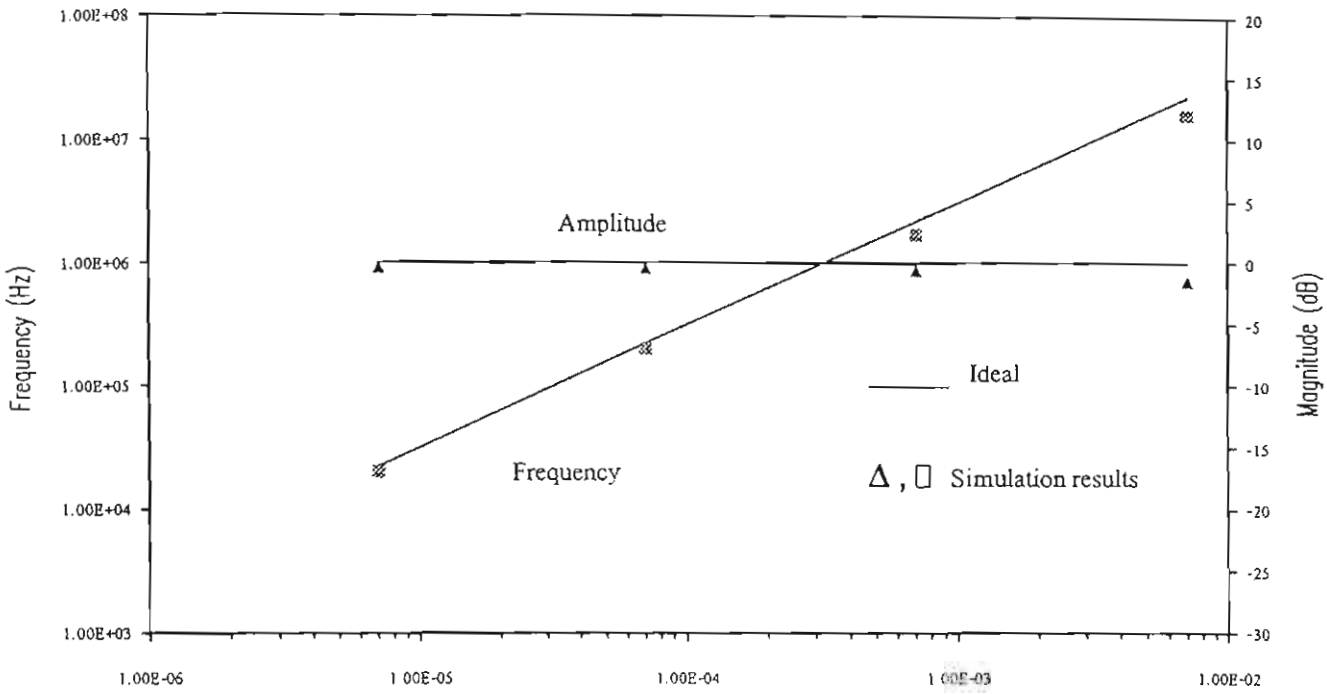

Figure 3 : Plots of oscillation frequencies and amplitude versus bias current I_F

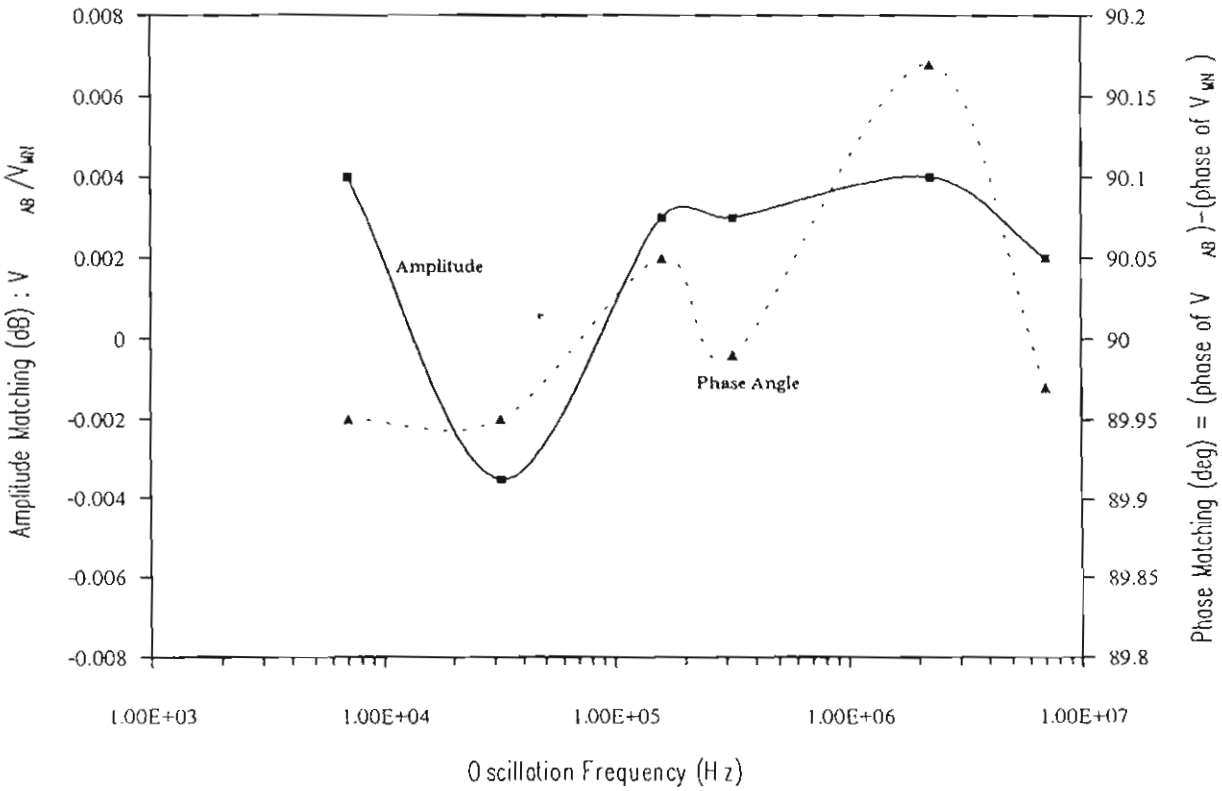

Figure 4 . Amplitude and phase matching of the quadrature signals versus frequency

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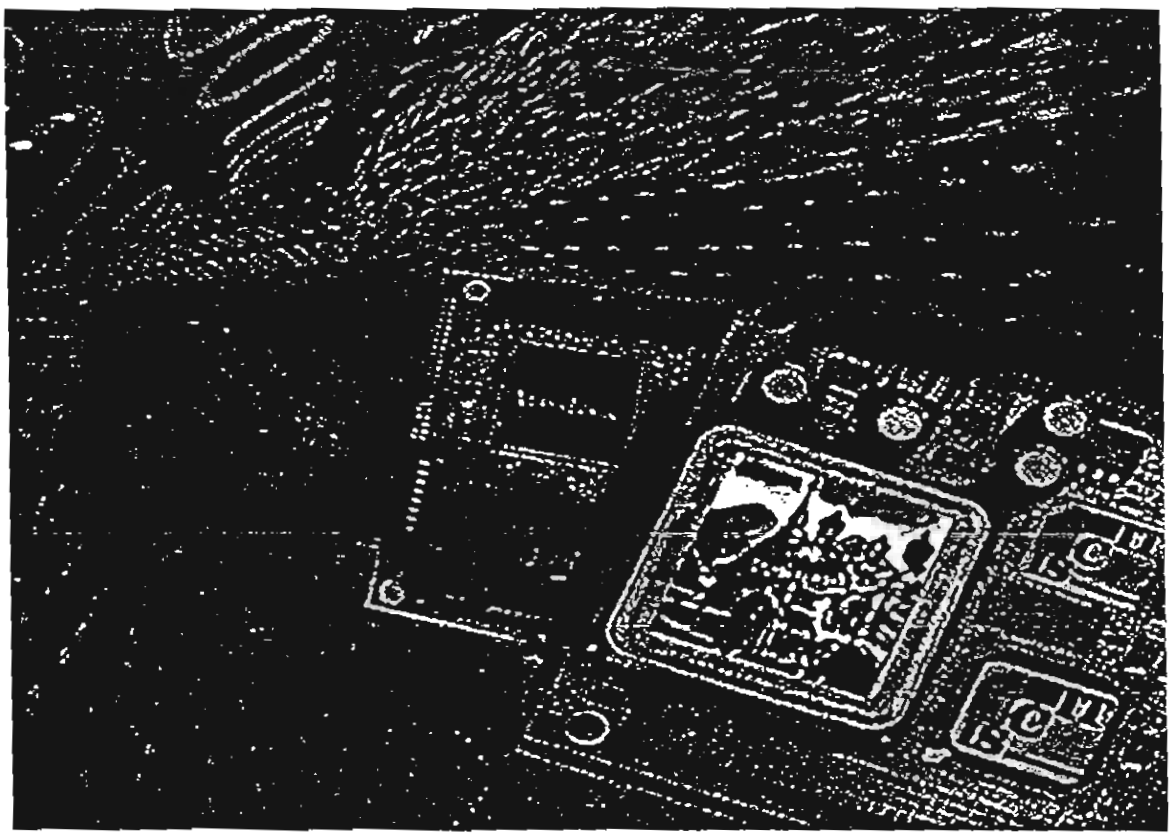

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TUNABLE FTFN AND ITS APPLICATIONS

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ABSTRACT

This paper proposes a circuit configuration for the realization of a four-terminal floating nullor (FTFN) with electronically tunable current gain. It mainly employs a transconductance amplifier, an improved translinear cell, two complementary current mirrors with variable current gain and five improved Wilson current mirrors, which provides wide bandwidth and suitability to implementation in monolithic bipolar technology. The validity of the performance of the scheme is verified through PSPICE simulation results. Some example applications employing the proposed tunable FTFN as a tunable active element show that the circuit properties can be varied by electronic means are also included.

1. INTRODUCTION

Presently, current-mode circuits have drawn a considerable owing to their significant advantages, which are elementary wide bandwidth, wider dynamic range, simpler circuitry and low power consumption [1]. The realizations of current-mode circuits using high performance active devices such as, a second-generation current conveyor (CCII), a current feedback op-amp (CFA) and a four-terminal floating nullor (FTFN), have been recently reported. However, it has been demonstrated that the FTFN is more flexible and versatile building block than other active devices [2-3]. These lead up to the growing interest in designing current-mode circuits based on the use of FTFN as an active element, for instance, filters, gyrators, sinusoidal oscillators and floating immittances [2-5]. This is due to the fact that the FTFN-based structures provide a number of potential advantages such as, complete absence of passive component-matching requirement, minimum number of employed passive elements and improvement of high frequency characteristic [6]. Although there are many FTFN realizations that have been available in the literatures [7-9], the realization scheme of an electronically tunable FTFN that is suitable for implementing monolithic integrated circuit form has not yet been reported. The FTFN whose the current gain can be tuned by electronic means seems to be more attractive, flexible and suitable for design and implementation of the frequency selective systems, such as, biquads, oscillators and so forth.

Therefore, this paper proposes an alternative scheme for realizing a monolithically integrable FTFN that can provide variable current gain. The proposed circuit is simple and based on the use of a transconductance amplifier, an improved translinear cell and some current mirrors. Some applications using the proposed tunable FTFN are given with the simulation results and will show that the characteristics of the resulting circuit become an electronically tunable.

2. CIRCUIT DESCRIPTION

2.1 Nullor Model of the FTFN

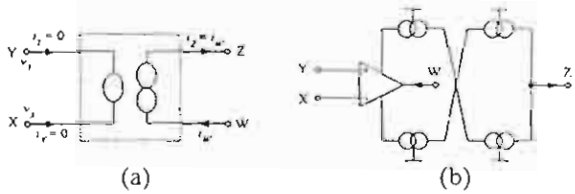

Fig.1 : Model of the FTFN
(a) an ideal nullor model
(b) possible implementation model

An FTFN is a high gain transconductance amplifier with floating input and output terminals or can be called as an operational floating amplifiers (OFAs) [6]. The nullor model of an ideal FTFN is shown in Fig.1(a), where the port characteristics can be described as :

$$i_Y = i_X = 0 \ , \ v_X = v_Y \quad \text{and} \quad i_Z = i_W \qquad (1)$$

It should be noted that the output impedance of the W- and Z-ports are generally arbitrary. However, most of the FTFNs are traditionally realized from the basic type shown in Fig.1(b), where the output impedance of the W-port is very low and that of the Z-port is very high. This type of FTFN is also called as operational mirrored amplifiers (OMAs) [7]. In addition, the usefulness of the FTFN can be extended if eqn.(1) is implemented in such a way that the current transfer ratio between i_W and i_Z can be varied by electronic means, in which case

a more generalized tunable FTFN should be investigated.

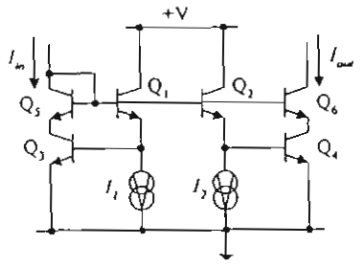

Fig.2 : Cascode npn current mirror with adjustable current gain

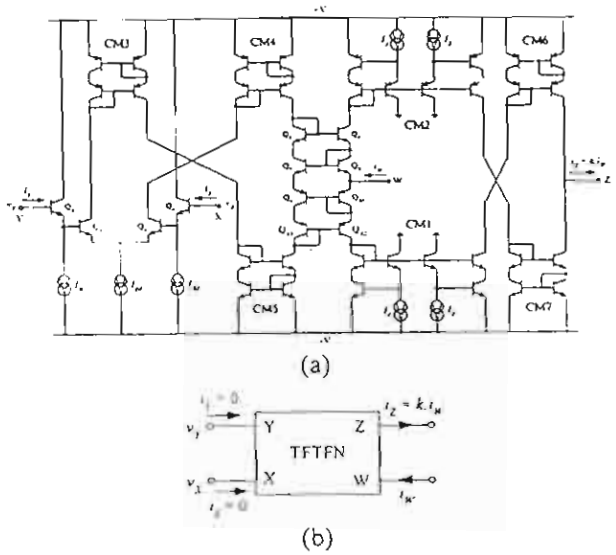

Fig.3 : The proposed tunable FTFN (a) circuit diagram (b) its symbol

2.2 Current Mirror with Adjustable Current Gain

Fig.2 shows the cascode npn current mirror that can adjustable the current gain by the external bias currents, where I_{in} and I_{out} are the input and output signal currents. Transistors Q_1 to Q_4 function as a classical translinear loop, and the currents I_1 and I_2 are the external dc bias currents with controllable values [10]. In addition, the cascode stages Q_5 and Q_6 provide the high output impedance and also lead to minimize the severe peaking of the frequency responses. Applying the translinear principle and assuming that all the transistors are well matched with the common-emitter current gains β are >> 1, then the relationship of the collector currents can be characterized by the following equation :

$$I_{C1}I_{C3} = I_{C2}I_{C4} \qquad (2)$$

where $I_{C1} = I_1$, $I_{C2} = I_2$, $I_{C3} = I_{in}$ and $I_{C4} = I_{out}$. Therefore, the output current I_{out} of this circuit becomes

$$I_{out} = k.I_{in} \qquad (3)$$

where k is the current gain of the mirror and equals to the ratio of the external bias currents I_1/I_2.

2.3 Proposed Tunable FTFN

The circuit implementation and representation of the proposed tunable FTFN, namely TFTFN, with variable current gain is shown in Fig.3, which is suitable for the implementation in bipolar integrated circuit form. The proposed circuit consists of a transconductance amplifier Q_1-Q_4, an improved translinear cell Q_5-Q_{12}, two complementary current mirrors with controlled current gain CM1-CM2 and five standard improved Wilson current mirrors CM3-CM7. Transistors Q_1-Q_4 and the bias currents I_{B1}-I_{B3} function as a transconductance amplifier with very high input impedance so that $iY \cong iX \cong 0$. If Q_1-Q_4 are perfectly matched, then the voltage at node X will follow the voltage at the port Y, or $vX \cong vY$. Group of transistors Q_5-Q_{12} forms an improved translinear cell, which Q_7-Q_{10} functions as a dual translinear loop. It should be noted that the so called "piled-stage structure" [11] consisting of eight transistors which can improve performance and accuracy of the basic loop is employed, where the standard translinear condition $V_{CB} = 0$ are forced by the additive cascode transistors Q_5, Q_6, Q_{11} and Q_{12}.

Ideally, it is required that the pair of transistors Q_7-Q_8 and Q_9-Q_{10} are closely matched and the cascode current mirrors CM3, CM4 and CM5 have the exactly unity gain. Consequently, for $vY \cong vX \cong 0$, the quiescent currents through Q_6, Q_8 and Q_{10}, Q_{12} are respectively equal to the quiescent current of the diode-connected transistors Q_5 and Q_{11}, and are equal to $I_{B1}/2$. This translinear cell performs as a current follower, where its allow an input current iW to source and sink at terminal W. By two complementary variable-gain current mirrors CM1-CM2 and assuming that the current gain of the current mirrors CM6-CM7 are equal to unity, the current iW flowing through the port W will be reflected and inverted to the port Z, which has the current transfer ratio as $k = iZ/iW$. The output impedance at the port W is low since it is looking into the emitters of translinear cell's transistors while the output impedance of the port Z is very high due to the effective parallel combination of output impedances of the cascode current mirrors CM6 and CM7. Therefore, this TFTFN will provide a unity voltage transfer between ports Y and X, and a current transfer between ports W and Z that the gain value is equal to k. The voltage-current characteristics of this device can be characterized as follows:

$$i_Y = i_X = 0 \ , \ v_X = v_Y \quad \text{and} \quad i_Z = k.i_W \quad (4)$$

we can see that the proposed FTFN in Fig.3 can be tuned electronically by adjusting the ratio of the external bias currents I_1/I_2.

3. SIMULATION RESULTS

The performance of the proposed TFTFN in Fig.3 has been verified by PSPICE simulation results. The simulation results were obtained employing the AT&T ALA400-CBIC-R process parameters of NR100N and PR100N for npn and pnp transistors, respectively [12]. The bias currents were set to I_{B1} = 1 mA, $I_{B2} = I_{B3}$ = 50 μA and the supply voltages were set to +V = -V = 5V. Fig.4 shows the characteristic of the open loop transconductance gain of the proposed circuit. From the response, it can be measured that the –3dB bandwidth in a high frequency as nearly as 1 4 MHz and the transconductance gain of about 1.3 A/V is obtained.

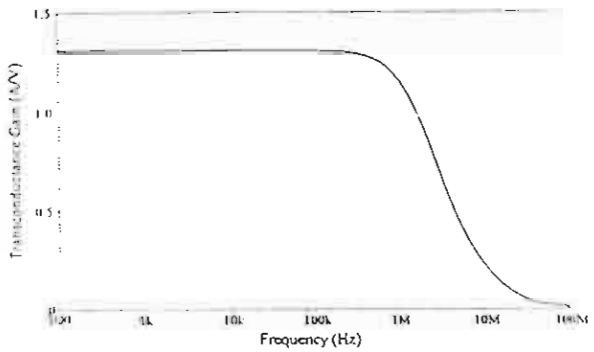

Fig.4: Simulated open loop transconductance gain

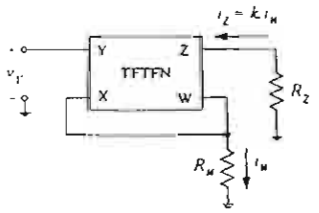

Fig.5: TFTFN-based voltage-to-current converter

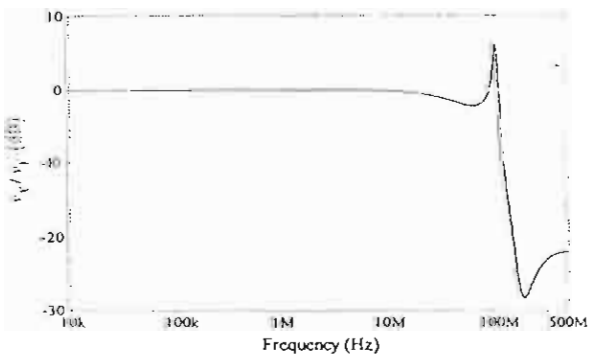

Fig.6 : Voltage transfer characteristic v_X/v_Y

In order to demonstrate the tunable performances of the proposed circuit, the TFTFN was used to construct the voltage-to-current converter shown in Fig.5 with R_W = 1 kΩ and output Z short-circuited. The voltage transfer characteristic from the port Y to the port X is shown in Fig.6. Fig.7 represents the frequency responses of the current gain k , for three different values of the dc bias current I_1 whereby I_2 is set to 100 μA . The simulated current transfer characteristic proves that the circuit can exhibit an electronically tunable current gain over a very wide current range.

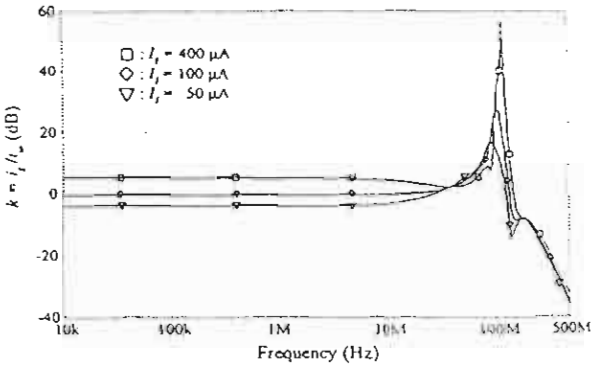

Fig.7 : Current transfer characteristic i_Z/i_W when the external bias current I_1 was varied.

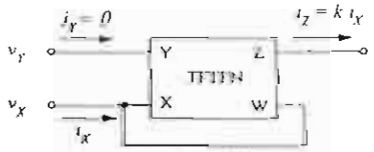

Fig.8 : An electronically tunable current conveyor

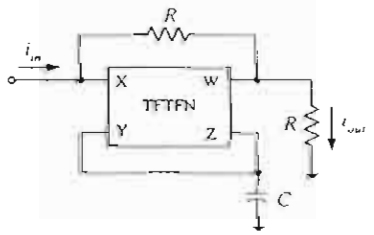

Fig.9 : Current-mode allpass filter using TFTFN

4. APPLICATION EXAMPLES

In this section, the outlines of some examples on the application of the proposed TFTFN as a tunable active element will be described, demonstrating the wide-ranging usefulness of this device. The first one is an electronically tunable current conveyor. It can be slightly modified from the circuit of Fig.3 by connecting the low-output-impedance port W to the port X as shown in Fig.8, then the circuit behaves as an electronically tunable negative current conveyor. From direct inspection of the circuit readily shows that the port relations of the tunable current conveyor of this case can be written

as :

$$v_X = v_Y \ , \ i_Y = 0 \quad \text{and} \quad i_Z = k i_X \qquad (5)$$

As the second example of the proposed TFTFN, it was constructed an electronically tunable current-mode allpass filter shown in Fig.9. The circuit is based on a current-mode allpass filter by using FTFN with grounded capacitor [3], routine analysis yields the current transfer function expressed by

$$\frac{I_{out}(s)}{I_{in}(s)} = \frac{1-\left(sRC/k\right)}{1+\left(sRC/k\right)} \qquad (6)$$

and

$$\theta_d = -2\tan^{-1}\left(\frac{\omega RC}{k}\right) \qquad (7)$$

where θ_d is the phase angle of the filter. As an example, the simulation results of a current-mode allpass filter in Fig.9 were presented with R = 1 kΩ, C = 1 nF, this phase shifter was designed for a 90° phase shift at $\omega_0/2\pi$ = 159 kHz when k = 1 (I_1 = I_2 = 100 μA). Fig.10 shows the frequency responses of the filter of Fig.9 for three different values of the control currents, I_1. In the figure, it can be seen that the parameter θ_d can be adjusted by controlling the current gain $k = I_1 / I_2$. This confirms the validity of the results of the theoretical analysis.

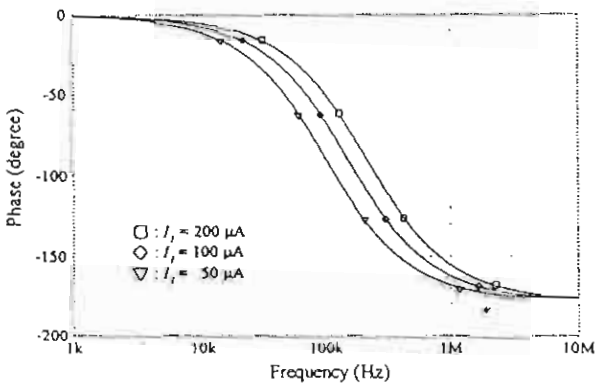

Fig.10 : Frequency responses of the TFTFN-based current-mode allpass filter

5. CONCLUSIONS

A generalized electronically tunable FTFN, which is suitable for realizing in bipolar monolithic integrated circuit form, has been presented. Simulation results obtained from PSPICE program verify the high qualification performances of the proposed circuit. Some application examples have been demonstrated that the use of the proposed scheme is attractive in that the obtained characteristic of the circuit will become electronically tunable.

6. ACKNOWLEDGEMENT

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REALIZATION OF CURRENT-MODE FTFN-BASED LOWPASS FILTER FROM THE OPTIMAL SALLEN AND KEY LOWPASS FILTER (SARAGA DESIGN) USING DRIVING POINT IMPEDANCE AND SIGNAL-FLOW GRAPH (DPI/SFG) METHOD TO PRESERVE THE SENSITIVITIES OF THE ORIGINAL CIRCUIT

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ABSTRACT

This paper shows that the current-mode FTFN-based lowpass filter obtained from the optimal voltage-mode op-amp-based Sallen and Key lowpass filter (Saraga Design) using driving point impedance and signal-flow graph (DPI/SFG) method preserves the optimal passive sensitivities and has better active sensitivities.

1. INTRODUCTION

Analog circuits are always requested to work at high frequencies where digital signal processing faces difficulties with implementation. In particular recent increasing needs of wireless communications, such as W-CDMA, Bluetooth, ITS. etc., require analog circuits which process signals in a giga-hertz frequency range [1]. Nowadays, Semiconductor Industry Association needs low power consumption chip and analog and digital circuits are implemented on the same chip using the same dc power supply that is less than 1.5V and will decrease to 0.5V in 2011 [1]. In order to correspond to the severe demands for high frequency and low power-supply voltage operation on analog circuits, current is found to be a key word in the 1990's. So, current signal processing is one of the most promising solutions. Circuits with current input and output signals are often called a 'current-mode' circuit. Reduction in power-supply voltage restricts voltage-signal swings extremely. To avoid this problem, current-mode circuits are used because current-signal swings are not restricted by power supply voltages.

Because passive and active RC circuits are already excellent tabulated, if we can use some transformation to obtain their current-mode circuit counterparts and use proper active devices. They may have better performances. In this paper, we use the optimal voltage-mode op-amp-based Sallen and key lowpass filter (Saraga Design) as the prototype because it is still popular to use in many fields such as wireless communications [2]. We use driving point impedance and signal-flow graph (DPI/SFG) method [3-4] to obtain its current-mode circuit counterpart. We use four-terminal floating nullor (FTFN) as an active device because of its versatility [5-7].

2. REALIZATION

The prototype of a voltage-mode op-amp-based Sallen and Key lowpass filter [8] is shown in figure 1.

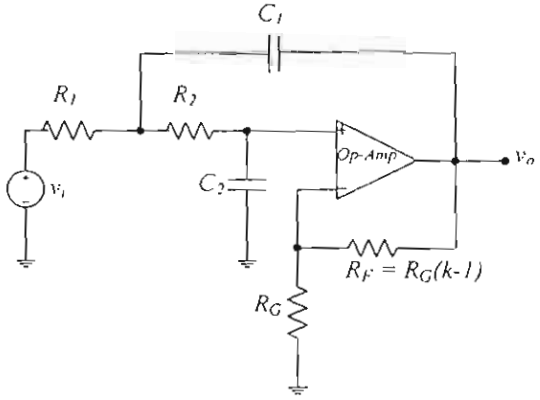

Fig. 1 A voltage-mode op-amp-based Sallen and Key lowpass filter

The voltage transfer function of the circuit in Figure 1 is as follows :

$$\frac{V_o}{V_i} = \frac{k_v/R_1R_2C_1C_2}{s^2 + s\left[\frac{1}{R_1C_1} + \frac{1}{R_2C_1} + \frac{(1-k_v)}{R_2C_2}\right] + \frac{1}{R_1R_2C_1C_2}} \quad (1)$$

where

$$k_v = 1 + \frac{R_F}{R_G} = \text{noninverting voltage gain} \quad (2)$$

$$K_v = k_v / R_1 R_2 C_1 C_2 = \text{voltage gain constant} \quad (3)$$

$$\omega_p = \sqrt{1/R_1 R_2 C_1 C_2} = \text{pole angular frequency} \quad (4)$$

$$Q_p = \frac{\sqrt{1/R_1 R_2 C_1 C_2}}{\frac{1}{R_1 C_1} + \frac{1}{R_2 C_1} + \frac{1-k_v}{R_2 C_2}} = \text{pole } Q \quad (5)$$

Saraga Design equations are as follows :

$$k = \frac{4}{3}, C_1 = \sqrt{3} Q_p, C_2 = 1,$$
$$R_1 = \frac{1}{Q_p \omega_p}, R_2 = \frac{1}{\sqrt{3}\omega_p}, \frac{R_2}{R_1} = \frac{Q_p}{\sqrt{3}} \quad (6)$$

Follow the proposed procedure of DPI/SFG method in References [3-4], the obtained current-mode Sallen and Key lowpass filter is shown below.

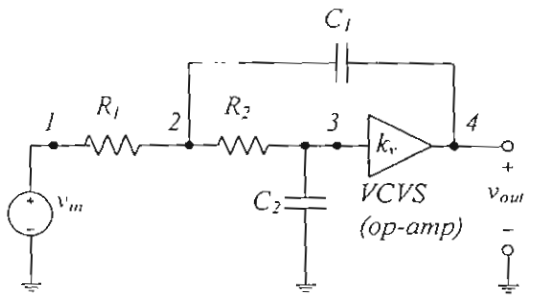

Fig. 2 A voltage-mode op-amp-based Sallen and Key low pass filter

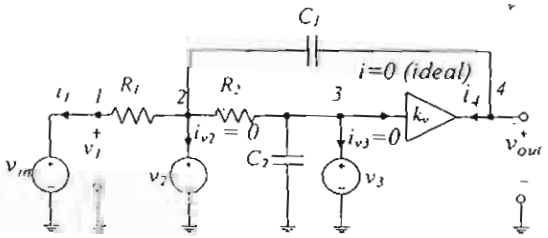

Fig. 3 The same filter as shown in Fig.2 with auxiliary sources (v_2 and v_3)

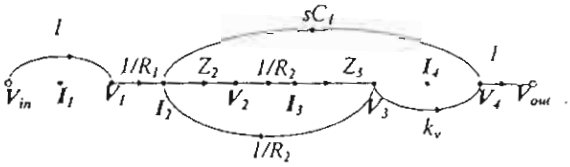

Fig. 4 Signal – flow graph of the circuit in Fig. 3

Some notations in Figure 4 are described below.

I_2 = the sum of currents contributed by all voltage sources except the auxiliary voltage source V_2

Z_2= the driving point impedance at node 2

$$= \frac{1}{\frac{1}{R_1} + \frac{1}{R_2} + sC_1} \quad (7)$$

$$V_2 = I_2 Z_2 \quad (8)$$

I_3 = the sum of currents contributed by all voltage sources except the auxiliary voltage source V_3

Z_3= the driving point impedance at node 3

$$= \frac{1}{\frac{1}{R_2} + sC_2} \quad (9)$$

$$V_3 = I_3 Z_3 \quad (10)$$

Apply Mason's gain formula [9] to the signal-flow graph in Figure 4, we get the voltage transfer function shown in equation *(11)*.

$$\frac{V_{out}}{V_{in}} = \frac{k_v / R_1 R_2 C_1 C_2}{s^2 + s\left[\frac{1}{R_1 C_1} + \frac{1}{R_2 C_1} + \frac{(1-k_v)}{R_2 C_2}\right] + \frac{1}{R_1 R_2 C_1 C_2}} \quad (11)$$

Equation *(11)* is exactly the same as equation *(1)*.

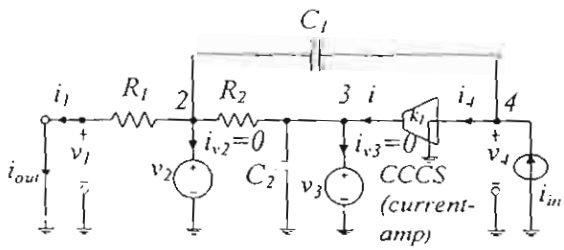

Fig. 5 The obtained current-mode Sallen and Key lowpass filter

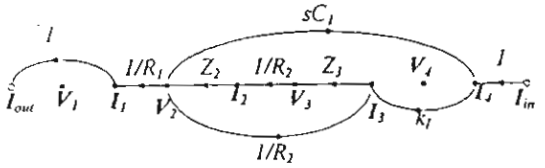

Fig. 6 Signal-flow graph of the circuit in Fig.5

Again, apply Mason's gain formula [9] to the signal-flow graph in Figure 6, we get the current transfer function shown in equation *(12)*.

$$\frac{I_{out}}{I_{in}} = \frac{k_1/R_1R_2C_1C_2}{s^2 + s\left[\frac{1}{R_1C_1} + \frac{1}{R_2C_1} + \frac{(1-k_1)}{R_2C_2}\right] + \frac{1}{R_1R_2C_1C_2}} \quad (12)$$

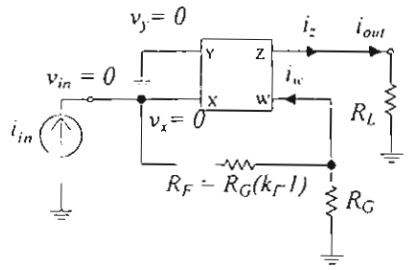

Fig. 7 FTFN-based current amplifier

The circuit in Figure 7 is proposed in Reference [7] for ideal FTFN-based current amplifier. So that the noninverting current gain (k_1) is given in equation *(13)*.

$$k_1 = 1 + \frac{R_F}{R_G} \quad (13)$$

Since k_1 is equal to k_v, hence the right-hand side of equation *(12)* is equal to the right-hand side of equation *(11)* for the ideal active devices.

In the case of real FTFN, we consider non-linearities of voltage and current too. Let

$$\alpha = 1 - \varepsilon, \ |\varepsilon| << 1 \quad (14)$$

and

$$\beta = 1 - \delta, \ |\delta| << 1 \quad (15)$$

where α = voltage tracking coefficient
ε = voltage tracking error
β = current tracking coefficient
δ = current tracking error

Given

$$v_x = \alpha v_y \quad (16)$$

And

$$i_z = \beta i_w \quad (17)$$

For the circuit in Figure 7,

$$v_{in} = v_x = v_y = 0 \quad (18)$$

From routine circuit analysis of Figure 7 that incorporated nonlinearities, we get

k_{IR} = real noninverting current gain = βk_1 *(19)*

Thus, the transfer function of current-mode real FTFN-based Sallen and Key lowpass filter is as follows :

$$\frac{I_{out}}{I_{in}} = \frac{\beta k_1/R_1R_2C_1C_2}{s^2 + s\left[\frac{1}{R_1C_1} + \frac{1}{R_2C_1} + \frac{(1-\beta k_1)}{R_2C_2}\right] + \frac{1}{R_1R_2C_1C_2}} \quad (20)$$

3. SENSITIVITY ANALYSIS

Since the RHS of equation *(12)* is exactly the same as the RHS of equation *(11)* because $k_1 = k_v$, then, all biquad parameters are the same. Thus, all the passive sensitivities are preserved.

Active sensitivities are found from equation *(20)*.

Given

$K_1 = k_1/R_1R_2C_1C_2$ = current gain constant *(21)*

and

$$K_{1R} = \beta K_1 \quad (22)$$

Thus

$$S_\alpha^{K_{IR}} = S_\alpha^{\omega_p} = S_\alpha^{Q_p} = S_\beta^{\omega_p} = 0 \quad (23)$$

If equations *(14)* and *(15)* hold, then

$$S_\beta^{Q_p} \cong 0 \quad (24)$$

And

$$S_\beta^{K_{IR}} = S_\beta^{\beta K_1} = 1 \quad (25)$$

All active sensitivities are very low. Thus, the current-mode circuit is better than its voltage-mode counterpart.

4. CONCLUSIONS

This paper shows that using DPI/SFG method with the optimal voltage-mode op-amp-based Sallen and Key lowpass filter (Saraga Design) to

obtain the current-mode FTFN-based lowpass filter can preserve the optimal passive sensitivities, has better active sensitivities and added condition is not needed.

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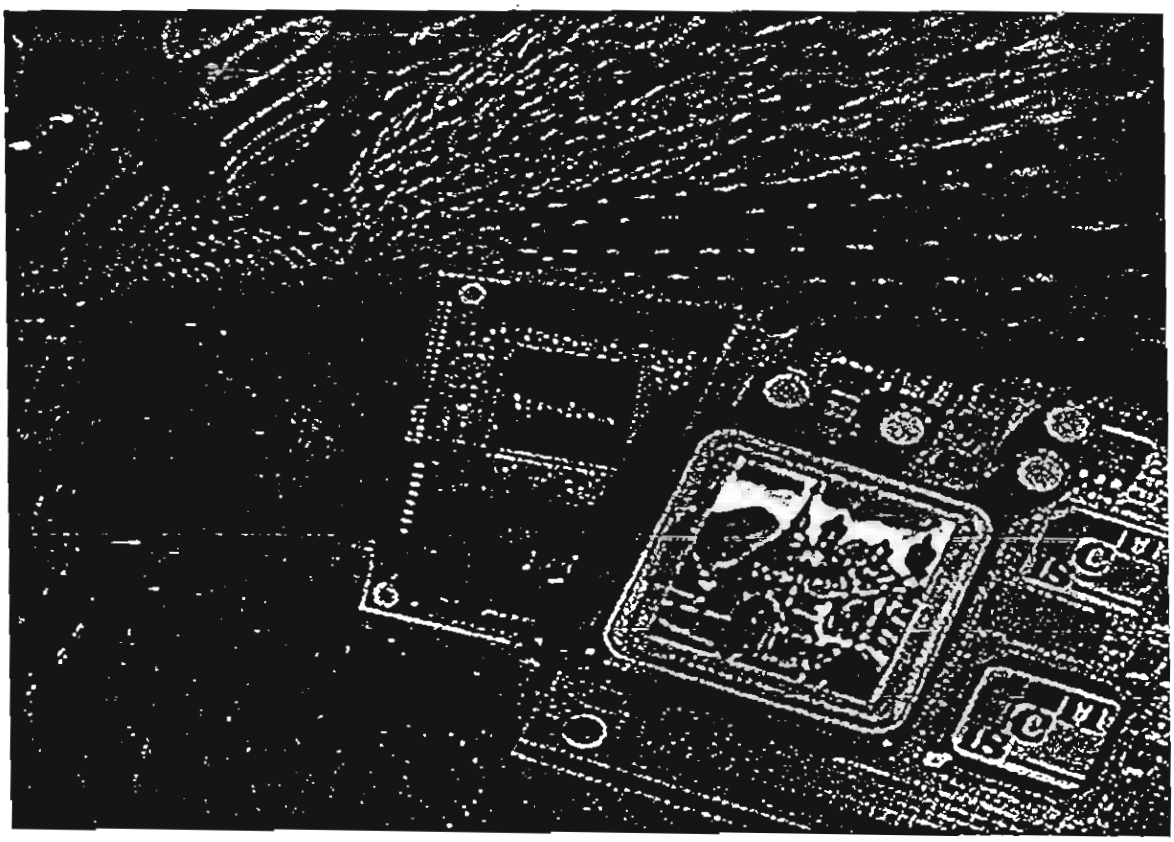

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AN INTEGRABLE CMOS-BASED TRUE RMS-TO-DC CONVERTER USING CLASS AB AMPLIFIER

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ABSTRACT

In this paper, a new integrable CMOS circuit designs technique to realize a grounded-capacitor true RMS-to-DC converter is described. The true RMS-to-DC converter does not require a full-wave rectifier and is implemented using a low-pass filter and squarer circuits. The conversion circuit consists of a class AB amplifier circuit, five simple current mirrors and a grounded capacitor. The circuit is suitable for many input waveforms of both voltage and current inputs. In order to reduce the value of the capacitor suitable for monolithic integration, a capacitance multiplier circuit that can multiply the value of the capacitance for the order of 1,000 time is also presented. The performance of the proposed circuit and the Layout is studied through SPICE and Cadence simulation results.

1. INTRODUCTION

A true RMS-to-DC converter, that is able to convert an AC signal into the DC signal in the RMS value, is usually used for measuring the average energy content in an electrical signal [1]. The true RMS to DC converter is found useful in the fields of instrumentation, communication and display system, for example, thermal RMS-to-DC converter automatic gain control and zero mean random signal etc. [1]. Many true-RMS-to DC converter circuits do exit in the literature [2-4]. However, their design methods are based on bi-polar integrated circuit technology and the RMS-to-DC conversions are mostly performed through the use of a full-wave rectifier and a multiplier/divider circuits employing a log-antilog principle. Due to the bandwidth and the slew-rate of the full-wave rectifiers, the accuracy and the useful frequency range of the converters are limited. And the size of the circuit is quite large, because the design methods are based of the use of OP-AMPs (Operational Amplifiers)[5]. The purpose of this paper is to present a CMOS circuit design technique for the realization of a true RMS-to-DC converter, where a grounded capacitor is used. A full-wave rectifier is not require for this realization scheme. The conversion circuit is simple, suitable for implementing in monolithic integrated form. The performances of the conversion circuit are studied from SPICE of Cadence simulation results.

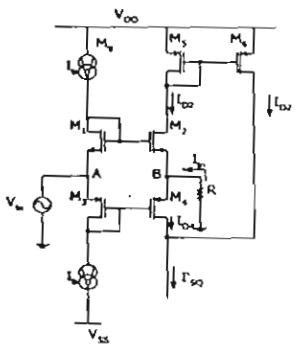

Fig. 1 A Squaring circuit

2. CIRCUIT DESCIRPTION

2.1 The Class AB squaring circuit

Consider the schematic diagram of the squaring circuit in Fig.1. Transistors M_1 through M_4 function as a class AB amplifier circuit. The transistors M_1 and M_3 are biased by the bias current I_b and $I_{D1} = I_{D3} = I_b$. Assuming that all the MOSFET transistors are biased in the strong inversion region, an input signal current I_{in} is injected into point B, then the currents I_{D2} and I_{D4} can be respectively written as

$$I_{D2} = \frac{\left(4I_b - I_{in}\right)^2}{16I_b} \quad \text{for} \quad |I_{in}| \le 4I_b \tag{1}$$

and

$$I_{D4} = \frac{\left(4I_b + I_{in}\right)^2}{16I_b} \quad \text{for} \quad |I_{in}| \le 4I_b \tag{2}$$

Since transistors M_5 and M_6 form the negative current mirror (CM_1) that reflects the current I_{D2} (current transfer ratio of 1:1) in order to add with the current I_{D4}, then the output current I'_{SQ} becomes

$$I'_{SQ} = I_{D2} + I_{D4} = 2I_b + \frac{I_{in}^2}{8I_b} \tag{3}$$

We can see that the current I'_{SQ} consists of the DC current $2I_b$ and the signal current that is the squaring of the input signal I_{in}.

For a voltage mode, the input voltage V_{in} will applied at port A and the conversion resistance R, that convert the input voltage V_{in} in to the input current I_{in}, is connected at port B. By assuming the voltage at

port A is accurately transformed to port B, where $I_{in} = V_{in}/R$ [6], then in this case the current I'_{SQ} can be expressed as

$$I'_{SQ} = 2I_b + \frac{V_{in}^2}{8I_bR^2} \tag{4}$$

From the eqns. (3) and (4), if the DC currents $2I_b$ can be compensated, the circuit will be functioned as a squaring circuit. This class AB current squaring circuit will be the key circuit building block to realize the true RMS-to-DC converter.

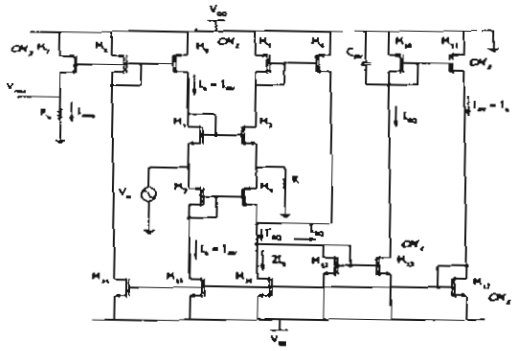

Fig.2 Schematic diagram of true RMS-to-DC converter

2.2 The Proposed True RMS-to-DC converter

The proposed true RMS-to-DC converter circuit is shown in the Fig.2, where the circuit is composed of the class AB squaring circuit in the Fig.1 in combination with four current mirrors (CM_2 through CM_5). From the circuit of Fig.2 and from the eqn. (3), since the drain current of the transistor M_{16} of the current mirror CM_5 sources the current $2I_b$ from the current I'_{SQ}, the current I_{SQ} can be expressed as

$$I_{SQ} = \frac{I_{in}^2}{8I_b} \tag{5}$$

By the reflection of the current mirror CM_4 formed by transistors M_{12} and M_{13}, the current I_{SQ} is injected into the first-order current mode low-pass filter or the averaging circuit, which is formed by the current mirror CM_3 and the capacitor C_{AV} that connected in parallel to the current mirror input. Then the current I_{AV} can be written as

$$I_{AV} = \frac{1}{8I_b} \cdot \frac{1}{T}\int_0^T I_{in}^2 dt \tag{6}$$

where $T = \frac{C_{AV}}{gm_{10}}$ is the time constant of the filter and gm_{10} is the transconductance of the transistor M_{10}. Noting that the capacitor C_{AV} is a grounded capacitor. We design the current mirror CM_5 such that: the drain current of the transistor M_{16} sources to compensated the bias current $2I_b$, and the bias current passes through the class AB amplifier circuit $I_b = I_{AV}$. The drain current of the transistor M_{14}, $I_{D9} = I_{AV}$ is the input current of the negative current mirror CM_2. If we set the dimension of the transistor M_7 equal to $\sqrt{8}$ times of the dimension of the transistor M_8, then the output current I_{RMS} can be expressed as

$$I_{RMS} = \sqrt{8}I_{AV} = \sqrt{8}I_b \tag{7}$$

From the eqn. (6), by setting $I_b = I_{AV}$ and solving for I_{AV}, we can write

$$I_{AV} = \frac{1}{\sqrt{8}}\sqrt{\frac{1}{T}\int_0^T I_{in}^2 dt} \tag{8}$$

And from the eqns. (7) and (8) and solving for I_{RMS}, we get

$$I_{RMS} = \sqrt{\frac{1}{T}\int I_{in}^2 dt} \tag{9}$$

We can see from the eqn. (9) that the output current is in the form of the root-mean-square value as required. For the voltage input mode, V_{in} is applied at port A. Similar to the calculation of I_{RMS}, from the eqns. (4) and (9) with R_o= R, the output voltage V_{RMS} can be expressed as

$$V_{RMS} = I_{RMS} \times R_o = \sqrt{\frac{1}{T}\int_0^T V_{in}^2 dt} \tag{10}$$

However, in order that the proposed rms-to-dc converter give a good performance in the required frequency range, the value of the capacitor C_{AV} must be chosen such that

$$C_{AV} >> \frac{gm_{10(max)}}{4\pi f_{(min)}} \tag{11}$$

where $f(min)$ is the lower end of the frequency range of interest, and

$$gm_{10(max)} = \sqrt{2K_pWI_{D10}/L}\,AV^{-1} \tag{12}$$

For example, when $K_p = 4.4927 \times 10^{-4}$ AV^{-2}, W=50 μm, L = 5 μm and $I_{D10} = I_M$, where I_M is the peak amplitude of the input signal. Then $gm_{10(max)}$ can be given by $gm_{10(max)} = 29.98 \times 10^{-3}\sqrt{I_M}\,AV^{-1}$. In this case C_{AV} must be chosen such that

$$C_{AV} >> \frac{2.39 \times 10^{-3}\sqrt{I_M}}{f_{(min)}} \tag{13}$$

If a sinusoidal input signal with I_M = 1 mA and $f(MIN)$ = 100 Hz, the averaging capacitance must be chosen such that $C_{AV} >> 0.75$ μF. Therefore, C_{AV} = 1 μF must be employed.

It should be noted that, although, the output of the circuit of the figure 2 is in the form of the root-mean-square values, V_{RMS} or I_{RMS}. The circuit can be easily modified to provide the output in the form of the average values V_{avg} or I_{avg}, where

$$V_{avg} = \frac{1}{T}\int_0^T |V(t)|\, dt \tag{14}$$

$$I_{avg} = \frac{1}{T}\int_0^T |I(t)|\, dt \tag{15}$$

From the relation between V_{RMS} and V_{avg} and between I_{RMS} and I_{avg}, we get

and $V_{avg} = 0.9V_{RMS}$ (16)

$$I_{avg} = 0.9I_{RMS} \quad (17)$$

In this case, we will set the dimension of the transistor M_7 equal to $0.9\sqrt{8}$ times of the dimension of the transistor M_8.

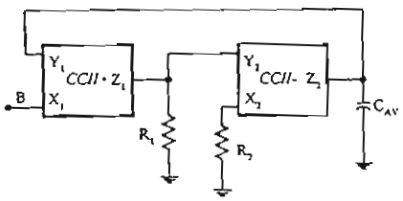

Fig.3 Block diagram of C-multiplier circuit

2.3 A Current-Controlled Capacitance Multiplier

From the eqn. (13), it is indicated that, for an I_{RMS} with low ripple, a large capacitance is required. This value of capacitance is not suitable for monolithic integration. To reduce the size of the capacitor used, a current-controlled C-multiplier as shown in the Fig. 3 is presented, where the current conveyors (CCIIs) that reported in reference 7 have been used. The current-controlled C-multiplier, which is composed of two CCII (CCII+ and CCII-), is similar to the voltage-controlled C-multiplier proposed in the reference 8. But, in this case, the input signal is a current signal that injected into port X_1 and the capacitor C_{AV} is connected at the port Y_1. If we let $n = R_2/R_1$, the value of the capacitance that appeared at the port B to ground or C_{EQV} will be equaled to

$$C_{EQV} = nC_{AV} = (R_2/R_1)C_{AV} \quad (18)$$

Table.1 Transistors dimension

Transistors	W(μm)	L(μm)
M1,M2,M3,M4,	200	5
M5,M6,M8,M9,M10,M11, M12. M13,M14,M15,M17	100	5
M7	283	5
M16	200	5

Table.2 Summary of the characteristics of the circuit of Fig. 2

Parameters	Simulated results
Supply voltage (rated)	±3V to ±15V
Input current range(max)	1mA
Gain error	2%Max. nonlinearity, 10μA to 1mA input
Peak amplitude value	-3dB bandwidth
I_{IN} = 10 μA (1.0% of $I_{IN(MAX)}$)	1 MHz
I_{IN} = 100 μA (10% of $I_{IN(MAX)}$)	5 MHz
I_{IN} = 200 μA (20% of $I_{IN(MAX)}$)	10 MHz
I_{IN} = 500 μA (50% of $I_{IN(MAX)}$)	20 MHz
I_{IN} = 900 μA (90% of $I_{IN(MAX)}$)	40 MHz
I_{IN} = 1000 μA(100% of $I_{IN(MAX)}$)	45 MHz

Table.3 Equivalent capacitance of C-multiplier circuit.

n	Expected Capacitance (F)	Equivalent Capacitance (F)
1	1nF	0.983nF
10	10nF	9.731nF
100	100nF	96.73nF
1000	1uF	0.955uF

3. SIMULATION RESULTS

The characteristics of the converter were studied through the simulation results using SPICE and cadence simulation results. The transistor dimensions of the circuit in Fig.2 are in micron and are listed in the Table 1. The dimensions of all the transistor of the circuit in Fig.3 are W=50μm and L=5μm. The simulation was carried out using the transistor parameter of the 0.5 microns SCN05H Technology MOSIS process. The simulation characteristics were listed in the Table 2. Note that the circuit exhibits the bandwidth of 45 MHz at I_{IN} = 1 mA_{rms}. The maximum conversion nonlinearity, for the input signal in the range from 10 μA_{rms} to 1 mA_{rms}, of about 2 % was achieved. The simulation for the frequency responses for the sine wave input current signal with the amplitude of 1, 10, 20, 50, 90 and 100 percents of the full scale current ($I_{IN(MAX)}$=1mA) were also carried out. The results show the bandwidth of about 1 MHz, 5 MHz 10 MHz, 20 MHz, 40 MHz and 45 MHz, respectively. Fig.4 shows the plots of the percent ripple of I_{RMS} versus frequency of the circuit in Fig.2. The percent ripple of I_{RMS} versus frequency, simulated from the SPICE-compatible text file that extracted from the Layout in the Fig.5 by using the Layout extractor of the Cadence program, is also plotted in the Fig.4. The simulation results demonstrate that the percent ripple is small for high value of C_{AV}. To reduce the size of capacitor suitable for monolithic integration the C-multiplier circuit is incorporated in the true RMS-to-DC converter. The Analog Artist Design Environment is used to simulation the C-multiplier characteristic. Table.3 shows the C_{AV} of the C-multiplier circuit of Fig.3

Fig.6 shows the I_{RMS} of the triangular input signal from the circuit in Fig.2, when input signal is a triangular waveform with the amplitude of 1mA, f = 1kHz. The result shows the DC signal with the amplitude is 0.577V. The circuit is also able to convert the square-wave AC signal into the DC signal in the RMS value.

However, the simulation performance of the circuit using SPICE is much depending on the chosen transistor parameters. Therefore, in order to test for the

circuit workability, the performance of the true RMS-to-DC converter circuit and the C-multiplier circuit will be further studied through the layout by using Cadence's IC Circuit Design Systems, which is an integrated circuit design software running on Workstation. Using the Virtuoso Layout Editor of Cadence's system drew the layout. Fig. 5 shows the layout of the RMS-to-DC converter. The Diva interactive Electrical Rules Checker program, which is the layout extractor in the Cadence program, was then employed to translate the layout drawing into the SPICE-compatible text file for the simulation.

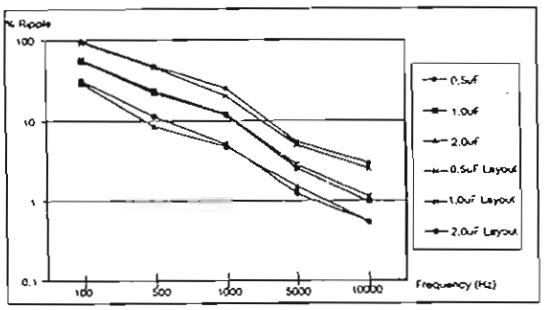

Fig.4 Plots of percent ripple versus frequency for difference value of C_{AV}

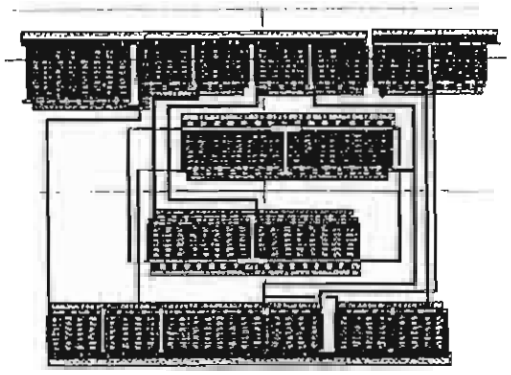

Fig.5 Layout of the true RMS-to-DC converter

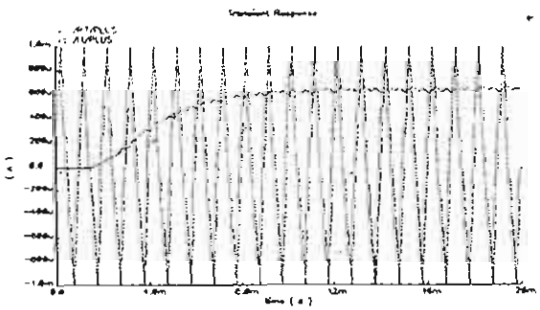

Fig.6 The output current of the true RMS-to-DC converter.

4. CONCLUSIONS

The true RMS-to-DC converter that is more suitable for monolithic integration is proposed. In order to reduce the value of the capacitor, the capacitance multiplier circuit has been used. The realization scheme is suitable for implemented in standard CMOS process. The characteristics of the proposed are confirm from SPICE and Cadence simulation results.

ACKNOWLEDGMENT

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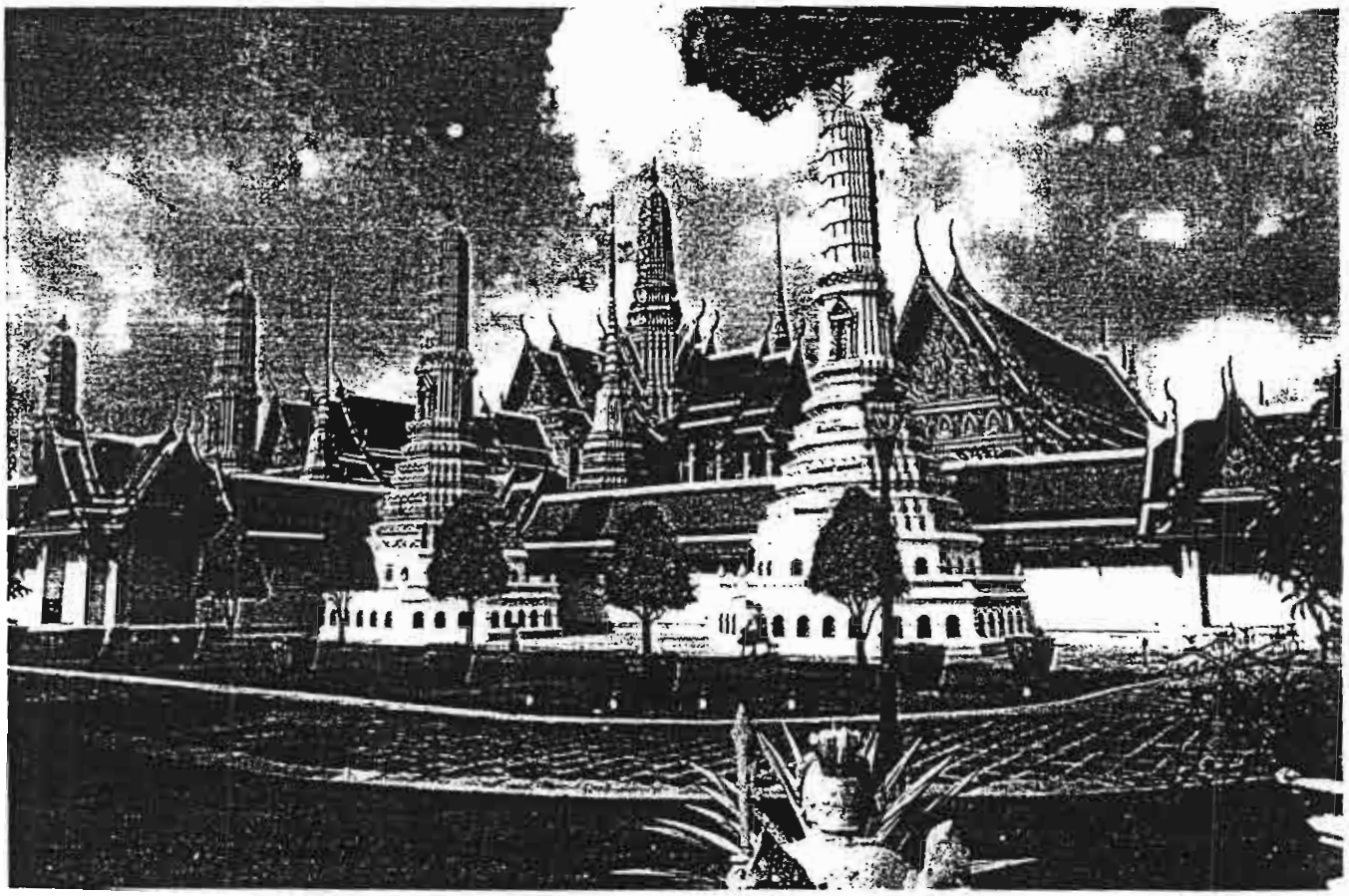

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A 100-MHz 1.5-mW Quarter-Square Four-Quadrant Analog Multiplier

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Abstract

In this paper, a novel CMOS circuit configuration for the realization of a four-quadrant analog multiplier is presented. It is based on a source-coupled pair which is modified to work as a voltage squaring and a sum/difference circuit. The proposed multiplier has been simulated with HSPICE, where $-3dB$ bandwidth of $100MHz$ is achieved. The power consumption is about $1.5mW$, from a $\pm 2.5V$ supply, and the total harmonic distortion is less than 0.8%, with a $1V$ peak-to-peak $5MHz$ input signal.

Key word: Four-quadrant analog multiplier. Squarer, MOS analog integrated circuits

1. Introduction

An analog multiplier is an importance basic building block for the design of analog nonlinear function circuits, for examples, frequency translation, waveform generation, linear modulation, neural networks, and other signal processing circuits. Usually, the variable transconductance technique which operates on Gilbert's translinear circuit is widely used for the design of multiplier circuits in Bipolar and CMOS technologies. The other approaches in CMOS technology are that based on square-law characteristics of MOS transistor which are biased in saturation region [1], [2], [5], [6], and that on the current-voltage characteristics of MOS transistor in the nonsaturation region [4]. While the common source differential-input squaring circuit with resistance load is always used for the quarter-square technique [2]. The multiplier proposed in this paper also uses the square-law of the MOS transistor based upon the quarter-square algebraic identity. But, however, the proposed circuit does not require resistors to obtain the output signal in voltage.

2. Circuit description

2.1 MOS Differential Squaring Circuit

Fig. 1 shows the voltage squaring circuits which are made up of a differential-input source-coupled pair. Assuming that all NMOS devices in Fig. 1 (a) are biased in the saturation region with individual wells connected to their sources to eliminate the body effect [3]. If the differential-input voltage V_d, with the same common-mode dc voltage V_C is applied, the drain currents of MOS transistors can be expressed as

$$I_{d1} = K_1(V_C + \frac{V_d}{2} - V_{o1} - V_T)^2 \qquad (1)$$

$$I_{d2} = K_2(V_C - \frac{V_d}{2} - V_{o1} - V_T)^2 \qquad (2)$$

$$I_{d3} = K_3(V_{G3} - V_{SS} - V_T)^2 \qquad (3)$$

$$I_{d1} + I_{d2} = I_{d3} \qquad (4)$$

where $K_i = \mu_n C_{ox} W_i / 2L_i$ is transconductance parameter, μ_n is the effective surface mobility, C_{ox} is the gate capacitance per unit area , and V_T is the threshold voltage of the transistor, respectively.

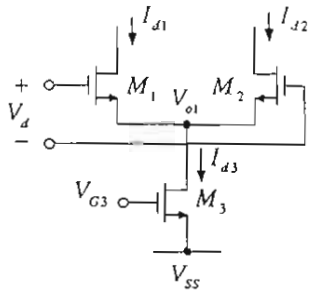

Fig.1 (a). Source-coupled pair circuit

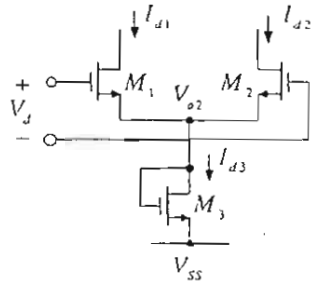

Fig. 1 (b). Voltage squaring circuit

Let M_1 and M_2 are identical, and the aspect ratio of M_3 be twice that of M_1. Substituting eqns. (1), (2), and (3) into eqn.(4), the output voltage V_{o1} of the squaring circuit in Fig. 1(a) can be given by

$$V_{o1} = V_C - V_T - \sqrt{(V_{G3} - V_{SS} - V_T)^2 - \left(\frac{V_d}{2}\right)^2} \quad (5)$$

where $V_{G3} - V_{SS}$ is the gate-to-source voltage of M_3. On the other hand V_{o1} can be rewritten as

$$V_{o1} = V_C - V_T - (V_{GS3} - V_T)\sqrt{1 - \left(\frac{V_d/2}{V_{GS3} - V_T}\right)^2} \quad (6)$$

If the approximation of the form $\sqrt{1+x} \cong 1 + \frac{1}{2}x$ for $|x| << 1$ is employed, then eqn.(6) can be approximately written as

$$V_{o1} = V_C - V_{GS3} + \frac{V_d^2}{8(V_{GS3} - V_T)} \quad (7)$$

where, for good approximation, the value of the differential-input voltage V_d should be restricted to $|V_d / 2(V_{GS3} - V_T)| << 1$. It should be noted from eqn. (7) that the output voltage V_{o1} includes a component that is proportional to the square of the differential-input voltage V_d. Therefore, the source-coupled pair circuit as shown in Fig. 1(a) can be used as a squaring circuit for quarter-square multiplier.

Fig. 1(b) shows the voltage squaring circuit which is modified from the differential-input source-coupled pair. Let M_1 and M_2 are identical, the aspect ratio of M_3 be twice that of M_1 and M_2. Assuming that all transistors operate in their saturation region, the drain currents of $M_1 - M_3$ can be written as

$$I_{d1} = K_1(V_C + \frac{V_d}{2} - V_{o2} - V_T)^2 \quad (8)$$

$$I_{d2} = K_2(V_C - \frac{V_d}{2} - V_{o2} - V_T)^2 \quad (9)$$

$$I_{d3} = K_3(V_{o2} - V_{SS} - V_T)^2 \quad (10)$$

where, in this case, the output voltage V_{o2} becomes

$$V_{o2} = \frac{(V_C - V_T)^2 - (V_{SS} + V_T)^2}{2(V_C - V_{SS} - 2V_T)} + \frac{V_d^2}{8(V_C - V_{SS} - 2V_T)} \quad (11)$$

The output voltage V_{o2} is related to the square of the differential-input voltage V_d. The eqns. (8)-(11) are valid if $(V_C - V_{SS} - V_d/2) > 2V_T$, where all devices are biased in the saturation mode. However, it should be noted that the linearity of the circuit in Fig. 1(b) is better than Fig.1 (a) and more suitable to design a squaring circuit.

2.2 Sum/difference circuit

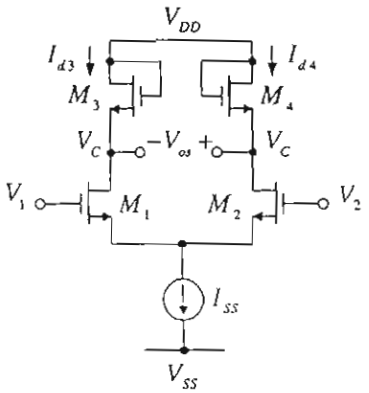

Fig. 2. Sum/difference circuit

Fig. 2 shows a sum/difference circuit based on source-coupled pair $M_1 - M_2$ with $M_3 - M_4$ act as an active load. Assuming that the transistors $M_1 - M_4$ are identical with transconductance parameter K and are biased in saturation region, the differential voltage $(V_1 - V_2)$ can be expressed as

$$V_1 - V_2 = V_{gs1} - V_{gs2} \quad (12)$$

where V_{gs1} and V_{gs2} are the voltage drop from gate-to-source of transistors M_1 and M_2, respectively, which can be given by

$$V_{gs1} = \sqrt{\frac{I_{d1}}{K}} + V_T$$

and

$$V_{gs2} = \sqrt{\frac{I_{d2}}{K}} + V_T \quad (13)$$

By substituting eqn.(13) into eqn.(12), we get

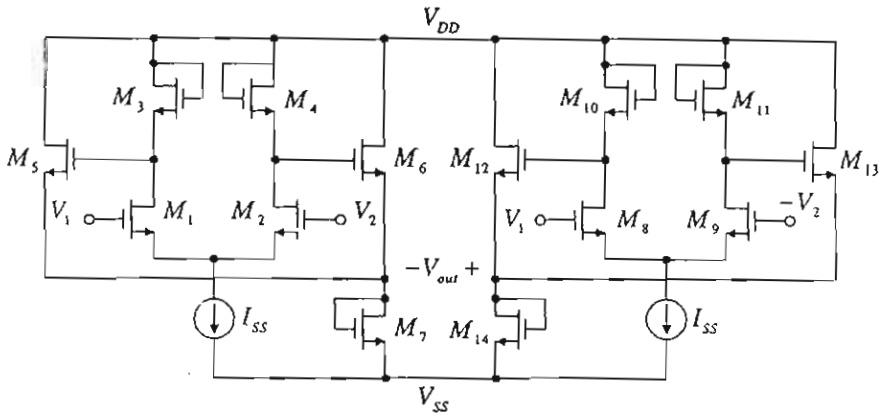

Fig. 3. The proposed four-quadrant analog multiplier

$$\sqrt{K}(V_1 - V_2) = \sqrt{I_{d1}} - \sqrt{I_{d2}} \tag{14}$$

And the differential-output voltage V_{os} is given by

$$V_{os} = V_{gs3} - V_{gs4} \tag{15}$$

or

$$\sqrt{K}V_{os} = \sqrt{I_{d3}} - \sqrt{I_{d4}} \tag{16}$$

From the circuit in the Fig. 2, the drain current of transistor M_1 is equal to the drain current of M_3 and the drain current of M_2 is the drain current of transistor M_4. Therefore, from eqn. (14) and eqn. (16), the differential-output voltage V_{os} can be written as

$$V_{os} = V_1 - V_2 \tag{17}$$

where the common-mode dc voltage V_C at the drain of transistors M_1 and M_2 are written by

$$V_C = V_{DD} - \left(\sqrt{\frac{I_{SS}}{2K}} + V_T \right) \tag{18}$$

From eqn.(17), we can see that the output voltage V_{os} is a linear function of the differential-input voltage $(V_1 - V_2)$. This means that the circuit is function as a unity-gain linear amplifier, where the operation range of the circuit is limited by $|V_1 - V_2| \le \sqrt{I_{SS}/K}$.

2.3 Quarter-Square Multiplier

By combining the source-coupled pair circuit or voltage squaring circuit with the sum/difference circuit which are shown in Fig. 1 (a) - (b) and Fig. 2, respectively, the complete four-quadrant analog multiplier is shown in Fig. 3. For good linearity, the voltage squaring circuit of the Fig. 1(b) is selected. The multiplication is achieved by subtracting the square of the difference from the square of the sum of two inputs, where the output voltage V_{out} is obtained as

$$V_{out} = \frac{(V_1 + V_2)^2 - (V_1 - V_2)^2}{8(V_C - V_{SS} - 2V_T)} = \frac{V_1 V_2}{2(V_C - V_{SS} - 2V_T)} \tag{19}$$

where V_C is the common-mode dc voltage of voltage squaring circuit which is shown in eqn.(18).

3. Simulation Results

The proposed multiplier circuit of Fig. 3 has been simulated by HSPICE using the model parameters of HP 0.5μ level 49 CMOS process. The aspect ratios of transistors $M_1 - M_6$ and $M_8 - M_{13}$ are 5/5, M_7 and M_{14} are 10/5, respectively. The power supply voltage is $\pm 2.5V$ and the bias current I_{SS} is $100\mu A$.

The dc characteristic curves of the proposed multiplier are shown in Fig. 4, where it should be noted that the linear input voltage range is almost the same as the range of the sum/difference circuit.

Fig. 5 shows the application of the multiplier to work as a modulator. V_1 and V_2 are sinusoidal signals with peak amplitude of $0.5V$, and the frequencies are $1MHz$ and $15MHz$.

The total harmonic distortion against input voltages is shown in Fig. 6, where the input voltage V_2 is dc voltage and V_1 is the sinusoidal input voltage with the frequency of $5MHz$. The maximum THD at both the input voltages of $0.5V$ is about 0.73%, and the power consumption is about $1.5mW$.

To measure the frequency characteristic of the multiplier, a $0.5V$ dc voltage is applied to V_2 while V_1

is the variable frequency sinusoidal input voltage with peak amplitude of $0.5V$. From the simulation, the $-3dB$ bandwidth up to $115MHz$ is achieved.

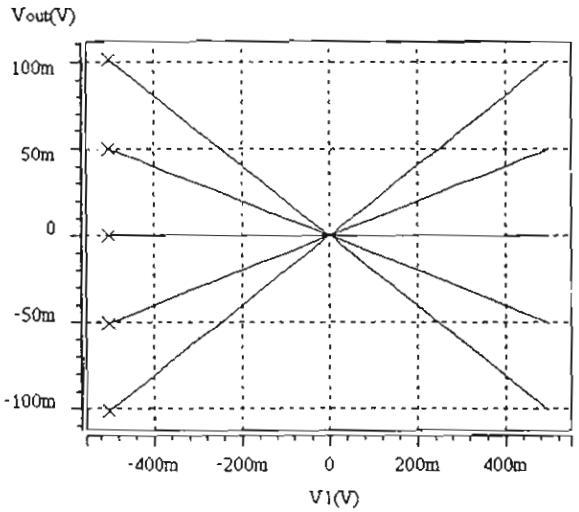

Fig. 4. The transfer characteristic curves of the multiplier

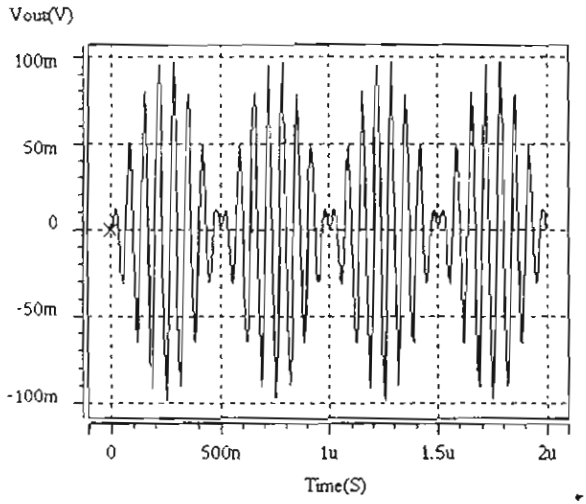

Fig. 5. Amplitude modulator with two sinusoidal inputs

4.Conclusion

A new NMOS four-quadrant analog multiplier base on the differential-input source-coupled pair has been presented. To obtain the differential-output voltage, the proposed circuit is performed by using two squaring circuits. There performances have been demonstrated by using HSPICE simulations.

Acknowledgment

The authors would like to thank Electronic Engineering Department, Faculty of Engineering, Mahanakorn University of Technology for support in the realization of the circuit simulation. This work is partly funded by the Thailand Research Fund (TRF) under the Senior Research Program, grant number RTA/04/2543. The support provided by the Japan International Cooperation Agency (JICA) is also acknowledged.

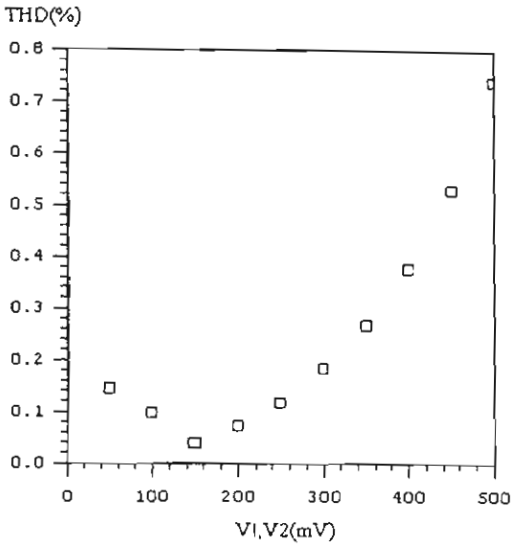

Fig. 6. Simulated THD of V_{out}

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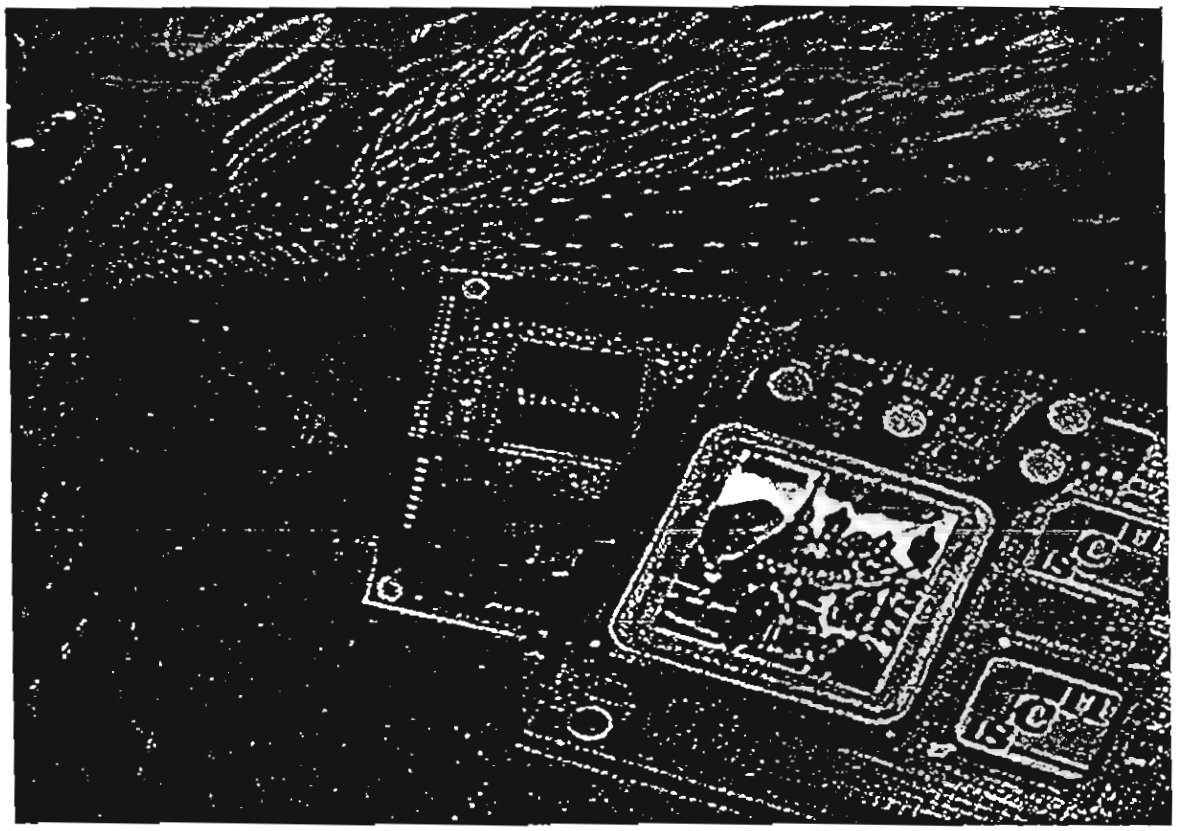

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REALIZATION OF CURRENT-MODE FTFN-BASED LOWPASS FILTER AND ITS INVERSE FILTER FROM THE OPTIMAL SALLEN AND KEY LOWPASS FILTER (SARAGA DESIGN) USING RC:CR DUAL TRANSFOMATION TO PRESERVE THE SENSITIVITIES OF THE ORIGINAL CIRCUIT

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ABSTRACT

This paper shows that the current-mode FTFN-based lowpass filter and its inverse filter obtained from the optimal voltage-mode op-amp-based Sallen and Key lowpass filter (Saraga Design) using RC:CR dual transformation preserve the optimal passive sensitivities and have better active sensitivities.

1. INTRODUCTION

Analog circuits are always requested to work at high frequencies where digital signal processing faces difficulties with implementation. In particular recent increasing needs of wireless communications, such as W-CDMA, Bluetooth, ITS, etc., require analog circuits which process signals in a giga-hertz frequency range [1]. Nowadays, Semiconductor Industry Association needs low power consumption chip and analog and digital circuits are implemented on the same chip using the same dc power supply that is less than 1.5 V and will decrease to 0.5 V in 2011 [1]. In order to correspond to the severe demands for high frequency and low power-supply voltage operation on analog circuits, current is found to be a key word in the 1990's. So, current signal processing is one of the most promising solutions. Circuits with current input and output signals are often called a 'current-mode' circuit. Reduction in power-supply voltage restricts voltage-signal swings extremely. To avoid this problem, current-mode circuits are used because current-signal swings are not restricted by power supply voltages.

Because passive and active RC circuits are already excellent tabulated, if we can use some transformation to obtain their current-mode circuit counterparts and use proper active devices. They may have better performances. In this paper, we use the optimal voltage-mode op-amp-based Sallen and Key lowpass filter (Saraga Design) as the prototype because it is still popular to use in many fields such as wireless communications [2]. We, also, use RC:CR dual transformation and nullor network analysis as design tools to obtain its current-mode circuit counterpart both lowpass and inverse lowpass filters [3-8]. We use four-terminal floating nullor (FTFN) as an active device because of its versatility [3], [6-9].

2. REALIZATION

The prototype of a voltage-mode op-amp-based Sallen and Key lowpass filter [10] is shown in Figure 1.

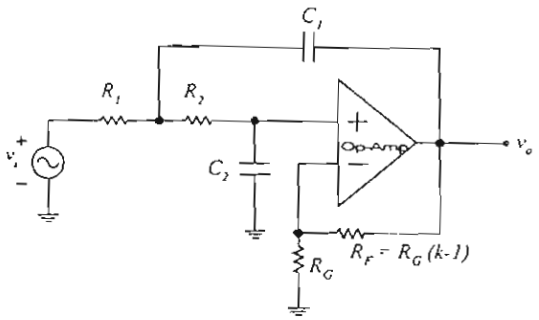

Fig. 1 A voltage-mode op-amp-based Sallen and Key lowpass filter

The voltage transfer function of the circuit in Figure 1 is as follows:

$$\frac{V_o}{V_i} = \frac{k/R_1R_2C_1C_2}{s^2 + s\left[\frac{1}{R_1C_1} + \frac{1}{R_2C_1} + \frac{(1-k)}{R_2C_2}\right] + \frac{1}{R_1R_2C_1C_2}} \quad (1)$$

where

$$k = 1 + \frac{R_F}{R_G} = \text{noninverting voltage gain} \quad (2)$$

$$K = k/R_1R_2C_1C_2 = \text{voltage gain constant} \quad (3)$$

$$\omega_p = \sqrt{1/R_1R_2C_1C_2} = \text{pole angular frequency} \quad (4)$$

$$Q_p = \frac{\sqrt{1/R_1R_2C_1C_2}}{\frac{1}{R_1C_1} + \frac{1}{R_2C_1} + \frac{1-k}{R_2C_2}} = \text{pole } Q \quad (5)$$

Saraga Design equations are as follows:

$$k = \frac{4}{3}, C_1 = \sqrt{3}Q_p, C_2 = 1,$$
$$R_1 = \frac{1}{Q_p \omega_p}, R_2 = \frac{1}{\sqrt{3}\omega_p}, \frac{R_2}{R_1} = \frac{Q_p}{\sqrt{3}} \quad (6)$$

Follow the proposed procedure in Reference [8], the obtained current-mode FTFN-based Sallen and Key lowpass filter is shown in Figure 2 and its inverse lowpass filter is shown in Figure 3, respectively.

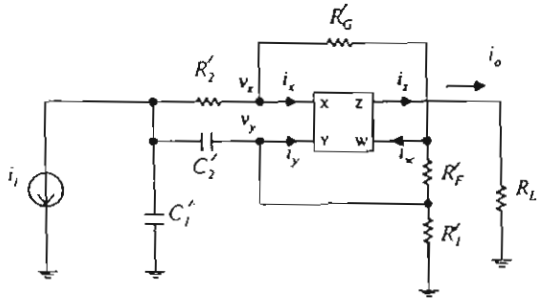

Fig.2 The current-mode FTFN-based Sallen and Key lowpass filter

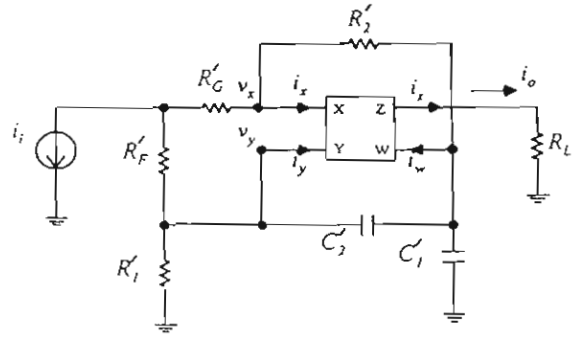

Fig.3 The current-mode FTFN-based Sallen and Key inverse lowpass filter

For ideal FTFN, the current transfer function of the circuit in Figure 2 is as follows:

$$\frac{I_o}{I_i} = \frac{k'/R'_1R'_2C'_1C'_2}{s^2 + s\left[\frac{1}{R'_1C'_1} + \frac{1}{R'_1C'_2} + \frac{(1-k')}{R'_2C'_2}\right] + \frac{1}{R'_1R'_2C'_1C'_2}} \quad (7)$$

where

$$k' = 1 + \frac{R'_G}{R'_F} \text{ – noninverting current gain} \quad (8)$$

$$K' = k'/R'_1R'_2C'_1C'_2 = \text{current gain constant} \quad (9)$$

$$\omega'_p = \sqrt{1/R'_1R'_2C'_1C'_2} \quad (10)$$

$$Q'_p = \frac{\sqrt{1/R'_1R'_2C'_1C'_2}}{\frac{1}{R'_1C'_1} + \frac{1}{R'_1C'_2} + \frac{1-k'}{R'_2C'_2}} \quad (11)$$

Equation *(7)* is equal to equation *(1)* if one set of the following added important conditions is satisfied.

The first set of added important conditions are:

$$R'_1 = C_1, C'_1 = R_1, R'_2 = C_2, C'_2 = R_2,$$
$$R'_F = R_G, R'_G = R_F \quad (12)$$

The second set of added important conditions are:

$$R'_1 = R_1, C'_1 = C_1, R'_2 = R_2, C'_2 = C_2,$$
$$R'_F = R_G, R'_G = R_F, R_1C_2 = R_2C_1 \quad (13)$$

But for Saraga Design, the equation *(13)* is impossible. So, equation *(12)* is used in this case. We get the following relations:

$$k' = k, K' = K, \omega'_p = \omega_p, Q'_p = Q_p \quad (14)$$

So that,

$$\frac{I_o}{I_i} = \frac{V_o}{V_i} \quad (15)$$

For real FTFN, we consider nonlinearities of voltage and current too. Let

$$\alpha = 1 - \varepsilon, |\varepsilon| << 1 \quad (16)$$

and

$$\beta = 1 - \delta, |\delta| << 1 \quad (17)$$

where

α = voltage tracking coefficient
ε = voltage tracking error
β = current tracking coefficient
δ = current tracking error

So that,

$$v_x = \alpha v_y \quad (18)$$

and

$$i_z = \beta i_w \quad (19)$$

The real current transfer function of the circuit in Figure 2 will be:

$$\frac{I_o}{I_i} = \frac{\beta\left[k' - s\left\{(\alpha-1)C'_2R'_1\left(\frac{1}{R'_F} + \frac{R'_2}{R'_F} + k'\right)\right\}\right]}{\left[s^2\left(R'_1R'_2C'_1C'_2\right) + s\left\{\begin{matrix}R'_2C'_2 + R'_2C'_1 + \\ R'_1C'_1(1-\alpha k')\end{matrix}\right\} + 1\right] + \left[\begin{matrix}s^3\left(R'^2_1C'_1C'^2_2\right) + \\ s^2\left\{\begin{matrix}C'_1C'_2\frac{R'^2_1}{R'_F} + C'_1C'_2R'_1 + \\ C'^2_2R'_1 - C'_1C'_2R'^2_1\end{matrix}\right\} - \\ (\alpha-1)\left\{\begin{matrix}C'_1\frac{R'^2_1}{R'_F} + C'_1\frac{R'_1R'_2}{R'_F} + \\ C'_2\frac{R'_1R'_2}{R'_F} + (1+k')(C'_2R'_1)\end{matrix}\right\} + \\ R'_1 \\ R'_F\end{matrix}\right]} \quad (20)$$

If equations *(16)* and *(17)* hold, then equation *(20)* reduces to

$$\frac{I_o}{I_i} = \frac{(\beta k')/R_1'R_2'C_1'C_2'}{s^2 + s\left[\frac{1}{R_1'C_1'} + \frac{1}{R_1'C_2'} + \frac{(1-k')}{R_2'C_2'}\right] + \frac{1}{R_1'R_2'C_1'C_2'}} \quad (21)$$

For Saraga Design, equations *(12)* and *(14)* hold, the equation *(21)* changes to

$$\frac{I_o}{I_i} = \frac{\beta k/R_1R_2C_1C_2}{s^2 + s\left[\frac{1}{R_1C_1} + \frac{1}{R_2C_1} + \frac{(1-k)}{R_2C_2}\right] + \frac{1}{R_1R_2C_1C_2}} \quad (22)$$

where

k, K, ω_p and Q_p are the same as in equations *(2)* to *(5)*.

The same analysis is done for the circuit in Figure 3. For Saraga Design and ideal FTFN, the inverse current transfer function is the inverse of the right-hand side of equation *(1)*. And the same analysis is done for real FTFN, we get the inverse current transfer function as the inverse of the right-hand side of equation *(22)*.

3. SENSITIVITY ANALYSIS

Since equation *(22)* is equal to equation *(1)* multiplied by β, then all biquad parameters are the same. Thus, all the passive sensitivities are preserved.

The active sensitivities are as follows:

$$S_\alpha^{\beta K} = S_\alpha^{\omega_p} = S_\alpha^{Q_p} = S_\beta^{\omega_p} = S_\beta^{Q_p} = 0 \quad (23)$$

and

$$S_\beta^{\beta K} = 1 \quad \text{(for I-mode, LP filter)} \quad (24)$$

and

$$S_\beta^{\beta K} = -1 \quad \text{(for I-mode, inverse LP filter)} \quad (25)$$

All active sensitivities are very low. Hence, the current-mode circuit is better than its voltage-mode counterpart.

4. CONCLUSIONS

This paper shows that using RC:CR dual transformation with the optimal voltage-mode op-amp-based Sallen and Key lowpass filter (Saraga Design) to obtain the current-mode FTFN-based lowpass filter and its inverse filter can preserve the optimal passive sensitivities and have better active sensitivities.

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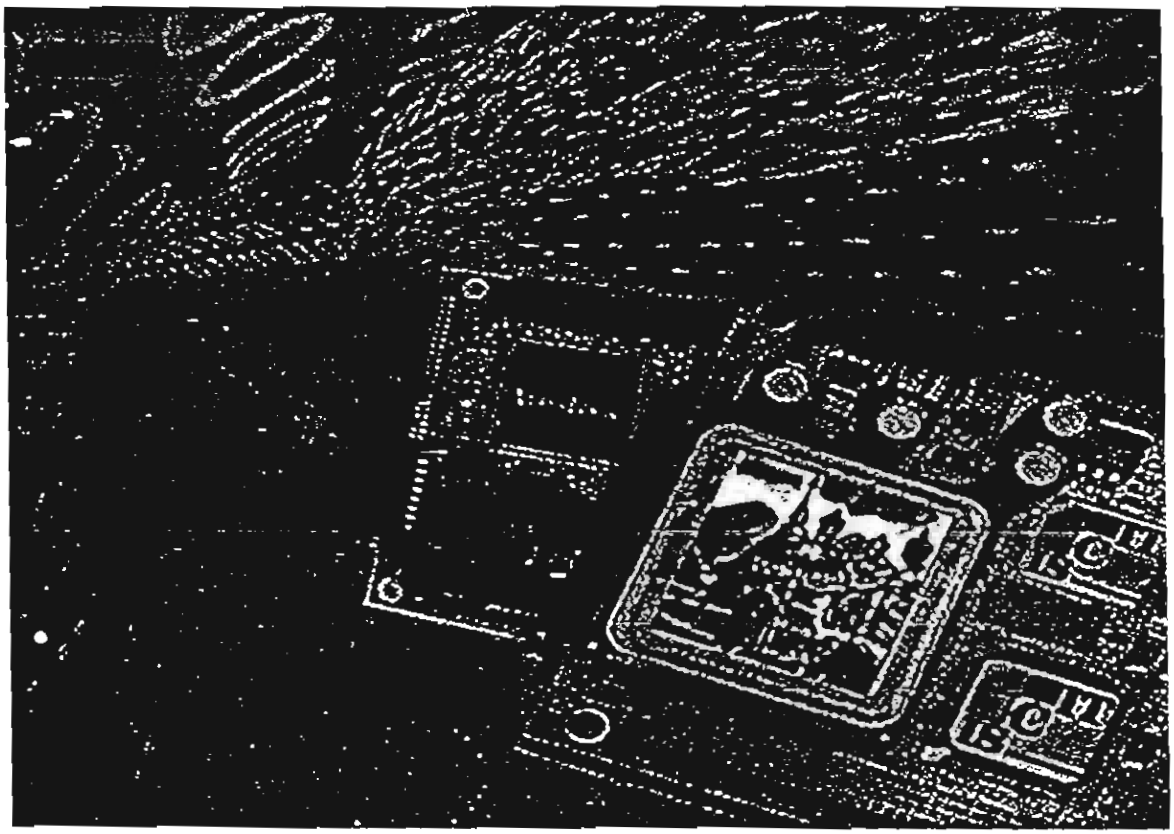

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LOW-VOLTAGE CURRENT MULTIPLIER USING LINEAR MOS RESISTOR

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ABSTRACT

In this paper, a four-quadrant current multiplier circuit configuration based on the linear MOS resistor which the output current is independent from the power supply voltage is presented. The proposed multiplier has been simulated with HSPICE, where $-3\,dB$ bandwidth of $10\,MHz$ is achieved. The power consumption is about $280\mu W$, from a $\pm 1.5V$ supply. The total harmonic distortion is less than 1.2%, with a $20\mu A$ peak-to-peak $1MHz$ input signal.

1. INTRODUCTION

An analog multiplier provides useful importance basic building block to design many analog signal processing systems, e.g., correlators, adaptive filter, and curve-fitting generators. It is also applied to amplitude modulation, frequency translation, automatic gain control, squaring, square rooting and neural networks. Many four-quadrant analog multiplier design techniques have been reported in Bipolar and CMOS technologies. They are, for examples, the variable transconductance technique [1], the voltage-controlled transconductance technique [2], the technique based on linear transconductor [3], the bias feedback technique [4], and the use of square-law characteristic of MOS transistor which are biased in saturation or nonsaturation region [5], [6], [7]. However most of those reported multiplier circuits require resistors in order to obtain the output signal. The multiplier proposed in this paper also uses the square-law characteristic of MOS transistor that is based on linear MOS resistor, but achieves the single-ended current/voltage output signal.

2. CIRCUIT DESCRIPTION

2.1 Linear MOS resistor

Fig. 1 shows the linear MOS resistor [9]. Assuming that transistors $M_1 - M_2$ are matched pair transistors and biased in saturation region with individual wells connected to their sources.

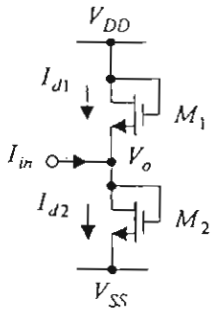

Fig. 1. Linear MOS resistor.

Applying the input current I_{in}, we can express the following equations

$$V_{DD} - V_{SS} = V_{gs1} + V_{gs2} \qquad (1)$$

where V_{gs1} and V_{gs2} are the voltage drop from gate-to-source of transistors M_1 and M_2 respectively, and can be given by

$$V_{gs1} = \sqrt{\frac{I_{d1}}{K_1}} + V_{th}$$

and

$$V_{gs2} = \sqrt{\frac{I_{d2}}{K_2}} + V_{th} \qquad (2)$$

where $K_i = \mu_n C_{ox} W_i / 2L_i$ is transconductance parameter of transistor M_i, μ_n is the effective surface mobility, C_{ox} is the gate capacitance per unit area, and V_{th} is the threshold voltage of the transistor. Substituting eqn.(2) into eqn.(1), we can write

$$\sqrt{K_1}\left(V_{DD} - V_{SS} - 2V_{th}\right) = \sqrt{I_{d1}} + \sqrt{I_{d2}} \qquad (3)$$

From the circuit in Fig. 1, we find that

$$I_{d2} = I_{d1} + I_{in} \qquad (4)$$

By substituting eqn.(4) into eqn.(3), we can express the drain currents I_{d1} , I_{d2} and V_o in the term of the input current I_{in} as

$$I_{d1} = \frac{1}{4}K_1(V_{DD} - V_{SS} - 2V_{th})^2 - \frac{I_{in}}{2} + \frac{I_{in}^2}{4K_1(V_{DD} - V_{SS} - 2V_{th})^2} \quad (5)$$

$$I_{d2} = \frac{1}{4}K_2(V_{DD} - V_{SS} - 2V_{th})^2 + \frac{I_{in}}{2} + \frac{I_{in}^2}{4K_2(V_{DD} - V_{SS} - 2V_{th})^2} \quad (6)$$

and

$$V_o = \frac{I_{in}}{4K_1V_x} \quad (7)$$

where $V_x = (V_{DD} - V_{th}) = -(V_{SS} + V_{th})$. The eqns. (1)-(7) are valid when the transistors stay in their saturation mode which is true if $|V_o| \le V_x$.

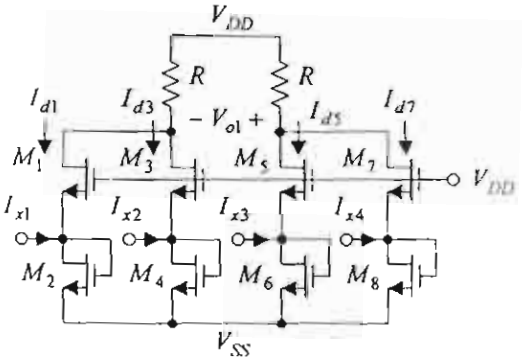

Fig. 2. Proposed current multiplier.

2.2 Four-Quadrant Current Multiplier

Fig. 2 shows the four-quadrant current multiplier which is modified from the linear MOS resistor of the Fig. 1. Let $M_1 - M_8$ are identical, with transconductance parameter K_1, and are biased in saturation region. I_{x1} to I_{x4} are the input currents of the multiplier. We obtain the output voltage V_{o1} as

$$V_{o1} = R[(I_{d1} + I_{d3}) - (I_{d5} + I_{d7})] \quad (8)$$

Let the input currents $I_{x1} = I_1 + I_2$, $I_{x2} = 0$, $I_{x3} = I_1$, and $I_{x4} = I_2$. From eqns.(5)-(8), this output voltage becomes

$$V_{o1} = \frac{R}{2K_1(V_{DD} - V_{SS} - 2V_{th})^2} I_1 I_2 \quad (9)$$

The output voltage is equal to the multiplication of the two input currents and a factor which is in the form of the power supply voltage.

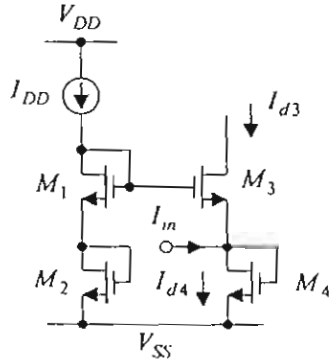

Fig. 3. Four-transistor linear MOS resistor.

2.3 Four-Transistor Linear MOS Resistor

Fig. 3 shows a four-transistor linear MOS resistor or a current-to-voltage converter [10]. Compared with the circuit structure of Fig. 1, the differences are that the gate of transistor M_3 is not connected to the positive supply. Transistors M_1, M_2 and I_{DD} provide the bias voltage while transistors M_3, M_4 perform the current-to-voltage conversion. Assuming that the transistors $M_1 - M_4$ are identical with transconductance parameter K and are biased in saturation region, we can write the following equations

$$V_{gs1} + V_{gs2} = V_{gs3} + V_{gs4} \quad (10)$$

where

$$V_{gs1} = V_{gs2} = \sqrt{\frac{I_{DD}}{K}} + V_{th}$$

$$V_{gs3} = \sqrt{\frac{I_{d3}}{K}} + V_{th}$$

$$V_{gs4} = \sqrt{\frac{I_{d4}}{K}} + V_{th} \quad (11)$$

Substituting eqn.(11) into eqn.(10), we get

$$2\sqrt{I_{DD}} = \sqrt{I_{d3}} + \sqrt{I_{d4}} \quad (12)$$

From the circuit in Fig. 3, we can see that $I_{d4} = I_{d3} + I_{in}$. By substituting in eqn.(12), the drain currents I_{d3} and I_{d4} are written by

$$I_{d3} = I_{DD} - \frac{I_{in}}{2} + \frac{I_{in}^2}{16I_{DD}} \quad (13)$$

$$I_{d4} = I_{DD} + \frac{I_{in}}{2} + \frac{I_{in}^2}{16I_{DD}} \quad (14)$$

The total harmonic distortion is measured by setting the input current I_2 to $10\mu A$ dc current. I_1 is the sinusoidal signal with peak amplitude of $10\mu A$ and the frequency is $1MHz$. The simulated maximum THD is about 1.2%, and the power consumption is about $280\mu W$.

To measure the frequency characteristic of the multiplier, a $10\mu A$ dc current is applied to I_2 while I_1 is the variable frequency sinusoidal input current with peak amplitude of $10\mu A$. From the simulation, the $-3dB$ bandwidth up to $10MHz$ is achieved.

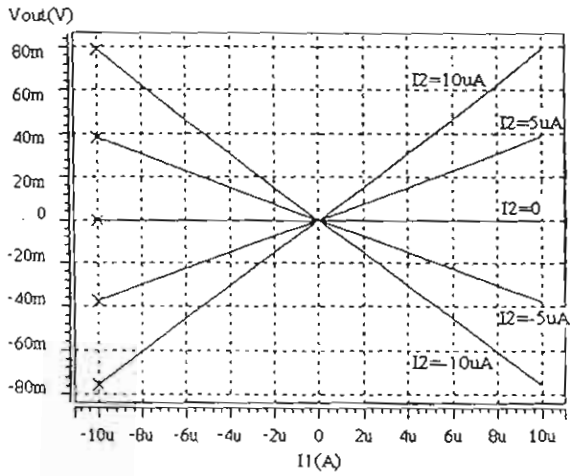

Fig. 6. Transfer characteristic curves.

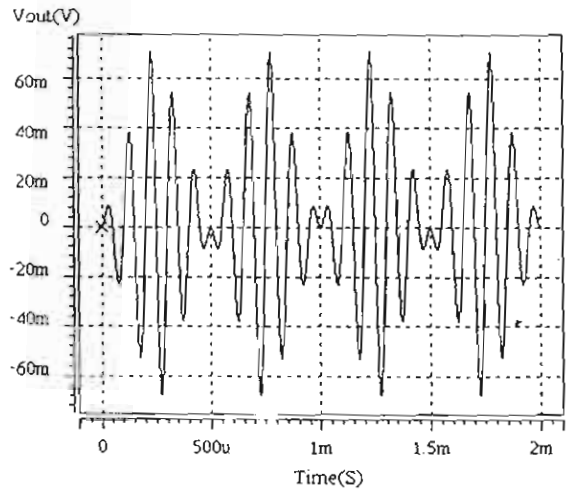

Fig. 7. Amplitude modulation of sinusoidal signal with triangle signal.

4.CONCLUSIONS

A new low-voltage current-mode CMOS four-quadrant analog multiplier based on the square-law characteristic of MOS transistor has been presented. The proposed circuit obtain the single-ended current/voltage output that is performed by using current mirrors and linear MOS resistor. Their performances have been demonstrated by using HSPICE simulations.

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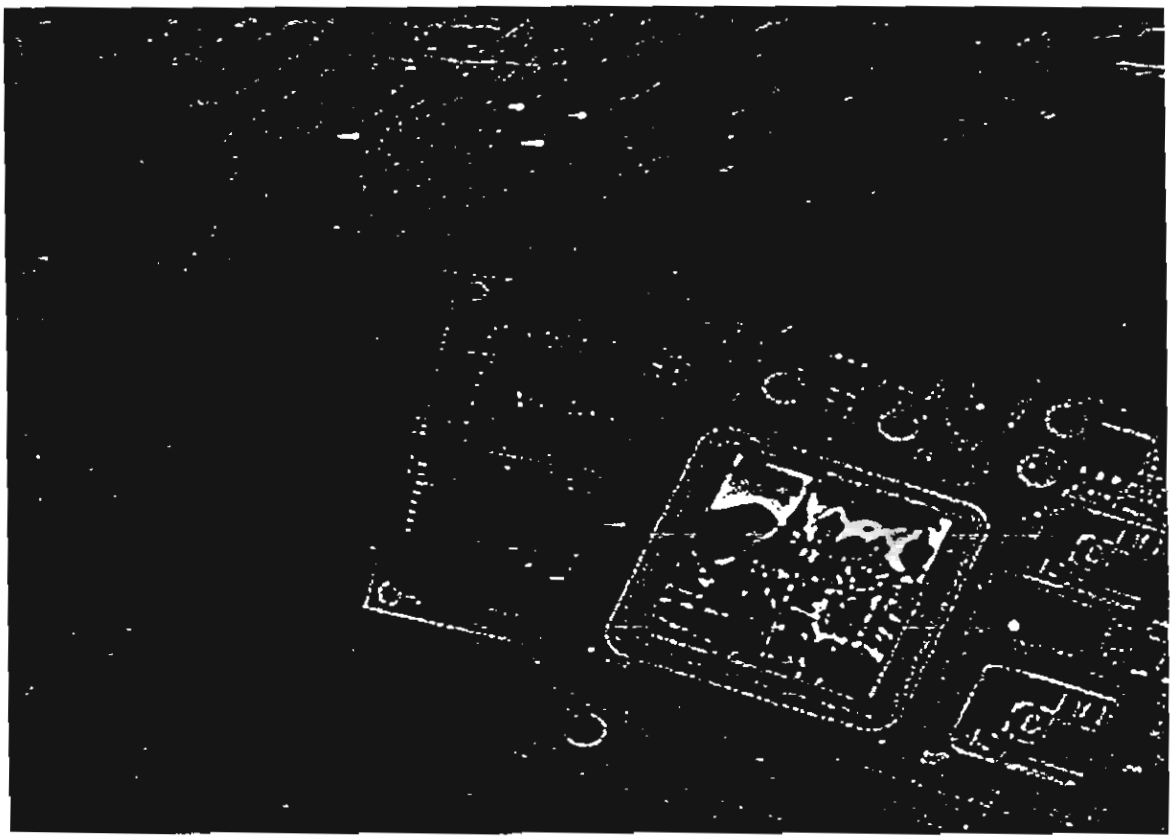

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AN ACTIVE-ONLY CURRENT-MODE DIFFERENTIATOR AND ITS APPLICATIONS

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ABSTRACT

A novel continuous-time current-mode differentiator, which is composed only of internally compensated type operational amplifier (OA) and operational transconductance amplifiers (OTAs), is proposed. The differentiator is suitable for integrated circuit implementation in either bipolar or CMOS technologies, since it does not require any external passive elements. Moreover, the differentiator gain can be electronically tuned through adjusting the bias currents of the OTAs. The performances of the proposed differentiator and its applications to realize current-mode transfer functions and driving-point impedance functions have been demonstrated.

1. INTRODUCTION

Presently, their has been a strong motivation to design resistor-less and capacitor-less filter circuits utilizing the finite and complex gain natures of internally compensated OAs and OTAs. This is due to the fact that they are very suitable for high-frequency operation and for monolithic integration [1]. Some implementations in active-only filter design based on OTAs and OAs are available in the literature [2-3]. It is well accepted that a differentiator is an important circuit building block that is widely useful in many applications, such as, in automatic control systems, communication and instrumentation systems [4]. Although some differentiator circuits have been reported [5-6], the implementation of a continuous-time current-mode differentiator that employs only active elements is not yet available.

Therefore, a new circuit configuration for realizing an active-only current-mode differentiator is proposed in this paper. The proposed current-mode differentiator consists solely of the active OA and OTAs. The differentiator can be implemented in integrated circuit form with small chip area, since no passive element is required. The circuit characteristic can be tuned by adjusting the transconductance gains of the OTAs. In addition, since this circuit provide high output impedance, filter networks in cascading form can be easily implemented. The workability of the proposed differentiator and some applications in the realization of active transfer functions have been demonstrated by simulation results.

2. THE PROPOSED CURRENT-MODE DIFFERENTIATOR

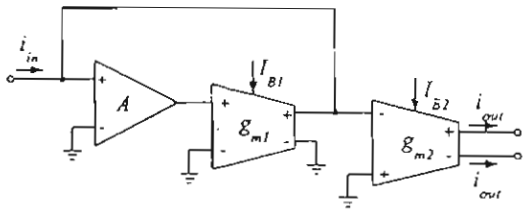


Fig. 1 : The proposed active-only current-mode differentiator

Fig.1 shows the proposed current-mode differentiator. It is constructed only with an OA and dual-current output OTAs, where the plus and minus current outputs of the dual-current output OTA indicate the positive and negative polarity, respectively. If ω_a is the 3-dB bandwidth of the OA and by considering the OA for the frequencies $\omega >> \omega_a$, the open-loop gain $A_{OA}(s)$ of the OA can be approximately given by

$$A_{OA}(s) = \frac{A_o \omega_a}{s + \omega_a} \cong \frac{B}{s} \qquad (1)$$

where B denotes the gain-bandwidth product (GBP) of the OA, which is the product of the dc gain A_O and the 3-dB bandwidth ω_a. For the OTAs, let g_{m1} and g_{m2} denote the transconductance gains of the OTA1 and OTA2, respectively. Therefore from the elementary circuit analysis, the current transfer function of the current-mode differentiator shown in Fig.1 can be derived as

$$\frac{I_o(s)}{I_{in}(s)} = \frac{s}{B}\left[\frac{g_{m2}}{g_{m1}}\right] = s\left[\frac{A_G}{B}\right] \qquad (2)$$

where A_G denotes the differentiator gain, which is the ratio between g_{m2} and g_{m1}. Equation (2) indicates that the relationship of the currents I_o and I_{in} is in the form of the differentiating action as required. It should be noted that, for the bipolar OTAs, $g_{m1} = I_{B1}/2V_T$ and $g_{m2} = I_{B2}/2V_T$, where V_T is the thermal voltage and I_{B1} and I_{B2} are the bias currents of the OTA1 and OTA2, respectively. In this case, the temperature

dependence of the transconductance gains g_{m1} and g_{m2} are also compensated.

In case of the non-ideal performance of the current-mode differentiator, the parasitic effects of the OA and OTAs are taken into consideration. Therefore, the frequency response of the current-mode differentiator in Fig.1 that including the second dominant pole of the OA and the transconductance internal-pole of the OTAs can now be given by

$$\frac{I_o(s)}{I_{in}(s)} = s\left[\frac{1+\tau_b s}{B}\right]\left[\frac{1+\tau_{c1}s}{g_{m01}}\right]\left[\frac{g_{m02}}{1+\tau_{c2}s}\right] \qquad (3)$$

where τ_b (= $1/\omega_b$) is the second dominant pole of the OA, and τ_{ci} (= $1/\omega_{ci}$) and g_{m0i} are the transconductance internal-poles and the low frequency transconductance gains of the i-th OTA (i = 1, 2), respectively. Since these poles are usually equaled (or $\tau_{c1} \cong \tau_{c2}$) and let us define that $A_{G0} = g_{m02}/g_{m01}$ is the dc differentiator gain, then equation (3) can be reduced to

$$\frac{I_o(s)}{I_{in}(s)} = s\left[\frac{A_{G0}}{B}\right](1+\tau_b s) \qquad (4)$$

The frequency characteristic of the proposed current-mode differentiator has a dc current gain equaled to equation (2) and has a high-frequency dominant zero located at ω_b. For example, the commercially available LF356N OA has the gain-bandwidth product $B = 2\pi(4.5)\times10^6$ rad/s and the second dominant pole is $\omega_b = 2\pi(9)\times10^6$ rad/s [7]. Hence, the major high-frequency limitation of the proposed differentiator is approximately located at 9 MHz.

3. APPLICATION EXAMPLES

In the following sections, we will demonstrate the usefulness of the proposed current-mode differentiator. An application to realize current-mode transfer functions employing the proposed differentiator as an active element is introduced. Some application examples to simulate driving-point impedance function elements are also presented.

3.1 General first-order active-only current-mode filter

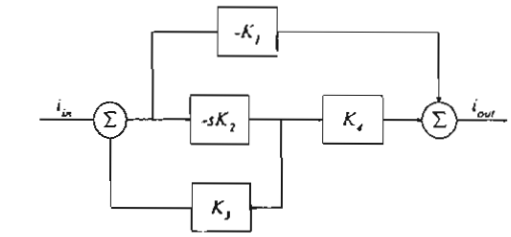
Fig.2(a) shows the basic block diagram used to generate the general first-order transfer function [8]. Based on the use of the proposed differentiator, the general first-order active-only current-mode filter can be implemented and shown in Fig.2(b) with the gains $K_1 = g_{m7}/g_{m6}$, $K_2 = A_G/B = g_{m2}/g_{m1}B$, $K_3 = g_{m5}/g_{m3}$ and $K_4 = g_{m4}/g_{m3}$. The current transfer function of this configuration can be given by

$$\frac{I_o(s)}{I_{in}(s)} = -\left(\frac{sK_2K_4 + K_1}{sK_2K_3 + 1}\right) \qquad (5)$$

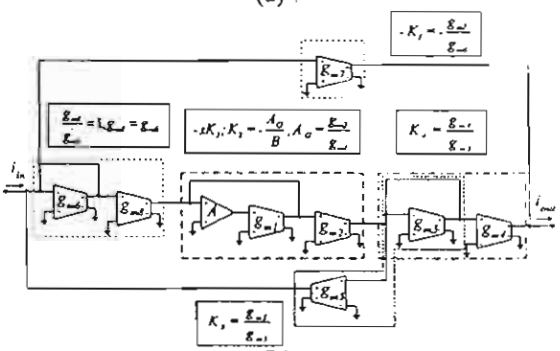
The natural frequency ω_O for this case can be written by

$$\omega_o = \frac{g_{m1}g_{m3}B}{g_{m2}g_{m5}} \qquad (6)$$

Clearly, the natural frequency ω_O can be properly adjusted through the transconductance gains of the OTAs. In addition, for the bipolar OTAs, the temperature sensitive on the parameter ω_O is also compensated.



(a)



(b)

Fig. 2: General first-order building block
(a) block diagram representation
(b) circuit implementation

3.2 Capacitance multiplier

Fig. 3(a) shows the circuit diagram for the application of the current-mode differentiator to realize a grounded capacitance multiplier circuit. Its analysis yields the driving–point impedance function as follows :

$$Z_{in}(s) = \frac{1}{s}\left[\frac{B}{g_{m3}A_G}\right] \qquad (7)$$

where the magnitude of the grounded simulated capacitance can be given by

$$C_{eq} = \frac{g_{m3}A_G}{B} \qquad (8)$$

It is seen from equation (8) that the magnitude of the equivalent capacitance C_{eq} can be electronically controlled by the current ratio A_G and/or the transconductance gain g_{m3}. Moreover, the grounded capacitance multiplier of Fig.3(a) can conveniently be converted into a corresponding floating capacitance multiplier by using only an additional dual-current output OTA2 as shown in Fig.3(b).

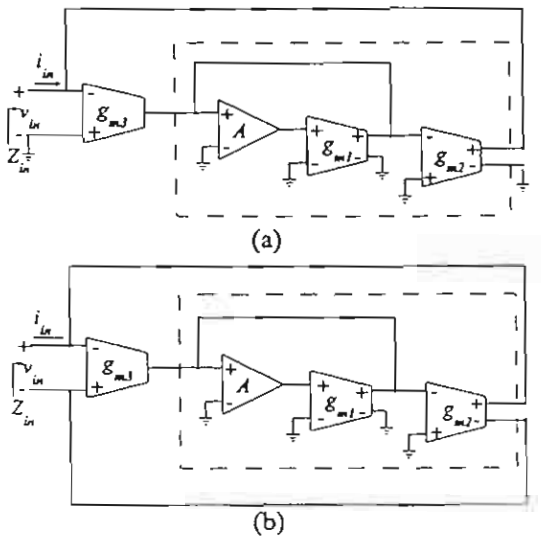


Fig. 3 : (a) grounded capacitance multiplier
(b) floating capacitance multiplier

3.3 Inductance simulation

An application of the proposed current differentiator to simulate a tunable grounded inductance simulation circuit is shown in Fig.4. In this case, the magnitude of the simulated inductance can be given by

$$L_{eq} = \left[\frac{g_{m3} A_G}{g_{m4} g_{m5} B} \right] \qquad (9)$$

Since the ratio of the bias current A_G and the transconductance gains, g_{mi} (i = 3, 4, 5), are electronically variable, the simulated-grounded inductance magnitude will also be electronically variable.

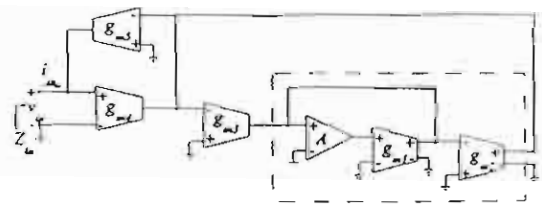


Fig. 4: Inductance simulation

4. SIMULATION RESULTS

PSPICE simulation has been carried out to verify the performance of the proposed current-mode differentiator. In this simulation, the OTA is modeled by employing CA3080 type OTA with a macro model, whereas the dual-current output OTA is constructed by using paralleled-connected single-ended OTAs [9]. The μA741 type OA with the gain-bandwidth product B = 5.906 Mrad/s is used [2]. Fig.5 shows the simulated frequency responses of the proposed differentiator. The obtained results prove that the circuit acts as differentiator with a slope +20 dB per decade from 10 Hz to 1 MHz and has 10% phase error from about 30 Hz to 500 kHz.

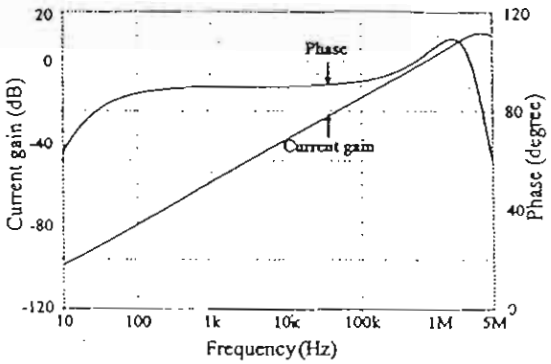


Fig. 5 : Frequency responses of the proposed current-mode differentiator

To verify the characteristic of the first-order active-only current-mode filter, the filter of Fig.2 (a) was constructed as the high-pass filter with the transconductance gains having the following values : g_{m2} = 10 mS and $g_{m3} = g_{m4} = g_{m5} = g_{m6} = g_{m8}$ = 1 mS. The simulated responses for the high-pass output are shown in Fig.6 with g_{m1} varying from 1 mS, 0.5 mS and 0.1 mS. The filter cut-off frequencies are obtained from 103.69 kHz, 52.43 kHz and 10.56 kHz, respectively, which is the same as the expected values given by equation (6).

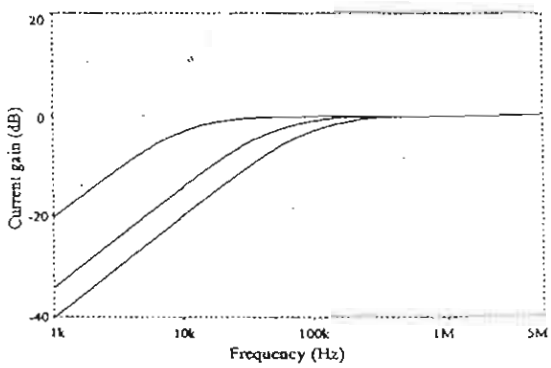
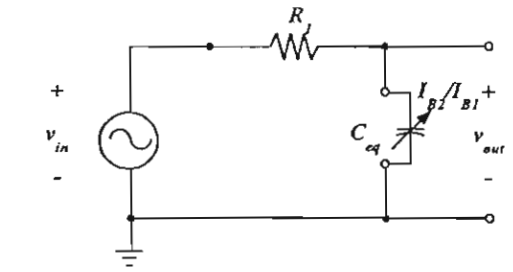
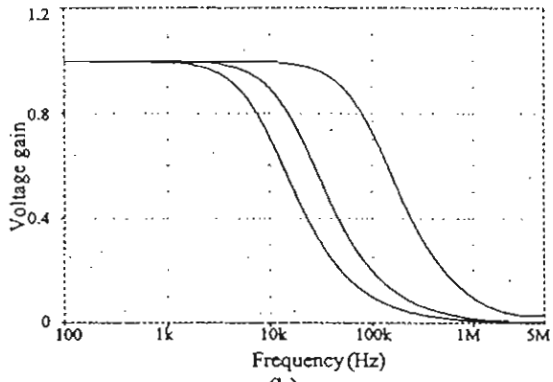


Fig. 6 : Simulated frequency responses of the current-mode filter in Fig.2(b)

The tunable active RC low-pass filter of Fig.7(a) has been chosen to demonstrate the performance of the grounded capacitance multiplier in Fig.3(a). The filter was built with R_1 = 1 kΩ, g_{m1} = 1 mS and g_{m3} = 10 mS. The simulation results when the bias current ratio A_G (= g_{m2}/g_{m1}) is respectively adjusted to 1, 5 and 10 are shown in Fig.7(b). The theoretical cut-off frequencies are 100 kHz, 20 kHz and 10 kHz, where the simulated cut-off frequencies are approximately equal to 106.75 kHz, 20.38 kHz and 10.13 kHz, respectively.



(a)



(b)

Fig. 7 : (a) first-order RC low-pass filter
(b) frequency responses of the RC low-pass filter

5. CONCLUSIONS

An alternative scheme for realizing a continuous-time active-only current-mode differentiator is presented. The proposed differentiator is realizable with only internaliy compensated type OA and OTAs and does not require any external passive elements. Because of its active-only nature and provides high output impedance, the circuit is cascadable structure and is very compatible with integrated circuit implementation in both bipolar or CMOS technologies. Since the proposed circuit utilizes an OA pole, it is also suitable for high frequency operation. The simulation results that agree well with the theoretical analysis are proved to demonstrate the feasibility of the proposed differentiator.

ACKNOWLEDGMENT

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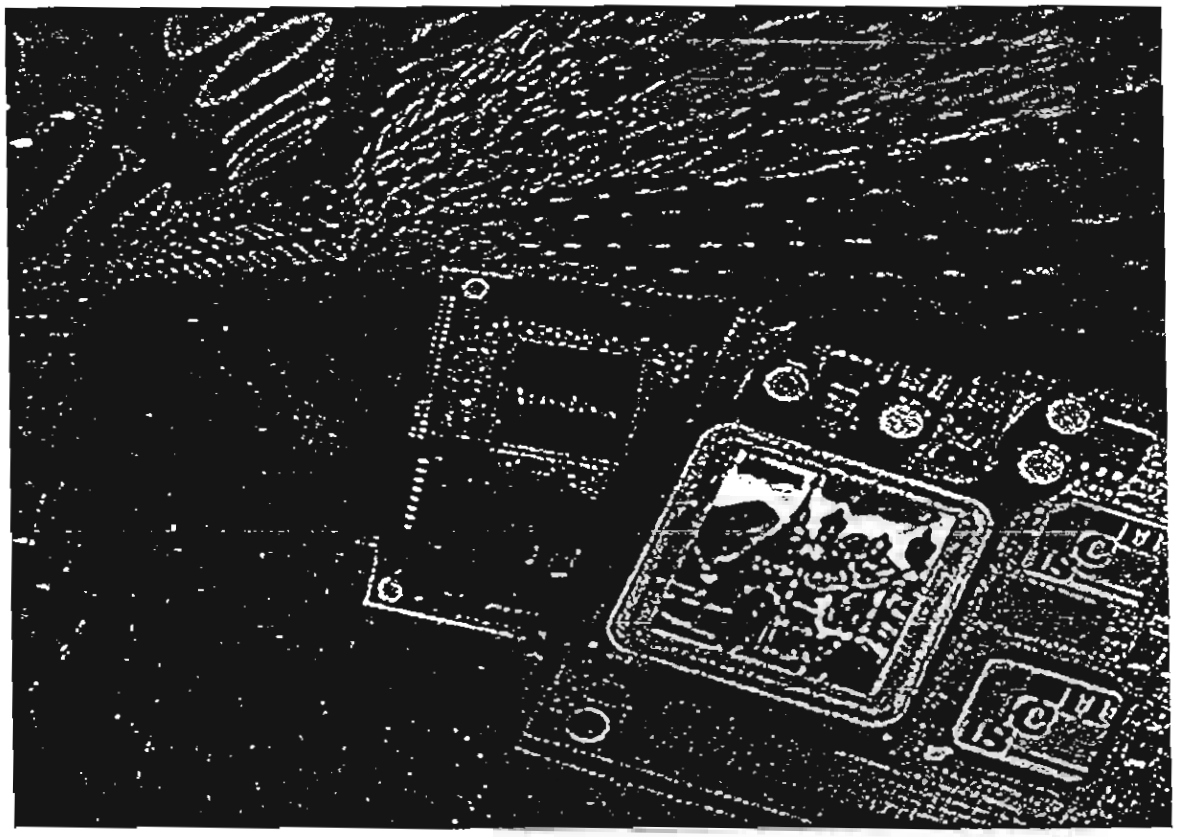

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OTA-BASED TEMPERATURE-INSENSITIVE SINUSOIDAL N-TIMES FREQUENCY MULTIPLIER

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ABSTRACT

A sinusoidal frequency multiplication by any integer factor based on OTA temperature-insensitive is presented. The conception of circuit designs from relationship of trigonometry function. The proposed circuit consists of multiplier and voltage to current which it has temperature insensitive stability and improves dynamic range of signal input. All of these are this circuit advantage in practice. To illustrate this approach, the circuit is simulated in HSPICE.

1. INTRODUCTION

Recently, frequency multiplication is received considerable attention because it's used in analogue signal processing, communications and control system design. There appear researches to frequency multiplication base on application of analogue multiplier[1]-[5], translinear principle[6]-[7]and fundamental-rejecting feedback[8].Most of researches realize the frequency multipliers that are primarily used to extend the output frequency by multiplying the source's fundamental frequency by a specific factor. And it exactly, the output contain besides the desired harmonic output, unwanted signal. These unwanted signals consist of the fundamental input signal leakage, and lower and higher order harmonics generated in the multiplier. Frequency multiplier is typically include of OPAMP and transistor and very few approaches include of OTA[8]. Notice that designed frequency multiplier circuits has disadvantage. The design circuits depend on the absolute temperature.

The major intention of this paper is to present an approach for realizing frequency multiplier using OTA. The proposed circuit can be generate output at n times the input frequency. Trigonometric identities are used to design circuit[2]. In addition, we know that the characteristic of the OTA dependent on the temperature and input voltage is limited to less than 50 mV for linear operation. Thus, the circuit is improved dynamic range and it has temperature insensitive stability[9]

2. REALIZATION OF SINUSOIDAL FREQUENCY MULTIPLIERS

Using the trigonometric identity of cosine term

$$\cos 2\theta = 2\cos^2\theta - 1 \quad (1)$$

$$\cos 3\theta = 2\cos 2\theta \cos\theta - \cos\theta \quad (2)$$

$$\cos 4\theta = 2\cos 3\theta \cos\theta - \cos 2\theta \quad (3)$$

$$\cos 5\theta = 2\cos 4\theta \cos\theta - \cos 3\theta \quad (4)$$

From above equation we can express a general building block in Fig. 1. The Fig. 1 composes of analog multiplier and summing amplifier. The frequency multiplying is straightforward and with out any mathematical approximation.

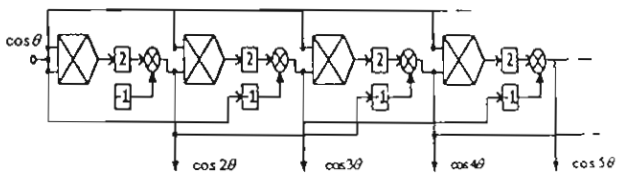

Fig. 1 Block diagram of n-time frequency multiplier

3. PRINCIPLE OF OPERATION

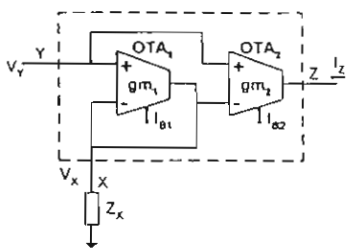

Fig. 2 Circuit of the temperature-insensitive V/I

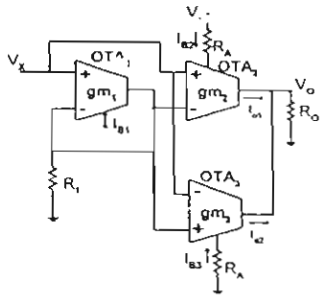

Fig. 3 Temperature-insensitive OTA-based analogue multiplier

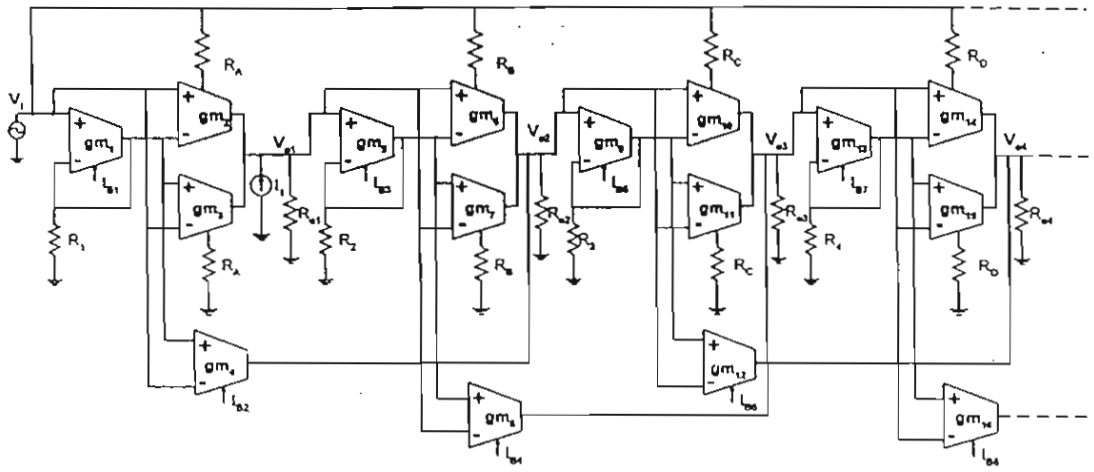

Fig. 4 Proposed circuit of n-time frequency multiplier

Fig. 2 is temperature-insensitive voltage to current converter. We let $gm_1 Z_x >> 1$ then output current can be approximately given by [9]

$$I_Z = \frac{I_{B2}}{I_{B1}} \frac{V_Y}{Z_X} \qquad (5)$$

From eqn.(5), the output current I_z can be settled by bias current ratio between I_{B2} and I_{B1}. The g_{m1} and g_{m2} which vary according to the temperature change is compensated its value in the equation. In addition, the dynamic range of input voltage can approximately be given by $V_{in} \le |2V_T + I_{B1} Z_X|$ .So the dynamic range can be improved by increasing I_{B1} or Z_x .

Apply input voltage V_y to provide current bias I_{B2} and adding OTA3 which acts as OTA2 , we get the analog multiplier in Fig. 3

The output voltage can be expressed as[9]

$$V_o = \{I_{o1} + I_{o2}\} R_o \qquad (6)$$

$$= \frac{R_o}{I_{B1} R_X R_A} V_x V_y \qquad (7)$$

$$V_o = k V_X V_Y \qquad (8)$$

Therefore $k = \dfrac{R_o}{I_{B1} R_x R_A}$

From eqn. (8) shows that the circuit of Fig. 3 provides the function of analog multiplier and k is the multiplication constant

4. CIRCUIT DESCRIPTION

In the Fig. 4, the circuit is relationship of trigonometry function eqn. (1) to eqn. (4) and building block in Fig. 1, we let express cos2θ, cos3θ, cos4θ and cos5θ .

$$V_{o1} = \frac{R_{O1}}{I_{B1} R_1 R_A} V_i^2 - 1 \qquad (9)$$

$$V_{o2} = \frac{R_{O2}}{I_{B3} R_2 R_B} V_{o1} V_{Vi} - \frac{R_{O2} I_{B2}}{I_{B1} R_1} V_i \qquad (10)$$

$$V_{o3} = \frac{R_{O3}}{I_{B5} R_3 R_C} V_{o2} V_{Vi} - \frac{R_{O3} I_{B4}}{I_{B3} R_2} V_{o1} \qquad (11)$$

$$V_{o4} = \frac{R_{O4}}{I_{B7} R_4 R_D} V_{o3} V_{Vi} - \frac{R_{O4} I_{B6}}{I_{B5} R_4} V_{o2} \qquad (12)$$

5. SIMULATION RESULT

The performance of the proposed circuit is verified by HSPICE circuit simulation program. CA3080-type OTA's is used to construct schematic diagram of OTA. From eqn. (1) to eqn. (4) define $R_{o1}/I_{B1}R_1R_A = R_{o2}/I_{B3}R_2R_B = R_{o3}/I_{B5}R_3R_C = R_{o4}/I_{B7}R_4R_D = 2$ and $R_{o2}I_{B2}/I_{B1}R_1 = R_{o3}I_{B4}/I_{B3}R_2 = R_{o4}I_{B6}/I_{B5}R_4 = 1$. So we set $I_{B1}=I_{B3}=I_{B5}=I_{B7}=100\mu A$, $I_{B2}=I_{B4}=I_{B6}=I_{B8}=10\mu A$, $R_A=R_B=R_C=R_D=10k\Omega$, $R_{o1}=R_{o2}=R_{o3}=R_{o4}=100k\Omega$ and $I_1 = 10\mu A$. The response of the n-times frequency multiplier of Fig. 4 is shown in Fig. 5. For $2V_{p-p}$ with 1 kHz frequency input signal, the output signal with nearly to $2V_{P-P}$ amplitude and 2kHz, 3kHz, 4kHz and 5kHz sinusoidal frequency can be simulated. The spectrum of the output Vo1 Vo2 Vo3 and Vo4

are shown in Fig. 6. The total harmonic distortion (THD) of output signal (Vo1, Vo2, Vo3 and Vo4) was calculated by program HSPICE. It was shown in table 1. In Fig. 7 shows the amplitude of output which vary according to the change of temperature –30°c to 100°c. It is clearly seen that the temperature insensitive for the amplitude output signal.

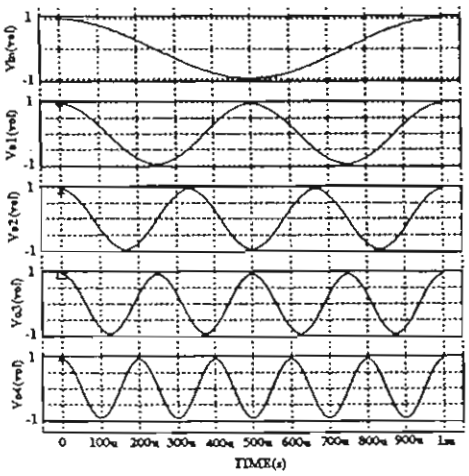

Fig. 5 Input and output signal of the frequency multiplier

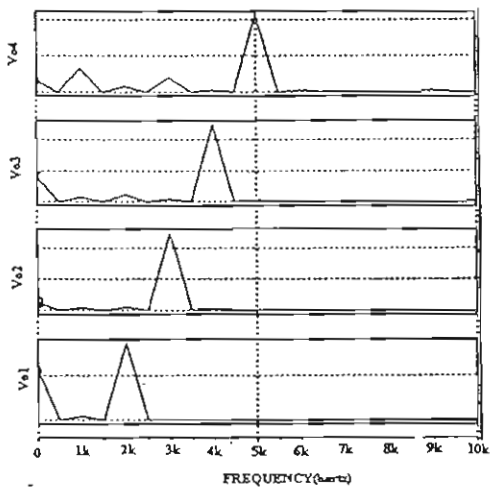

Fig. 6 Spectrum of the output of the frequency multiplier

Frequency	%THD
2kHz	0.57%
3kHz	1.09%
4kHz	0.95%
5kHz	1.4%

Table 1. Total harmonic distortion

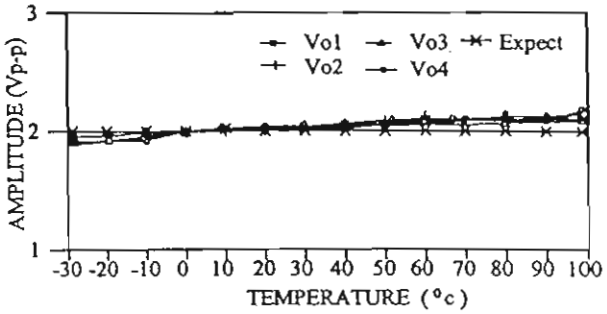

Fig.7 Amplitude of output versus temperature

6. CONCLUSION

OTA-based temperature-Insensitive Sinusoidal n-time frequency multiplier can be builded by using relationship of trigonometry function. This principle is exploited by employing the temperature insensitive stability and wide dynamic range of voltage to current converter circuit, based on OTA. In addition, dynamic range of signal input can be increased by increasing I_B or R.The dynamic range of this circuit was designed approximately ±1 V for I_B=100uA and R=10kΩ. Simulation results have been used to confirm the performance of the proposed circuit.

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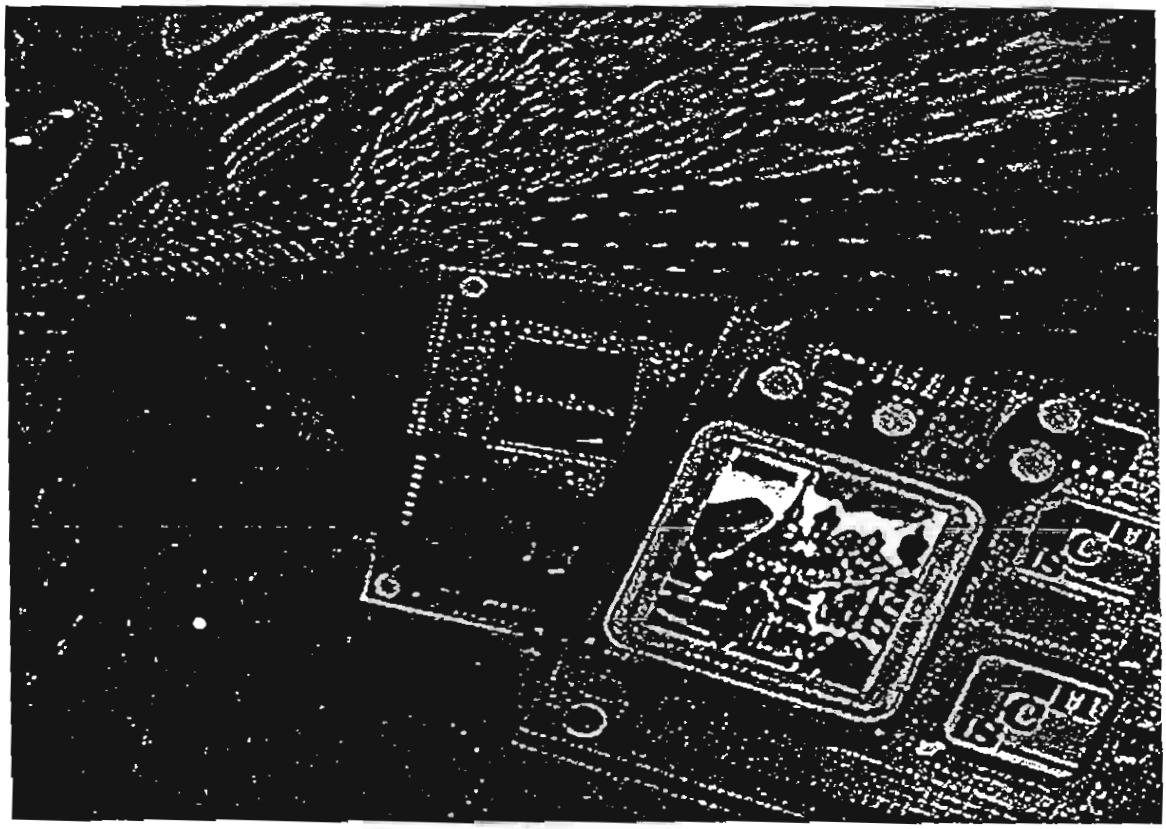

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The implementation of OTA-based full-wave rectifiers

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ABSTRACT

Simple configuration of full-wave rectifier circuits that using operational transconductance amplifiers (OTAs) as only active circuit elements are described in this report. The proposed method is realized through the use of the differential pair, which is the input stage of the OTA. The realization method that suitable for the commercially available CA3280 OTA is also proposed. It is worth to note that the full-wave rectifier implementation circuits consist only of three OTAs. Performance of the scheme is confirmed through PSPICE simulation and experimental results.

1. INTRODUCTION

A rectifier is one of important circuit building block in analog signal processing, signal conditioning and instrumentation systems. For examples, it is employed to implement demodulators, peak amplitude detectors and RMS converters. Usually, the rectifiers can be realized by using diodes and active circuit building block such as operational amplifier and current conveyor [1-2]. And the full-wave rectifier circuit that widely used is operational amplifiers with diodes and resistors. It should be noted that, diodes are the key elements that provide the rectifying action. Recently, in stead of using diodes, several circuit elements have been employed, such as, a single transistor [3], the complementary transistor push-pull amplifiers [4-5], the class AB amplifier [6], the operational amplifier supply-current sensing [7-8], and the translinear current conveyor [9]. However, it seems that none of them have been build by using only OTA. In this paper, we proposed the design of a simple and versatile full-wave rectifier circuits using only OTA, which avoids the use of diode. The circuit rectifier action is exploited from the characteristic of the differential pair inside OTA. Further, the proposed scheme provide very low distortion and high frequency response.

2. CIRCUIT DESCRIPTION

2.1 Basic principle

Consider the differential pair circuit configuration that is shown in Fig. 1. It consists of two closely match transistors, Q_1 and Q_2, whose emitters are joined together and are biased by current source I_B, and the differential voltage V_d is applied between the base of the transistors. It is well known that, if the differential voltage V_d is much greater than $2V_T$, where V_T is the usual thermal voltage, the circuit is saturate, the collector currents become independent of V_d, and the current I_B is flowing in only one of the transistors.

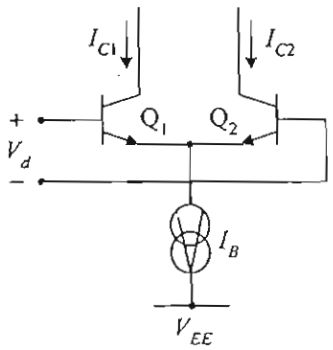

Fig. 1 Differential pair configuration.

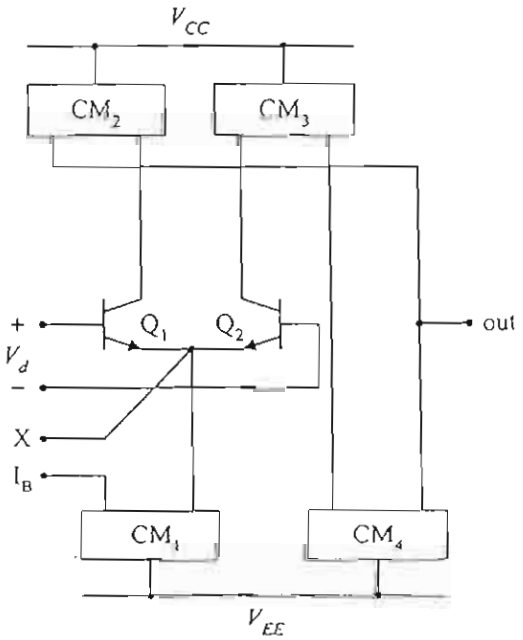

Fig. 2 Equivalent circuit of the CA3280 OTA.

This action is similar to a rectification function and will be particularly useful if we can use the differential amplifier for the design of a rectification circuit. Since the input stage of the

OTA is the differential amplifier, therefore, in the following sections rectifier circuits that make use of the differential amplifier inside the OTA will be proposed. Fig. 2 shows the equivalent circuit of the commercially available OTA CA3280. It should be noted that the equivalent circuit is similar to most of the OTA. However, for the CA3280, it allows us to access to the emitters of the differential pair, which is a special feature of this OTA. We can see that the terminal X is directly access to the emitters of the differential pair. A rectifier circuit that using this special feature of the CA3280 OTA is also presented.

2.2 Half-wave rectifiers

In this section two new topologies for the design of half-wave rectifiers using OTAs are developed. The first design method is shown in the Fig. 3. Let V_{in} is an input signal voltage and g_{m1} is the transconductance gain of the OTA A_1, where $g_{m1} = I_{B1}/2V_T$ and I_{B1} is the bias current. The output current of the OTA A_1 is equaled to $I_1 = g_{m1}V_{in}$ and the current I_1 is fed as the bias current of the OTA A_2. From the Fig. 3, if $V_C >> 2V_T$, the output current I_2 of the circuit can flow only in one direction and can be expressed as

$$I_2 = \begin{cases} g_{m1}V_{in} & for\ V_{in} > 0 \\ 0 & for\ V_{in} < 0 \end{cases} \quad (1)$$

Then the circuit is functioned as a half-wave rectifier.

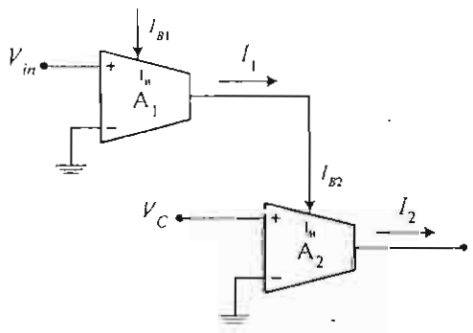

Fig. 3. The proposed OTA-based half-wave rectifier circuit.

The alternative scheme for the realization of the half-wave rectifier is shown in Fig. 4. This configuration uses the advantage of the commercially available CA3280 OTA that the emitters of the differential pair are accessible. The OTA A_2 is the CA3280 OTA and the output current I_1 of the OTA A_1 is fed into the terminal X of the OTA A_2. If I_{B2} is small, then there is the output current I_2 only for the case $V_{in} < 0$ and flow out to the output terminal of the OTA A_2, where

$$I_2 = \begin{cases} 0 & for\ V_{in} > 0 \\ g_{m1}V_{in} & for\ V_{in} < 0 \end{cases} \quad (2)$$

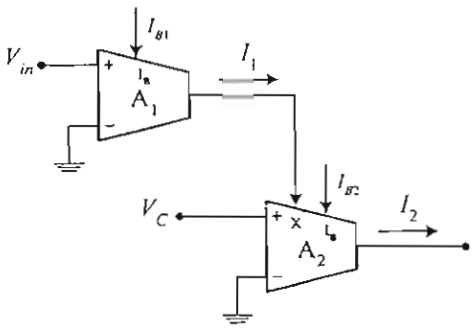

Fig. 4 The half-wave rectifier using CA3280 OTA.

2.3 Full-wave rectifiers

The positive half-wave rectifiers in the Fig. 3 and 4 can now be extended to form a full-wave rectifier. Fig. 5 shows the circuit diagram of the proposed full-wave rectifier that using the half-wave rectifier of the Fig. 3. The OTA A_1 and the OTA A_3 are biased such that $I_{B1} = 2I_{B3} = 2I_B$, where $g_{m1} = 2g_{m3} = 2g_m$. The operation of the circuit can be explained as follow. For $V_{in} > 0$, the current I_1 and I_3 of OTAs A_1 and A_3 can respectively be expressed as

$$I_1 = g_{m1}V_{in} = 2g_mV_{in} \quad (3a)$$

and

$$I_3 = -g_{m3}V_{in} = -g_mV_{in} \quad (3b)$$

Since the current I_1 is the bias current of the OTA A_2, for $V_C >> 2V_T$ then the relationship of the current I_1 and I_2 are

$$I_2 = I_1 = 2g_mV_{in} \quad (4)$$

From eqns. (3) and (4), the output current I_{out}, which is the summation of the currents I_2 and I_3, can be given by

$$I_{out} = I_2 + I_3 = g_mV_{in} \quad for\ V_{in} > 0 \quad (5)$$

Similarly, from the eqn. (1) and for $V_{in} < 0$, the current $I_2 = 0$. The output current I_{out} can be given as

$$I_{out} = I_3 = g_mV_{in} \quad for\ V_{in} < 0 \quad (6)$$

From eqns. (5) and (6), we can summarize that the output current are in the form of full-wave rectifier action and can be expressed as

$$I_{out} = g_m |V_{in}| = \frac{I_B}{2V_T} |V_{in}| \qquad (7)$$

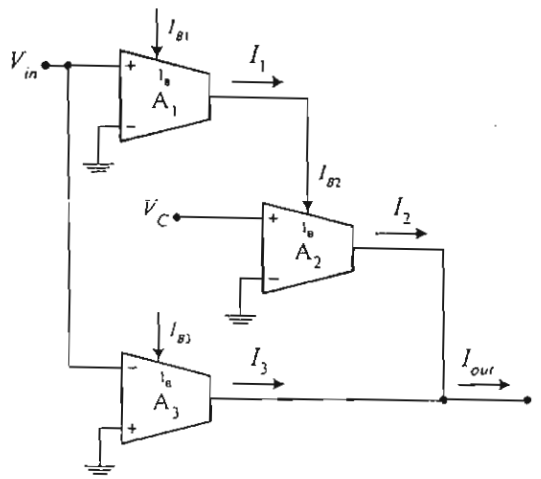

Fig. 5. The proposed full-wave rectifier circuit.

Alternatively, the full-wave rectifier can be realized from the CA3280 OTA. As shown in the Fig. 6, the OTA A_2 is the CA3280 OTA, the current I_1 input at the terminal X of the OTA A_2, and the input signal V_{in} is fed at the positive terminal of the OTA A_3. It can easily be shown that the output current I_{out} becomes a full-wave rectification function as same as eqn.(7).

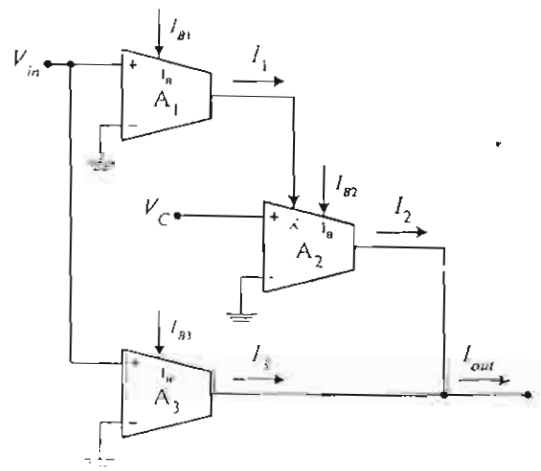

Fig. 6 The full-wave rectifier using CA3280 OTA.

It should be noted that the dynamic ranges of these rectifiers are approximately equal to $V_{in} = V_T$. Using the linearizing diodes inside the OTAS A_1 and OTA A_3 can increase the dynamic range.

3. SIMULATION AND EXPERIMENT RESULTS

To verify the performance, the circuits in Fig. 5 and 6 were simulated with the PSPICE simulation program. The OTA 3280 type is used to construct schematic using bipolar transistor parameter for NPN and PNP transistors, respectively [10]. The OTAs bias currents I_{B1} and I_{B3} were set 1mA and 0.5mA, respectively, for g_{m1} = 0.02A/V and g_{m3} = 0.01A/V, respectively. The power supply voltages were set V_{CC} = -V_{EE} = 15V and V_C = 1V. Fig. 7 shows the simulated result for dc transfer characteristic of the proposed circuits. It is shown that the circuit exhibits high accuracy and linearity for V_{in} as small as ±20mV. The simulation result of the Fig. 8 shows the superposition trances of the sinusoidal input signal with full-wave rectifiers signal. The sine wave input amplitude is $10mV_{p\text{-}p}$ for the frequency of 1KHz and a load resistance of R_L = 100Ω. It is seen that the circuit response is a very good full-wave rectifiers. The experimental circuit is constructed by utilizing the commercially available dual CA3280 OTAs. The experimental result of the Fig. 9 shows that the circuit exhibited very low distortion for low-level input signal as full-wave rectifiers.

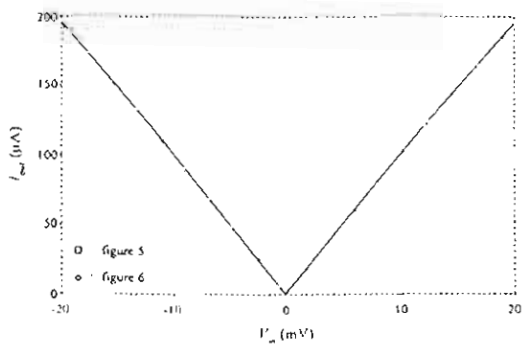

Fig. 7 DC transfer characteristic of the proposed circuits.

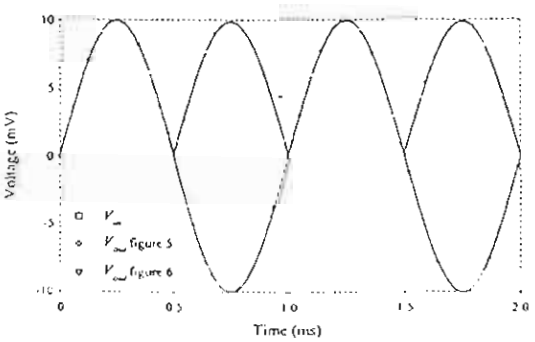

Fig. 8 Simulation result.

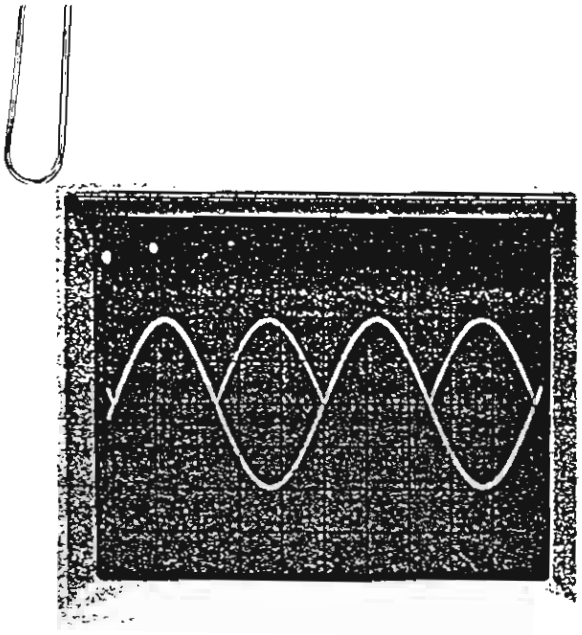

Fig. 9 Experiment result.
Vertical scale : 5mV/division
Horizontal scale : 0.2ms/division

4. CONCLUSION

The use of commercially available OTA CA3280 as full-wave rectifier circuits has been shown in this paper. The rectifiers have a simple configuration and can be implementing using only OTA. The realization method comprises three OTAs. The basic performance of the circuits have been verified through PSPICE simulation and experimental results.

5. ACKNOWLEDGEMENT

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Constant-g_m Rail-to-Rail CMOS Multi-Output FTFN

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Abstract: An alternative CMOS implementation of a multi-output four-terminal floating nullor (FTFN) with constant-g_m rail-to-rail input stage is proposed. This presented circuit is based on the advantages of a complementary transconductance amplifier and class AB dual translinear cell circuit that comes up with wide bandwidth. The constant-g_m characteristic is controlled by the maximum-current selection circuits, maintaining the smooth response over the change of input common mode voltage. The circuit performances are confirmed through HSPICE simulations. A current-mode multifunction filter is used to exhibit the potentiality of this proposed scheme.

1. Introduction

Recently, there are many attempts to design a high performance four-terminal floating nullor (FTFN), which has been stood out as a more flexible and versatile than the other building blocks [1-4], especially, in current-mode circuits. This work shows the other choice to achieve an integrable multiple-output port FTFN in CMOS technology, which offers high bandwidth and low-voltage operation. This proposed circuit scheme is the combination of a low-voltage P-N complementary transconductance amplifier, a dual translinear cell and some of current mirrors. The sufferings from transconductance variation and degradation of common mode rejection ratio (CMRR) [5] have been reduced by using the current-selector circuit technique. In addition, the number of output ports can be expanded to support the designer applications. The characteristics of the FTFN are explained by mean of simulation results using HSPICE program. The current-mode multifunction filter is adopted to demonstrate the performance of this proposed circuit.

2. Multi-output FTFN

FTFN is an active device that equivalent to an ideal nullor, which can imply to be a high gain transconductance amplifier with floating characteristic at input and output terminals. Fig. 1(a) shows a nullor model of an FTFN that can be described by its port relation characteristics as:

$$v_Y = v_X \qquad i_Y = i_X = 0 \qquad i_Z = -i_W \qquad (1)$$

One of the most famous realisation techniques is built up from a basic type shown in Fig. 1 (b) [1, 2]. It is using one op-amp and supply current sensing technique, where the output impedance of port W is very low and the impedance of port Z is very high.

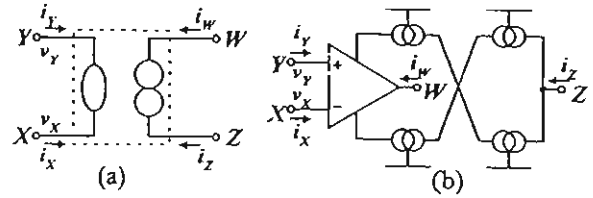

Fig. 1 (a) A nullor model (b) traditional implementation

A modification from the original FTFN to be a multi-output FTFN is done by adding the new output terminals as shown in Fig. 2, where its characteristics can be point out by the following port relations:

$$v_Y = v_X \quad , \quad i_Y = i_X = 0$$

$$i_{Z1} = i_{Z2} = \cdots = i_{Zn} = -i_{W1} = -i_{W2} = \cdots = -i_{Wn} \qquad (2)$$

where n is number of the output ports.

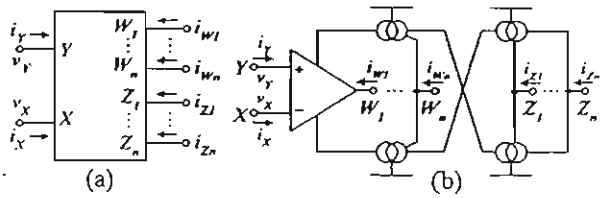

Fig.2 (a) Multi-output FTFN symbol (b) implementation

3. Circuit Description

The proposed circuit can be divided into 2 main sections, the constant-g_m low-voltage P-N complementary input stage and the dual translinear loop output stage, that will be described below.

3.1 Input stage

For lowering supply voltage in an amplifier, it is highly desirable to have a rail-to-rail input voltage swing. The P-N complementary differential pairs have been widely used in the input stage of low-voltage op-amp to achieve this requirement [6]. However, the P-N complementary structure is known to suffer from low common mode rejection ratio (CMRR) due to mismatch errors and the tail current switching between the P and N input stage [5]. Several techniques are invented to resolve this problem. Most of them are usually based on controlling the summation of the tail currents [5-6]. This work, in contrast, uses the maximum current selector circuits to choose only one current from P and N differential pairs, which has the highest magnitude at that time, preventing doubleo utput current when P and N pairs are both turned-on.