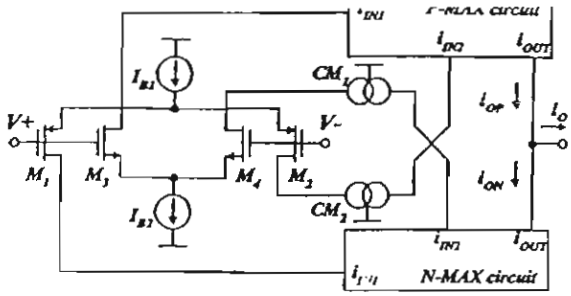
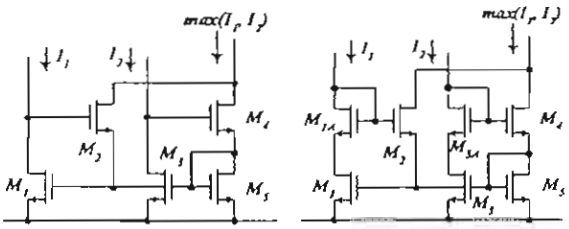


Fig.3 Rail-to-rail input stage using current selector circuit

The proposed structure is shown in Fig. 3. Transistors M_1 to M_4 and the bias current sources I_{B1}, I_{B2} perform the P-N complementary differential pairs. The output signal currents are sent to the maximum current selector P-MAX and N-MAX, where PMAX and NMAX are symbols of PMOS-type and NMOS-type circuit, respectively. CM_1 and CM_2 are replaced with the unity gain current mirrors. The maximum-current selector proposed by Huang and Lui has been chosen for our work and the NMOS-type circuit is redrawn in Fig. 4(a). This maximum circuit was developed based on the bounded difference equation analysis, which can diminish the accumulated errors in the old type binary tree structure [7]. It works like a Wilson current mirror, therefore, the accuracy of the selector circuit can be gained up by appending the additional diode in the same manner as improved Wilson current mirror. In this case, transistor M_{1A} and M_{3A} have been added to the circuit as shown in Fig. 4(b). From the basic analysis of the differential amp, the total output current i_O can be simply depicted as

$$i_O = \max(g_{mN}, g_{mP})(v_+ - v_-) \qquad (3)$$



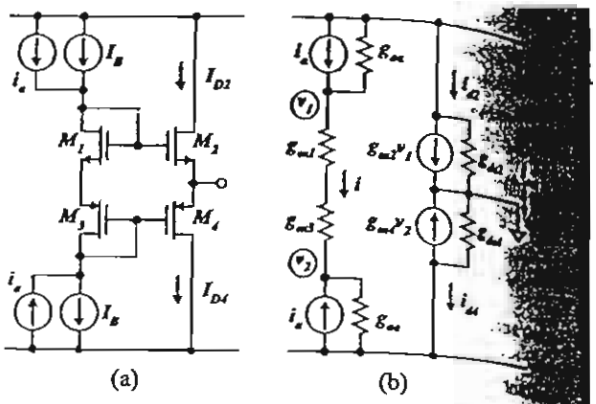
(a) (b)

Fig.4 (a) maximum current selector (b) improved circuit

where g_{mN} and g_{mP} are transconductance gain of N and P pairs, respectively. Moreover, since this technique directly measures current from diff-amp using only current maximum selector circuit, it can work well independent of transistor process (bipolar or CMOS) and mode of operation (weak or strong inversion).

3.2 Output stage

The dual translinear loop output stage is shown in Fig. 5(a) which has been modified by injecting small signal current i_o along with DC current bias I_B. The small signal model for calculating current gain A_i of this stage appears in Fig. 5(b). Assume all transistors are identical, we can estimate the current gain as



(a) (b)

Fig.5 (a) translinear O/P stage (b) small signal model

$$A_i = \frac{i_{out}}{i_o} = \frac{g_{m(tran)}}{g_{oo} // g_{oa}}$$

where $g_{m(tran)}$ is the transconductance gain of MOS transistor in translinear loop and g_{oo} is the output conductance of current signal source i_o.

3.3 Overall amplifier

The simplified schematic of the constant-g_m rail-to-rail CMOS multi-output FTFN is illustrated in Fig. 6. It is designed with the building blocks introduced above, using the 0.7 μm CMOS process supplied by EUROPRACTICE. According to the complete circuit, the maximum selected current from the input stage will be sensed and enlarged by transistor M_{27}, M_{32} before injected to the translinear cell, M_{28} – M_{31}, and then summed to be output current at port W_1. This configuration provides high transconductance gain over a wide frequency range. Transistors M_{33} and M_{34} detect output current at port W_1an d then copy to the other ports. Ideally, it is required that the translinear loop transistors M_{28} – M_{31} are closely matched and all current mirrors have the exact unity gain. We can evaluate the total transconductance gain G_m of this FTFN from combining equation (3) and (4) and give

$$G_m = \frac{i_{W1}}{(v_Y - v_X)} = \frac{\max(g_{mN}, g_{mP}) g_{m(tran)} \frac{(W/L)_{27}}{(W/L)_{13}}}{g_{ds27} // g_{ds32}} \qquad (5)$$

It should be noted that the transistor with a box at its gate imply to be the super transistor such as cascode or regulated cascode transistor. After using the FTFN in the network with a proper feedback, the translinear cell act as a current-follower that allows output current i_{W1} to sources and sinks at port W_1 and will be reflected and inverted to be current i_{Z1} at terminal Z_1, which keeps up $i_{Z1} \cong -i_{W1}$. The multi-output topology can be easily adapted by adding transistors to the output current mirror set. Transistors M_{34-2} – M_{34-n} and M_{37-2} – M_{37-n} are used to perform the output terminals W_2 to W_n, respectively. Similarly, transistorsM_{40-2} – M_{40-n} and M_{42-2} – M_{42-n} are used to perform the output terminals Z_2 to Z_n.

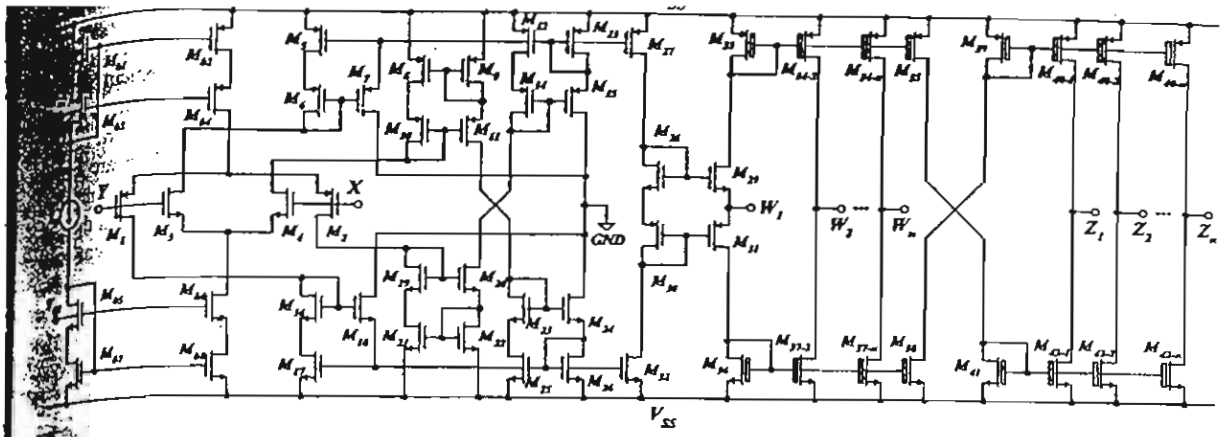


Fig.6 Complete circuit of constant-g_m rail-to-rail multi-output FTFN

3. Simulation Results

The performance of the proposed circuit is verified by HSPICE circuit simulation program based on 0.7-μm CMOS process level-49. All transistor dimensions are listed in Table 1, where W is channel width and L is channel length. The bias currents are set to I_B = 50 μA where the bias voltages are V_{B1} = +1.5V and V_{B2} = -1.5V. Supply voltages are taken as V_{DD} = +2.5V and V_{SS} = -2.5V. The characteristic of open loop transconductance gain is given in Fig. The –3 dB bandwidth can be estimated as about 7 MHz and the transconductance gain about 120 mA/V is obtained.

Table 1 Transistors dimension

Transistors	W/L
M_1, M_2	150μ/0.7μ
M_3, M_4	50μ/0.7μ
M_5 – M_{15}, M_{b1}, M_{b2}, M_{b5}, M_{b6}, M_{33}, M_{34-2} – M_{34-n}, M_{35}, M_{39}, M_{40-1} – M_{40-n}	15μ/0.7μ
M_{b3}, M_{b4}	45μ/0.7μ
M_{16} – M_{26}, M_{b7}, M_{b8}, M_{36}, M_{41}, M_{37-2} – M_{37-n}, M_{42-1} – M_{42-n}	5μ/0.7μ
M_{28}, M_{29}	100μ/0.7μ
M_{30}, M_{31}	300μ/0.7μ

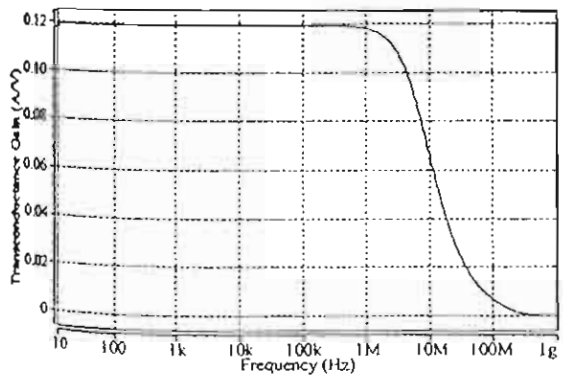
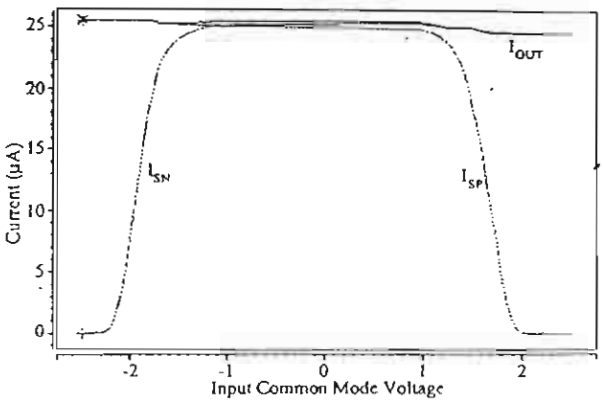
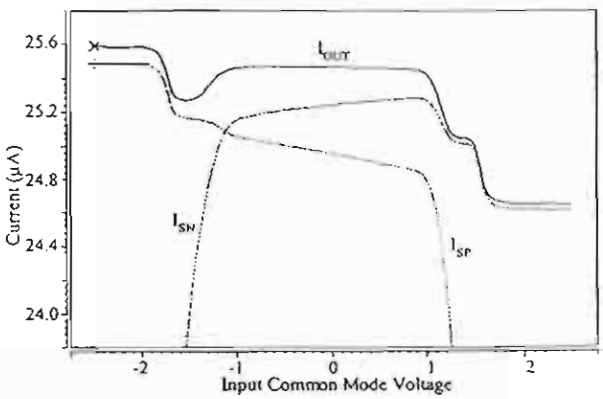


Fig.7 Open loop transconductance gain

This circuit consumeab out 3mW power dissipation. Fig. 8(a) shows the input constant-g_m feature where I_{SN} and I_{SP} are currents from N-differential pair and P-differentialp air, respectively. Fig.8 (b) shows the enlarged view of the maximum current selector operation that can notice a quite good in tracking of output current I_{OUT}. The CMRR of the amplifier is also simulated and shown in Fig. 9.



(a)



(b)

Fig.8 (a) Input stage current (b) enlarged view

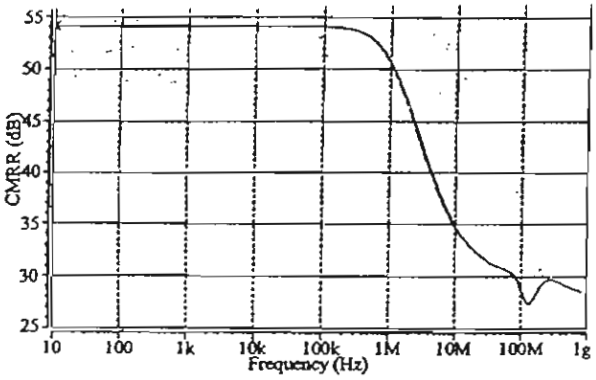


Fig.9 Simulated CMRR of the multi-output FTFN

The frequency response of the CMRR can keep in the same length both in magnitude and bandwidth with a bit better compared to the method mentioned in reference 5 while our proposed structure is simpler. Realisation of a current-mode multifunction filter from reference 2 is chosen as an illustrative example. Filter's structure is redrawn in Fig. 10. MFTFN symbol refers to our proposed multi-output FTFN. The simulation result of the current-mode filter using the proposed multi-output FTFN is given in Fig. 11. It can be observed that the current-mode multifunction filter cannot response correctly since the frequency up to about 100MHz. This is due to the parasitic elements inside the FTFN, which can also be noticed the deviation at the same point of the simulated CMRR result in Fig. 9. One of the major limitations is from current selector circuit itself, which cannot operate in high frequency. The improvement can be done by improving current selector circuit's characteristic.

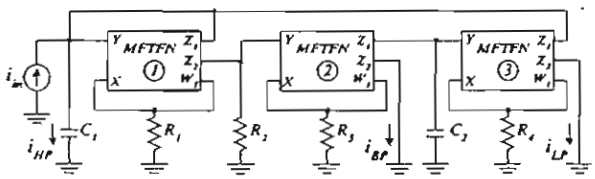


Fig.10 Current-mode multifunction filter

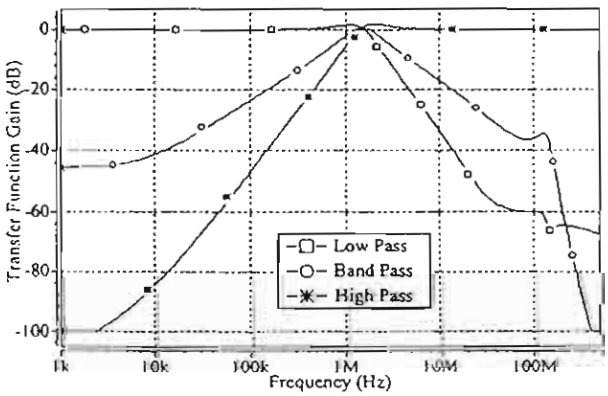


Fig.11 Simulated results of the current-mode multifunction filter

4. Summary

We have proposed a constant-g_m FTFN circuit with additional extended output port. The achievement is realised through the use of a P-N complementary transconductance amplifier, a translinear cell and standard current mirrors. The maximum current selectors are used to control the overall transconductance of the amplifier. Simulation results from HSPICE program confirm the qualification of our presented circuit. A current-mode multifunction filter is an example to identify the features of the circuit.

5. Acknowledgement

This work was partly funded by the Thailand Research Fund (TRF) under the Senior Research Scholar Program grant number RTA/04/2543. The support provided by the Japan International Cooperation Agency (JICA) is acknowledged.

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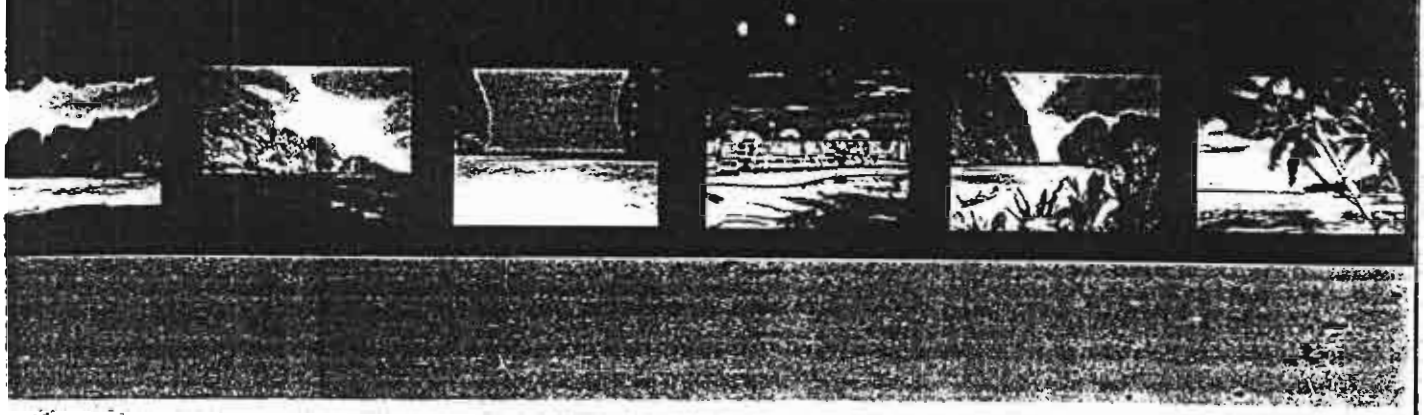

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Volume 1

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A Simple Current-Mode Analog Multiplier-Divider Circuit Using OTAs

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Abstract: An analog multiplier-divider circuit that realized through the use of OTAs, which does not require external passive circuit elements and temperature compensated, is proposed in this paper. Since the scheme is realized in such a way that employs only OTA as a standard cell, the circuit is simple and can be easily constructed from commercially available IC. The circuit bandwidth is wide and close to the transistor f_T. Simulation results that demonstrate the performances of the multiplier-divider circuit are included.

1. Introduction

Analog multipliers and dividers are important nonlinear building blocks that have found useful in a wide range of applications, such as telecommunication, control, instrumentation and signal processing. At present, because of the main featuring of wider bandwidth, greater linearity, wider dynamic range and simple circuitry compared with their voltage-mode counterparts, current-mode circuits have been received growing interest in analog signal processing circuits. Many techniques to design current-mode analog multiplier-divider circuits have been presented in the literature [1-3]. Recently, a multiplier-divider circuit using only two second-generation current-controlled current-conveyors (CCCIIs) has been presented, where no resistors, no capacitors and no MOS transistors are required by such a realization scheme [4].

It is well accepted that OTA is a useful circuit building block in the design of analog circuits. It has been employed in the realization of active network elements, such as filters, oscillators, instrumentation amplifiers and gyrators. The OTA is a commercially available, low cost device that incorporates all the attractive features of an operational amplifier (OA). Since OTA is a programmable device and has only a single high-impedance node, this makes the OTA an attractive device for high frequency and programmable basic building block [5,6]. Therefore, the implementation of analog circuits in such a way that employs only OTA as a standard cells will not only be easily constructed from readily available cells, but also significantly simplified the design and layout. A circuit technique to employ OTAs to implement analog multiplier has been presented [7]. However, the circuit is voltage-mode circuit and only multiplication function is implemented. In this paper, a current-mode temperature compensated multiplier-divider circuit using only OTAs as active circuit elements has been presented, where no passive elements are required by this realization scheme. PSPICE simulation results will be used to demonstrate the performance of the proposed scheme.

2. Basic principle

The schematic diagram of the proposed current multiplier-divider circuit using OTAs is shows in Fig. 1. The input signal current i_{in1} is injected into the operational transconductance amplifier OTA1, which is connected as a grounded resistor. The voltage across the OTA1 is then used as the input voltage for the OTA2 and OTA3. The input signal current i_{in2} is added with the bias current I_{B2} of the OTA2. If g_{m1}, g_{m2} and g_{m3} are the transconductance gains of the OTA1, OTA2 and OTA3, respectively; then, from routine circuit analysis, the output currents I_{O2} and I_{O3} of the OTA2 and OTA3, respectively, can be written as

$$I_{o2} = \frac{g_{m2}}{g_{m1}} i_{in1} = \frac{(I_{B2} + i_{in2})}{I_{B1}} i_{in1} \qquad (1)$$

and

$$I_{o3} = -\frac{g_{m3}}{g_{m1}} i_{in1} = -\frac{(I_{B3})}{I_{B1}} i_{in1} \qquad (2)$$

where $g_{m1} = I_{B1}/2V_T$, $g_{m2} = (I_{B2}+i_{in2})/2V_T$ and $g_{m3} = I_{B3}/2V_T$ and V_T is the thermal voltage.

If we set $I_{B2} = I_{B3} = I_B$, the output current I_{OUT} of the circuit, that is the summation of the currents I_{O2} and I_{O3}, can now be given by

$$I_{out} = I_{o2} + I_{o3} = \frac{i_{in1} i_{in2}}{I_{B1}} \qquad (3)$$

which is in the form of a current-mode analog multiplication/division function. The circuit performs as a four-quadrant multiplier if i_{in1} and i_{in2} are the input signals, while it performs as a divider circuit if i_{in1} (or i_{in2}) and I_{B1} are the input signals. It should be noted that, since it is the ratio of OTAs transconductance gain, the output current I_{out} is less sensitive to temperature.

The major factors that contribute to the error and non-linearity in the circuit can be classified as follows. The first factor is due to the offset current at the output port of the OTA1. From (3), if I_{os} is the offset current, the output current I_{out} can be rewritten as

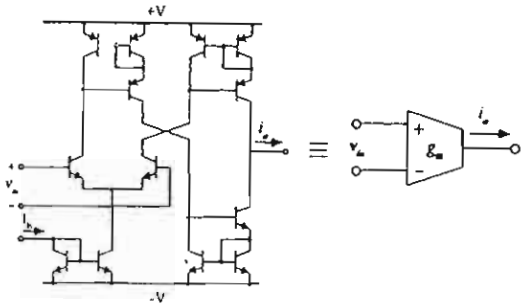

Fig. 1 The schematic diagram of the OTA.

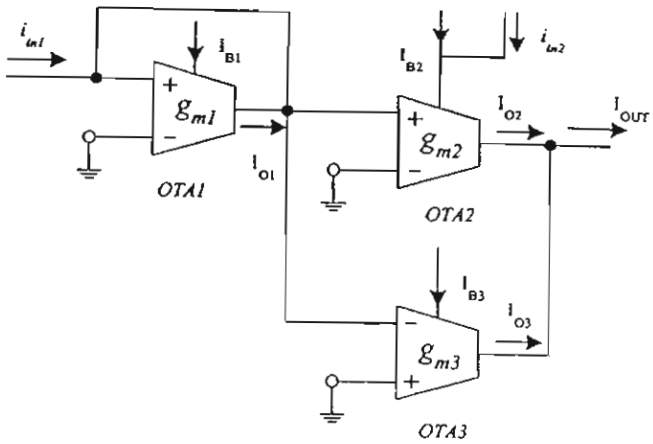

Fig. 2 The proposed current-mode multiplier-divider circuit using OTAs.

$$I_{out} = \frac{(i_{in1} + I_{os})\, i_{in2}}{I_{B1}} \qquad (4)$$

We can see that, particularly for the peak value $|i_{in1}| \le I_{os}$, the multiplication for the positive peak and the negative peak of i_{in1} will not be equal. Thus the signal peak value should be selected such that $|i_{in1}| \ge I_{os}$. While the offset currents at the output ports of the OTA2 and OTA3 are not contribute to the multiplication error, but will produce a DC current at the output of the circuit. The second factor affecting the non-linearity of the circuit is due to the limited linear range of the input stage of the OTA2 and OTA3. For a bipolar-based OTA, where the input stage is a conventional differential pair, the input differential voltages for linear operation are restricted to be less than 26 mV. Since $1/g_{m1} = 2V_T/I_{B1}$, this restricted linear range can be improve by increasing I_{B1}.

3. Simulation results

As shown in Fig.1, in this work an OTA that realized in bipolar transistor technology will be employed as active circuit elements. Its transconductance gain ($g_m = V_T/2I_B$) can be tune by the DC bias current (I_B). The performance of the proposed multiplier-divider circuit of Fig.1 was verified through the use of SPICE simulation results. All the OTA was simulated by using the bipolar transistor parameters of the 2N3904 and 2N3906 for the NPN and PNP transistors, respectively. The transistors f_T were 186 MHz. The circuit of Fig. 2 was simulated using the PSPICE circuit simulation program. The multiplier function was tested by multiplying two sinusoidal signals. The result obtained are shown in Fig. 3 for $i_{in1} = 0.5\sin(2\pi 1000t)$ mA, $i_{in2} = 0.5\sin(2\pi 3000t)$ mA and $I_{B1} = 1$mA. Since the DC offset current will distort the output signal, a DC current of about 6μA was injected at the output of the OTA1 to adjust the offset to be less than ±0.1μA.

Similarly, a DC current of about 4μA was used to keep the offset current at the output of the circuit to be less than ± 0.1μA. The power supply voltages were set to Vcc = 10V and VEE = -10V.

The divider function was tested by inverting a triangular signal. The results obtained are show in Fig. 4 . Fig.4 show the simulated transient response of the circuit that function as a divider. The output current I_{OUT}, which in this case is an inverting function of a triangular signal, was simulated for i_{in1} = 100μA, i_{in2} = 300μA, and I_{B1} is a 500Hz triangular wave with amplitude of 100μA and DC component of equal to 200μA.

Fig.5 shows the simulated DC transfer characteristics for the multiplier function, where the bias currents were set to $I_{B1} = I_{B2} = I_{B3} = 1$mA. The figure shows the plot of the output current I_{OUT} against the input signal current i_{in1} from −1mA to 1mA and the input signal current i_{in2} from −1mA to 1mA with 0.5mA per step. The simulation and calculated data are agree very well over the ±0.8mA input range with an error of less than 0.1%. We can see large non-linearity for i_{in1} close 1mA this is due to that the voltage across the OTA1 is closed to the limited linear range. Fig.5 show the simulated transient response of the circuit that function as a divider. The output current I_{OUT}, which in this case is an inverting function of a triangular signal, was simulated for i_{in1} = 100μA, i_{in2} = 300μA, and I_{B1} is a 500Hz triangular wave with amplitude of 100μA and DC component of equal to 200μA Fig.6 shows the simulated frequency response of the circuit from the input i_{in1} to the output, with i_{in2} = 100μA and I_{B1} = 1mA. The response indicates that the circuit −3dB bandwidth is about 162 MHz that is close to the transistor f_T. The total harmonic distortion (THD) against input current, for the case that the input signal i_{in2} is a dc current, i_{in2} = 100μA and the input signal current $i_{in1} = 0.1\sin(2\pi 10000t)$ mA, is about 0.24% . On the other hand, when the input current i_{in1} is dc current, i_{in1} = 100μA, and the signal current $i_{in2} = 0.1\sin(2\pi 10000t)$ mA, the THD is about 0.39%

Fig.7. Shows the simulation result of the output current (I_{OUT}) due to the change of temperature for operating temperature variations from 0 °C to 100 °C. We set the input signal currents i_{in1} and i_{in2} as dc currents, where i_{in1} = 1000μA and i_{in2} = 60μA, where I_{OUT} = 60μA. From the figure, the output current varies only from 59.62μA to 61.38μA, for the temperature 0 °C to 100 °C respectively. This simulation result shows that the temperature dependence of transconductance gains g_{m1}, g_{m2} and g_{m3} of the bipolar OTAs are compensated.

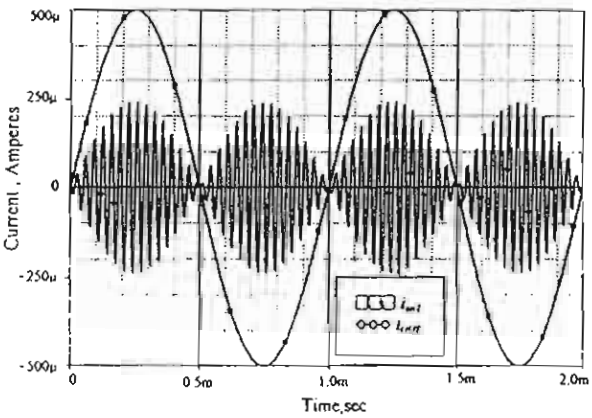

Fig. 3 Simulated transient response for the multiplier function.

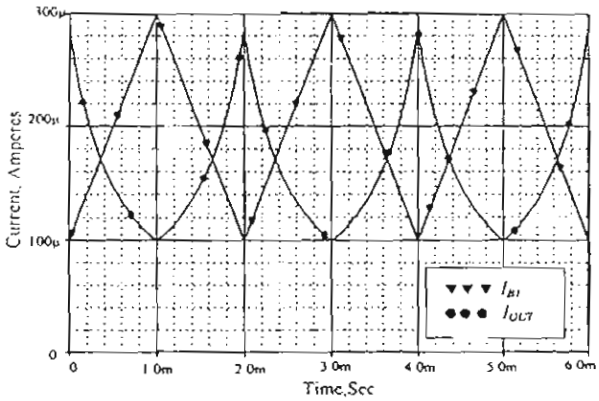

Fig. 4 Simulated transient response for the divider function.

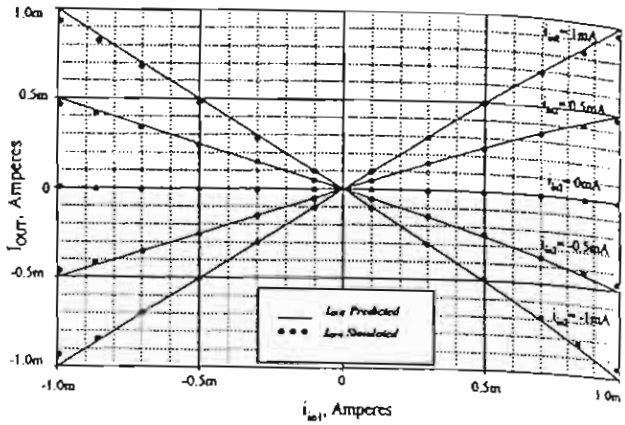

Fig. 5 Simulated DC transfer characteristic of the multiplier-divider.

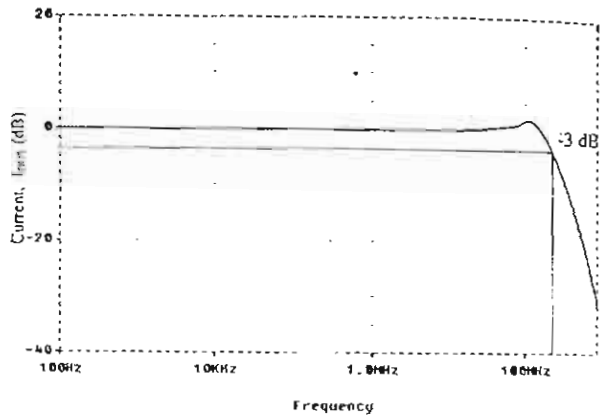

Fig. 6 Frequency response of current-mode multiplier-divider circuit using OTAs.

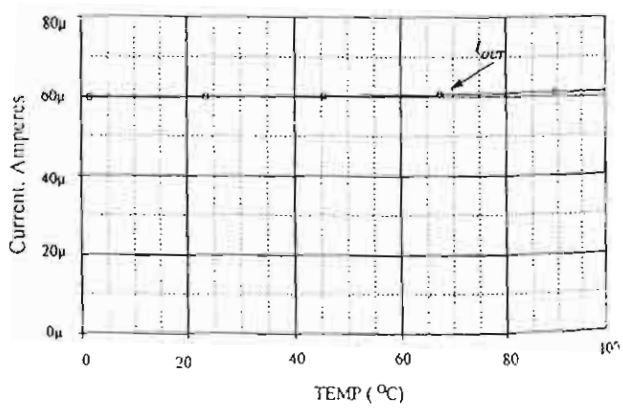

Fig. 7 Frequency response of current-mode multiplier-divider circuit using OTAs.

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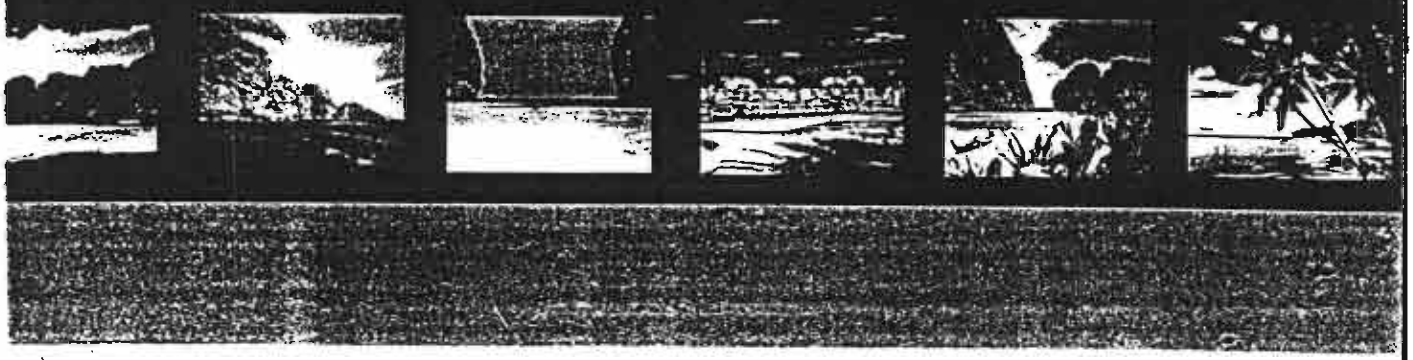

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Voltage-Mode CMOS Squarer/Multiplier Circuit

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Abstract: In this paper, a low-voltage CMOS squarer and a four-quadrant analog multiplier are presented. It is based on a source-coupled pair and a scaled-floating voltage generator which are modified to work as a voltage squaring and a sum/difference circuits. The proposed squarer/multiplier have been simulated with HSPICE, where $-3dB$ bandwidth of $10MHz$ is achieved. The power consumption is about $0.6mW$, from a $\pm 1.5V$ supply, and the total harmonic distortion is less than 0.7%, with a $1.2V$ peak-to-peak $1MHz$ input signal.

Introduction

A squarer circuit is an importance basic building block for the design of analog nonlinear function circuits, for examples, frequency translation, waveform generation, neural networks, and it can be applied to work as a quarter-square multiplier circuit. Usually, the common-source differential squaring circuit configuration as a two-input NOR gate with resistance load is widely used for the design of squarer/multiplier circuits in CMOS technologies [1]-[2]. The other approaches are that based on square-law current to voltage characteristics of MOS transistor which are biased in the saturatoin and nonsaturation region [3]-[9]. The squarer and multiplier proposed in this paper also use the square-law of the MOS transistor. But, however, the proposed circuit does not require resistors to obtain the output signal in voltage [10]

2. Circuit Description

2.1 MOS Differential Squaring Circuit

Fig. 1 shows the voltage-mode squaring circuit and its symbol which is made up of a differential-input source-coupled pair. Assuming that all NMOS devices are biased in the saturation region with individual wells connected to their sources to eliminate the body effect [3]. Let M_1 and M_2 are identical, and the aspect ratio of M_3 be twice that of M_1. If the differential-input voltage V_d, with the same common-mode dc voltage V_C is applied, the drain currents of MOS transistors can be expressed as

$$I_{d1} = K_1(V_C + \frac{V_d}{2} - V_o - V_T)^2 \quad (1)$$

$$I_{d2} = K_2(V_C - \frac{V_d}{2} - V_o - V_T)^2 \quad (2)$$

$$I_{d3} = K_3(V_o - V_{SS} - V_T)^2 \quad (3)$$

$$I_{d1} + I_{d2} = I_{d3} \quad (4)$$

where $K_i = \mu_n C_{ox} W_i / 2L_i$ is transconductance parameter, μ_n is the effective surface mobility, C_{ox} is the gate capacitance per unit area , and V_T is the threshold voltage of the transistor, respectively. The output voltage V_o becomes

$$V_o = \frac{(V_C - V_T)^2 - (V_{SS} + V_T)^2}{2(V_C - V_{SS} - 2V_T)} + \frac{V_d^2}{8(V_C - V_{SS} - 2V_T)} \quad (5)$$

The output voltage V_o is related to the square of the differential-input voltage V_d. The eqns. (1)-(5) are valid if $(V_C - V_{SS} - V_d/2) > 2V_T$, where all devices are biased in the saturation mode.

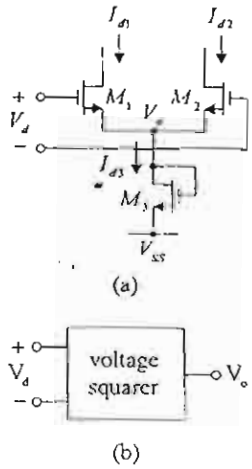


Fig. 1. Voltage-mode squaring circuit (a) circuit and (b) symbol.

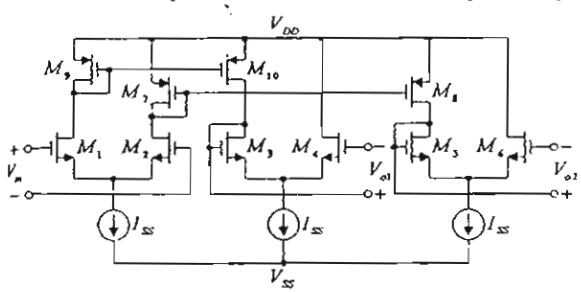
2.2 Scaled Differential-Voltage Generator

A circuit for generating differential-voltage generator is shown in Fig. 2 [8]. Matched transistor M_1 and M_2 form an input differential pair, while the other four identical NMOS devices, M_3, M_4 and M_5, M_6 form floating differential outputs that are biased by current sources I_{SS}

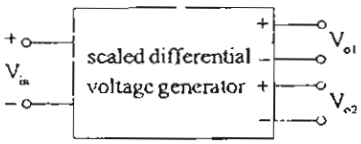
of the same magnitude. If voltage V_{in} is applied to the input, the output voltages V_{o1} and V_{o2} can be given by

$$V_{o1} = -V_{o2} = \sqrt{\frac{K_3}{K_1}} V_{in} \tag{6}$$

The output voltages is a scaled voltage which is equal to input voltage multiplied by a factor that is depend on transconductance parameter of the transistors M_3 and M_1



(a)



(b)

Fig. 2. Scaled differential-voltage generator (a) circuit and (b) its symbol.

2.3 Voltage-Mode Squaring Circuit

By combining the voltage squarer circuit and the scaled differential-voltage that shown in Fig. 1 and Fig.2, respectively, the block diagram of the voltage-mode squaring circuit is shown in Fig. 3, where the reference voltage V_{ref} is the constant dc voltage, V_{in} and V_o are the input and output voltage respectively. From eqns.(5)-(6) we find that

$$V_o = \frac{(V_{ref} - V_T)^2 - (V_{SS} + V_T)^2}{2(V_{ref} - V_{SS} - 2V_T)} + \frac{V_{in}^2}{2(V_{ref} - V_{SS} - 2V_T)} \tag{7}$$

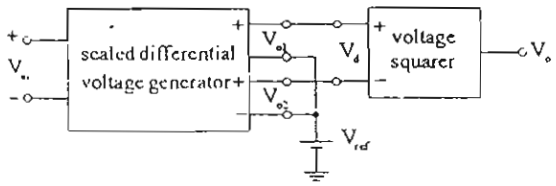


Fig. 3. Block diagram of the proposed squaring circuit.

The eqn.(7) shows that the output voltage V_o is equal to the square of the input voltage V_{in} and a factor which is in the form of the voltage reference V_{ref}. Then, we can adjust the output-offset voltage and the magnitude of V_{in}^2 by tuning V_{ref}.

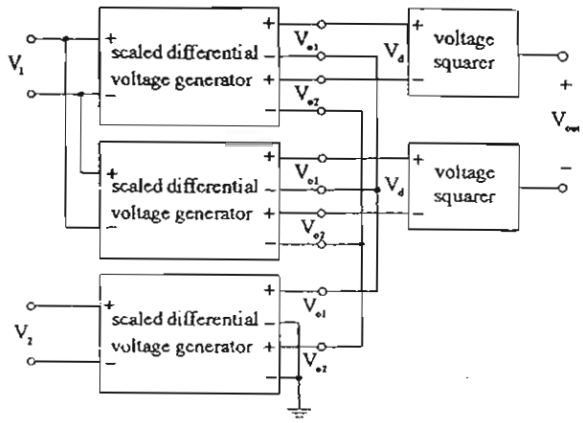


Fig. 4. Block diagram of the proposed multiplier.

2.4 Voltage-Mode Four-Quadrant Multiplier

Fig. 4 shows a block diagram of the four-quadrant analog multiplier that consists of three basic scaled differential-voltage generator and two voltage squarer, where V_1, V_2 and V_{out} are the input and output voltage of the multiplier, respectively. From the quarter-square algebraic identity $(V_1+V_2)^2-(V_1-V_2)^2 = 4V_1V_2$, therefore, the output voltage of the voltage-mode multiplier can be written as

$$V_{out} = \frac{(V_1+V_2)^2-(V_1-V_2)^2}{8(V_C - V_{SS} - 2V_T)}$$

$$= \frac{V_1V_2}{2(V_C - V_{SS} - 2V_T)} \tag{8}$$

The output voltage is equal to the multiplication of the two input voltage and a factor which is in the form of the common-mode dc voltage V_C and the power supply voltage V_{SS}. Consider the multiplier circuit block diagram in Fig. 4, if we set both the input voltages to zero, then V_C will be zero.

The channel length modulation, which causes the effective channel length, and thus the device W/L ratio, to be a function of the device drain-to-source voltage. However, this effect can be neglected if the long channel transistors are used.

3. Simulation Results

The proposed squarer/multiplier circuit have been simulated by HSPICE using the model parameters of HP 0.5μ level 49 CMOS process. For the voltage-mode squaring circuit that is shown in Fig. 1, the aspect ratios of transistors $M_1 - M_2$ are $5/5$, and M_3 is $10/5$. The ratios

of the devices of the scaled differential-voltage generator that is shown in Fig. 2, $M_1 - M_6$ and $M_7 - M_{10}$ are 5/10 and 20/5, respectively. The power supply voltage is $\pm 1.5V$ and the bias current I_{SS} is $20\mu A$.

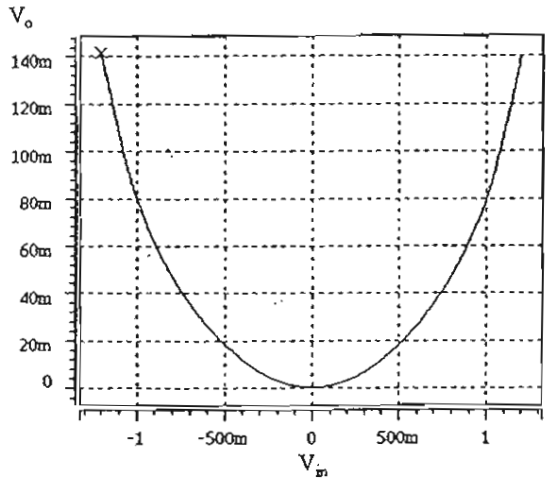


Fig. 5. The transfer characteristic curves of the squaring circuit.

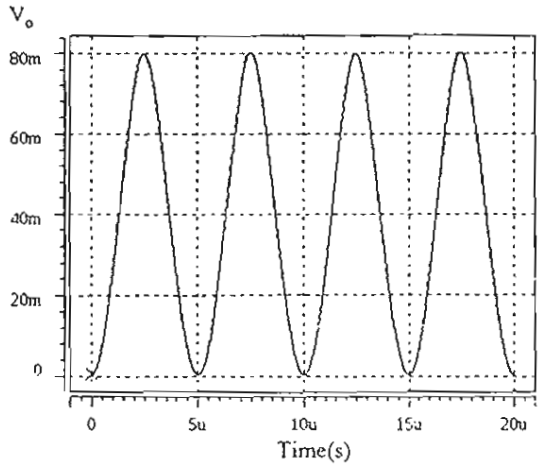


Fig. 6. The output waveform of the proposed squaring circuit

Fig.5 and Fig.6 show the simulations for the voltage-mode squaring circuit. The transfer characteristic curve is shown, where V_{in} is varied from $-1.2V$ to $1.2V$. The output signal shown in Fig.6 is measured by applying the sinusoidal input voltage V_{in} with peak amplitude of $1V$ and the frequency is $100kHz$.

The dc characteristic curves of the proposed multiplier are shown in Fig. 7, for the input voltage V_1 varied from $-0.6V$ to $0.6V$ and V_2 changing from $-0.6V$ to $0.6V$ with $200mV$ steps.

Fig.8 demonstrates the use of this multiplier as an amplitude modulator, a $100kHz$ sine wave is modulated by $2MHz$, where the amplitude of the signals are $500mV$

The total harmonic distortion is measured by setting V_2 to $600mV$ dc voltage. V_1 is the sinusoidal signal with peak amplitude of $600mV$ and the frequency is $1MHz$. The simulated maximum THD is about 0.7%, and the power consumption is about $550\mu W$.

To measure the frequency characteristic of the multiplier, a $600mV$ dc voltage is applied to V_2 while V_1 is the variable frequency sinusoidal input current with peak amplitude of $600mV$. From the simulation, the $-3dB$ bandwidth up to $10MHz$ is achieved.

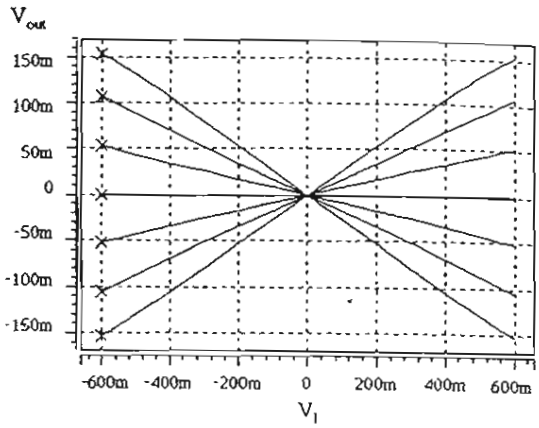


Fig. 7. The transfer characteristic curves of the multiplier

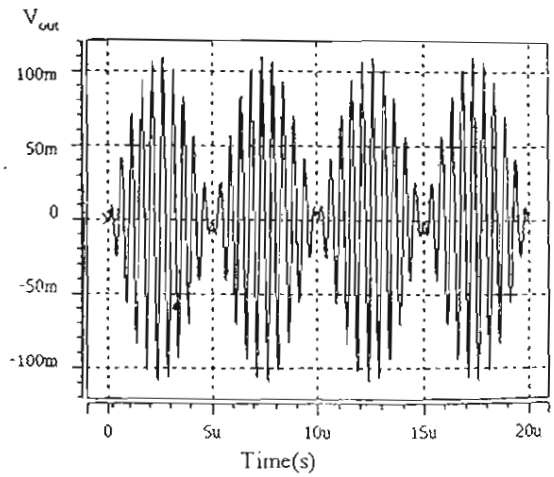


Fig. 8. Amplitude modulation of the two sinusoidal input signals

4. Conclusion

A new CMOS voltage-mode squarer and four-quadrant analog multiplier base on the differential-input source-coupled pair and scaled differential-voltage generator have been presented. To obtain the output voltage, the proposed circuits are performed by using the voltage-mode squaring circuits which does not require a resistor. There performances have been demonstrated by using HSPICE simulations.

Phuket

ITC-CSCC 2002

ITC-CSCC 2002

The 2002 International Technical Conference On Circuits/Systems, Computers and Communications

Proceedings

Volume

Phuket Arcadia Hotel & Reso
Phuket, Thailand

July 16-19, 2002

Co-Sponsored by
Sirindhorn International Institute of Technology, Thammasat University, Thailand
King Mongkut's University of Technology Thonburi, Thailand
National Electronic and Computer Technology Center, Thailand
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With Technical Cooperation of
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Current-Mode Integrator using OA and OTAs and Its Applications

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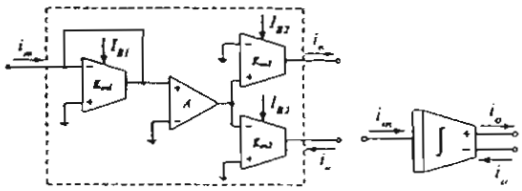
Abstract: A circuit building block for realizing a continuous-time active-only current-mode integrator is presented. The proposed integrator is composed only of internally compensated type operational amplifier (OA) and operational transconductance amplifiers (OTAs). The integrator is suitable for integrated circuit implementation in either bipolar or CMOS technologies, since it does not require any external passive elements. Moreover, the integrator gain can be tuned through the transconductance gains of the OTAs. Some application examples in the realization of current-mode network functions using the proposed current-mode integrator as an active element are also given.

1. Introduction

In the last decade, the realizations of various active circuits utilizing the operational amplifier (OA) pole have received considerable attention for their potential advantages such as attractive for monolithic IC integration, ease to design, and suitable for high frequency operation [1-2]. Several OA-based active-R capacitor-less circuits for realizing analog transfer functions have been reported [3-4]. Presently from the above reasons, there is the strong motivation to design resistor-less and capacitor-less filter circuits utilizing the finite and complex gain natures of internally compensated OAs and OTAs. Due to the active only nature, the resistor-less and capacitor-less active filter would be attractive for its integratability, programmability and wide frequency range of operation. Many implementations in active-only filter design are available in the literature [5-7].

It is well-known fact that an integrator is an important circuit building block, which are widely used in analog signal processing applications, such as, filter design, waveform shaping, process controller design, and calibration circuit, etc. However, the implementation of a continuous-time current-mode integrator that employs only active elements has not yet been reported. Therefore, a circuit configuration for realizing active-only current-mode integrator is proposed in this paper. The proposed integrator consists of one OA and two OTAs. Since no passive element is required, the integrator can be implemented in integrated circuit form in both bipolar and CMOS technologies. The integrator gain can be electronically tuned by adjusting the transconductance gains of the OTAs. The various realizations of active-only analog signal processing circuits employing the proposed integrator will also be presented. Finally, the workabilities of the proposed integrator and its applications have been simulated based upon a LM741 type IC OA and a CA3080 type IC OTA.



(a) (b)

Fig.1 : The proposed active-only current-mode integrator (a) circuit implementation (b) circuit representation

2. Circuit Description

The proposed active-only dual-output current-mode integrator implementation and its representation are shown in Fig.1. It consists of only an OA and OTAs, where the dual-current-output OTA2 is implemented by using single-ended output OTAs in parallel connection [8]. If ω_o is the 3-dB bandwidth of the OA and by considering the OA for the frequencies $\omega >> \omega_o$, the open-loop gain $A_{OA}(s)$ of the OA can be approximately given by

$$A_{OA}(s) = \frac{A_o\omega_o}{s+\omega_o} \approx \frac{B}{s} \qquad (1)$$

where B represents the gain-bandwidth product (GBP) of the OA, which is the product of the dc gain A_o and the 3-dB bandwidth ω_o. Let assume that g_{m1} and g_{m2} denote the transconductance gains of the OTA1 and OTA2, respectively, then the current transfer function of the current-mode integrator can be expressed as:

$$\frac{I_o(s)}{I_{in}(s)} = \frac{B}{s}\left[\frac{g_{m2}}{g_{m1}}\right] = \frac{B}{s}A_G \qquad (2)$$

where A_G denotes the integrator gain, which is the ratio between g_{m2} and g_{m1}. Eqn.(2) indicates that the relationship of the currents I_o and I_{in} is in the form of the integrating

action as required. It should be noted that, for ordinary bipolar OTAs, $g_{m1} = I_{B1}/2V_T$ and $g_{m2} = I_{B2}/2V_T$, where V_T is the thermal voltage and I_{B1} and I_{B2} are the bias currents of the OTA1 and OTA2, respectively. Thus, eqn.(2) becomes

$$\frac{I_o(s)}{I_{in}(s)} = \frac{B}{s}\left[\frac{I_{B2}}{I_{B1}}\right] = \frac{B}{s}A_G \qquad (3)$$

Now A_G is the current gain that is the bias current ratio between I_{B2} and I_{B1}. In this case, the temperature dependence of the transconductance gains g_{m1} and g_{m2} of the bipolar OTAs are also compensated.

Deviation from the ideal performance that predicted from the eqn.(2) is due to the parasitic effects of the non-ideality characteristics of the OA and OTAs. If the second dominant pole ω_b of the OA is taken for consideration, the OA open-loop gain $A_{OA}(s)$ can be rewritten by

$$A_{OA}(s) = \frac{B}{s}\frac{\omega_b}{(s+\omega_b)} = \frac{B}{s}\frac{1}{(1+\tau_b s)} \qquad (4)$$

where $\tau_b = 1/\omega_b$. For the OTAs, let $\omega_c = 1/\tau_c$ represents the effective transconductance internal-pole of the OTA and g_{m0} is the low frequency transconductance gain. The OTA open-loop gain $g_m(s)$ for general case can be described by

$$g_m(s) = \frac{g_{m0}}{\left(1+s/\omega_c\right)} \cong g_{m0}\left(1-s/\omega_c\right) \qquad (5)$$

Therefore, the frequency response of the current-mode integrator in Fig.1 that including the second dominant pole of the OA and the transconductance internal-poles of the OTAs can now be given by

$$\frac{I_o(s)}{I_{in}(s)} = \left[\frac{B}{s}\right]\left[\frac{1}{1+\tau_b s}\right]\left[\frac{g_{m02}}{g_{m01}}\right]\left[\frac{\omega_{c2}-s}{\omega_{c2}}\right]\left[\frac{\omega_{c1}}{\omega_{c1}-s}\right] \qquad (6)$$

where ω_{c1} and ω_{c2} are the effective transconductance internal-poles of the OTA1 and OTA2, respectively. It can be seen that if the conditions ($\omega_{c1} \cong \omega_{c2}$) and ($\omega_{c1}, \omega_{c2} >> \omega$) are satisfied, then eqn. (6) becomes frequency independent. Let us define that $A_{G0} = g_{m02}/g_{m01}$ is the dc integrator gain, as a result, it can be reasonably reduced to

$$\frac{I_o(s)}{I_{in}(s)} = \left[\frac{A_{G0}B}{s}\right]\left[\frac{1}{1+\tau_b s}\right] \qquad (7)$$

One can see that the frequency characteristic of the proposed current-mode integrator has a dc current gain equaled to eqn.(2) and has a high frequency dominant pole located at ω_b. Hence, the OA pole ω_b should be the major high-frequency limitation of the proposed current-mode integrator

3.Application examples

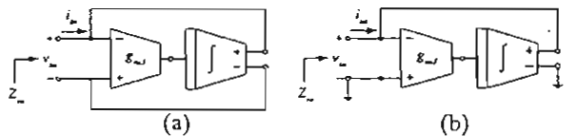
The following sections will concentrate on the usefulness of the proposed current-mode integrator. Some application examples to realize driving-point impedance function elements, current-mode biquadratic filter and current-mode nth-order filter will be demonstrated.

3.1. Inductance simulations

Fig. 2(a) shows the circuit diagram of a tunable floating inductance simulation. From this circuit, it can easily be shown that the value of the floating simulated inductance is

$$L_{eq} = \left[\frac{1}{g_{m3}A_G B}\right] \qquad (8)$$

It should be noted that the equivalent inductance L_{eq} can properly be tuned by electronic means through the current ratio A_G and/or the transconductance gain g_{m3}. In addition, the circuit in Fig.2(a) can easily be modified to simulate a grounded inductor by replacing the dual-output OTA2 with the single-output OTA2 as shown in Fig.2(b).



(a) (b)

Fig.2 : Active-only inductance simulations

3.2. Electronically tunable active-only current-mode biquadratic filter

Fig.3 shows the circuit diagram of the tunable current-mode filter based on the use of the proposed current-mode integrator, where i_{LP}, i_{BP}, and i_{HP} are the lowpass, bandpass and higpass current-output terminals, respectively. The circuit parameters ω_o and Q-factor of this filter can be written by

$$\omega_o = \sqrt{A_{G1}A_{G2}B_1B_2} \qquad (9)$$

and

$$Q = \frac{g_{mc}}{g_{md}}\sqrt{\frac{A_{G2}B_2}{A_{G1}B_1}} \qquad (10)$$

One can see that the filter also enjoys orthogonal tuning of ω_o and Q-factor via the transconductance gains of the OTAs and it's also temperature independent.

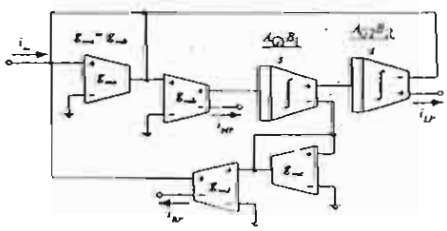


Fig.3 : Active-only current-mode biquadratic filter

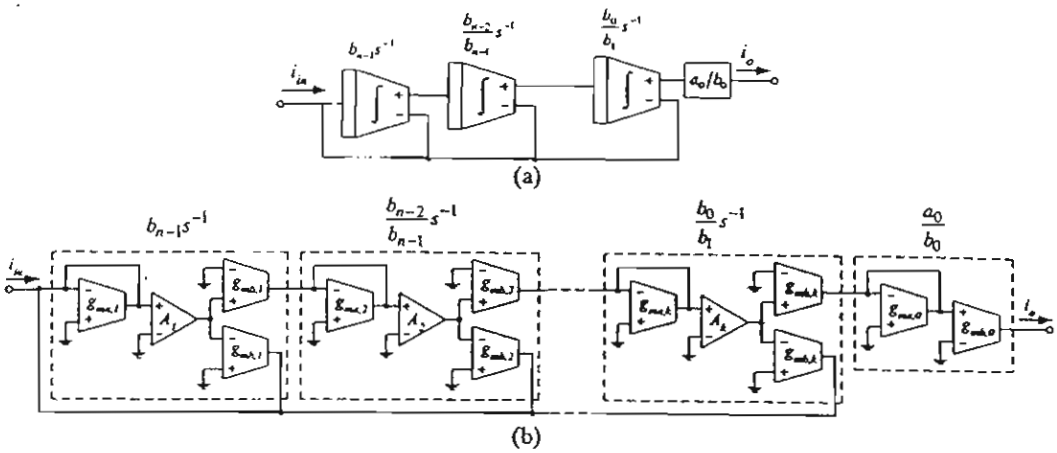


Fig.4 : (a) nth-order current-mode filter representation
(b) nth-order current-mode filter realization using only active elements

3.3 nth-order current-mode filters

The standard current transfer function of an nth-order lowpass filter is often expressed as the following form :

$$\frac{I_o(s)}{I_{in}(s)} = \frac{a_0}{s^n + b_{n-1}s^{n-1} + \ldots + b_1 s + b_0} \qquad (11)$$

One can straightforwardly realize the nth-order current transfer function of equation (11) by cascading the proposed current-mode integrator of Fig.1. The system diagram thus obtained can be shown in Fig.4(a) and the coefficient of the standard function in terms of the circuit parameters can be expressed as follows :

$$b_{n-1} = A_{G1}B_1 \quad ; \quad A_{G1} = \frac{g_{mb,1}}{g_{ma,1}} \qquad (12)$$

$$\frac{b_{n-k}}{b_{n-1-k}} = A_{Gk}B_k \quad ; \quad A_{Gk} = \frac{g_{mb,k}}{g_{ma,k}} \qquad (13)$$

and

$$\frac{a_0}{b_0} = \frac{g_{mb,0}}{g_{ma,0}} \qquad (14)$$

where A_{Gk} and B_k represent the current gain and GBP of the k-th integrator (for k = 2, 3, ... , n). For this implementation, n active-only current integrators and two additional transconductance elements that employed for realizing the output proportional gain block ($g_{mb,0}/g_{ma,0}$) are required. Fig.4(b) shows the nth-order current-mode filter realization based on the use of only active components. In addition, if coefficients a_0 and b_0 are equaled, then two additional transconductance elements will also be eliminated.

4. Design examples and Simulation results

In order to verify the theoretical study of the proposed current-mode integrator, PSPICE simulation results are included. In this simulation, the OTA is modeled by employing CA3080 type OTA with a macro model [8] and LM741 type OA with the gain-bandwidth product B = 5.906 Mrad/s is used [5]. Fig.5 shows the simulated frequency responses of the proposed current-mode integrator. The results show that the circuit acts as an integrating function with a slope -20 dB per decade for the frequency range from 10 Hz to 1 MHz and has less than 10% phase error from the frequency range of 30 Hz to 500 kHz.

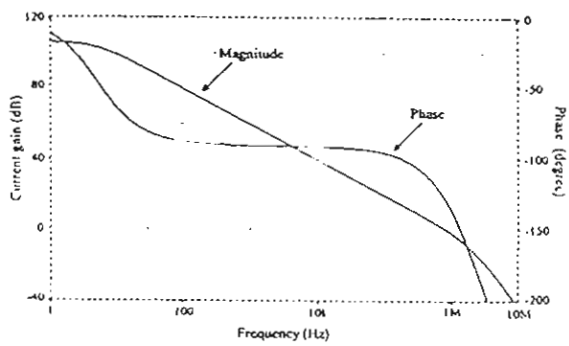
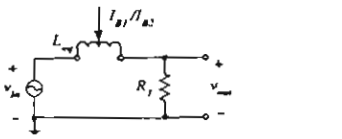


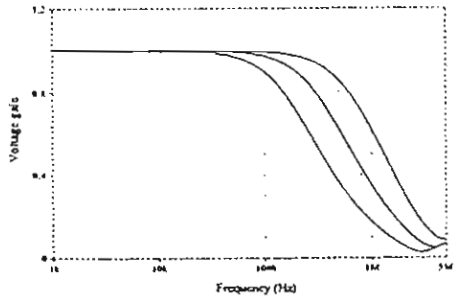
Fig.5 : Frequency responses of the proposed integrator

The performance of the floating inductance circuit of Fig.2(a) is demonstrated through the use of an electronically tunable active RL low-pass filter in Fig.6(a) with the external resistor R_1 = 1 kΩ. The bias current ratio $A_G = I_{B2}/I_{B1}$ (= g_{m2}/g_{m1}) is set to 0.5, 1 and 2, while g_{m1} and g_{m3} are respectively set to constant at 1 mS and 0.4 mS ; thus the cut-off frequencies f_C are approximately equal to 200 kHz, 400 kHz and 800 kHz, respectively. The frequency responses of the low-pass filter are shown in Fig.6(b).

Fig.7 shows simulated responses of the tunable current-mode multifunctional filter of Fig.3, when $A_{G1} = A_{G2} = 0.05$ and $g_{mc}/g_{md} = 0.1$. This filter is designed for $\omega_o/2\pi$ = 50 kHz at the unity Q-factor. All the simulated results shown above imply that the proposed integrator exhibit reasonably good agreement with the predicted values.



(a)



(b)

Fig.6 : (a) first-order RL lowpass filter
(b) frequency responses of the simulated RL lowpass filter

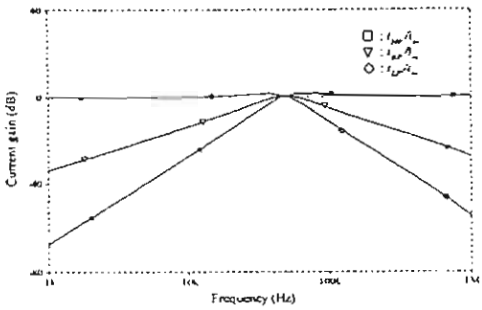


Fig.7 : Simulated frequency response of current-mode filter of Fig.3

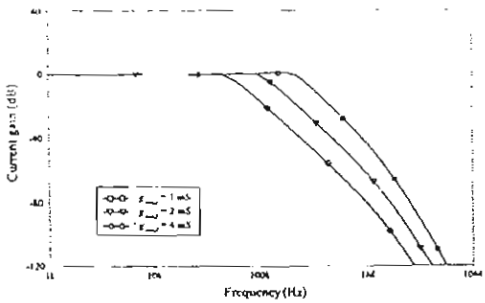


Fig.8 : Simulated frequency response of nth-order current-mode filter of Fig.4

To illustrate the current-mode filter using all active elements of Fig.4(b), a design of a third-order Butterworth filter with a cut-off frequency of 100 kHz is an example. The normalized transfer function for this filter can be written by

$$\frac{I_o(s)}{I_{in}(s)} = \frac{1}{s^3 + 2s^2 + 2s + 1} \qquad (15)$$

The active-only filter realization based on the circuit of Fig.4 is constructed, in which the transconductance elements $g_{ma,0}$ and $g_{mb,0}$ will be eliminated due to the coefficient values a_0 and b_0 equal to unity. Thus, by calculating the circuit parameters we obtain : $g_{mb,1}$ = 0.424 mS, $g_{mb,2}$ = 0.212 mS and $g_{mb,3}$ = 0.106 mS, while $g_{ma,i}$ (i = 1, 2, 3) are set equal to 2 mS. In addition, the values of $g_{ma,i}$ can be used to change the cut-off frequency. The simulated frequency responses are shown in Fig.8 that exhibit reasonably close agreement with theoretical results. It is also shown that the cut-off frequency can be tuned electronically through adjusting the transconductance gains ($g_{ma,1} = g_{ma,2} = g_{ma,3}$).

5. Conclusions

This paper presented an alternative scheme for realizing continuous-time active-only current-mode integrator. The proposed integrator is realizable with only internally compensated type OA and OTAs, and does not require any external passive elements. Because of their active-only nature, the integrator can be easily employed to realize active network functions and are suitable for implementing in monolithic integrated form in both bipolar or CMOS technologies. Since the proposed circuit utilizes an OA pole, it is also suitable for high frequency operation. The simulated results have been used to verify the theoretical analysis.

6. Acknowledgment

This work is partly funded by the Thailand Research Fund (TRF) under the Senior Research Scholar Program, grant number RTA/04/2543. The support provided by the Japan International Cooperation Agency (JICA) is also acknowledged.

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Proceedings

Volume 2

Phuket Arcadia Hotel & Resor
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Design of a Current-Mode CCII-Based Bandpass Filter from Immittance Function Simulator using Commercial Available CCII (AD844)

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Abstract: This paper proposes the design of a current-mode CCII-based 2nd-order bandpass biquad filter from a grounded series capacitor and frequency-dependent negative conductor (C-D) immittance function simulator using the macro model of a commercial available CCII+, AD844, from Analog Devices,Inc. The results are compared with the other results those are designed using ideal model of CCII-. The gain and phase deviations; due to the effects of passive sensitivity, active sensitivity, gain sensitivity and component variability; are considered using Monte-Carlo analysis of PSpice program.

1. Introduction

CCII has been proposed since 1970 by A. Sedra and K.C. Smith [1]. Now, it is a famous and versatile current-mode device. One important class of its application is continuous-time filter. Filter can be designed by many methods. One method uses immittance function simulator [2-5]. But the method proposed by T. Sattaya-aphitan,et. al. [6] uses less components, component matching is not required and more generalized method than the previous papers. Nevertheless, they use ideal model of CCII-.

Nowadays, there are only CCII+ in the market. We must use 2-CCII+ connected in cascade to form CCII-. The real characteristics of CCII+ and CCII- are not exactly the same as the ideal cases. In this paper, we use off-the-shelf integrated circuit no. AD844 of Analog Devices,Inc. functions as CCII+, and use macro model [7] in design a current-mode 2nd-order bandpass biquad filter from a grounded series capacitor and frequency-dependent negative conductor (C-D) immittance function simulator.

2. Theory

2.1 CCII ±

In general, the characteristic of an ideal second generation current conveyor (CCII) is given by the following hybrid matrix :

$$\begin{bmatrix} i_Y \\ v_X \\ i_Z \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ 1 & 0 & 0 \\ 0 & \pm 1 & 0 \end{bmatrix} \begin{bmatrix} v_Y \\ i_X \\ v_Z \end{bmatrix} \quad (1)$$

+1 in equation(1) is referred to CCII+ and −1 is referred to CCII-. All currents go into the terminals of CCII+.

The macro (or real) model of AD844 functions as CCII+ is shown in figure 1.

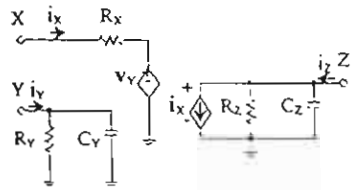

Figure 1. Macro model of AD844.

Where $R_X = 50\ \Omega$, $R_Y = 10\ M\Omega$, $R_Z = 3\ M\Omega$, $C_Y = C_Z = 4.5$ pF. The two-cascaded AD844 functions as CCII- is shown in figure 2.

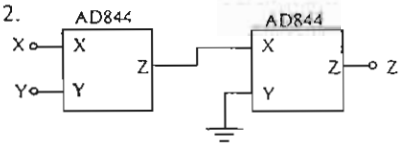

Figure 2. AD844 implementation as CCII-.

2.2 Grounded Series Immittance Function Simulator

The grounded series immittance function simulator [6] is shown in figure 3 and its input impedance is shown in equation (2).

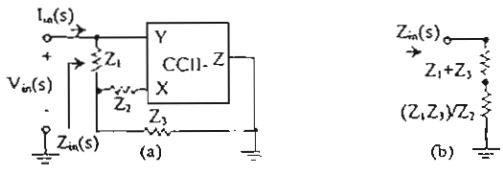

Figure 3. (a) Grounded series immittance function simulator.

(b) Equivalent circuit.

$$Z_{in}(s)=\frac{1}{Y_{in}(s)}=\frac{V_{in}(s)}{I_{in}(s)}=Z_1+Z_3+\frac{Z_1Z_3}{Z_2} \quad (2)$$

Given $Z_1 = 1/sC_1$, $Z_2 = R_2$ and $Z_3 = 1/sC_3$. We obtain the grounded series C-D immittance function as shown in equation (3).

$$Z_{in}(s)=\frac{1}{sC_{eq}}+\frac{1}{s^2D_{eq}} \quad (3)$$

where $C_{eq} = C_1C_3/(C_1+C_3)$ and $D_{eq} = C_1C_3R_2$
which D_{eq} = equivalent frequency-dependent negative conductance (FDNG)

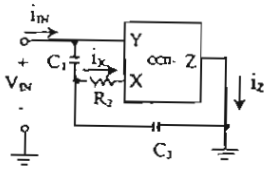

Figure 4. Grounded series C-D immittance function simulator.

We substitute the macro model of AD844 of figure 1 into the blocks of figure 2, after that, substitute it in CCII- of figure 4. We will obtain the input admittance as shown in equation (4) below.

$$Y_{in}(s)=\frac{I_{in}(s)}{V_{in}(s)}=\frac{As^2+Bs+C}{Ds+E} \quad (4)$$

where

$$A=C_1C_3+C_1C_Y+C_3C_Y+C_1C_YG_2R_X+C_3C_YG_2R_X+C_1C_3G_2R_X$$
$$B=C_1G_Y+C_YG_2+C_3G_Y+C_1G_2G_YR_X+C_3G_2G_YR_X$$
$$C=G_2G_Y$$
$$D=C_1+C_3+C_1G_2R_X+C_3G_2R_X$$
$$E=G_2$$

3. The Practical Bandpass Filter

We construct the practical bandpass filter as shown in figure 5 and the obtained current-mode bandpass transfer function is shown in equation (5).

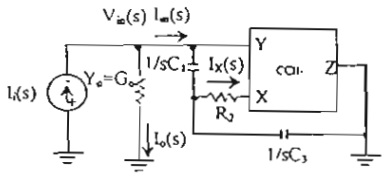

Figure 5. The practical bandpass filter.

$$T_{BP}(s)=\frac{I_o(s)}{I_i(s)}=\frac{K\frac{\omega_p}{Q_p}s}{s^2+\frac{\omega_p}{Q_p}s+\omega_p^2} \quad (5)$$

where $\omega_p=\sqrt{(C+EG_o)/A}=\omega_0$ (for BP filter)

$$Q_p=\sqrt{A(C+EG_o)}/(B+DG_o)$$
$$K=-C_3G_2/(B+DG_o)$$

4. Simulation Results

We use PSpice program as the tool for simulation. First, given $C_1 = C_3 = 22.5$ pF, $R_2 = 5$ kΩ and $R_o = 10$ kΩ. The gain and phase responses are shown in figure 6 and important data are shown in table 1.

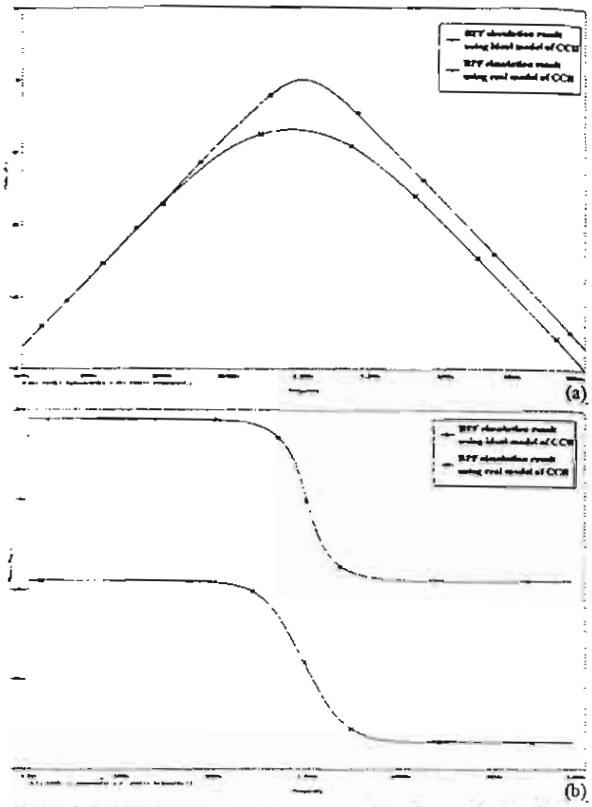

Figure 6. Uncompensated BP filter vs ideal-model BP filter.

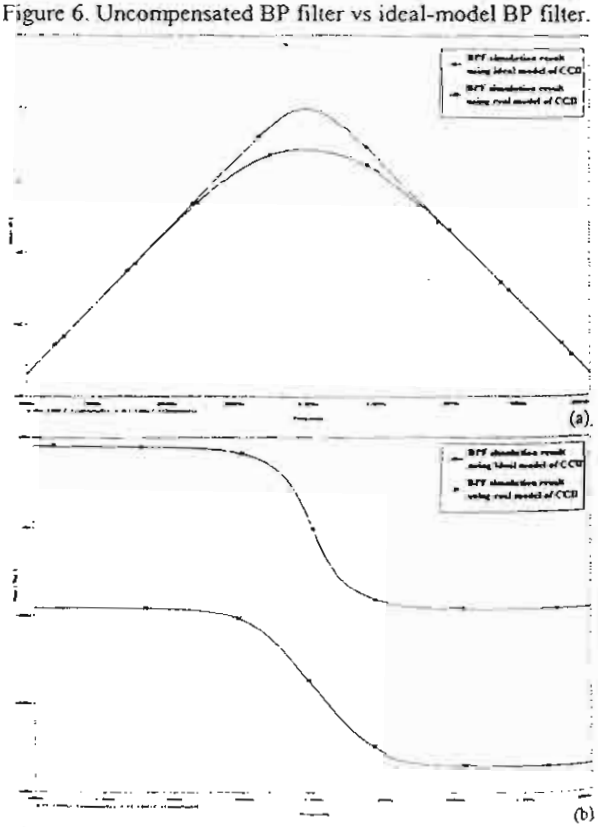

Figure 7. Compensated BP filter vs ideal-model BP filter.

Table 1. Bandpass filter characteristics of figure 6.

	BPF using ideal model of CCII-	BPF using real model of CCII-
f_0 = center frequency	1.0 MHz	833.28 kHz
Lower and upper cutoff frequency (f_1 and f_2)	515 kHz and 1.93 MHz	284 kHz and 2.48 MHz
Bandwidth (BW)	1.415 MHz	2.196 MHz
Quality factor (Q)	0.707	0.38
Gain at f_0 (dB)	75.04n	-6.89

Second, given $C_1 = C_3 = 22.5$ pF, $R_o = 10$ kΩ and adjust R_2 to be 3.5 kΩ. The gain and phase responses of the compensated BP filter are shown in figure 7 and important data are shown in Table 2.

Table 2. Bandpass filter characteristics of figure 7.

	BPF using ideal model of CCII-	BPF using real model of CCII-
f_0 = center frequency	1.0 MHz	1.0 MHz
Lower and upper cutoff frequency (f_1 and f_2)	515 kHz and 1.93 MHz	330 kHz and 3 MHz
Bandwidth (BW)	1.415 MHz	2.67 MHz
Quality factor (Q)	0.707	0.375
Gain at f_0 (dB)	75.04n	-5.62

If all values of components in the model of CCII- are changed within ±1%, the gain and phase deviations are shown in figure 8 and table 3.

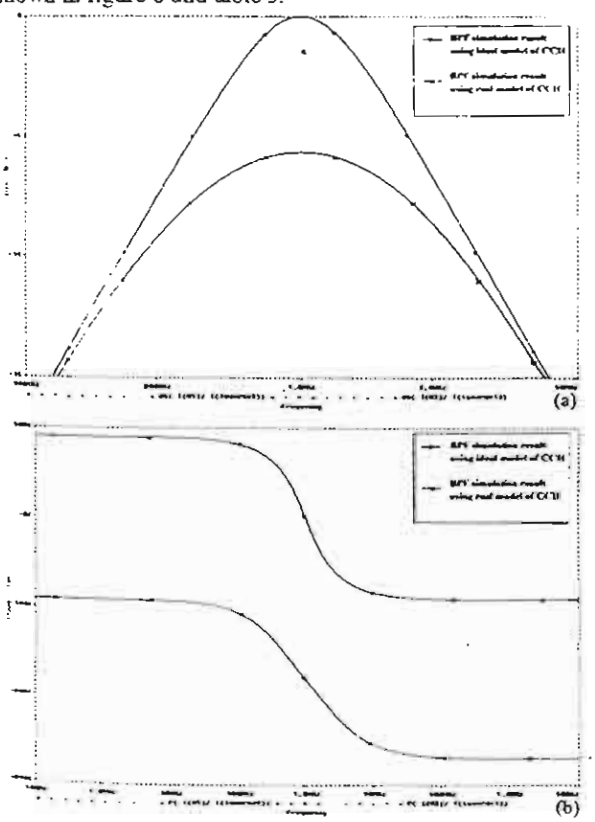

Figure 8. Gain and phase deviations due to active devices

If all values of other passive components are also changed within ±1%, the gain and phase deviations are shown in figure 9 and table 3.

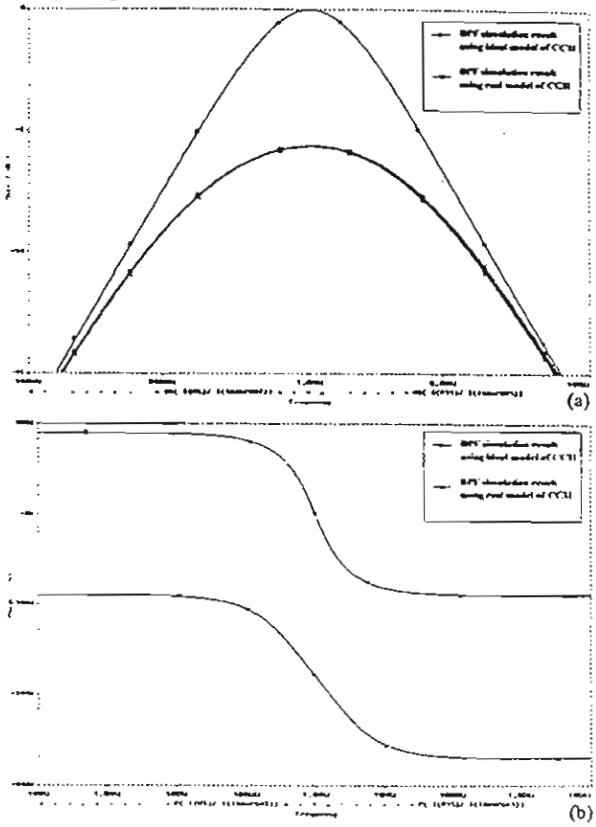

Figure 9. Gain and phase deviations due to passive elements.

Table 3. ΔG and Δϕ at lower and upper cutoff frequency and at center frequency.

(a) Due to active elements only.

frequency	330 kHz	1 MHz	3 MHz
ΔG (dB)	0.0046	0.0139	0.0281
Δϕ (degree)	0.061	0.093	0.096

(b) Due to passive elements only.

frequency	330 kHz	1 MHz	3 MHz
ΔG (dB)	0.1155	0.0779	0.1878
Δϕ (degree)	0.666	0.785	0.818

(c) Due to both active and passive elements .

frequency	330 kHz	1 MHz	3 MHz
ΔG (dB)	0.1317	0.636	0.1041
Δϕ (degree)	0.708	0.78	0.64

If all values of active devices and passive elements are changed within ±1%, the gain and phase deviations are shown in figure 10 and table 3.

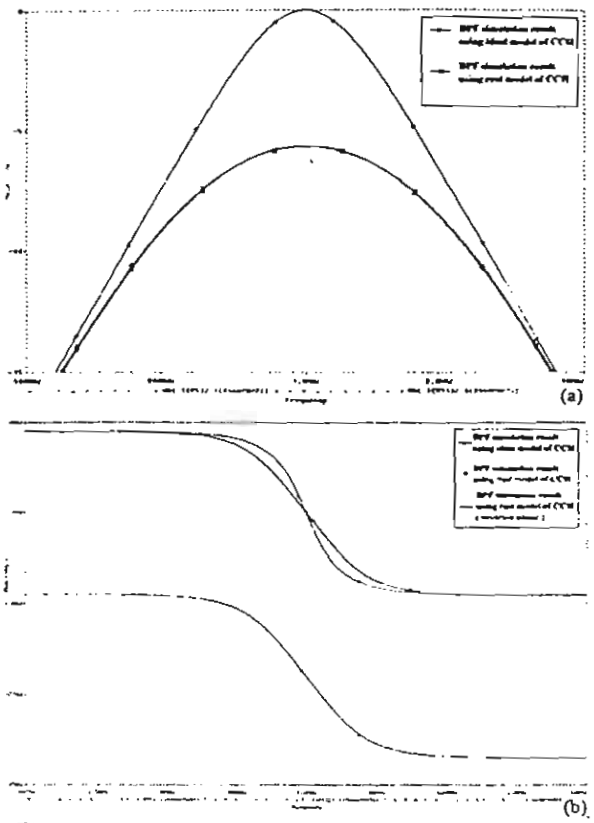

Figure 10. Gain and phase deviations due to all elements.

5. Discussion & Conclusion

Real model of commercial CCII- (2-cascaded AD844) causes the gain and phase responses deviate from the responses of the prototype that uses ideal model of CCII-, although we use the same values of passive components.

We can see the effect in figure 6 that we call "uncompensated BP filter". The phase response is shifted about 180° for all frequency range.

After trying to adjust all components and observed the effects that happened. We found that it will give the best results when adjust R_2 only. The results is shown in figure 7 that we call "compensated BP filter". Nevertheless, the phase response is still shifted about 180° for all frequency range.

The right way to correct the phase response is to use 180°-phase shifter at the source or at the output.

In this design, we use Butterworth approximation for the clear picture of graphs.

There are still deviations both gain and phase responses around center frequency due to the effects of nonidealities of the real CCII-.

The effects of passive sensitivity, active sensitivity, gain sensitivity and component variability to the gain and phase deviations are very small. We can observe the effects in the graphs of figure 8 to figure 10 and table 3.

i_X is drawn from the BP filter by wide band current amplifier and is transmitted to a load.

If we break terminal Z from ground to draw current i_Z instead of i_X as the output current, the responses are not as good as we do because of the effect of R_Z and C_Z.

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Acknowledgement

This work is partly funded by the Thailand Research Fund (TRF) under the Senior Research Scholar Program, grant number RTA/04/2543. The support provided by the Japan International Cooperation Agency (JICA), the Japan Society for the Promotion of Sciences (JSPS), and King Mongkut's University of Technology Thonburi are also acknowledged.

Besides, the authors would like to thank Miss Trungjai Tangsakul, Mr. Parinya Disomtetiwatana, Mr. Pantin Nantajiwakornchai, Mr. Rangsan Chaisrichareon, Mr. Seksan Mathulaprung-san, Mr. Tanya Sattaya-aphitan, Associate Professor Dr. Booncharoen Sirinaovakul, and Associate Professor Dr. Kobchai Dejhan for their support.

Proceedings

2002 IEEJ International Analog VLSI Workshop

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Dual Translinear Loop Multi-Output FTFN

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ABSTRACT

An alternative implementation scheme of a multi-output four-terminal floating nullor (FTFN) using dual translinear loops in BiCMOS technology is proposed. This presented circuit is simple and realized by base on the advantages of dual translinear loop cell circuit that comes up with high gain and wide bandwidth. The negative impedance is inserted between translinear loops to compensate the parasitic elements. The circuit performances are confirmed through HSPICE simulations. A current-mode low-pass filter and current-mode inverse low-pass filter with 10 MHz cut-off frequency are determined to exhibit the potentiality of this proposed scheme.

Keywords: Translinear, Multi-output, FTFN, Current-mode Filter

1. Introduction

In recent, there are many attempts to design a high performance four-terminal floating nullor (FTFN), which has been stood out as a more flexible and versatile than the other building blocks [1] - [4], especially in current-mode circuits. This paper shows another way to realize an integrable multiple-output FTFN in BiCMOS technology, which offers higher gain and wider bandwidth.

Since many FTFNs are usually implemented by using the conventional op-amp with a supply current sensing method, which are suffering from the critical limitation of op-amp itself and ungeneralized feedback path caused from using the cross-coupled current mirrors [1] - [2]. Translinear implementation, in contrast, allows the design of high performance circuits that provide both extended bandwidth and high thermal stability [5] - [6].

In addition, the number of output ports can be easily expanded to support the designer applications. It has been specified in the literature that an inappropriate implementation of the nullor can lead to errors in the realization of inverse filter [8]. Therefore, the current-mode low-pass and inverse low-pass filters are adopted to demonstrate the performance of this proposed circuit.

2. Basic Theory

2.1 Multi-Output FTFN

FTFN is an active device that equivalent to an ideal nullor, which can imply to be a high gain transconductance amplifier with floating characteristic at input and output terminals. Fig. 1(a) shows a nullor model of an FTFN that can be described by its port relation in matrix form as:

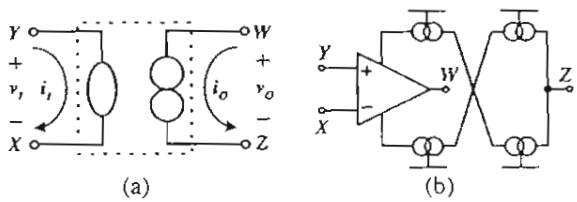

Fig. 1. (a) A nullor model (b) traditional implementation.

$$\begin{bmatrix} v_I \\ i_I \end{bmatrix} = \begin{bmatrix} 0 & 0 \\ 0 & 0 \end{bmatrix} \begin{bmatrix} v_O \\ -i_O \end{bmatrix} \quad (1)$$

This mean the differential voltage across and the current feed through the input port are both zero. Moreover, the output properties are arbitrary without any restriction to input signal[9].

One of the most famous realisation techniques is built up from a basic type shown in Fig. 1 (b) [1] - [2]. It is using one op-amp and supply current sensing technique, where the output impedance of the port W is very low and the impedance of the port Z is very high.

The multi-output idea can be easily applied to the original FTFN by adding the new output terminals as shown in Fig. 2, where its characteristics can be

pointed out by the matrix

$$\begin{bmatrix} v_X \\ i_Y \\ i_{Zn} \end{bmatrix} = \begin{bmatrix} 0 & 1 & \cdot \\ 0 & 0 & 0 \\ 0 & 0 & -1 \end{bmatrix}$$

where n = 1, 2, 3, ... is number of the ou

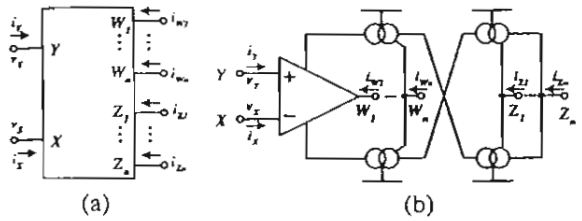

Fig. 2. (a) Multi-output FTFN block (b) possible implementation.

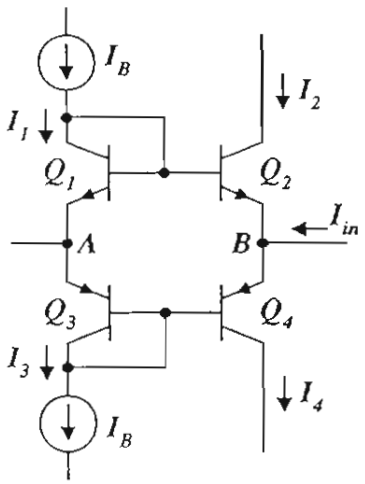

Fig. 3. Schematic form of the dual translinear loop.

2.2 Dual Translinear Loop

The dual translinear loop as shown in Fig. 3 composes of two PNP's and two NPN's transistors. Its characteristic is analyzed from the translinear relationship between collector currents of those transistors [5]:

$$I_1 I_3 = I_2 I_4 \tag{3}$$

The dc currents I_B are biased both Q_1 and Q_3. Thus, we can get $I_1 = I_3 = I_B$ by assuming that the current gain β of the transistors are much greater than unity.

The voltage between this two points depends on the ent $I_{in}(t)$ as given by

$$V_{BA}(t) = \frac{V_T}{2I_B} I_{in}(t) \tag{4}$$

$T/q \simeq 26$ mV at 27°C is the thermal ume that the magnitude of the cur- uch smaller than $2I_B$ [7]. It should be t the impedance at port A is high and the ance at port B is low. Therefore, this dual slinear cell can be used to realize the FTFN of Fig. 1(b).

3. Circuit Diagram

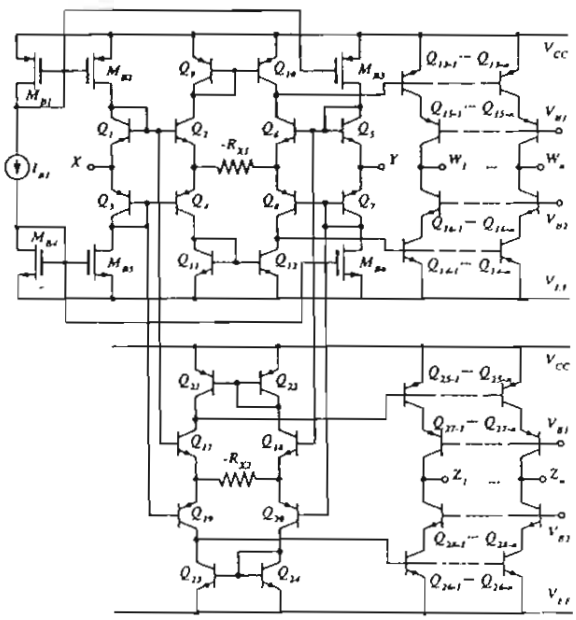

Fig. 4. Complete circuit of the dual translinear loop multi-output FTFN.

3.1 Overall Circuit

Fig. 4 show the complete circuit of the multi-output FTFN. This circuit basically comprises of 4 dual translinear loop cells connected each 2 cells' low-impedance ports together. Transistors Q_1 to Q_8 and the bias circuit, current source I_{B1} and transistor M_{B1} to M_{B6}, perform the first 2-dual translinear cells. Note that MOS transistors are used for the biasing to minimize noise; the main contribution in noise coming from current mirrors.

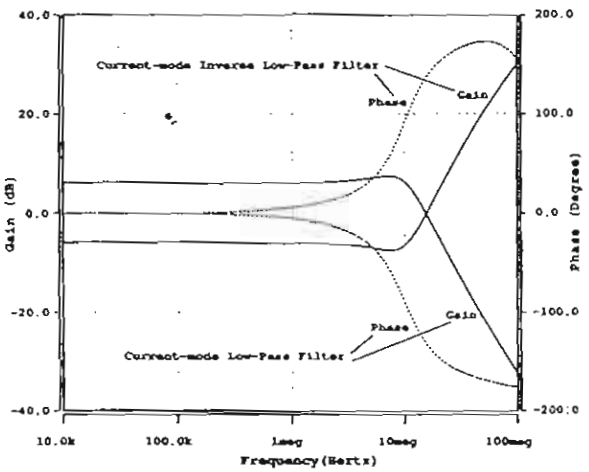

Fig. 9. Frequency response of current-mode filter.

5. Conclusions

We have proposed a simple FTFN circuit with additional extended output ports. The achievement has been realized through the use of quad dual translinear loop cells. The negative impedance implemented from dual translinear loop is added to compensate the internal parasitic impedance that can boot up the gain and also extend the operation frequency. Simulation results from HSPICE program confirm the high qualification of our presented circuit. A current-mode low-pass filter and its inverse filter are good examples to identify the feasibility of the circuit, however, the useful applications from the multi-output topology are still need some further researches.

6. Acknowledgements

This work was partly funded by the Thailand Research Fund (TRF) under the Senior Research Scholar Program grant number RTA/04/2543. The support provided by the Japan International Cooperation Agency (JICA) is also acknowledged.

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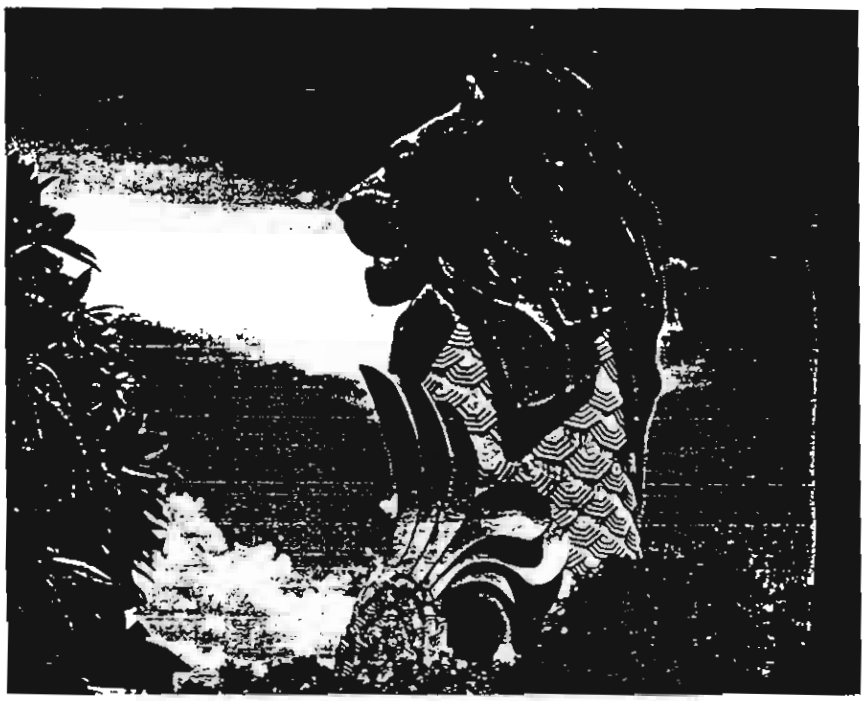

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A Wide-Band Current-Mode Analog Multiplier-Divider Using OTAs

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ABSTRACT

An analog multiplier-divider circuit that realized through the use of OTAs is proposed in this paper. Since the scheme is realized in such a way that employs only OTAs, which does not require external passive circuit elements and temperature compensated as a standard cell and does not require external passive circuit elements, the circuit is simple and can be easily constructed from commercially available IC. The circuit bandwidth is wide and close to the transistor f_T. Simulation results that demonstrate the performances of the multiplier-divider circuit are included.

Keywords: Current-Mode, Multiplier-Divider, OTAs

1. Introduction

Analog multipliers and dividers are important nonlinear building blocks that have found useful in a wide range of applications, such as telecommunication, control, instrumentation and signal processing. At present, because of the main featuring of wider bandwidth, greater linearity, wider dynamic range and simple circuitry compared with their voltage-mode counterparts, current-mode circuits have been received growing interest in analog signal processing circuits. Many techniques to design current-mode analog multiplier-divider circuits have been presented in the literature [1-3]. Also, a multiplier-divider circuit using only two second-generation current-controlled current-conveyors (CCCIIs) has been presented recently, where no resistors, no capacitors and no MOS transistors are required by such a realization scheme [4].

It is well accepted that OTA is a useful circuit building block in the design of analog circuits. Since OTA is a programmable device and has only a single high-impedance node, this makes the OTA an attractive device for high frequency and programmable basic building block [5,6]. Therefore, the implementation of analog circuits in such a way that employs only OTA as a standard cells will not only be easily constructed from readily available cells, but also significantly simplified the design and layout. Although, a circuit technique to employ OTAs to implement analog multiplier has been presented [7]. However, the circuit is a voltage-mode circuit where only multiplication function is realized and the circuit bandwidth is only about 2 MHz. In this paper, a current-mode temperature compensated multiplier-divider circuit using only OTAs as active circuit elements has been presented, where no passive elements are required by this realization scheme. It should be mentioned that this realization scheme is suitable for the bipolar-based and CMOS-based OTAs that their transconductance gain can be tune by DC bias currents [8-9]. PSPICE simulation results will be used to demonstrate the performance of the proposed scheme.

2. Basic principle

As shown in Fig.1, in this work an OTA that realized in bipolar transistor technology will be employed as active circuit elements. Its transconductance gain ($g_m = I_B/2V_T$)can be tune by the DC bias current (I_B). The schematic diagram of the proposed current multiplier-divider circuit using OTAs is shows in Fig 2. The input signal current i_{in1} is injected into the operational transconductance amplifier OTA1, which is connected as a grounded resistor. The voltage across the OTA1 is then used as the input voltage for the OTA2 and OTA3. The input signal current i_{in2} is added with the bias current I_{B2} of the OTA2. If g_{m1}, g_{m2} and g_{m3} are the transconductance gains of the OTA1, OTA2 and OTA3, respectively; then, from routine circuit analysis, the output currents I_{o2} and I_{o3} of the OTA2 and OTA3, respectively, can be written as

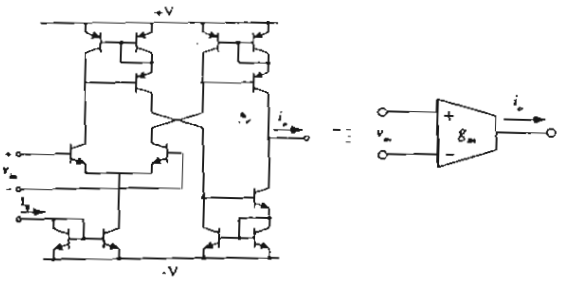

Fig. 1. The schematic diagram of the OTA.

$$I_{O2} = \frac{g_{m2}}{g_{m1}} i_{in1} = \frac{(I_{B2} + I_{in2})}{I_{B1}} i_{in1} \quad (1)$$

and

$$I_{O3} = -\frac{g_{m3}}{g_{m1}} i_{in1} = -\frac{(I_{B3})}{I_{B1}} i_{in1} \quad (2)$$

where $g_{m1} = I_{B1}/2V_T, g_{m2} = (I_{B2} + i_{in2})/2V_T$ and $g_{m3} = I_{B3}/2V_T$ and V_T is the thermal voltage. If we set $I_{B2} = I_{B3} = I_B$, the output current I_{out} of the circuit, that is the summation of the currents I_{O2} and I_{O3} can now be given by

$$I_{out} = I_{O2} + I_{O3} = \frac{i_{in1} i_{in2}}{I_{B1}} \quad (3)$$

which is in the form of a current-mode analog multiplication-division function. The circuit performs as a four-quadrant multiplier if i_{in1} and i_{in2} are the input signals, while it performs as a divider circuit if i_{in1} (or i_{in2}) and I_{B1} are the input signals. It should be noted that, since it is the ratio of OTAs transconductance gain, the output current I_{out} is less sensitive to temperature.

The major factors that contribute to the error and non-linearity in the circuit can be classified as follows. The first factor is due to the offset current at the output port of the OTA1. From (3), if I_{os} is the offset current, the output current $Iout$ can be rewritten as

$$I_{out} = \frac{(i_{in1} + I_{os}) i_{in2}}{I_{B1}} \quad (4)$$

We can see that, if i_{in1} is small or the peak value $|i_{in1}| < I_{os}$, the multiplication for the positive peak and the negative peak of i_{in1} will not be equal. While the offset currents at the output ports of the OTA2 and OTA3 are not contribute to the multiplication

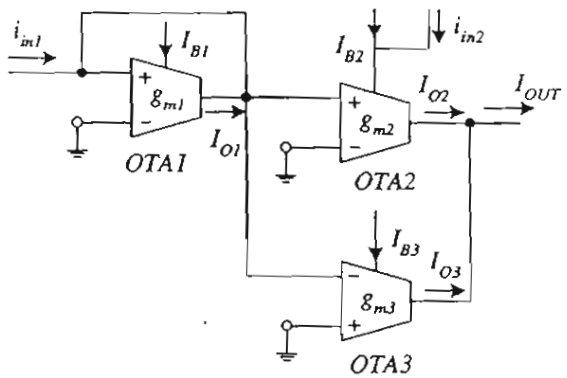

Fig. 2. The proposed current-mode multiplier-divider circuit using OTAs.

error, but will produce a DC current at the output of the circuit. The second factor affecting the non-linearity of the circuit is due to the limited linear range of the input stage of the OTA2 and OTA3. For a bipolar-based OTA, where the input stage is a conventional differential pair, the input differential voltages for linear operation are restricted to be less than 26 mV. Therefore, to minimize this error, the voltage swing across the OTA1 should be kept to be less than 26 mV. Since $1/g_{m1} = 2V_T/I_{B1}$, this restricted linear range can be improve by increasing I_{B1} .

3. Simulation results

The performance of the proposed multiplier-divider circuit of Fig.2 was verified through the use of SPICE simulation results. All the OTA was simulated by using the bipolar transistor parameters of the 2N3904 and 2N3906 for the NPN and PNP transistors, respectively. The transistors f_T were 186MHz. The multiplier function was tested by multiplying two sinusoidal signals. The result obtained are shown in Fig.3 for $i_{in1} = 0.5sin(2\pi 1000t)$mA, $i_{in2} = 0.5sin(2\pi 30000t)$mA and $I_{B1} = 1$mA. Since the DC offset current will distort the output signal, a DC current of about 5μA was injected at the output of the OTA1 to adjust the offset to be less than 0.1μA. Similarly, a DC current of about 5μA was used to keep the offset current at the output of the circuit to be less than 0.1μA. The power supply voltages were set to $V_{CC} = 10$V and $V_{EE} = -10$V.

The divider function was tested by inverting a triangular signal. The results obtained are show in

Fig.4. Fig.4 show the simulated transient response of the circuit that function as a divider. The output current I_{out}, which in this case is an inverting function of a triangular signal, was simulated for i_{in1} = 100mA, i_{in2} = 300mA, and I_{B1} is a 500Hz triangular wave with amplitude of 100μA and DC component of equal to 200μA.

Fig.5 shows the simulated DC transfer characteristics for the multiplier function, where the bias currents were set to $I_{B1} = I_{B2} = I_{B3}$ = 1mA. The figure shows the plot of the output current I_{out} against the input signal current i_{in1} from -1mA to 1mA and the input signal current i_{in2} from -1mA to 1mA with 0.5mA per step. The simulation and calculated data are agree very well over the 0.8mA input range with an error of less than 0.1%. Fig.6 shows the simulated frequency response of the circuit from the input i_{in1} to the output, with i_{in2} = 100μA and I_{B1} = 1mA. The response indicates that the circuit -3dB bandwidth is about 162 MHz that is close to the transistor f_T. The total harmonic distortion (THD) against input current, for the case that the input signal i_{in2} is a dc current, i_{in2} = 100μA and the input signal current $i_{in1} = 0.1\sin(2\pi 10000t)$mA, is about 0.24% . On the other hand, when the input current i_{in1} is dc current, i_{in1} = 100mA, and the signal current $i_{in2} = 0.1\sin(2\pi 10000t)$mA the THD is about 0.39%. Fig.7. Shows the simulation result of the output current (I_{out}) due to the change of temperature for operating temperature variations from 0°C to 100°C. We set the input signal currents i_{in1} and i_{in2} as dc currents, where i_{in1} = 1000μA and i_{in2} = 60μA, where I_{out} = 60μA. From the figure, the output current varies only from 59.62μA to 61.38μA, for the temperature 0°C to 100°C respectively. This simulation result shows that the temperature dependence of transconductance gains g_{m1} , g_{m2} and g_{m3} of the bipolar OTAs are compensated.

4. Conclusions

In this paper, we have proposed a temperature compensated analog multiplier-divider circuit that realized through the use of OTAs. The circuit does not require any external passive circuit element and the circuit bandwidth is close to transistor f_T Simulation results that demonstrate the performances of the multiplier-divider circuit are included. Noting that although the bipolar-based OTA has been used as the active circuit elements, however, the CMOS-based OTA which its transconductance gain g_m can

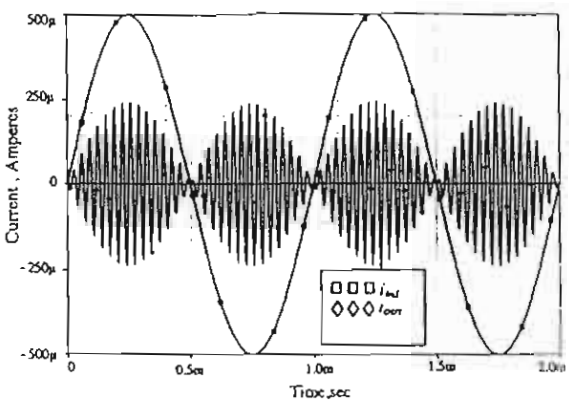

Fig. 3. Simulated transient response for the multiplier function.

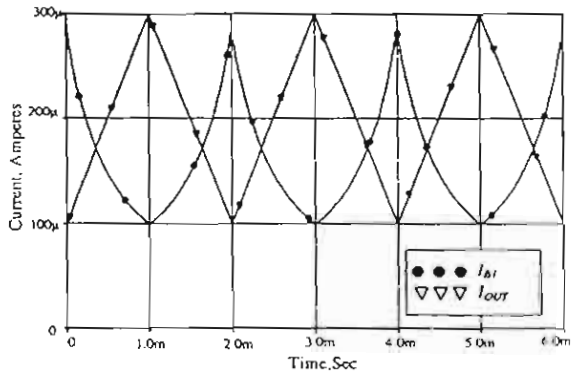

Fig. 4. Simulated transient response for the divider function.

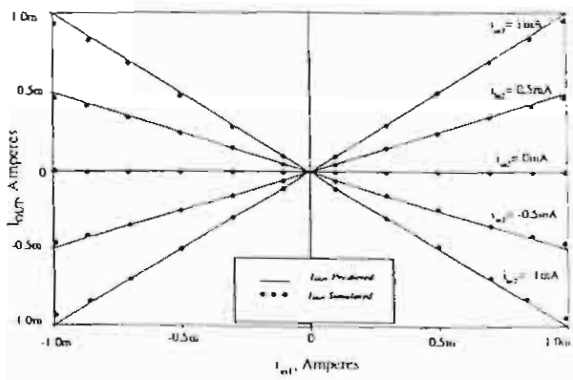

Fig. 5. Simulated DC transfer characteristic of the multiplier-divider.

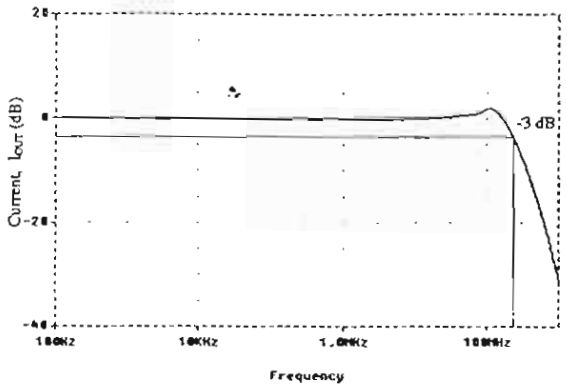

Fig. 6. Frequency response of current-mode multiplier-divider circuit using OTAs.

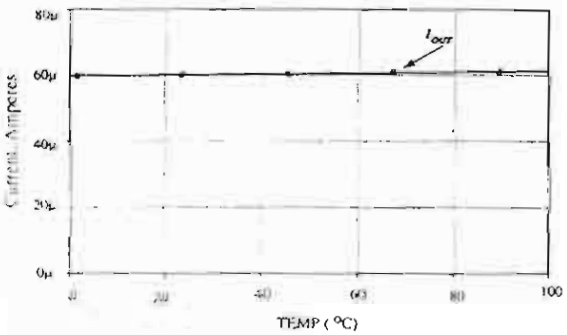

Fig. 7. Simulated transient response of I_{out} versus temperature.

be tune by the DC bias current [9] can also be used. Therefore the realization scheme is also suitable for implemented in CMOS technology.

5. Acknowledgment

This work is partly funded by the Thailand Research Fund (TRF) under the Senior Research Scholar Program, grant number RTA/04/2543. The support provided by the Japan International Cooperation Agency (JICA) is also acknowledged.

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bandpass responses of the filter when g_{ma} is varied are shown in Fig.4. The corresponding natural frequencies obtained by simulation are 48.98 kHz, 97.72 kHz and 484.17 kHz, and are correspond to theoretical values calculated from the equation (13). All the simulated results shown above imply that the proposed filter exhibits reasonably good agreement with the predicted values.

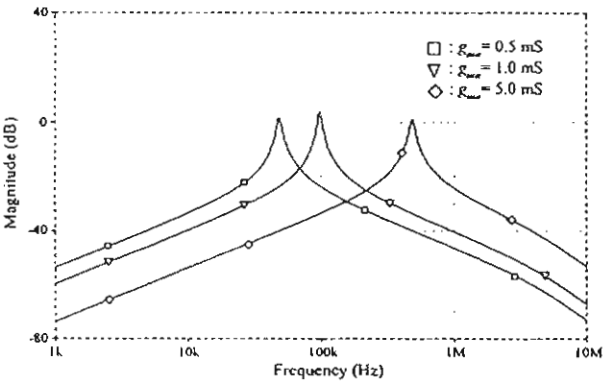

Figure 4 : Simulated responses of bandpass filter when g_{ma} is varied.

5. Conclusions

This paper presented an alternative scheme for realizing continuous-time electronically tunable active-only current-mode and voltage-mode filter. The proposed filter is realizable with only internally compensated type OA and multiple current output OTAs, and does not require any external passive elements. It has been shown that the proposed circuit can realize three voltage and current transfer functions simultaneously, and that the circuit characteristics can be electronically and independently tuned. Because of their active-only nature, the circuit can be easily employed to realize active network functions and are suitable for implementing in monolithic integrated form in both bipolar or CMOS technologies. The simulated results have been used to verify the theoretical analysis.

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On the Realization of FTFN with Variable Voltage and Current Gains

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Abstract: A design technique for the practical implementation of a variable four-terminal floating nullor (FTFN) is presented, which contains three operational mirrored amplifiers (OMAs) and four grounded resistors. The proposed FTFN provides tunable both voltage-gain and current-gain with constant bandwidth property by varying the value of a single grounded resistor. PSPICE simulation results that agree with the theoretical analysis are obtained by modeling a variable-gain FTFN using a commercial AD844 ICs.

1. Introduction

At present, current-mode circuits have been receiving significant attention owing to its advantage over the voltage-mode, particularly for higher frequency of operation and simpler filtering structure [1]. Recently, the applications and advantages in the realization of transfer functions using four-terminal floating nullors (FTFNs) have received considerably attention. The designs of current-mode circuits employing FTFN as active devices such as amplifiers [2], current-mode filters [3-4], sinusoidal oscillators [5-6] and floating immittances [7], have been developed in the literature. Some previous-mentioned topologies have been demonstrated that an FTFN is a more flexible and all-round building block than an operational amplifier and a current conveyor [2],[4]. This is due to the fact that the nullor model of FTFN, the nullator and the norator, are isolated from each other, which is more flexible in active network synthesis. Moreover, the FTFN-based structures also provide a number of potential advantages, such as, complete absence of passive component-matching requirement, minimum number of employed passive elements. In addition, the FTFN whose the gain can be independently tuned seems to be more attractive, flexible and suitable for design and implementation of the frequency selective systems, such as, biquads, oscillator and so forth. Although some tunable FTFNs have been recently reported [8-9], they can variable only current-gain between i_w and i_z. There are no circuit realization based on tunable FTFN that can variable both voltage-gain and current-gain.

The aim of this paper is to propose a circuit technique for the practical implementation of the FTFN with variable voltage and current gains. The circuit realization uses only three operational mirrored amplifiers (OMAs) and four grounded resistors. The proposed tunable FTFN offers independently variable dc voltage and current gains while remaining a constant bandwidth. Moreover, it is interesting to show that the dc gains of the circuit can be tuned by adjusting grounded resistors without effecting the useful bandwidth. The performances of the proposed variable-gain FTFN using a commercial AD844 ICs are given with the simulation results, which will show that the characteristics of the resulting circuit become tunable.

2. Circuit Description

An FTFN has the potential of being an extremely versatile analog active building block. It is a four-terminal active device with two input terminals (y, x) and two output terminals (w, z), whose circuit representation is shown in Fig.1. The terminal characteristics of the FTFN can be defined by means of the following relationship.

$$i_y = i_x = 0 \quad , \quad v_x = \beta . v_y \quad \text{and} \quad i_z = \pm\alpha . i_w \qquad (1)$$

where $\beta = 1-\varepsilon$, ($|\varepsilon| << 1$), and ε denotes the voltage tracking error, and $\alpha = 1-\delta$, ($|\delta| << 1$), and δ represents the current tracking error of an FTFN. The sign + is applied for the positive FTFN (FTFN+), whereas the sign – uses for the opposite polarity case, represented the negative FTFN (FTFN-). For an ideal FTFN, the voltage and current tracking error are equal to zero, i.e., $\varepsilon = \delta = 0$, or $\beta = \alpha = 1$. The usefulness of the FTFN can be extended if equation (1) is implemented in such a way that the voltage and current transfer ratios can be varied, in which case a more generalized tunable FTFN should be investigated.

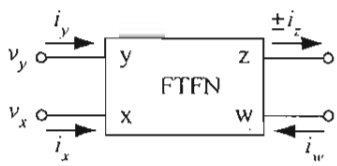
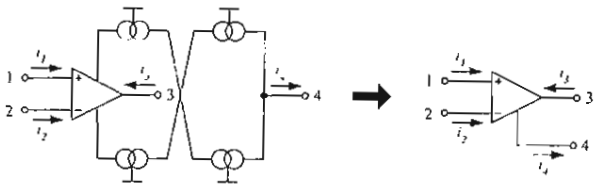


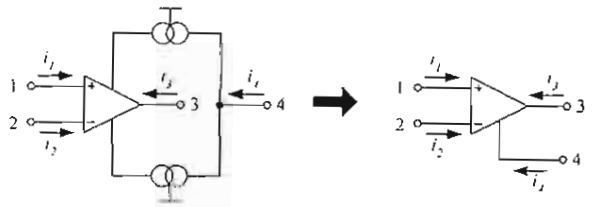
Figure 1 : Symbol of an FTFN

Fig.2 shows the circuit implementation and representation of the OMAs. The negative OMA (OMA-) comprising an op-amp and two pairs of current mirrors as shown in Fig.2(a) is a more general and flexible device owing to it can be equivalent to an ideal nullor or FTFN+ [1-2], whereas the other type of OMA which requires only one pairs of current mirrors is named the positive OMA (OMA+) and is shown in Fig.2(b). Therefore, it can be concluded from Fig.2 that the port characteristics of the OMA can be characterized as :

$$v_2 = v_1 \quad , \quad i_1 = i_2 = 0 \quad \text{and} \quad i_4 = i_3 \qquad (2)$$

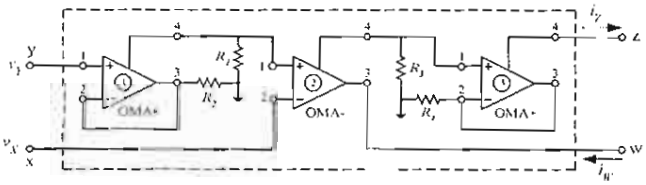


(a)

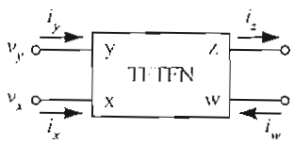


(b)

Figure 2 : Possible implementation of OMAs
(a) negative OMA (OMA-) (b) positive OMA (OMA+)



(a)



(b)

Figure 3 : Proposed tunable FTFN (TFTFN)
(a) circuit implementation (b) its symbol

The proposed tunable FTFN with arbitrary voltage-gain and current-gain, named TFTFN, is shown in Fig.3. It mainly consists of three OMAs and four grounded resistors. A detail analysis results that the voltage-current characteristics of this device can be defined by

$$i_y = i_x = 0 \quad , \quad v_x = \left(\frac{R_1}{R_2}\right) v_y \quad \text{and} \quad i_z = \left(\frac{R_3}{R_4}\right) i_w \qquad (3)$$

Also note that the proposed TFTFN of Fig.3 is more flexible, which can be varied the voltage-gain and the current-gain through the ratio of two grounded resistors. Furthermore, if the 3rd positive OMA (OMA+) of Fig.3(a) is used instead with the negative OMA (OMA-), then the variable-gain FTFN- will also be obtained.

3. Performance Analysis

One important issue that must to be taken into account is the non-idealities of each OMA on the frequency dependent performance. Fig.4 shows the macro-model of the OMA, where β and α denote the non-ideal voltage- and current gains of the OMA. By applying the model from Fig.4 into the sub-circuit between OMA1 and OMA2 of Fig.3(a), routine analysis obtains that

$$\frac{v_X}{v_Y} = \left(\frac{\beta_1\beta_2\alpha_3 R_A}{R_2}\right)\left(\frac{1}{1+sR_A C_A}\right) \qquad (4)$$

where $R_A = R_1 // R_y // R_z$, $C_A = C_y + C_z$ and β_i and α_i are the voltage gain and current gain of the OMAi (i = 1, 2, 3). Typically, the values of R_y and R_z are too large and can also approximate to R_y , $R_z >> R_1$, then equation (4) can be rewritten as :

$$\frac{v_X}{v_Y} \cong \left(\frac{\beta_1\beta_2\alpha_3 R_1}{R_2}\right)\left(\frac{1}{1+sR_1 C_A}\right) \qquad (5)$$

According to equation (5), the dc voltage gain, β_{dc}, and the high-frequency dominant pole between the port y and the port x, ω_{pv}, can respectively be given by

$$\beta_{dc} = \frac{\beta_1\beta_2\alpha_3 R_1}{R_2} \qquad (6)$$

and

$$\omega_{pv} = 2\pi f_{pv} = \frac{1}{R_1 C_A} = \frac{1}{R_1(C_y + C_z)} \qquad (7)$$

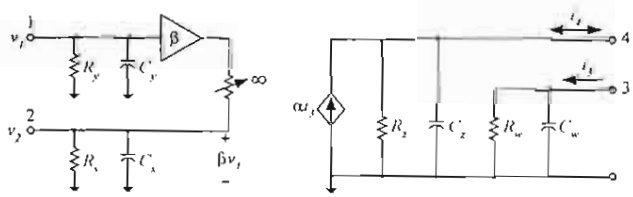


Figure 4 : Macro model for non-ideal OMA

It can easily be noted from equations (6) and (7) that the dominant pole frequency can be adjusted by tuning the value of the resistor R_1, while the dc voltage-gain of this circuit can be adjusted through the resistor R_2 without affecting the bandwidth property. For example, if R_1 = 5 kΩ, C_y = 2 pF and C_z = 4.5 pF, then this pole frequency will locate at 4.89 MHz. This means that the dc voltage-gain of the proposed TFTFN can be independently varied without changing the useful bandwidth.

In the same way as above, the transfer characteristic between the currents i_Z and i_W can be considered by applying the model from Fig.4 into the sub-circuits formed of OMA2 and OMA3 of Fig.3(a). Reanalysis gives the relations :

$$\frac{i_z}{i_w} = \left[\frac{\beta_3\alpha_2\alpha_3 R_m R_z}{R_n(R_z + R_L)}\right]\left[\frac{1}{(1+sR_mC_A)(1+sR_LC_z)}\right] \tag{8}$$

where $R_m = R_3 // R_y // R_z$, $R_n = R_4 // R_x$ and R_L is the load resistance connected to the port z. Since R_3 and R_4 are very small, comparable to those resistances, i.e., R_y , $R_z >> R_3$, $R_x >> R_4$. Thus equation (8) can be reduced to :

$$\frac{i_z}{i_w} = \left[\frac{\beta_3\alpha_2\alpha_3 R_3}{R_4}\right]\left[\frac{1}{(1+sR_3C_A)(1+sR_LC_z)}\right] \tag{9}$$

if we choose $R_3 >> R_L$, then the above equation becomes

$$\frac{i_z}{i_w} = \left[\frac{\beta_3\alpha_2\alpha_3 R_3}{R_4}\right]\left[\frac{1}{(1+sR_3C_i)}\right] \tag{10}$$

Hence, the dc current-gain, α_{dc}, and the high-frequency dominant pole between the port w and the port z, ω_{pi}, are

$$\alpha_{dc} = \frac{\beta_3\alpha_2\alpha_3 R_3}{R_4} \tag{11}$$

and

$$\omega_{pi} = 2\pi f_{pi} = \frac{1}{R_3C_A} = \frac{1}{R_3(C_y + C_z)} \tag{12}$$

From equations (11) and (12), R_3 should be selected so as to meet the desired bandwidth, whereas R_4 can be modified to change the gain without disturbing the bandwidth. Similarly, if R_3 = 5 kΩ, C_y = 2 pF and C_z = 4.5 pF, then this pole frequency is also located at 4.89 MHz. It also concludes that the dc current-gain of the proposed TFTFN can be independently controlled without changing the useful bandwidth.

4. Simulation Results

The performances of the proposed variable-gain FTFN of Fig.3 have been simulated with PSPICE using an OMA, which consists of AD844 transimpedance op-amps as shown in Fig.5 [6]. The simulation was performed using macro-model of the AD844 IC shown in Fig.6 [10].

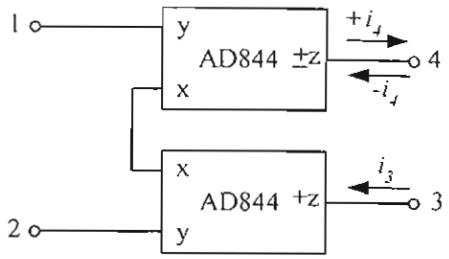


Figure 5 : Realization of OMA± with commercial available AD844 ICs

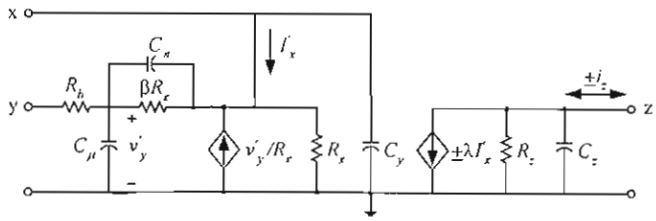


Figure 6 : Small signal equivalent circuit for the AD844 transimpedance amplifier [10] : R_b = 300 Ω, R_x = 50 Ω, βR_x = 20 kΩ, R_z 2 MΩ, C_μ = 2 pF, C_π = 26 pF, C_y = 2 pF and C_z 4.5 pF

Fig.7 shows the voltage frequency responses, v_x / v_y , when R_1 = 5 kΩ and R_2 is changed to 5 kΩ, 2.5 kΩ, 1 kΩ and 0.5 kΩ, which corresponds to the dc voltage gain β = 1, 2, 5 and 10, respectively.

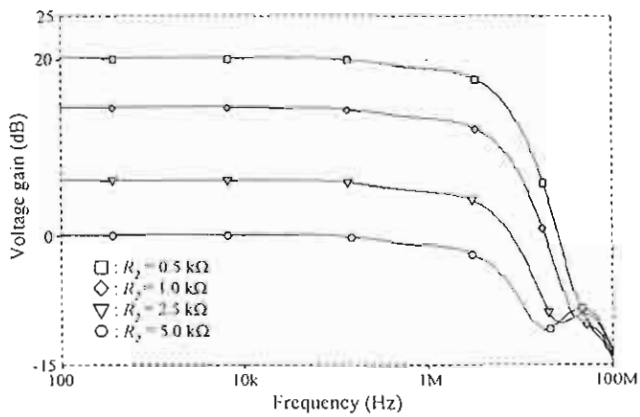


Figure 7 : Voltage transfer characteristics of the proposed tunable FTFN for R_1 = 5 kΩ

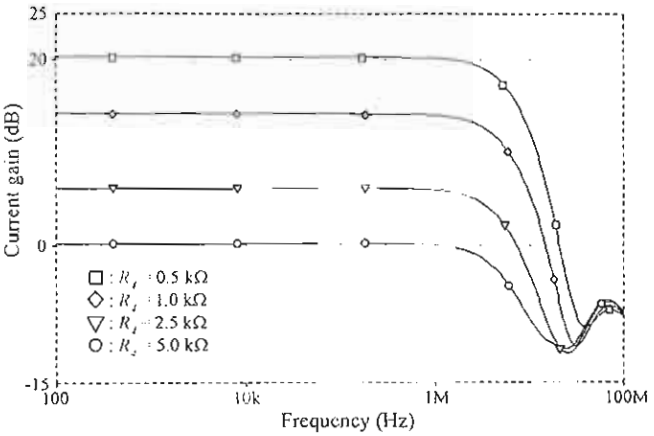


Figure 8 : Current transfer characteristics of the proposed tunable FTFN for R_3 = 5 kΩ

The ac current responses of the proposed TFTFN for R_3 = 5 kΩ are shown in Fig.8. From the simulated frequency responses in Figs.7 and 8, it is evidenced in both cases that the useful bandwidth is nearly constant with respect to the variation of the voltage-gain or the current-gain of the proposed TFTFN, which are well confirmed the theoretical analysis.

5. Further Applications

Finally, the proposed FTFN with variable-gain can be applied for implementing active filters with electronic control of the important circuit parameters, such as, the natural angular frequency ω_o, the quality factor (Q-factor) and the absolute bandwidth. Moreover, oscillator with electronic control of the frequency and the condition of oscillators can also be realized. But it is not demonstrated in this paper, because of some applications employing this device have been recently reported in references [7-9].

6. Conclusions

In this paper, a circuit configuration for an FTFN with variable voltage- and current-gains is proposed in order to simplify the representation of different building block in the ideal case. The proposed tunable FTFN employs only three OMAs and four grounded resistors, and offers constant bandwidth, whereas both the dc voltage- and current-gains can be independently controlled through a single grounded resistor. PSPICE simulation results obtained from an implementation with the AD844 transimpedance op-amp have been demonstrated that its performance is quite satisfactory for discrete high-frequency circuit designs, such as, biquads, oscilaators and so forth.

7. Acknowledgment

This work is funded by the Thailand Research Fund (TRF) through the Senior Research Scholar Program, grant number RTA/04/2543.

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Realization of Lowpass and Bandpass Leapfrog Filters Using OAs and OTAs

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Abstract : The systematic procedure for realizing lowpass and bandpass leapfrog ladder filters using only active elements is presented. The proposed architecture is composed of only two fundamental active building blocks, i.e., an operational amplifier (OA) and an operational transconductance amplifier (OTA), without external passive element requirement, making the approach conveniently for further integrated circuit implementation with systematic design and dense layout. As illustrations to demonstrate the systematic realization of current-mode ladder filters, a 3rd-order Butterworth low-pass filter and a 6th-order Chebyshev bandpass filter are designed and simulated using PSPICE.

Keywords : Operational Amplifier (OA), Operational Transconductance Amplifier (OTA), Leapfrog filters, Ladder structure, Active-only circuits

1. Introduction

Analog designs have been viewed as a voltage-dominated form of signal processing for a long time. However in the last decade current-mode signal-processing circuits have been demonstrated and well appreciated over their voltage-mode counterparts due to the main featuring of wide bandwidth capability. Designs for active filter circuits using high performance active devices, such as, operational amplifier (OA), operational transconductance amplifier (OTA) and second generation current conveyor (CCII), have been discussed previously [1-3]. Due to the fact that active filter designs utilizing the finite and complex gain nature of an internally compensated type operational amplifier are suitable for integrated circuit (IC) fabrication and high frequency operation [4-5]. Several implementations in continuous-time filters using only active components are recently available in the literature [6-9]. They have been demonstrated that the realizations of the resistor-less and capacitor-less active-only circuit would be attractive for simplicity, integratability, programmability and wide frequency range of operation. However, a design approach with only active architectures that are efficient for systematic design and very large scale integration (VLSI) has not been reported sufficiently.

The following paper deals with the alternative systematic approach that has been used the leapfrog structure to obtain current-mode ladder active filters with the employment of all-active elements. The proposed design approach is quite simple and systematic which has no passive element requirements. The basic building blocks of all circuits mainly consist of OA and OTA. The obtained feature of the filter constructed in this way is a general structure and is able to adjust the characteristic of the current transfer function by electronic means. Owing to all-resulting circuits are implemented such a way that employs only active-element sub-circuits and minimizes the number of different fundamental building blocks. It is not only easy to construct from readily available IC type, but also significantly simplified in the IC design and layout. As examples to illustrate that the approach considerably simplifies for the current-mode ladder filter realizations, the leapfrog-based simulation of a 3rd-order Butterworth low-pass and a 6th-order Chebyshev bandpass filters are designed. Detailed analysis are given as well as some simulation results, as an example, being performed with a commercially available LM741 type IC OA and a CA3080 type IC OTA.

2. Basic active building blocks

2.1 Operational Amplifier (OA)

The first fundamental active device is to be an internally compensated type operational amplifier (OA) as shown with its symbolic representation in Fig.1. As is known in practice, the open-loop amplifiers have a finite frequency-

dependent gain. If ω_a is the -3 dB bandwidth and by considering for the frequencies $\omega >> \omega_a$, the open-loop voltage gain $A(s)$ of an OA will be henceforth characterized by

$$A(s) = \frac{A_o \omega_a}{s + \omega_a} \cong \frac{B}{s} \qquad (1)$$

where B denotes the gain-bandwidth product (GBP) in radian per second, which is the product of the open-loop dc gain A_o and the 3-dB bandwidth ω_a.

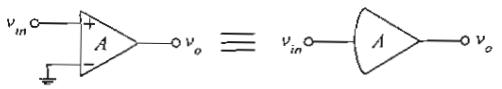


Fig.1 : Symbol of an OA

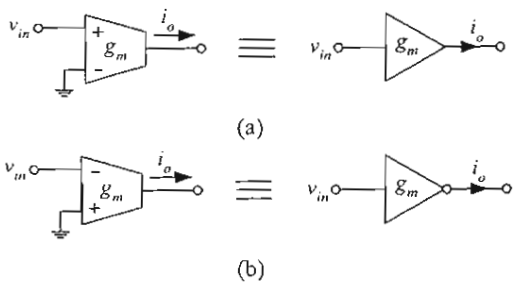


Fig.2 : Symbol of an OTA
(a) for positive g_m, $i_o = g_m v_{in}$
(b) for negative g_m, $i_o = -g_m v_{in}$

2.2 Operational Transconductance Amplifier (OTA)

An operational transconductance amplifier (OTA) is a voltage-controlled current source (VCCS), which its symbolic representation can be shown in Fig.2. For the ordinary bipolar OTA, the transconductance parameter g_m can be given by

$$g_m = \frac{I_B}{2V_T} \qquad (2)$$

where V_T is the thermal voltage and I_B is the external-bias current. It is indicated from equation (2) that the g_m value is tunable electronically by changing I_B.

After these circuit elementary considerations, an approach to derive leapfrog-based current-mode ladder filters from passive LC ladder prototypes will be presented in the following section.

3. Current-mode leapfrog ladder filters

Since the doubly terminated LC ladder network has been receiving considerable attention and popular due to it shares all the low sensitivity and low component spread of the RLC prototypes [10-12]. In this section the systematic approach to realize current-mode ladder filters using only active elements is proposed. It is based on the leapfrog structure representation, which is derived from the passive RLC ladder prototypes. To demonstrate the proposed design approach, consider the general resistively terminated current–mode ladder filter with parallel impedances and series admittances shown in Fig.3. The relations of the currents-voltages for the branches, the meshes and the nodes in this filter can be interrelated by :

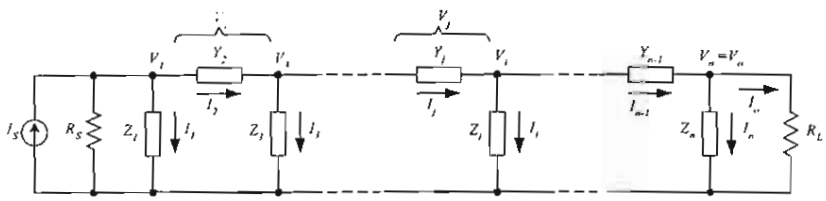


Fig.3 : General resistively terminated current-mode ladder prototype

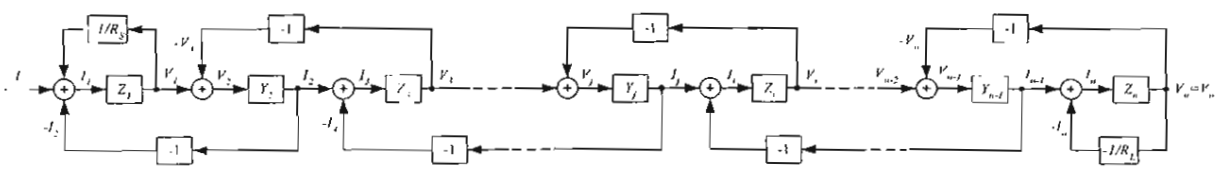


Fig.4 : Leapfrog block diagram of the general ladder prototype of Fig.3

$$I_1 = I_S - \frac{V_1}{R_S} - I_2 \;,\; V_1 = Z_1 I_1$$

$$I_2 = Y_2 V_2 \quad , \quad V_2 = V_1 - V_3$$

$$I_3 = I_2 - I_4 \quad , \quad V_3 = Z_3 I_3$$

$$\vdots \qquad , \qquad \vdots$$

$$I_j = Y_j V_j \quad , \quad V_j = V_{j-1} - V_{j+1}$$

$$I_i = I_{i-1} - I_{i+1} \quad , \quad V_i = Z_i I_i$$

$$\vdots \qquad , \qquad \vdots$$

$$I_{n-1} = Y_{n-1} V_{n-1} \quad , \quad V_{n-1} = V_{n-2} - V_n$$

and

$$I_n = I_{n-1} - I_o \quad , \quad V_n = Z_n I_n \tag{3}$$

where (i = 1 , 3 , 5 , ..., n) and (j = 2 , 4 , 6 , ..., n-1). Equation (3) can be represented by leapfrog block diagram depicted in Fig.4, where the output signal of each block is fed back to the summing point input of the preceding block. In contrast with the conventional simulation topology, however, we will present a simple, systematic and more efficient method unique to active-only current-mode ladder filters by using the features of an OA and an OTA.

4. Realization procedure

4.1 Lowpass leapfrog realization

As an example to illustrate the design procedure, consider the current-mode 3rd-order all-pole LC ladder lowpass prototype with regarding the terminating resistors shown in Fig.5. The design techniques of these partial conversions can be accomplished in the way as shown in Fig.6, through the use of only an OA and an OTA as mentioned in the section 2. Therefore, the circuit parameters have the typical values calculated by :

$$g_{mi} = B_i C_i \qquad \text{for } i = 1, 3, 5, 7, \ldots, n$$

and

$$g_{mj} = \frac{1}{B_j L_j} \qquad \text{for } j = 2, 4, 6, 8, \ldots, n\text{-}1 \tag{4}$$

where B_k ($k = i$ or j) represents the GBP of the k-th OA.

Based on the directed simulation of the LC branch as shown in Fig.6, the system diagram thus straightforwardly derived from the passive RLC ladder circuit of Fig.5 can be shown in Fig.7. The design equations of the circuit parameters can be expressed as follows :

$$g_m = \frac{1}{R} = \frac{1}{R_S} = \frac{1}{R_L}$$

$$g_{m1} = B_1 C_1$$

$$g_{m2} = \frac{1}{B_2 L_2}$$

and

$$g_{m3} = B_3 C_3 \tag{5}$$

Note that all elements, which simulate the behavior of capacitor and inductor, are tunable electronically through adjusting the transconductcane parameters, g_m.

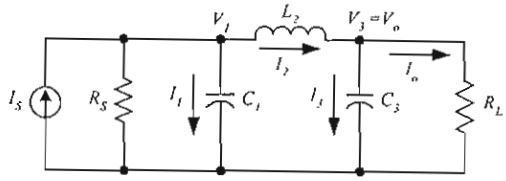


Fig.5 : 3rd-order all-pole LC ladder lowpass prototype

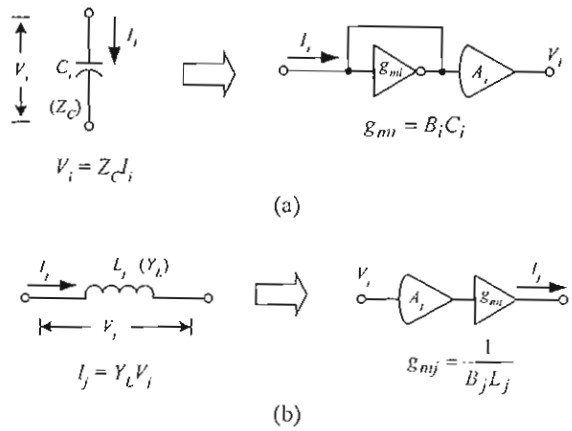


Fig.6 : Partial branch simulations using OA and OTA of the lowpass network of Fig.5
(a) parallel branch impedance
(b) series branch admittance

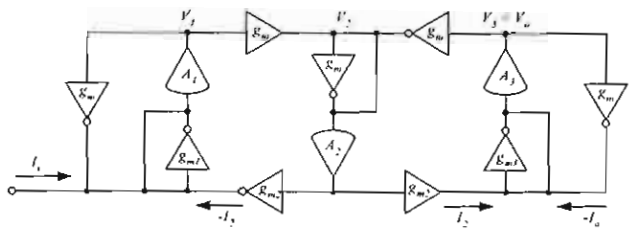


Fig.7 : Systematic diagram for current-mode 3rd-order lowpass filter using active-only elements

Let us first illustrate the step-by-step procedure for the design of the current-mode ladder lowpass filter based on the employment of all active elements.

Example 1 : a design of current-mode 3rd-order Butterworth lowpass filter of Fig.5 with a cut-off frequency of f_c = 100 kHz is realized as a prototype. The corresponding normalized passive component values of the ladder are given by :

$$R_S = R_L = 1\ \Omega \quad , \quad C_1 = C_3 = 1\ \text{F} \quad , \quad L_2 = 2\ \text{H}$$

We then denormalize these component values with the frequency f_c of 100 kHz and the scaling resistance R of 1 kΩ. The corresponding deormalized component values are obtained as :

$$R_S = R_L = R = 1\ \text{k}\Omega\ ,\ C_1 = C_3 = 1.59\ \text{nF}\ ,\ L_2 = 3.185\ \text{mH}$$

Assume that LM741 type OA having the gain-bandwidth product B = 5.906 Mrad/s is used [7]. Thus, by calculating the circuit parameters of the filter in Fig.7 obtained from equation (5) with the choice of the equal scaling conductance $g_m = 1/R$ yields :

$$g_m = 1\ \text{ms}\ ,\ g_{m1} = g_{m3} = 9.39\ \text{ms}\ \text{and}\ g_{m2} = 53\ \mu\text{s}$$

Since all circuit parameters depend on the g_m values, a property of the proposed filter implementations is, therefore, possible to tune the characteristic of the current transfer function proportional to external or on-chip controlled transconductances. It is shown that for the employment of all active elements, a further advantage is to allow integration in monolithic as well as in VLSI fabrication techniques.

4.2 Bandpass leapfrog realization

The proposed approach can also be employed in the design of current-mode LC ladder bandpass filters. Consider the current-mode 6th-order LC ladder bandpass prototype shown in Fig.8, having parallel resonators in parallel branches and series resonators in series branches. Observe that the repeated use of the bandpass LC structure branches typically consisting of parallel and series combinations of capacitor and inductor, shown respective in Figs.9(a) and 9(c), makes up the complete circuit. The voltage-current characteristics of these partial operations can be derived respectively as follows:

For the parallel combination branches of Fig.9(a) :

$$V_i = Z_C(I_i - Y_L V_i) = \frac{1}{sC_i}\left(I_i - \frac{V_i}{sL_i}\right) \qquad 6(a)$$

for $i = 1, 3, 5, 7, \ldots, n$.

For the series combination branches of Fig.9(c) :

$$I_j = Y_L(V_j - Z_C I_j) = \frac{1}{sL_j}\left(V_j - \frac{I_j}{sC_j}\right) \qquad 6(b)$$

for $j = 2, 4, 6, 8, \ldots, n$-1.

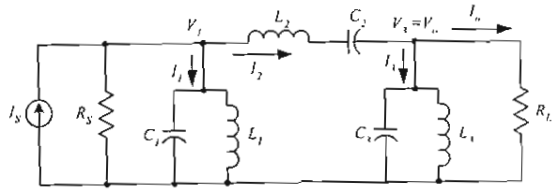


Fig.8 : 6th-order LC ladder bandpass prototype

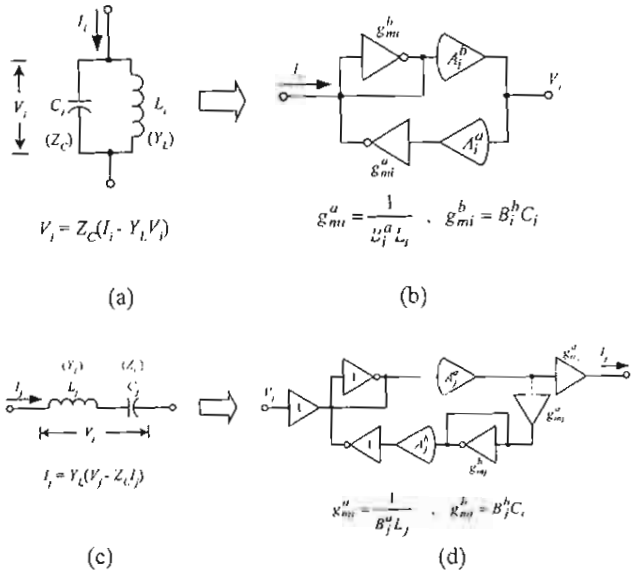


Fig.9 : Sub-circuit simulations using all-active elements of the bandpass network of Fig.8

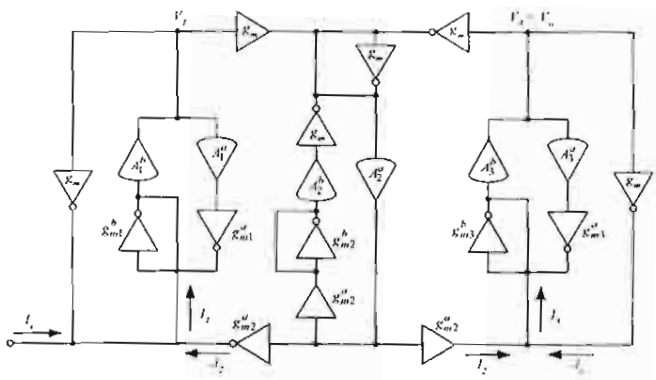


Fig.10 : Systematic diagram for current-mode 6th-order bandpass filter using active-only elements

The resulting circuits for the active-only implementation of these structures corresponding to the sub-circuit operations of Figs.9(a) and 9(c) are then resulted in Figs.9 (b) and 9(d), respectively. The design formulas for the circuit parameters of each branch can be summarized below:

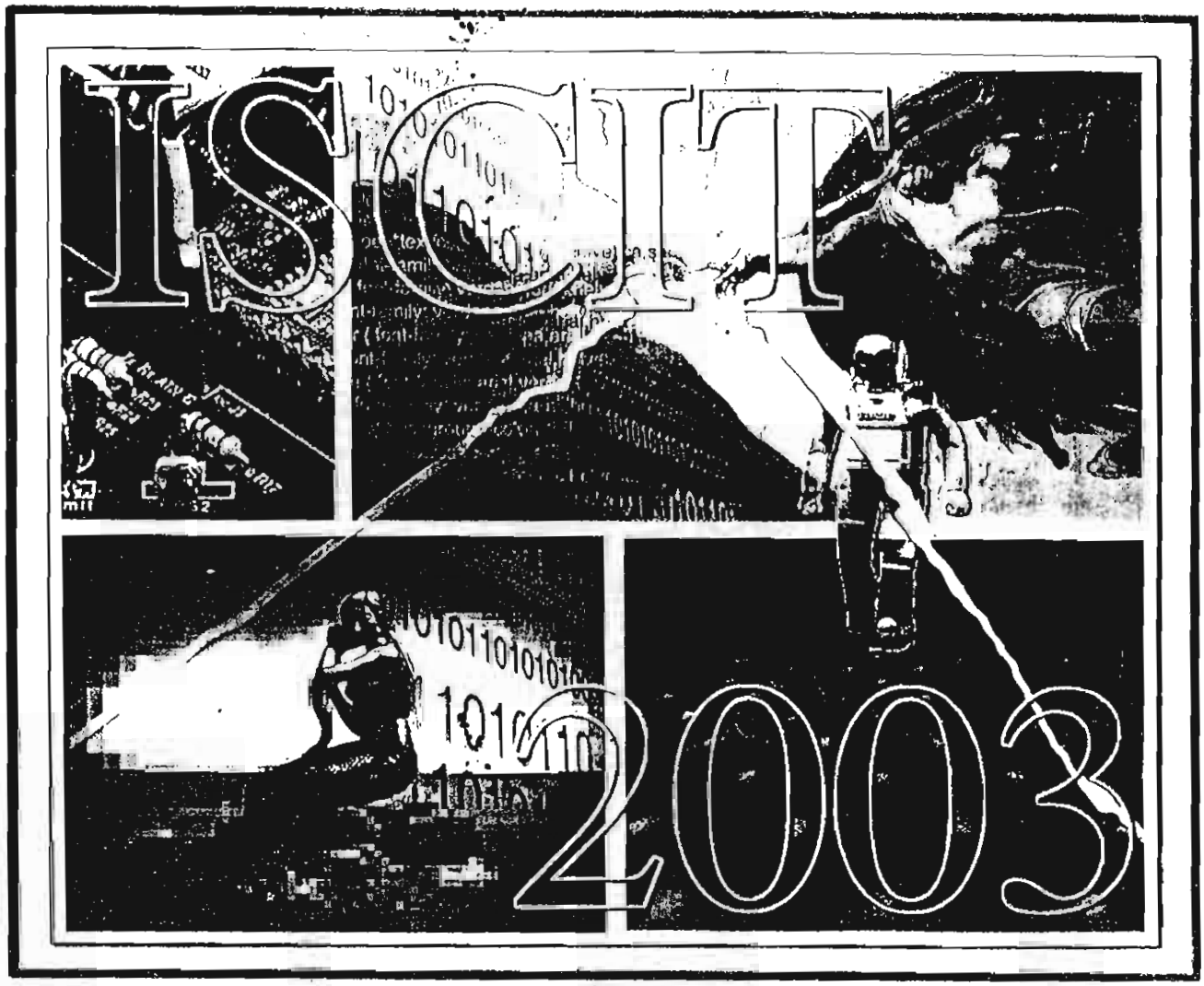
Volume I

Proceedings

The Third International Symposium on Communications and Information Technologies

September 3-5, 2003

BP Samila Beach Hotel and Resort, Songkhla, Thailand



ISCIT 2003

ISBN 974-644-437-9

Current-Mode Universal Biquadratic Filter Using Current Differencing Buffered Amplifiers

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Abstract

A circuit realization of three-inputs and single-output (TISO) current-mode universal biquadratic filter with the employment of current differencing buffered amplifiers (CDBAs) is presented in this paper. The proposed filter can realize simultaneously the highpass (HP), lowpass (LP), bandpass (BP), bandstop (BS) and allpass (AP) responses without changing the circuit configuration. The natural angular frequency ω_0 and the quality factor Q are independently controllable through the passive elements, and have low passive and active sensitivities. The PSICE simulation results are given to confirm the theoretical analysis.

1. Introduction

During the past few years, comparing with voltage-mode techniques, current-mode signal processing techniques have been received a wide attention due to its wide bandwidth, large dynamic range and simple implementation of signal operations such as addition and subtraction [1]. The realizations of high performance current-mode circuits usually employs active circuit building blocks, such as, second-generation current conveyors (CCIIs) and current feedback amplifiers (CFAs). Recently, a new active building block, which is called a current differencing buffered amplifier (CDBA), has been introduced [2]. Since the CDBA is considered as unity-gain current-mode and voltage-mode operations, this element would be quite large dynamic range and wide bandwidth similar to its current-mode counterparts, such as, CCIIs and CFAs [2-3]. Moreover, the structure of a CDBA is suitable for virtually grounded capacitance, which can reduce the effect from the stray capacitance [4], suitable for current mode operation and simple implementation while keeping the compatibility with existing voltage signal processing circuits. Although several versions of biquadretic filters based on CDBAs have been reported [3-6], the CDBA-based current-mode biquadratic filter that can generate all biquadratic current transfer functions in the same circuit has not yet been proposed.

Generally, it is well known that biquadratic filter is an important basic building block, which is widely used in analog signal processing applications, communication systems and instrumentation systems. Therefore, in this paper, we present a new TISO current-mode universal biquadratic filter employing three CDBAs, two really grounded capacitors and five virtually grounded resistors. By the proper choice of the input terminals, the proposed configuration can realize the HP, LP, BP, BS and AP current transfer functions without any change in the circuit topology. The filter provides orthogonal tuning of the parameters ω_0 and Q-factor, and also displays low passive and active sensitivities. PSPICE simulation results on the filter are included to verify the presented theory.

2. Circuit description

The circuit representation of the CDBA is shown in Fig.1, where p and n are the input terminals, and z and w are the output terminals. Its current and voltage characteristics can be described by the following relations [2-3].

$$v_p = 0 \ , \ v_n = 0 \ , \ i_z = i_p - i_n \ \text{ and } \ v_w = v_z \qquad (1)$$

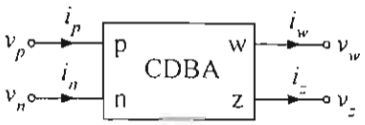


Figure 1 : Circuit representation of CDBA.

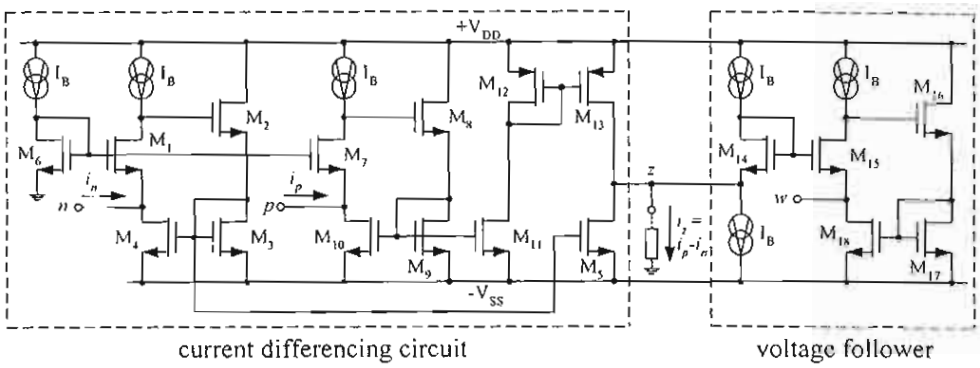


Figure 2. : Circuit configuration of the proposed CDBA

According to the CDBA characteristics, the differential input current i_p-i_n will convert into the output voltage v_w through the impedance connected at the terminal z, where ideally the input impedance's of the terminals p and n are zero. This means that the CDBA can be realized by a cascade connection of a current differencing circuit and a voltage follower.

Fig.2 shows the proposed low-voltage CDBA in CMOS technology. The realization scheme is based on the use of the CMOS unity gain current amplifier that composed of a source follower and a current mirror to provide the low input resistance at the input terminal [7]. From the figure, the current differencing circuit utilizes two unity gain current amplifiers (M_1-M_5 and M_7-M_{11}) and the current mirror M_{12}-M_{13}, where M_6 and the bias current source I_B are used to bias the terminals p and n at ground potential. Group of transistors M_{14}-M_{18} functions as a voltage follower, where the transistor M_{14} and the current source I_B are connected as a voltage level shift.

3. Proposed CDBA-based current-mode universal biquadratic filter

Fig.3 shows the proposed CDBA-based universal biquadratic filter. Routine circuit analysis yields the current transfer functions as follows :

$$I_{out} = \left[\frac{s^2\left(1+\frac{1}{sC_2R_5}\right)I_{in3} - s\left(\frac{1}{R_2C_2}\right)I_{in2} + \left(\frac{1}{R_1R_2C_1C_2}\right)I_{in1}}{D(s)} \right] \qquad (2)$$

where $D(s) = s^2 + s\left(\frac{1}{R_5C_2}\right) + \left(\frac{R_3}{R_1R_2R_4C_1C_2}\right)$.

The parameters ω_o and Q of the filter can be expressed as :

$$\omega_o = \sqrt{\frac{R_3}{R_1R_2R_4C_1C_2}}$$

and

$$Q = R_5\sqrt{\frac{R_3C_2}{R_1R_2R_4C_1}} \qquad (3)$$

The sensitivities with respect to the circuit passive parameters can be written as equations :

$$S^{\omega_o}_{R_1,\,R_2,\,R_4,\,C_1,\,C_2} = -S^{\omega_o}_{R_3} = -\frac{1}{2} \qquad (4)$$

$$S^{\omega_o}_{R_5} = 0 \qquad (5)$$

$$S^{Q}_{R_1,\,R_2,\,R_4,\,C_1} = -S^{Q}_{R_4,\,C_2} = -\frac{1}{2} \qquad (6)$$

$$S^{Q}_{R_5} = 1 \qquad (7)$$

All the filter passive sensitivities are within unity in magnitude. Furthermore, if setting R_j (j = 1, 2,..., 4) = R and $C_1 = C_2 = C$, then the circuit parameters ω_o and Q-factor can be rewritten as :

$$\omega_o = \frac{1}{RC}$$

and

$$Q = \frac{R_5}{R} \qquad (8)$$

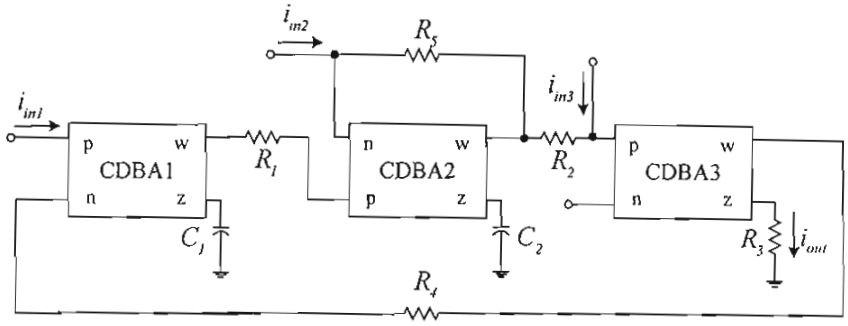


Figure 3. : The proposed current mode universal filter based on CDBAs.

It is interesting to note that the Q-factor parameter can independently be controlled by adjusting R_5/R without taking an effect to the ω_o that is adjusted by R and/or C. Moreover, the HP, LP, BP, BS and AP output currents will be obtained by selecting input currents appropriately from these specifications:

1. HP filter where $I_{in2} = I_{in3}$ are input currents and $I_{in1} = 0$.
2. LP filter where I_{in1} is an input current and $I_{in2} = I_{in3} = 0$.
3. BP filter where I_{in2} is an input current and $I_{in1} = I_{in3} = 0$.
4. BS filter where $I_{in1} = I_{in2} = I_{in3}$ are input currents and $R_5 = R$.
5. AP filter where $I_{in1} = I_{in2} = I_{in3}$ are input currents and $R_5 = 2R$.

By taking into consideration the non-idealities of the CDBA on the frequency performance, the port relations in equation (1) can be expressed as : $i_{zi} = \alpha_{pi} i_{pi} - \alpha_{ni} i_{ni}$ and $v_{wi} = \beta_i . v_{zi}$, where $\alpha_{pi} = 1 - \varepsilon_{pi}$ ($|\varepsilon_{pi}| << 1$), $\alpha_{ni} = 1 - \varepsilon_{ni}$ ($|\varepsilon_{ni}| << 1$), and $\beta_i = 1 - \varepsilon_{vi}$ ($|\varepsilon_{vi}| << 1$), and ε_{pi} and ε_{ni} are the current tracking errors from the terminal p and from the terminal n to the terminal z, and ε_{vi} is the voltage tracking error from the terminal z to the terminal w of the i-th CDBA, respectively. In this case, reanalysis the proposed filter configuration of Fig.3 yields the natural angular frequency ω'_o and quality factor Q' as :

$$\omega'_o = \sqrt{\frac{\alpha_{p1}\alpha_{p2}\alpha_{p3}\alpha_{n1}\beta_1\beta_2\beta_3 R_3}{R_1 R_2 R_4 C_1 C_2}}$$

and

$$Q' = \frac{R_5}{\alpha_{n2}}\sqrt{\frac{\alpha_{p1}\alpha_{p2}\alpha_{p3}\alpha_{n1}\beta_1\beta_3 R_3 C_2}{\beta_2 R_1 R_2 R_4 C_1}} \qquad (9)$$

The active sensitivities are written as

$$S^{\omega'_o}_{\alpha_{p1},\ \alpha_{p2},\ \alpha_{p3},\ \alpha_{n1},\ \beta_1,\ \beta_2,\ \beta_3} = \frac{1}{2} \qquad (10)$$

$$S^{\omega'_o}_{\alpha_{n2},\ \alpha_{n3}} = 0 \qquad (11)$$

$$-S^{Q'}_{\alpha_{p1},\ \alpha_{p2},\ \alpha_{p3},\ \alpha_{n1},\ \beta_1,\ \beta_3} = S^{Q'}_{\beta_2} = -\frac{1}{2} \qquad (12)$$

$$S^{Q'}_{\alpha_{n2}} = -1 \qquad (13)$$

$$S^{Q'}_{\alpha_{n3}} = 0 \qquad (14)$$

Equations (10)-(14) verify that the active sensitivities of the ω'_o and Q' with respect to α_{ni} ,α_{pi} and β_i are less than unity.

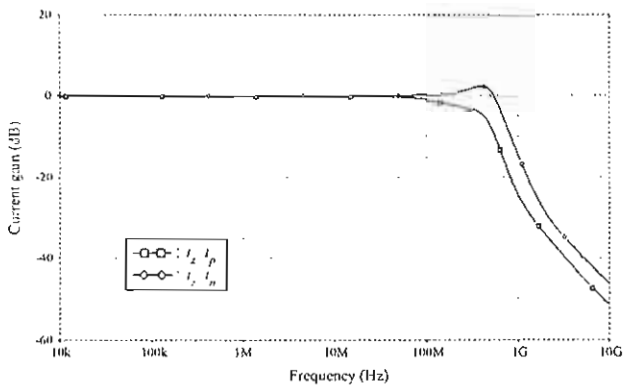
4. Simulation results

PSPICE simulation has been used to confirm the characteristics of the proposed CDBA-based universal biquadratic filter of Fig.3. The CMOS CDBA of Fig.2 has been constructed using the 0.5-μm CMOS LEVEL3 SCN05H technology supplied by MOSIS (vendor : HP-NID). The W/L ratios of all NMOS and PMOS transistors are set to 20μm/1μm and 40μm/1μm, respectively. The bias currents of I_B = 200 μA and power supply voltages of +V = -V = 1 V are used. Fig.4 shows the simulated frequency responses of the proposed filter when R_j = 1 kΩ (j = 1, 2,..., 5), excepted in AP case the resister R_5 = 2 kΩ, and $C_1 = C_2$ = 0.159 nF. This condition leads to f_o ($\omega_o/2\pi$) = 1 MHz at Q-factor = 1.

To demonstrate the independent adjustable of the ω_o without effecting the Q-factor, Fig.5 shows the BP current responses when the ω_o is respectively set to 200 kHz, 1 MHz and 5 MHz whereas Q-factor is set to constant at unity.

4. Simulation results and application

The performances of the proposed CDBA of Fig.2 has been simulated with PSPICE using the 0.5-μm CMOS LEVEL3 SCN05H technology supplied by MOSIS (vendor : HP-NID). The aspect ratios of the transistors used are W/L = 20 for the NMOS devices and W/L = 40 for the PMOS devices, respectively. The supply voltages used are $+V_{DD} = -V_{SS} = 1.25$V, and the bias currents are $I_B = 30\mu$A.



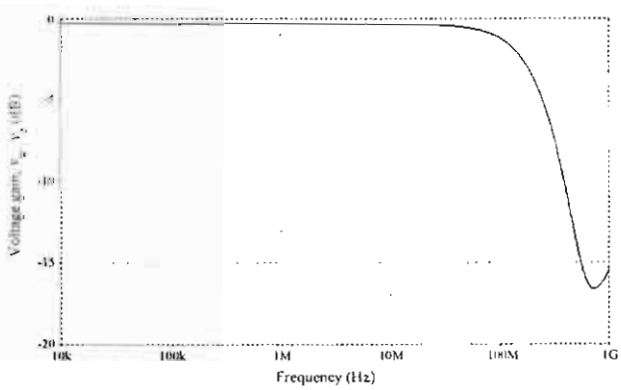


Figure 3 : Frequency characteristics of the CDBA
(a) current characteristics
(b) voltage characteristic

Fig.3 shows the simulated frequency response characteristics of the proposed CDBA, when the resistors $R_z = 1$ kΩ and $R_w = 1$ kΩ are connected at the port z and the port w, respectively. From the simulation, the current and voltage gains α_p, α_n and β_v are found to be 0.992, 0.994 and 0.962, respectively, corresponding to the errors of 0.8%, 0.6% and 3.9%, respectively.

Note that the error due to β_v can be reduced by increasing R_w. The input resistances r_p and r_n are 26Ω and the output resistances r_w and r_z are 10Ω and 200kΩ, respectively. The offset current from the ports p and n to the port z are about 0.52μA and the offset voltage from the z to w ports is 1.67 mV. The circuit power consumption for $i_p = i_n = 0$ and for $i_p = i_n = 30\mu$A are 0.62mW and 0.93mW, respectively. For the frequency response characteristics, the -3dB bandwidths of the current gains i_z/i_p and i_z/i_n, and the voltage gain v_w/v_z, are respectively located at 327MHz, 630MHz and 195MHz. This means that the performance of the proposed CDBA is excellent over a very high frequency range extending beyond 195MHz. Note that the high-frequency limitation of the circuit is due to the pole P_w at the port w, which is given by

$$P_w \cong -\left[\frac{g_{m15}R_w\left(1+\frac{g_{m18}r_{oB}}{2}\right)}{(1+g_{m15}R_w)r_{oB}C_{gs16}}\right] \tag{7}$$

Therefore, a higher frequency response can be extended by increasing the value of R_w.

In order to demonstrate the performance, a current-mode multifunction biquadratic filter as shown in Fig.4 has been simulated using the proposed CDBA, where the current transfer functions are as follows [5].

$$\frac{i_{HP}}{i_{in}} = \frac{s^2}{D(s)} \tag{8}$$

$$\frac{i_{BP}}{i_{in}} = \frac{s(1/R_3C_1)}{D(s)} \tag{9}$$

$$\frac{i_{LP}}{i_{in}} = -\frac{(1/R_2R_3C_1C_2)}{D(s)} \tag{10}$$

where $D(s) = s^2 + s\left(\frac{1}{R_1C_1}\right) + \left(\frac{1}{R_2R_3C_1C_2}\right)$.

Fig.5 shows the frequency characteristics of the highpass ($T_{HP} = i_{HP}/i_{in}$), bandpass ($T_{BP} = i_{BP}/i_{in}$) and lowpass ($T_{LP} = i_{LP}/i_{in}$) responses where R_i (i = 1, 2, 3, 4) = 3.18 kΩ and $C_1 = C_2 = 5$ pF. The filter is designed with a natural frequency of $f_o \cong 10$ MHz and Q-factor = 1. The simulated natural frequency is approximately equal to 9.77 MHz, which is found to be in good agreement with the predicted values.

Volume II

Proceedings

The Third International Symposium on Communications and Information Technologies

September 3-5, 2003

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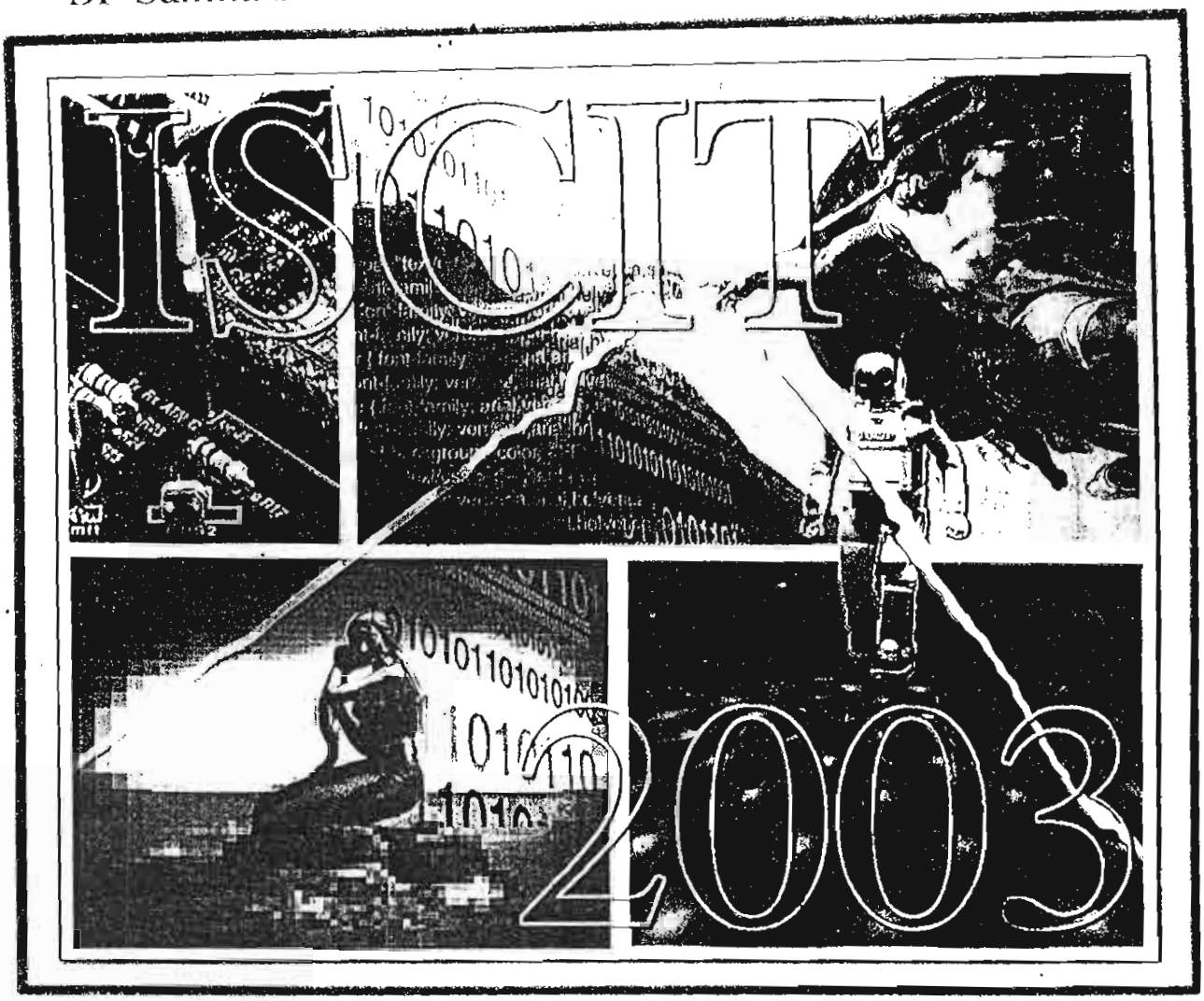


ISCIT 2003

ISBN 974-644-437-9

$$Y_n = \sum_{j=1}^{B} 2^{-j} F(X_n^j, X_{n-1}^j, X_{n-2}^j, Y_{n-1}^j, Y_{n-2}^j) - F(X_n^0, X_{n-1}^0, X_{n-2}^0, Y_{n-1}^0, Y_{n-2}^0) \quad (4)$$

where F(.) is

$$F(X_n^j, X_{n-1}^j, X_{n-2}^j, Y_{n-1}^j, Y_{n-2}^j) = a_0 X_n^j + a_1 X_{n-1}^j + a_2 X_{n-2}^j - b_1 Y_{n-1}^j - b_2 Y_{n-2}^j \quad (5)$$

Normally, 2^5 possible values of F (.) are generated from eqn. (5), rounded to B bits and stored in the memory. The signals $X_n^j, X_{n-1}^j, X_{n-2}^j, Y_{n-1}^j, Y_{n-2}^j$ are tapped from shift registers for addressing the data result contents in memory. The output Y_n is obtained by B+1 consecutive additions in the accumulator, which is shifted from the memory output [6].

2.2 Error Feedback and DA

Error Feedback (EF) is a general method that is useful in reducing the error inherent in any quantization operation. Thus, it can also help to reduce the quantization errors introduced in finite word length implementations of IIR filter [8]. To implement the system of eqn.(1), usually, the quantized value of the function F(.) is stored. However, if we apply the EF for improving the round off error, thus the eqn.(4) can be rewritten as eqn.(6) [6].

$$Y_n = \sum_{j=1}^{B} 2^{-j} \left\{ F_q(X_n^j, \ldots) + F_\varepsilon(X_n^j, \ldots) \right\} - \left\{ F_q(X_n^0, \ldots) + F_\varepsilon(X_n^0, \ldots) \right\} \quad (6)$$

where $F_q(.)$ is the quantized function of $F(.)$ and, $F_\varepsilon(.)$ is the noise function (depended on addressing). If $\bar{a}_0, \bar{a}_1, \bar{a}_2, \bar{b}_1$, and $\bar{b}_2$ are quantized coefficients. then

$$F_q(.) = \bar{a}_0 X_n^j + \bar{a}_1 X_{n-1}^j + \bar{a}_2 X_{n-2}^j - \bar{b}_1 Y_{n-1}^j - \bar{b}_2 Y_{n-2}^j \quad (7)$$

and,

$$F_\varepsilon(.) = (a_0 - \bar{a}_0) X_n^j + (a_1 - \bar{a}_1) X_{n-1}^j + (a_2 - \bar{a}_2) X_{n-2}^j - (b_1 - \bar{b}_1) Y_{n-1}^j - (b_2 - \bar{b}_2) Y_{n-2}^j \quad (8)$$

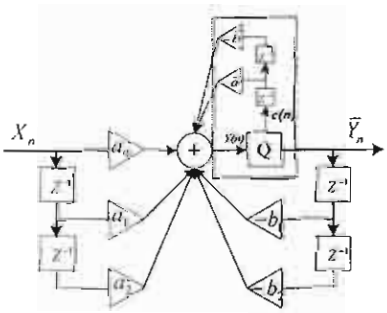


Fig.2 The 2nd order recursive digital filter with 2nd order quantizer error feedback structure

For the 2nd-order quantizer dash line block (error feedback block) shown in Fig. 2, the round off error occur in this quantizer that can be given by

$$\varepsilon_n = Y_n - \bar{Y}_n = e(n) - \tilde{a} e(n-1) + \tilde{b} e(n-2) \quad (9)$$

where the errors $e(n-1)$ and $e(n-2)$ in eqn.(9) can be pre-computed and approximated from eqn.(8), as follows

$$e(n-1) = (a_0 - \bar{a}_0) X_{n-1} + (a_1 - \bar{a}_1) X_{n-2} - (b_1 - \bar{b}_1) Y_{n-2} \quad (10)$$

$$e(n-2) = (a_0 - \bar{a}_0) X_{n-2} + (a_2 - \bar{a}_2) Y_{n-2} \quad (11)$$

Actually, $\tilde{a}$ and $\tilde{b}$ in eqn.(9) are difficult to find. Therefore, $\tilde{a}$ and $\tilde{b}$ in integer format can be used to search the grid point that will give the minimum noise. Then $F_\varepsilon(.)$ becomes

$$F_\varepsilon(.) = K_a \left\{ (a_0 - \bar{a}_0) X_{n-1}^j + (a_1 - \bar{a}_1) X_{n-2}^j - (b_1 - \bar{b}_1) Y_{n-2}^j \right\} + K_b \left\{ (a_0 - \bar{a}_0) X_{n-2}^j + (a_2 - \bar{a}_2) Y_{n-2}^j \right\} + K_c (a_2 - \bar{a}_2) Y_{n-1}^j \quad (12)$$

where K_a, K_b and K_c are integer weighting factors and accordingly and the difference filter will give the difference factors. Now the memory contents of the filter are the summing of the rounded values (4) and the pre-computed error of (9). Consequently, the filter can be represented as shown in Fig.3, which is same to that given by Peled and Liu [1], only the changing in memory contents are different. By programming LUT in VHDL formatted will give efficiently a programmable filter.

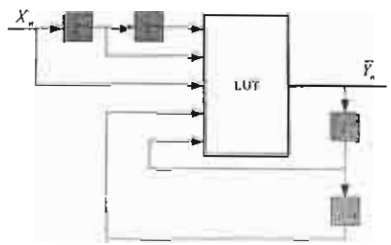


Fig.3 The 2nd-order IIR filter with error feedback

It should be noted that the round off bits are already stored in the memory. The accumulator word length can be kept to equal to the data word length, and/or extend it for the high precision filter.

3. Designing steps

The designing steps of this filter, can be separate in two main parts as shown in Fig.4.

1) Defining the Filter Specification: By using Matlab, the filter frequency response, filter coefficients, quantized coefficients are calculated. The quantized coefficients plus round off are converted to signed binary 2'complement number for programming the filter.

2) Designing through HDL language: From the DA filter structure as shown in Fig.3, we can design all components using VHDL language. Those component are comprised of parallel to serial shift registers, a look up table memory, a scaling accumulator, and controller unit. XilinxISE and Model SIM are used to design, synthesis, implement the VHDL components, and timing simulation.

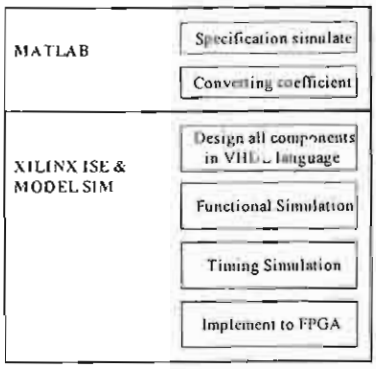


Fig.4 Steps in designing 2nd-order DA-IIR filter

Fig.5 shows the schematic diagram of the programmable 2nd-order DA IIR filter, which consists of a 8-bit PISO (Parallel in Serial out-shift register), four 8-bit SISOs (Serial in Serial out-shift registers), a 8-bit LUT (Look up table memory), and a parallel Add/Sub accumulator. The summation of the quantized coefficient, and noise error values were stored in LUT. Besides, the double precision block can be extended to the structure [7].

A brief description of the Fig.5 can be explain as following. The initial condition of the two taps (y_{n-2} and y_{n-1}) addressing from the SISOs is set to "0". During the 8-bits input data x_n from ADC is fed to a PISO, then, it is serially passed to the next registers. Each tap from the registers are connected to addressing the memory content. Every clock cycles, the data output from LUT and the filter output y_n are extended one-bit (at signed bit), after the addition in accumulator the output is valid.

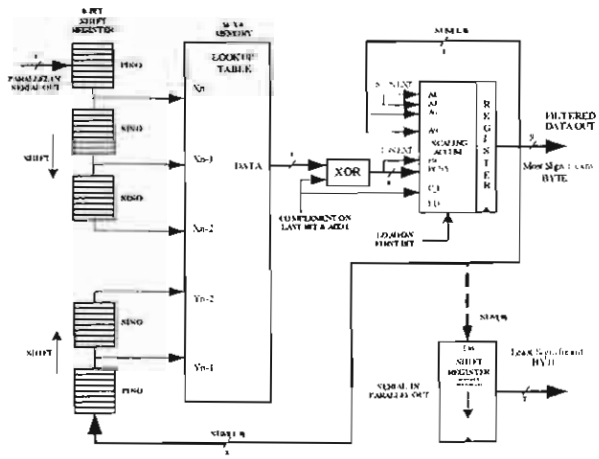


Fig.5 Hardware structure of 2nd-order DA IIR filter with error feedback

4. Simulation results and Filter Implementation

In this paper, two recursive digital filters are considered

(1) 2nd order Elliptic filter with $\omega_p = 0.4$, $A_p = 1$dB, and $A_s = 50$dB

(2) 2nd order Butterworth filter with $\omega_p = 0.3$

where ω_p is normalized passband frequency, A_p is the passband attenuation, and A_s is the stopband attenuation.

Using Matlab simulation, table 2 (a) and (b) are comparison of the reference filter coefficients and the quantized coefficients.

	Co	Quantized Coef.	Reference Coef.
Numerator	b_0	0.999969482421875	1.00000000000000000
	b_1	0.999969482421875	1.97587219341086810
	b_2	0.999969482421875	0.99999999999999922
Denominator	a_0	0.999969482421875	1.00000000000000000
	a_1	-0.350677490234375	-.35066371873525548
	a_2	0.330718994140625	.33071767543136732 0

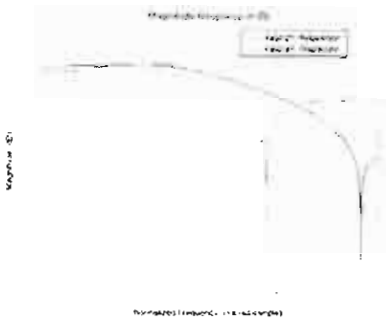
(a)

	Co	Quantized Coef.	Reference Coef.
Numerator	b_0	0.999969482421875	1.00000000000000000
	b_1	0.999969482421875	2.00000000000000000
	b_2	0.999969482421875	1.00000000000000000
Denominator	a_0	0.999969482421875	1.00000000000000000
	a_1	-0.747802734375000	-.74778917825850344
	a_2	0.272216796875000	0.27221493792500728

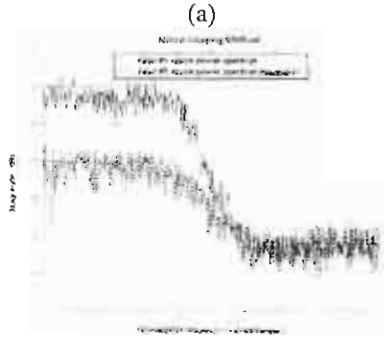
(b)

Tab.1 (a) The 2nd order Elliptic coefficients,(b) The 2nd order Butterworth coefficients

In Fig.6(a) and Fig.7(a) show the magnitude response of the two filters, which were effected by the quantization transfer function.



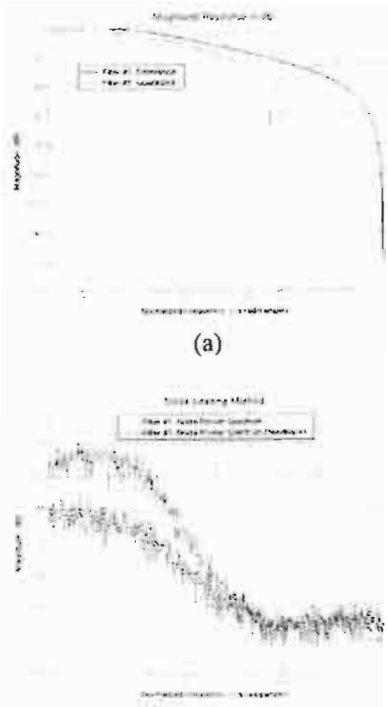
(a)



(b)

Fig.6 The 2nd order IIR Elliptic $\omega_p = 0.4$, $A_p = 1$dB, $A_s = 50$dB (a) Magnitude response. (b) Noise Loading Method.

From the Fig.6 (b) and Fig.7 (b), the solid line is a noise power spectrum of quantized filter, and the dashed line is a noise power spectrum of quantized filter with error feedback. We can see that the noise power spectrum of the EF filter can be attenuated approximate -10dB and -7dB respectively, at the transition band.



(a)

(b)

Fig.7 The 2nd order IIR Butterworth $\omega_p = 0.3$
(a) Magnitude response. (b) Noise Loading Method.

After, the specification of filter was defined and simulated. Then we start to design the hardware structures, which are realized on Xilinx FPGA (spartan2 xc2s50-tq144-5). The block components of DA-IIR filter structure from Fig.5 are written by VHDL code, after that, synthesis the VHDL code and implementation on FPGA. Fig.8 is shown the timming signals of the filter, that include the delay time on FPGA. The floor planner of realized structure can be shown in Fig.9.

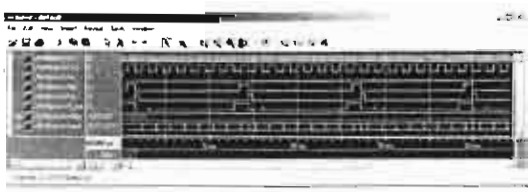


Fig.8 The timming simulation of a 2nd order DA-IIR filter.

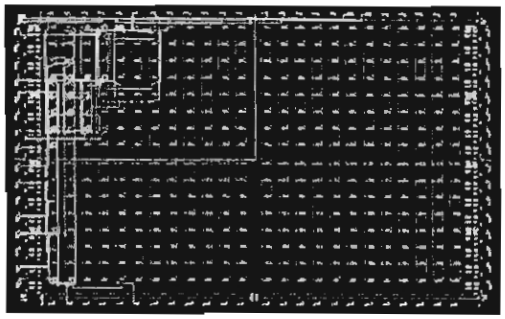


Fig.9 The floor planner of a 2nd order DA-IIR filter.

The results of implementation DA-IIR filter utilizes the environment of FPGA are as following.

Number of Slice Flip Flops:	47 out of 1,536	3%
Total Number 4 input LUTs:	30 out of 1,536	1%
Total equivalent gate count for design:	635	
Maximum Frequency:	131.631MH	

8-bits Analog to digital converter (ADC) MX7821 and Digital to analog converter (DAC) MX7224 were used in this research, and the connection of hardware circuits is shown below.

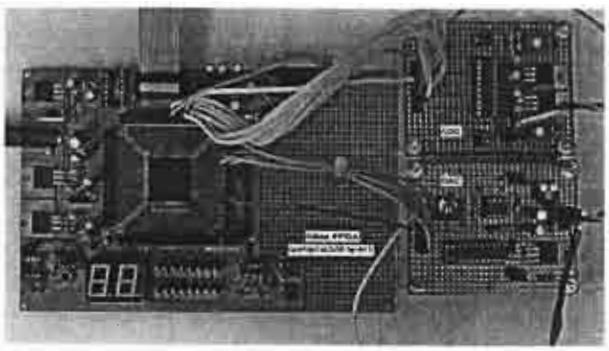


Fig.10 Interfacing analog input signal and digital output signal to FPGA board.

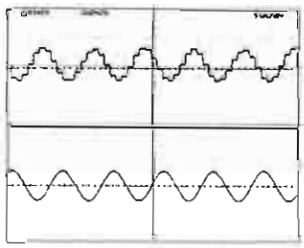


Fig.11 Analog input signal versus anolog output signal.

Cut off frequency 300KHz of 2nd order Butterworth filter is programed to the FPGA. The analog input signal with the amplitude of 2Vp-p at 120KHz is fed to ADC

MX7821, a sampling rate 1MHz, given the digital input data to FPGA. The digital output signal from FPGA is connected to DAC MX7224, conversion for analog signal as shown in Fig.11. In the transition band, the output signal without Error Feedback was gave noise magnitude more than Error Feedback output, which is agree to the simulation serult. Generally, most of digital filters are in higher order form; however, the order of filter can be increased from second order to N time of second order by cascading the group of 2nd order filter as demonstated in Fig.12.

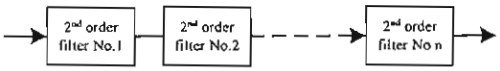


Fig.12 Block diagram of the cascade 2n-order filter

5. Conclusions

In this paper, the method has been introduced of programmable direct form digital filter realization. The lookup table contents of memory were modified for reducing coefficient round off noise, noise feedback was included in the memory. Designing steps and implementation have shown that reduction in noise output and low hardware size could be achieved by such a realization.

ACKNOWLEDGMENT

This work is funded by the Thailand Research Fund (TRF) through the Senior Research Scholar Program, grant number RTA/04/2543. The Support by The Japan International Coorperation Agency (JICA) is also acknowledge.

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การประชุมวิชาการ ทางวิศวกรรมไฟฟ้า ครั้งที่ 25

25th Electrical Engineering Conference

(EECON - 25)

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ณ ภาควิชาวิศวกรรมไฟฟ้า คณะวิศวกรรมศาสตร์

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ดำเนินการจัดการประชุมโดย

ภาควิชาวิศวกรรมไฟฟ้า คณะวิศวกรรมศาสตร์

มหาวิทยาลัยสงขลานครินทร์

การพัฒนาวิทยุติดตามตัวในระบบ POCSAG โดยใช้เอฟพีจีเอ

On the Implementation of Pocsag Paging using FPGA

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บทคัดย่อ

บทความนี้เสนอการพัฒนาวิทยุติดตามตัวในระบบ Pocsag ซึ่งสามารถแสดงข่าวสารข้อมูลได้ทั้งในรูปแบบตัวอักษรภาษาไทยและแบบภาษาอังกฤษ โดยระบบจะประกอบไปด้วย ภาครับสัญญาณวิทยุย่านความถี่สูง และภาคการทำงานทางด้านดิจิตอล ซึ่งได้แก่ ภาคถอดรหัสเพจเจอร์ ภาคถอดรหัสหมายเลขเรียกขาน และภาคแสดงผล โดยการออกแบบอยู่ในชิฟวงจรรวม ซึ่งแนวทางการพัฒนาใช้ภาษาวีเอชดีแอลในการบรรยายพฤติกรรมของฮาร์ดแวร์ที่ทำการออกแบบแล้วโปรแกรมลงในชิฟเอฟพีจีเอ

คำสำคัญ : โดยออกแบบเป็นชิฟวงจรรวม,วีเอชดีแอล,เอฟพีจีเอ

Abstract

This paper presents the development of a Pocsag pager which has the capability of displaying text both in Thai and English. The pager system consists of the VHF receiver part and the digital part, Which comprises pager decoder, address codeword decoder and LCD graphic display, is designed using VHDL to describe the behavior of the designed hardware, and programmed onto the FPGA chip.

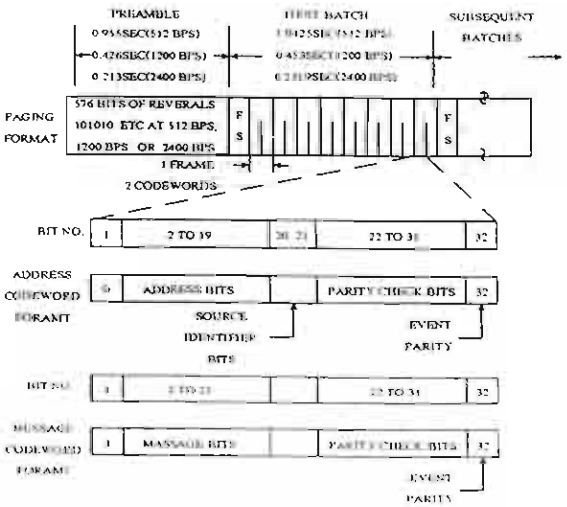
Keywords : VHDL, FPGA ,POCSAG

1. คำนำ

ในปัจจุบันการออกแบบชิฟวงจรรวมทางด้านวงจรดิจิตอลโดยใช้ภาษาวีเอชดีแอลในการอธิบายการทำงานของวงจรจะมีประสิทธิภาพมากยิ่งขึ้นทั้งในด้านขนาดของวงจรที่เล็กลงและมีการทำงานที่เร็วขึ้น ซึ่งบทความนี้จะเสนอการพัฒนาวิทยุติดตามตัวในระบบ POCSAG ซึ่งมีอัตราในการส่งข้อมูล 1200 บิทต่อวินาที โดยจุดประสงค์ก็เพื่อพัฒนาเป็นชิฟวงจรรวมในภาคการทำงานทางด้านวงจรดิจิตอลของวิทยุติดตามตัวเพื่อสามารถที่จะนำไปประยุกต์ใช้งานกับระบบอื่นๆให้มีความหลากหลายในการใช้งานมากยิ่งขึ้น เช่นการสั่งงานผ่านวิทยุติดตามตัวในการป้องกันความปลอดภัยจากการโจรกรรมรถหรือการควบคุมการสั่งงานอุปกรณ์ไฟฟ้าภายในบ้านเป็นต้น ซึ่งข้อดีของระบบสื่อสารแบบ เพจเจอร์ที่สามารถส่งข้อมูลได้ทั่วประเทศและมีความถูกต้องในการรับส่งข้อมูลตลอดจนการใช้งานของการให้บริการก็ยังมีอยู่อย่างต่อเนื่องอยู่ในหลายๆบริษัท จึงสามารถนำไปประยุกต์ใช้งานได้หลายรูปแบบโดยไม่ต้องยึดติดกับเครื่องรับวิทยุติดตามตัวที่สั่งเข้าจากต่างประเทศจึงมีแนวความคิดที่จะทำการออกแบบขึ้นมาเพื่อพัฒนาเทคโนโลยีภายในประเทศ

2. รูปแบบรหัสของเพจเจอร์

รหัสเพจเจอร์ที่ใช้กันอยู่ในประเทศปัจจุบันจะมีมาตรฐานในการสื่อสารข้อมูลที่แตกต่างกัน ซึ่งรหัสเพจเจอร์แบบ POCSAG (Post Office Code Standard Advisory Group)[1] ก็เป็นมาตรฐานหนึ่งที่มีรูปแบบการส่งสัญญาณแบบอะซิงโครไนซ์โดยรูปแบบของสัญญาณจะประกอบไปด้วย 2 ส่วน คือส่วนแรกเป็นพรีแอมเบิ้ล (Preamble) และตามด้วยรหัสคำที่เป็นส่วนของข้อมูลหรือหมายเลขเรียกขานซึ่งจะเริ่มด้วยเฟรมด้วยรหัสซิงโครไนซ์ หรือเฟรมซิงโครไนซ์ (Frame Synchronize) โดย รายละเอียดในส่วนต่างๆนั้นได้แสดงไว้รูปที่ 1

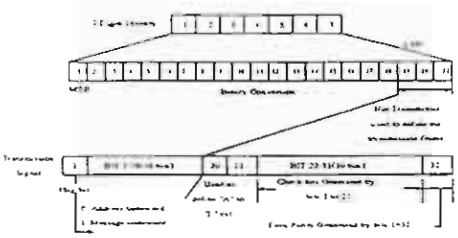


รูปที่ 1 รูปแบบรหัสเพจเจอร์แบบ POCSAG

2.1 พรีแอมเบิ้ล (Preamble) จะมีขนาด 576 บิท จะทำการส่ง "0" และ "1" สลับกันไป ใช้สำหรับกำหนดจุดเริ่มต้นการทำงานและการกู้สัญญาณนาฬิกาที่ภาครับ

2.2 รหัสคำ(Code Word) รหัสคำที่บรรจุแต่ละแบตช์จะเริ่มต้นรหัสคำด้วยรหัสคำซิงโครไนซ์ ซึ่งเป็นรหัสเฉพาะที่มีขนาด 32 บิท และตามด้วยเฟรมของรหัสคำอีก 8 เฟรมโดยแต่ละเฟรมจะมีขนาด 64 บิท หรือ 2 รหัสคำซึ่ง แบ่งรหัสคำได้เป็น

2.2.1 รหัสคำหมายเลขเรียกขาน (Address Codewords) รหัสคำหมายเลขเรียกขานจะมีบิทแรกเป็น "0" เสมอ โดยบิทที่ 2 ถึง 19 เป็นหมายเลขเรียกขาน ซึ่งสร้างขึ้นจากรหัสประจำเครื่อง (Radio Identity Code : RIC) โดยจะมีขนาด 7 หลัก แล้วนำเลข 7 หลักนี้มาแปลงเป็นเลขฐานสองจำนวน 21 บิท ซึ่ง 18 บิท ที่มีความสำคัญมากจะถูกนำมาใช้และส่งออกไป ในส่วนของอีก 3 บิท ที่มีความสำคัญน้อยจะไม่ส่งออกไป แต่จะใช้เป็นตัวกำหนดหมายเลขของเฟรม(0–7)ว่ารหัสเรียกขานถูกส่งไปเฟรมใด ส่วนบิทที่ 20 และ 21 ใช้สำหรับเลือกกลุ่มของหมายเลขเรียกขานซึ่งมีอยู่ 4 กลุ่ม ส่วนบิทที่ 22 ถึง 31 จะเป็นบิทที่ใช้สำหรับตรวจสอบข้อมูลและแก้ไขการผิดล่วงหน้าโดยใช้การตรวจสอบแบบ BCH สำหรับการใช้บิทตรวจสอบ 10 บิทสำหรับข่าวสาร 21 บิททำให้ตรวจสอบการผิดของบิทได้ 4 บิท และแก้ไขการผิดของบิทได้ 2 บิท สำหรับบิทสุดท้ายเป็นบิทพาริตี้ ซึ่งเป็นแบบพาริตี้คู่ (Even Parity) รูปแบบรหัสคำหมายเลขเรียกขานแสดงได้ดังรูปที่ 2



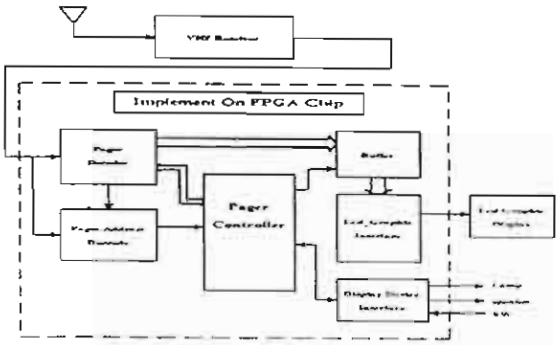
รูปที่ 2 รูปแบบรหัสหมายเลขเรียกขาน

2.3 รหัสคำข่าวสาร (Message Codeword) รหัสคำข่าวสารจะเริ่มต้นบิทแรกเป็น 1 โดยข่าวสารข้อมูลซึ่งบรรจุอยู่ในบิทที่ 2 ถึง บิทที่ 21 จะมีขนาด 8 บิท ต่อ 1 ตัวอักษรโดยมี รูปแบบตัวอักษรภาษาอังกฤษเป็นไปตามมาตรฐาน ASCII Code และ อักษรภาษาไทย อยู่ในรูปแบบตัวอักษรตามมาตรฐานของ สมอ จากการที่แต่ละตัวอักษรมีขนาด 8 บิททำให้ใน 1 รหัสคำบรรจุอักษรได้ 2 ตัวอักษรกับอีก 4 บิทซึ่งหมายความว่าบิทของตัวอักษรตัวท้ายจะต้องถูกเลื่อนไปอยู่ในรหัสคำอื่น

2.4 รหัสคำว่าง (Idle Codeword) รหัสคำว่างเป็นรหัสใช้สำหรับใส่รหัสลงในแบตช์ให้ครบ 8 เฟรม ในกรณีที่ข่าวสารส่งมาสิ้นสุดก่อนที่จะครบแบตช์โดยรูปแบบของคำคือ " 01111010100100111000011001011 "

3. การออกแบบฮาร์ดแวร์

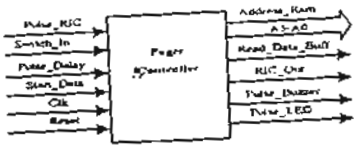
สำหรับแนวทางการพัฒนาวิทยุติดตามตัวในระบบ POCSAG [2] จะประกอบไปด้วยส่วนต่างๆคือภาครับสัญญาณวิทยุ (Receiver) ทำหน้าที่รับสัญญาณวิทยุที่ส่งข้อมูลเพจเจอร์ในย่านความถี่ VHF แล้วแปลงสัญญาณวิทยุเป็นสัญญาณดิจิตอลบสแบนด์ ส่วนภาคถอดรหัสเพจเจอร์ (Pager Decoder) จะถอดรหัสดิจิตอลเบสแบนด์เป็นรูปแบบรหัส POCSAG ให้เก็บในหน่วยความจำ (Static RAM : SRAM) ส่วนถอดรหัสสัญญาณเรียกขาน (Address Codeword Decoder) สามารถโปรแกรมค่า Address ใดๆก็ได้เมื่อมีสัญญาณเพจเจอร์เข้ามาส่วนการถอดรหัสสัญญาณเรียกขานจะเปรียบเทียบค่ารหัสของเครื่องที่ตั้งไว้กับสัญญาณที่รับเข้ามาโดยถ้าหากสัญญาณเรียกขานรับมาตรงกับค่าที่ตั้งไว้ก็จะเกิดสัญญาณอินเตอร์รัพท์ (Interrupt) เพื่อให้ภาคเชื่อมต่ออุปกรณ์แสดงผล (Display Device - Interface) จะแสดงผลเมื่อเริ่มรับข่าวสารข้อมูลเข้ามาส่วนภาคแสดงข้อมูลจะใช้กราฟฟิกแอลซีดี (Lcd Graphic Display) เป็นตัวแสดงข่าวสารข้อมูลที่รับเข้ามา แสดงดังรูปที่ 3



รูปที่ 3บล็อกไดอะแกรมเครื่องรับวิทยุติดตามตัวระบบ POCSAG

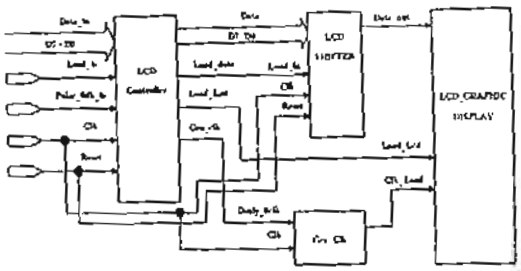
3.1 ภาครับสัญญาณวิทยุ (VHF Receiver)[3] การออกแบบภาครับสัญญาณวิทยุได้ออกแบบให้มีการรับสัญญาณเพจเจอร์ในย่านความถี่ 279.55 MHz ซึ่งเป็นความถี่ให้บริการในโหมดตัวอักษรโดยตัวอักษรจะถูกมอดูเลทแบบ Frequency Shift Keying โดยมีความถี่เบี่ยงเบนเท่ากับ ± 4.5 KHz ด้วยขนาดของบิทเรทข้อมูลเท่ากับ 1200 บิทต่อวินาที โดยการออกแบบล็อกใช้วงจรรวมเบอร์ MC3362 ของบริษัท Motola ซึ่งเป็นวงจรที่ทำหน้าที่ถอดสัญญาณวิทยุ FM แบบแบนด์แคบมีเอาท์พุทของภาคดีเทคสัญญาณ FSK โดยภายในจะเป็นภาครับแบบดูออลคอนเวอร์ชั่น (Dual Conversion) ใช้ความถี่ IF ภาคที่ 1 เท่ากับ 10.7 MHz และภาคที่ 2 เท่ากับ 455KHz โดยมีวงจรออสซิลเลเตอร์ภายในสำหรับผลิตความถี่เพื่อสร้างสัญญาณ IF ภาคที่ 1 สามารถผลิตความถี่ได้ถึง 200 MHz และภาคผลิตความถี่สำหรับสร้างสัญญาณ IF ภาคที่ 2 ซึ่งผลิตความถี่ขนาด 10.245 MHz โดยควบคุมความถี่ด้วยคริสตอลส่วนภาคดีเทคสัญญาณเป็นวงจรแบบควอดราเจอร์ดิสคริมิเนเตอร์ (Quadrature Discriminator)

3.5 ภาคควบคุมระบบเพจเจอร์ (Pager Controller) ทำหน้าที่ควบคุมการการเขียน-อ่านข้อมูลและสัญญาณควบคุมต่างๆในระบบดังรูปที่ 8



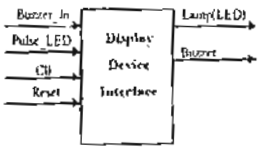
รูปที่ 8 บล็อกไดอะแกรมภาคควบคุมระบบ

3.6 ภาคแสดงผล (Display) เป็นภาคแสดงข่าวการข้อมูลโดยใช้อุปกรณ์กราฟฟิกแอลซีดี [6] เป็นตัวแสดงผลข้อมูลที่รับเข้ามาโดยสามารถแสดงผลได้ทั้งภาษาไทยและภาษาอังกฤษตามมาตรฐานสมอ.โดยมีขนาด 128×64 DOT สามารถแสดงตัวอักษรไทย และภาษาอังกฤษได้ 16×4 บรรทัด ซึ่งลักษณะการส่งข้อมูลจะทำการส่งข้อมูลแบบ 3 Bit Serial โดยมีภาคควบคุมการทำงานแสดงดังรูปที่ 9



รูปที่ 9 บล็อกไดอะแกรมภาคเชื่อมต่อกราฟฟิกแอลซีดี

3.7 ภาคเชื่อมต่ออุปกรณ์แสดงผล (Display Device Interface) ทำหน้าที่แสดงผลการเรียกเพจเจอร์โดยจะแสดงไฟและส่งเสียงเตือนเมื่อมีการเรียกเพจเจอร์ แสดงดังรูปที่ 10

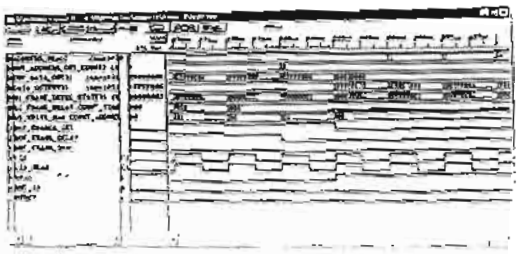


รูปที่ 10 บล็อกไดอะแกรมภาคเชื่อมต่ออุปกรณ์แสดงผล

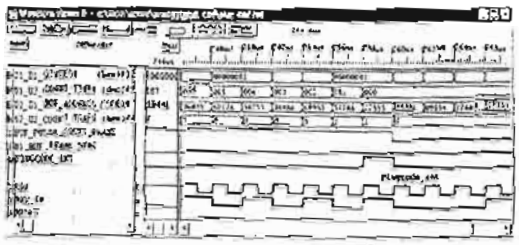
4. ผลการทดสอบ

ศึกษาการทำงานทั้งหมดของวงจรจากนั้นสร้างเป็นโมดูลของวงจร โดยใช้ภาษาวีเอชดีแอล (VHDL) ในการเขียนพฤติกรรมของวงจร (Behavioral) [4] ในแต่ละส่วนการทำงานของวงจรที่แบ่งไว้และทำการสังเคราะห์ (Synthesis Tools) โมดูลของวงจรต่างๆเพื่อให้ได้ฮาร์ดแวร์ที่เหมาะสมสอดคล้องกับความเร็วในการทำงานของวงจรเพื่อนำไปทดสอบกับชิปเอฟพีจีเอต่อไปส่วนโปรแกรมการออกแบบวงจรจะพัฒนาด้วยภาษาวีเอชดีแอลแล้วนำมาสังเคราะห์วงจรตลอดจนการโปรแกรมลงชิปเอฟพีจีเอโดยใช้โปรแกรม Xilinx Foundation F2.1i และชิปเอฟพีจีเอ (FPGA) ของบริษัท Xilinx

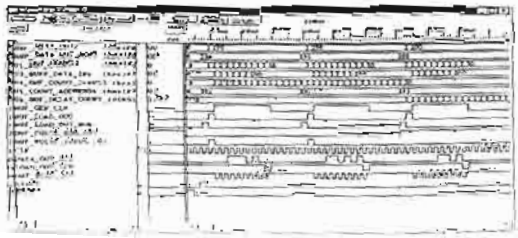
4.1 VHDL Simulation ทำการจำลองการทำงาน (Simulation) ของวงจรทั้งหมดที่ได้จากการใช้ภาษาวีเอชดีแอลอธิบายพฤติกรรมของวงจรโดยกำหนดรูปแบบสัญญาณอินพุทตามมาตรฐานรูปแบบของรหัส POCSAG แล้วป้อนเข้าไปในระบบเพื่อดูผลจำลองการทำงานของระบบโดยภาคถอดรหัสสัญญาณจะทำการเก็บข้อมูลและอ่านข้อมูลขนาด 32 บิทจาก SRAM ซึ่งแสดงผลดังรูปที่ 11 ส่วนภาคถอดรหัสหมายเลขเรียกขานทำหน้าที่ ตรวจสอบหมายเลขเรียกหมายโดยจะกำเนิดสัญญาณพัลซ์เพื่อแจ้งให้ทราบถึงการรับส่งข้อมูลแสดงดังรูปที่ 12 และภาคแสดงผลกราฟฟิกแอลซีดี จะรับข้อมูลข้ามาขนาด 8 บิทและทำการส่งข้อมูลเป็นแบบ 3 Bit Serial ซึ่งแสดงดังรูปที่ 13



รูปที่ 11 เขียน-อ่านข้อมูลจาก SRAM ในภาคถอดรหัสสัญญาณ



รูปที่ 12 สัญญาณรหัสหมายเลขเรียกขาน



รูปที่ 13 ผลการรับข้อมูลภาคแสดงผลกราฟฟิกแอลซีดี

re: An integrable temperature-sensitive gm-RC quadrature oscillator

authors: Kiattisak Kumwachara and Wanlop Surakampontorn

I am pleased to advise you that the above paper has been accepted for publication in the International Journal of Electronics.

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To: Kiattisak Kumwachara <kkkiatti@kmitl.ac.th>
Subject: Re: Manuscript (IJE/2001/125)

[Part 1, Text/PLAIN 5 lines.]

[Unable to print this part.]

[Part 2, Text/PLAIN (charset: ISO-8859-1 "Latin 1") 90 lines.]

[Unable to print this part.]

[The following text is in the "iso-8859-1" character set.]

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[Some characters may be displayed incorrectly.]

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Editorial Assistant

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Faculty of Engineering

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Sunday, 05 October 2003

Dear Dr Kumwachara

ref: IJE/2001/125

An integrable temperature-insensitive g_m–RC quadrature oscillator

Kiattisak Kumwachara and Wanlop Surakampontorn

The authors are with
The Faculty of Engineering and
The Research Center for Communication and Information Technology (ReCCIT)
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Ladkrabang Bangkok THAILAND 10520

A novel g_m-RC quadrature oscillator using operational transconductance amplifiers (OTAs) and grounded passive elements is proposed. The circuit provides two quadrature outputs of equal magnitude and the oscillation frequency is insensitive to temperature. The oscillation frequency can be linearly and electronically controlled without affecting the condition of oscillation. The active ω_o-sensitivity has been shown to be small. Experimental and simulation results that demonstrate the performance of the proposed oscillator are also included.

1. Introduction

It is well accepted that sinusoidal oscillators realized with operational transconductance amplifier (OTAs), transconductance-C or g_m–C technique, provide highly linear electronic tunability and have more reliable high-frequency performance than the operational amplifier based oscillators. Moreover the g_m–C sinusoidal oscillator circuits are suitable for integrated circuit implementation both in bipolar and CMOS technologies (Abuelma'atti 1989, Senani 1989, Linaress-Barranco et al. 1991). In recent years, a quadrature oscillator, which is typically an oscillator that provides two sinusoidal outputs with 90° phase difference, has received some attention (Ahmed et al. 1997, Srisuchinwong 2000, Khan and Khwaja 2000). The quadrature oscillator is an important unit in many applications in communication, signal processing and instrumentation systems. Some g_m–C based quadrature oscillators have been reported (Ahmed et al. 1997, Khan and Khwaja 2000). However, due to the transconductance gain g_m of the bipolar OTA is inversely proportional to temperature; this causes the characteristic of OTA-based circuit to be strongly dependent on the temperature which is undesirable. There is no any paper proposed a technique for g_m-RC oscillator that the oscillating frequency is insensitive to temperature. Although, a bias circuit with a current linearly proportional to temperature has been introduced recently for the temperature compensation of OTA-based circuits (Surakampontorn et al. 1998). But, however, due to the bias circuit, the OTA transconductance gain can be accurately tuned only for two decades.

In this paper, a novel technique is proposed to realize g_m–RC quadrature oscillator using bipolar OTAs, where the oscillating frequency ω_o is temperature-insensitive and the entire passive element is grounded. The frequency of oscillation of

frequency plane, hence avoiding the oscillation to begin. A practical oscillator must include some from of regeneration to ensure that the roots are initially located in the right half plane and hence that the oscillation is created (Rodriguez-Vazquez et al. 1990). We can see that by adjusting OTA5 and OTA6 the pole can be positioned close to the imaginary axis for $g_{m5}=g_{m6}$. For the case $g_{m5}>g_{m6}$ means that the roots of

characteristic equation are initially inside the right plane, it ensures that the system is self-starting. On the other hand, for the case that $g_{m5}<g_{m6}$ means that there roots move towards the left-half plane once the oscillation amplitude increases. Therefore, in order to initially locate the poles inside the right-half complex frequency plane to assure self-starting operation, the condition for the oscillation can be stated as

$$g_{m5} - g_{m6} \geq \varepsilon \tag{4}$$

or

$$I_{B5} - I_{B6} \geq \varepsilon \tag{5}$$

where ε is a small positive number. The oscillating frequency is

$$\omega_O = \sqrt{\frac{g_{m2} g_{m4}}{R_1 R_2 C_1 C_2 g_{m1} g_{m3}}} \tag{6}$$

For simplicity, if we select $R_1=R_2=R$, $C_1=C_2=C$, $g_{m2}=g_{m4}=I_{B2}/2V_T$ and $g_{m1}=g_{m3}=I_{B1}/2V_T$, the frequency of oscillation can be given by

$$\omega_O = \frac{g_{m2}}{g_{m1}}\left(\frac{1}{RC}\right) = \frac{I_{B2}}{I_{B1}}\left(\frac{1}{RC}\right) \tag{7}$$

It is obvious from the eqns. (5) and (7) that the oscillation frequency can be tuned without disturbing the oscillation condition. Moreover, the frequency of oscillation ω_o is temperature independent and can be linearly controlled by adjusting the DC bias current $I_{B2} = I_{B4}$.

4. Error analysis

In practice, the accuracy of the V/I circuit and the accuracy of the OTA transconductance gains are the major factors that contribute to the deviation from the ideal performance. The first factor is due to the accuracy of the V/I circuit. Using the eqn. (1), the characteristic equation of the oscillator can be given by

$$s^2 - s\left(\frac{g_{m5} - g_{m6}}{C_2}\right) + \frac{g_{m2} g_{m4}}{C_1 C_2 (1 + g_{m1} R_1)(1 + g_{m3} R_2)} = 0 \tag{8}$$

The frequency of oscillation can now be written from the eqn. (8) as

$$\omega_{OE} = \sqrt{\frac{g_{m2} g_{m4}}{C_1 C_2 (1 + g_{m1} R_1)(1 + g_{m3} R_2)}} \tag{9}$$

If we let ε_ω is the oscillating frequency error, by comparing with the eqn. (6), the frequency ω_{OE} can be rewritten as

$$\omega_{OE} = \omega_O (1 - \varepsilon_\omega) \tag{10}$$

Then, the oscillating frequency error is

$$\varepsilon_{\omega} = \left\{ \frac{1}{1 + \dfrac{g_{m1} g_{m3} R_1 R_2}{1 + g_{m1} R_1 + g_{m3} R_2}} \right\} \times 100\% \tag{11}$$

For example, if g_{m1}=0.0192 A/V, g_{m3}=0.0096 A/V, R_1=10 kΩ and R_2=50 kΩ then the error of less than 0.72% is obtained. This error can be further reduced by increasing the value of the term $g_{m1}g_{m3}R_1R_2$.

The second factor is the temperature dependence of transconductance gains g_{m1} and g_{m3} and the resistors R_1 and R_2 that affects the oscillating frequency ω_{OE}. In this case, the percentage error of the ω_{OE} that due to the variation of g_{m1}, g_{m3}, R_1 and R_2 can be expressed as

$$\frac{\delta\omega_{OE}}{\omega_{OE}} \cong \left\{ \frac{-1}{1 + \dfrac{I_{B1} I_{B3} R_1 R_2}{4V_T^2 + (I_{B1} R_1 + I_{B3} R_2) V_T}} \right\} \frac{\Delta T}{T} \times 100\% \tag{12}$$

where the T is the room temperature and ΔT is the change of temperature from room temperature. It is clearly seen from the eqn. (12) that the temperature influence can be reduced by increasing the value of the term $I_{B1}I_{B3}R_1R_2$. For example, if V_T = 26mV at room temperature, I_{B1} = 1000μA, I_{B3} = 100μA, R_1=10 kΩ, R_2=100 kΩ, and ΔT =25°C, then the percentage error of ω_{OE} is about 0.04 % for the case of temperature compensated. However, for the uncompensated (I_{B1}=0 and I_{B3}=0) case, the percentage error of ω_{OE} is about 8.39 %. This demonstrates that the temperature influence can be must reduced by the proposed scheme.

The third factor is the ω_{OE} sensitivity that can be given by

$$S_{g_{m2}}^{\omega_{OE}} = S_{g_{m4}}^{\omega_{OE}} = \frac{1}{2}, \quad S_{C_1}^{\omega_{OE}} = S_{C_2}^{\omega_{OE}} = -\frac{1}{2} \tag{13}$$

and

$$S_{g_{m1}}^{\omega_{OE}} = S_{R_1}^{\omega_{OE}} = -\frac{1}{2}\left(\frac{g_{m1} R_1}{1 + g_{m1} R_1} \right), \quad S_{g_{m3}}^{\omega_{OE}} = S_{R_2}^{\omega_{OE}} = -\frac{1}{2}\left(\frac{g_{m3} R_2}{1 + g_{m3} R_2} \right) \tag{14}$$

We can see that all the sensitivities with respect to the circuit passive and active elements has very low sensitivity, approximately 0.5.

5. Experimental and simulation results

The circuit of Fig. 2 was constructed using the LM13600-type OTA, 1-% tolerance discrete resistors and polystyrene capacitors. Fig. 3 shows the results obtained with R_1=R_2=10kΩ, C_1=C_2=0.5nF, I_{B1}=I_{B3}=500μA, I_{B2}=I_{B4}=785μA, I_{B5}=

CAPTION ON THE FIGURES

Figure 1 Circuit diagram of the OTA-based temperature-insensitive V/I
Figure 2 The g_m-RC quadrature oscillator with temperature-compensation
Figure 3 Experimental results of the g_m-RC quadrature oscillator
(Vertical scale: 2V/divider. Horizontal scale: 5 μs/divider)
Figure 4 Variation of the frequency of oscillation with the DC bias current $I_{B2}=I_{B4}$
Figure 5 Variation of the frequency of oscillation against temperature

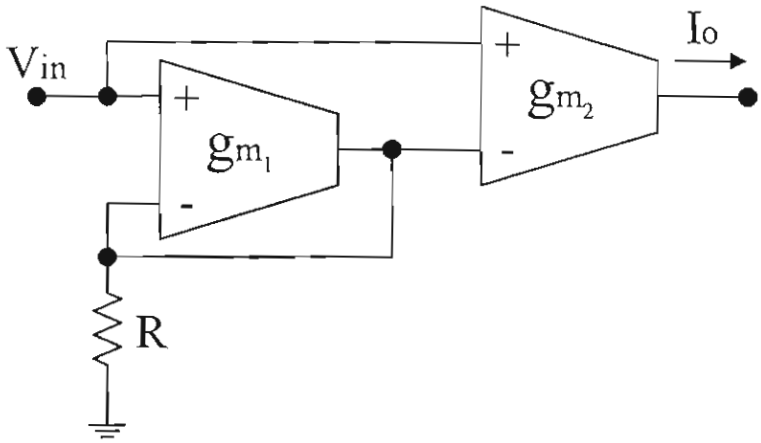

Figure 1 K.Kumwachara and W.Surakampontorn

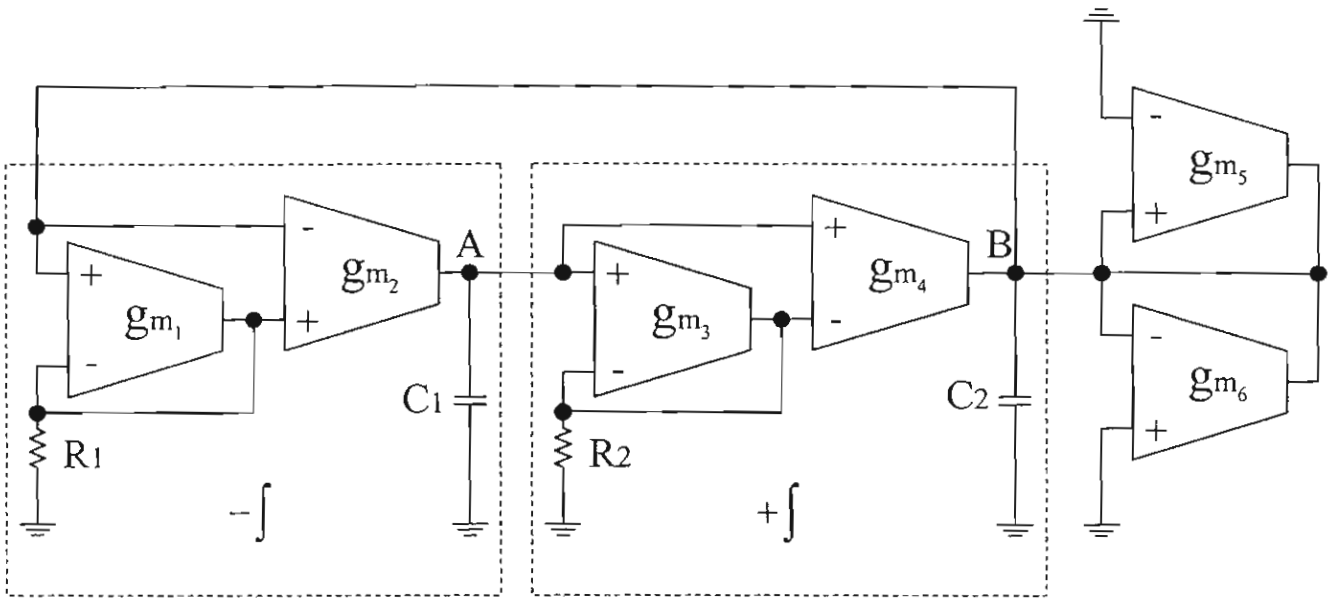

Figure 2 K.Kumwachara and W.Surakampontorn

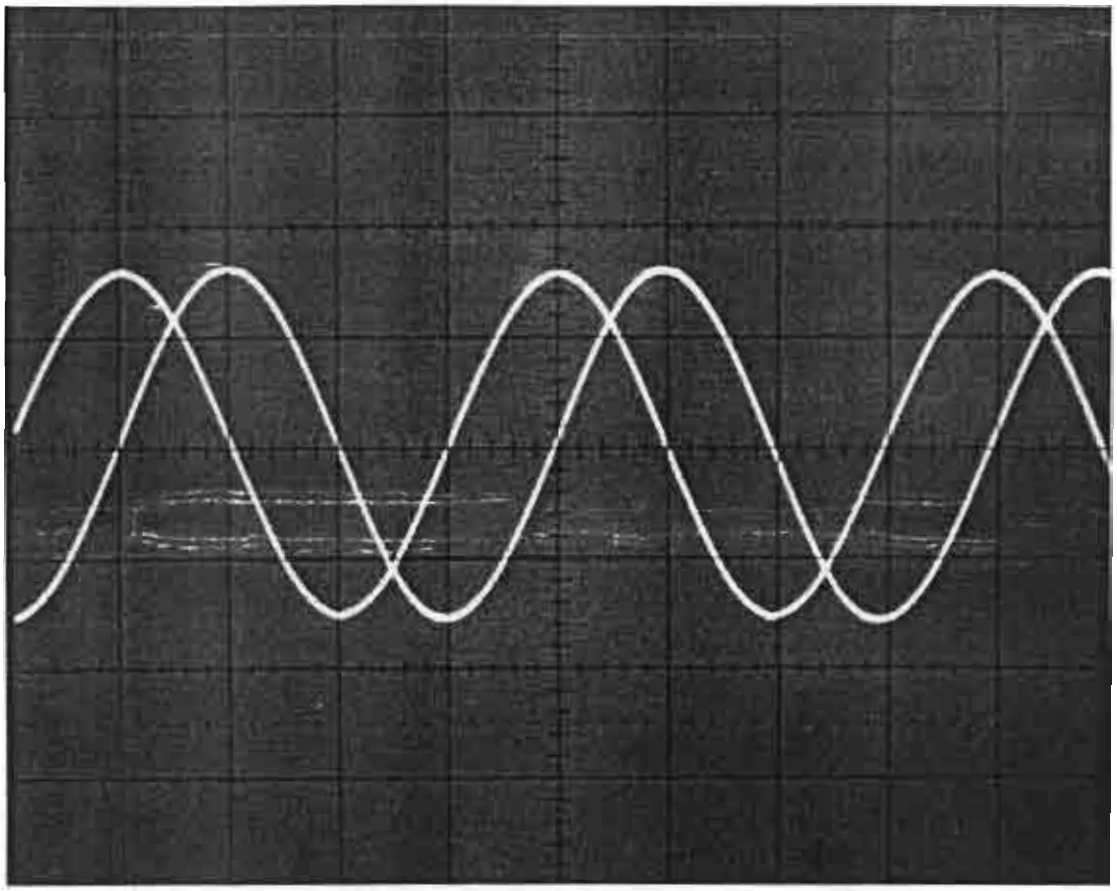

Figure 3 K.Kumwachara and W.Surakampontorn

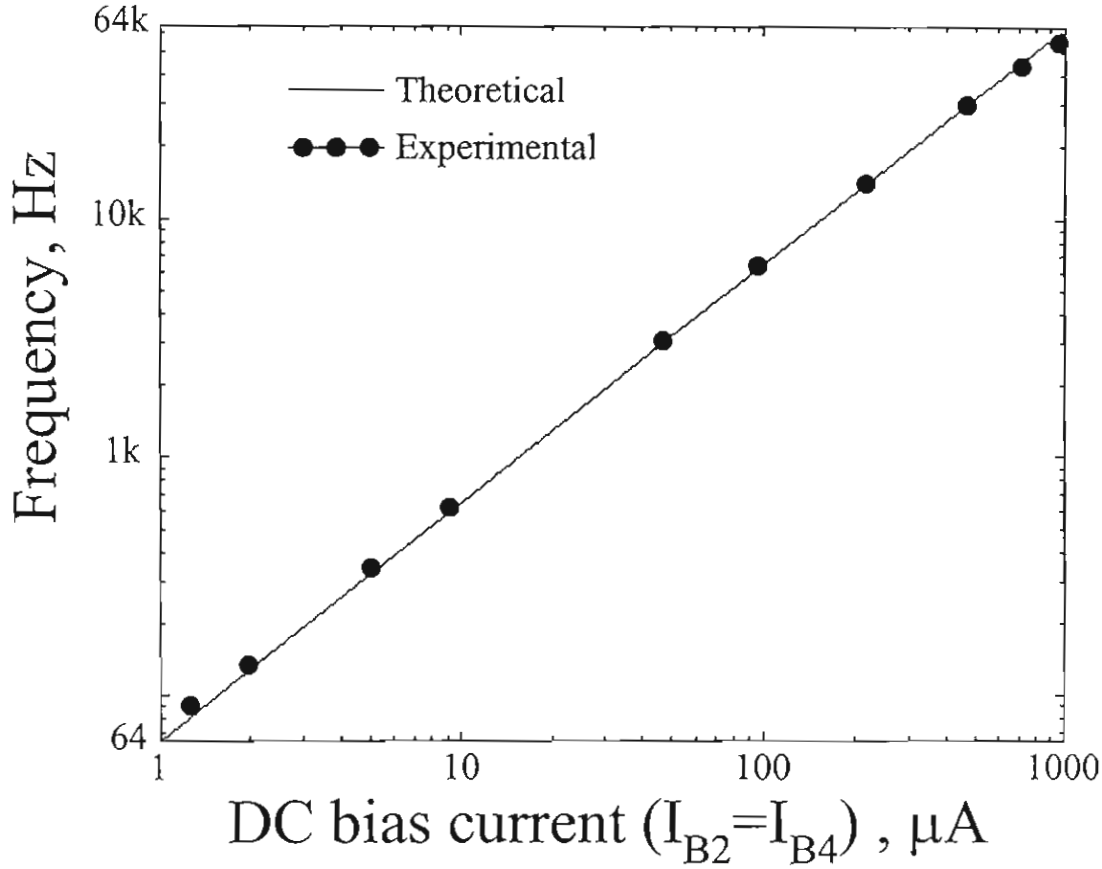

Figure 4 K.Kumwachara and W.Surakampontorn

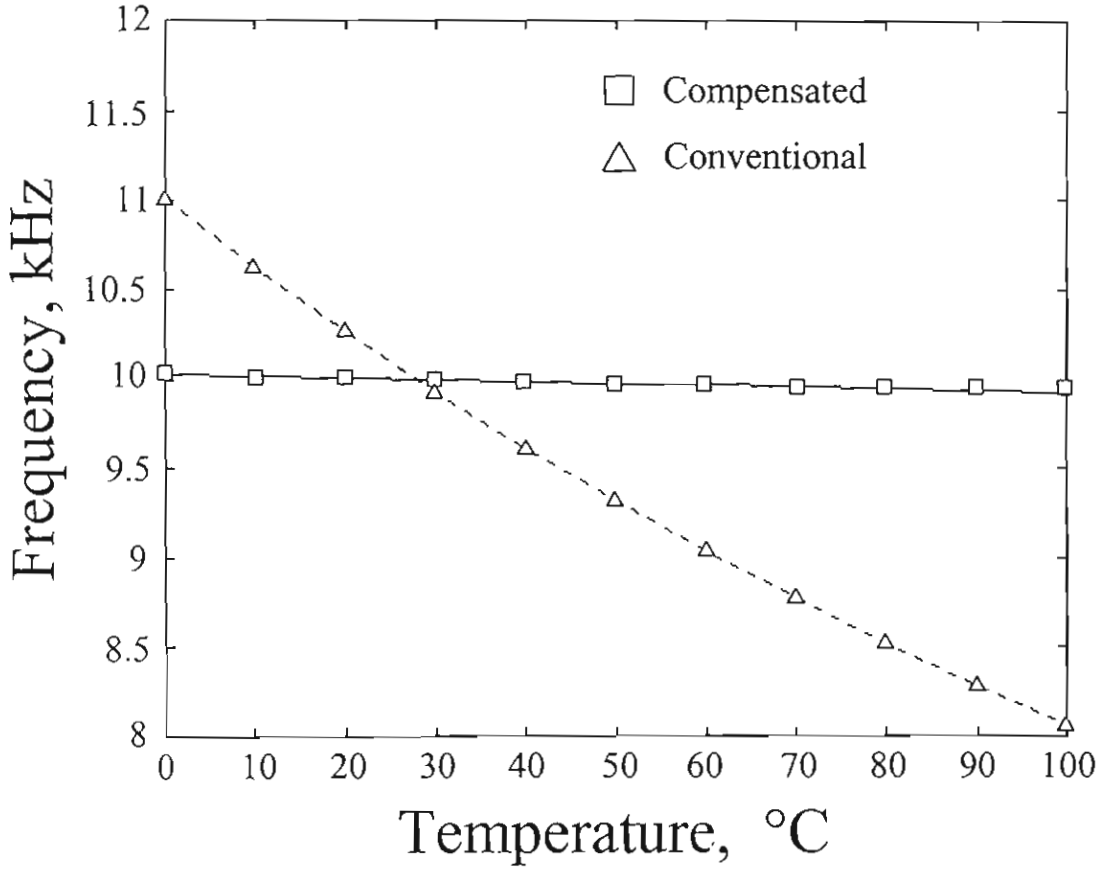

Figure 5 K.Kumwachara and W.Surakampontorn

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บทความวิจัยที่อยู่ในระหว่างการพิจารณา

Sinusoidal Frequency Doubler and Full-wave Rectifier Based on Translinear Current Controlled Conveyors

by

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$CCCII_D$, respectively. Due to the characteristics of the CCCIIs, the voltages V_A and V_B will also appear at ports X_3 and X_4 of the $CCCII_C$ and $CCCII_D$, respectively. Let us choose such that $R_{S1} = R_{S2}$, $R_{C2} = R_{C3}$ and $R_{X3} = R_{X4} = V_T/2I_1$, where R_X is the internal resistance at the port X of the CCCIIs and V_T is the thermal voltage at room temperature (approximately equal to 26 mV). Then, from the equations (1)-(5), the output current i_{out} can be expressed as

$$i_{out} = i_{z3} + i_{z4} \tag{7a}$$

and

$$i_{out} = 2k_1V_{CC} - 4k_1I_1R_{S1} - 2k_1R_{S1}\left(4I_1^2 + i_{x1}^2\right)^{1/2} \tag{7b}$$

where $k_1 = 1/(R_{C2} + R_{X3})$ and V_{CC} is the positive power supply voltage. It should be pointed out that it is the third term of the equation (7b), which is in the form of a root-sum of a square relation that will perform the frequency doubling action.

2.2A. Sinusoidal frequency doubler:

For a sinusoidal input voltage signal $v_{in} = V_m \sin \omega t$ and from the equation (6), the signal current i_{x1} is equal to $i_{x1} = I_m \sin \omega t$, where $I_m = V_m/R_{C1}$. If we set $k_2 = (2k_1V_{CC} - 4k_1I_1R_{S1})$ and select the signal amplitude such that $|i_{x1}| \le I_1$, then the equation (7b) becomes

$$i_{out} = k_2 - 4I_1k_1R_{S1}\left(1 + k_3 \sin^2 \omega t\right)^{1/2} \tag{8}$$

where $k_3 = I_m^2/(2I_1)^2$. If the power series of the form $\sqrt{(1+x)} = 1 + (1/2)x - (1/8)x^2 + \ldots$ are employed, then the equation (8) can be rewritten as

$$i_{out} \cong k_2 - 4I_1k_1R_{S1}\left(I_{DC} + I_{2\omega} \cos 2\omega t + I_{4\omega} \cos 4\omega t + \ldots\right) \tag{9}$$

where I_{DC}, $I_{2\omega}$, $I_{4\omega}$, ... represent the amplitudes of the DC component and the harmonic components and

$$I_{DC} \cong 4I_1k_1R_{S1}\left(1 + \frac{1}{4}k_3 - \frac{3}{64}k_3^2 + \frac{5}{256}k_3^3\right) \tag{10a}$$

$$I_{2\omega} \cong 4I_1k_1R_{S1}\left(-\frac{1}{4}k_3 + \frac{1}{16}k_3^2 - \frac{15}{512}k_3^3\right) \tag{10b}$$

$$I_{4\omega} \cong 4I_1k_1R_{S1}\left(-\frac{1}{64}k_3^2 + \frac{3}{256}k_3^3\right) \tag{10c}$$

For $k_3 < 1.0$, the k_3^2 and k_3^3 terms of the equation (10) can be neglected, then the output current can be approximately given by

$$I_{3A} = \frac{\left(4I_1^2 + i_{x1}^2\right)^{1/2} - i_{x1}}{2} \tag{16b}$$

From this circuit, the resistors R_{S1} and R_{S3} sense the currents I_{S1} and I_{S3}, respectively, resulting in voltage V_A and V_B at ports Y_3 and Y_4 of the $CCCII_C$ and $CCCII_D$, respectively. Due to the characteristics of the CCCII that $v_x \cong v_y$, the voltage V_A and V_B will also appear at ports X_3 and X_4 of the $CCCII_C$ and $CCCII_D$, respectively. Then, from equation (14) the expressions for V_A and V_B can be given by

$$V_A = V_{CC} - (2I_1 + 2I_{2A})R_{S1} \tag{17a}$$

$$V_B = V_{EE} + (3I_1 + 2I_{3A})R_{S3} \tag{17b}$$

The signal current i_{x3} is conveyed to port Z_3, which is the output port of this circuit, by the conveyor $CCCII_C$, where the output current i_{out} is

$$i_{out} = \frac{V_{RC2}}{R_{C2} + 2R_{X3}} = \frac{V_A - V_B}{R_{C2} + 2R_{X3}} \tag{18}$$

If $R_{S1} = R_{S3}$ and $R_{X3} = R_{X4} = V_T/2I_1$, then the output current i_{out} of the $CCCII_D$ can be expressed as

$$i_{out} = k_4\left(V_{CC} - V_{EE}\right) - 5k_4 I_1 R_{S1} - 2k_4 R_{S1}\left(4I_1^2 + i_{x1}^2\right)^{1/2} \tag{19}$$

where $k_4 = 1/(R_{C2} + 2R_{X3})$, V_{CC} and V_{EE} are the positive and negative power supply voltages, respectively. From equation (19), it is clearly seen that the third term is in the form of a root-sum of a square relation. By comparing the equation (19) with the equation (7b), we can see that the third terms, that perform the frequency doubling action, are the same. It is therefore expected that the circuit of figure 3 will give the similar performance as the circuit of figure 2, where the amplitudes of DC components and harmonic components are as follows:

$$I_{DC} \cong 4I_1 k_4 R_{S1}\left(1 + \frac{1}{4}k_3 - \frac{3}{64}k_3^2 + \frac{5}{256}k_3^3\right) \tag{20a}$$

$$I_{2\omega} \cong 4I_1 k_4 R_{S1}\left(-\frac{1}{4}k_3 + \frac{1}{16}k_3^2 - \frac{15}{512}k_3^3\right) \tag{20b}$$

$$I_{4\omega} \cong 4I_1 k_4 R_{S1}\left(-\frac{1}{64}k_3^2 + \frac{3}{256}k_3^3\right) \tag{20c}$$

It is should also be noted that by applying the same conditions as in the section 2.2B, the circuit of figure 3 is also working as a rectifier circuit.

3. Simulation and experimental results:

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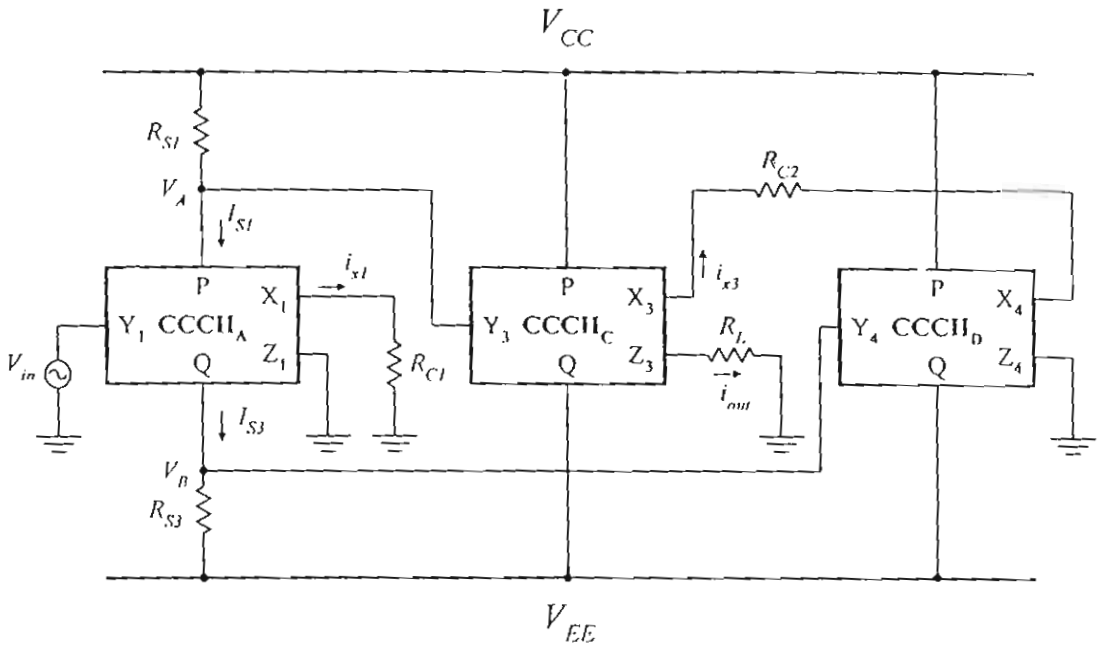

Fig. 3 K. Anuntahirunrat et al.

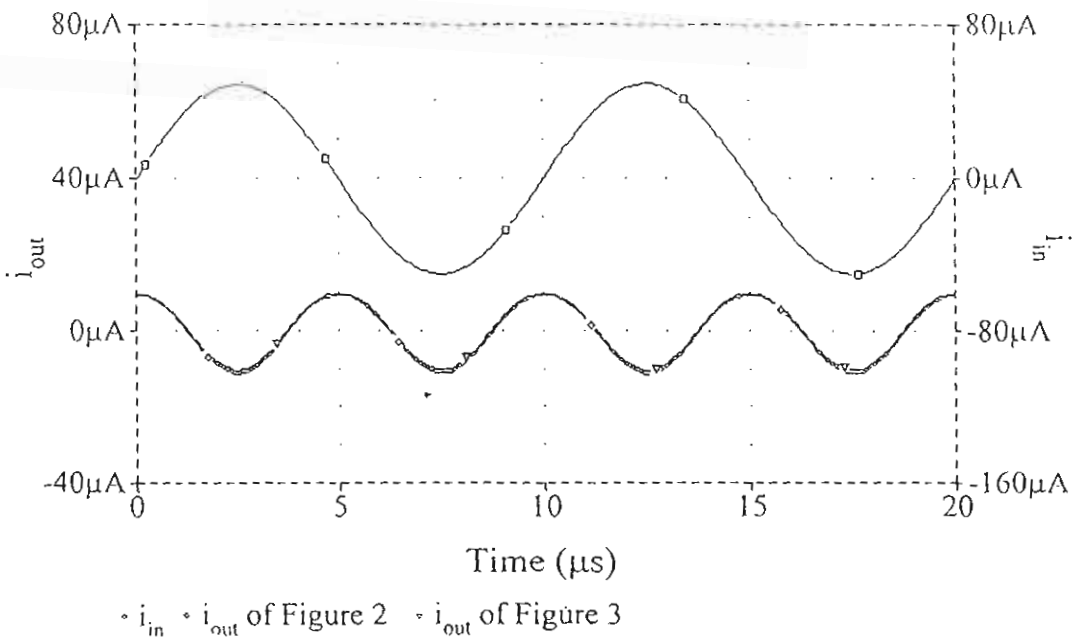

Fig. 4 K. Anuntahirunrat et al.

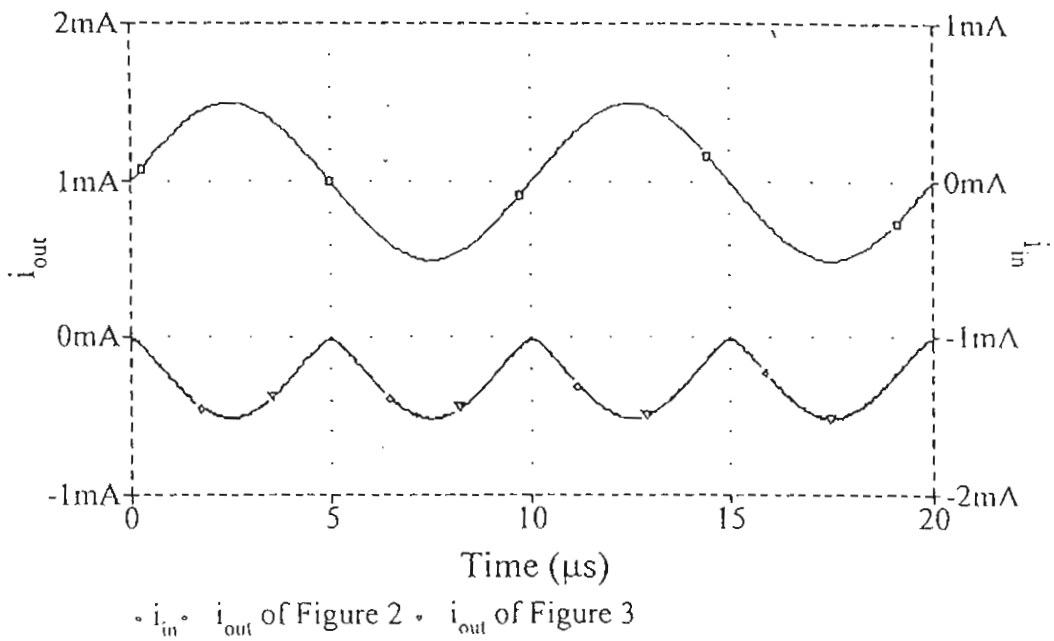

Fig. 5 K. Anuntahirunrat et al.

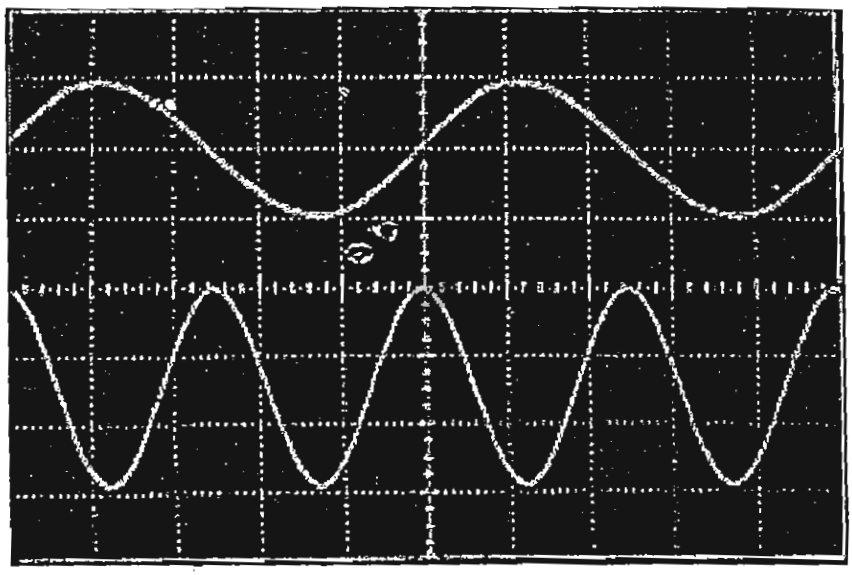

Fig. 6 K. Anuntahirunrat et al.

A Simple Wide-Band CMOS based True RMS-to-DC Converter

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drain currents of M_1 and M_2, respectively, the currents I_{D1} and I_{D2} can be respectively written as (Bult and Wallenga 1987, Landolt et al. 1992)

$$I_{D1} = \frac{(4I_b - I_{in})^2}{16I_b} \qquad \text{for} \quad |I_{in}| \le 4I_b \tag{1}$$

$$I_{D2} = \frac{(4I_b + I_{in})^2}{16I_b} \qquad \text{for} \quad |I_{in}| \le 4I_b \tag{2}$$

The unity gain positive current mirror CM_1, formed by transistors M_2 and M_3, reflects the current I_{D2} in order to add with the current I_{D1}. Then the summation of the currents I_{D1} and I_{D2} or $I_{SA} = I_{D1}+I_{D2}$ becomes

$$I_{SA} = \frac{I_{in}^2}{8I_b} + 2I_b \tag{3}$$

We can see that I_{SA} consists of the signal current that is the squaring of the input signal I_{in} and the DC current of value $2I_b$. If the DC current $2I_b$ can be compensated, the circuit will be functioned as a squarer/divider circuit (Antonio and Alfonso 2001), which can be used as a basic cell to realize rms-to-dc converter.

2.2 The proposed true rms-to-dc converter

Fig. 2 shows the proposed true rms-to-dc converter, which is composed of the squaring circuit in Fig.1 in combination with four current mirrors, CM_2 through CM_5. The circuit is constructed such that the drain current of the transistor M_5 of the current mirror CM_2 sources the

CAPTION ON THE FIGURES

Figure 1 Circuit diagram of the OTA-based temperature-insensitive V/I
Figure 2 The g_m-RC quadrature oscillator with temperature-compensation
Figure 3 Experimental results of the g_m-RC quadrature oscillator
(Vertical scale: 2V/divider. Horizontal scale: 5 μs/divider)
Figure 4 Variation of the frequency of oscillation with the DC bias current $I_{B2}=I_{B4}$
Figure 5 Variation of the frequency of oscillation against temperature

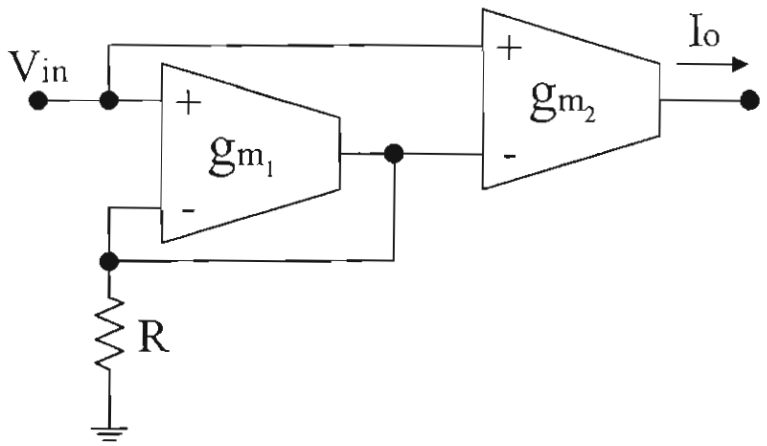

Figure 1 K.Kumwachara and W.Surakampontorn

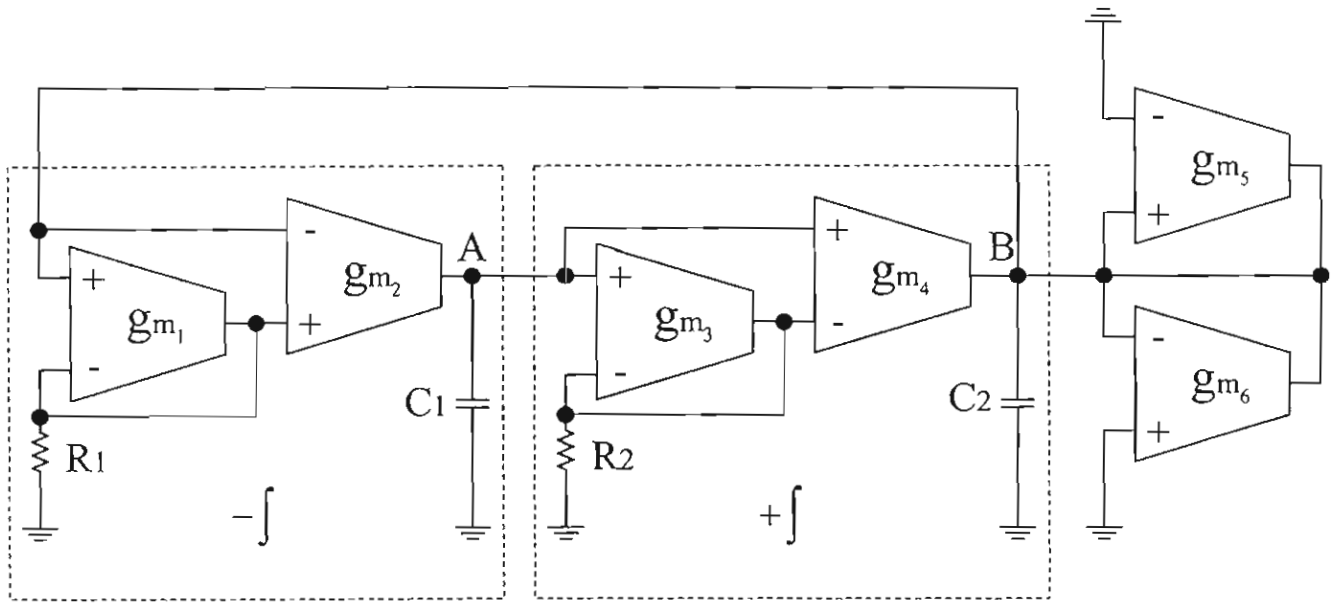

Figure 2 K.Kumwachara and W.Surakampontorn

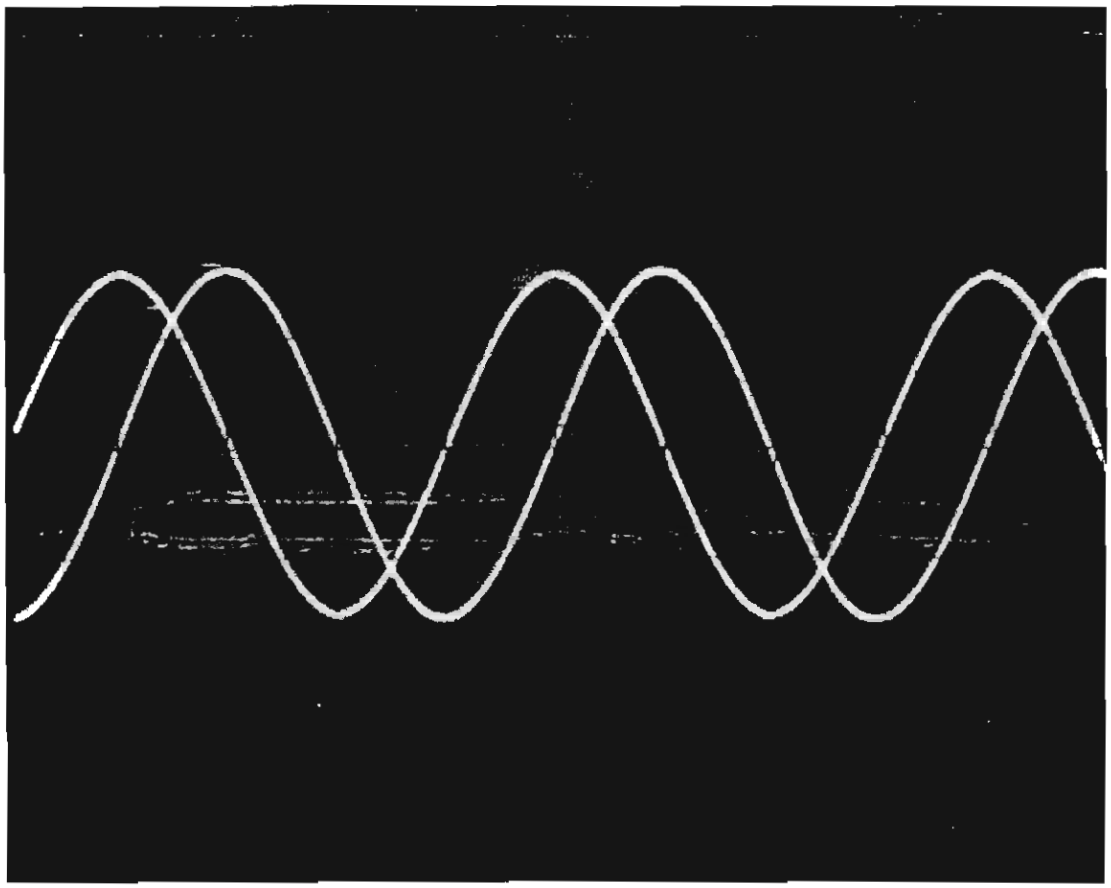

Figure 3 K.Kumwachara and W.Surakampontorn

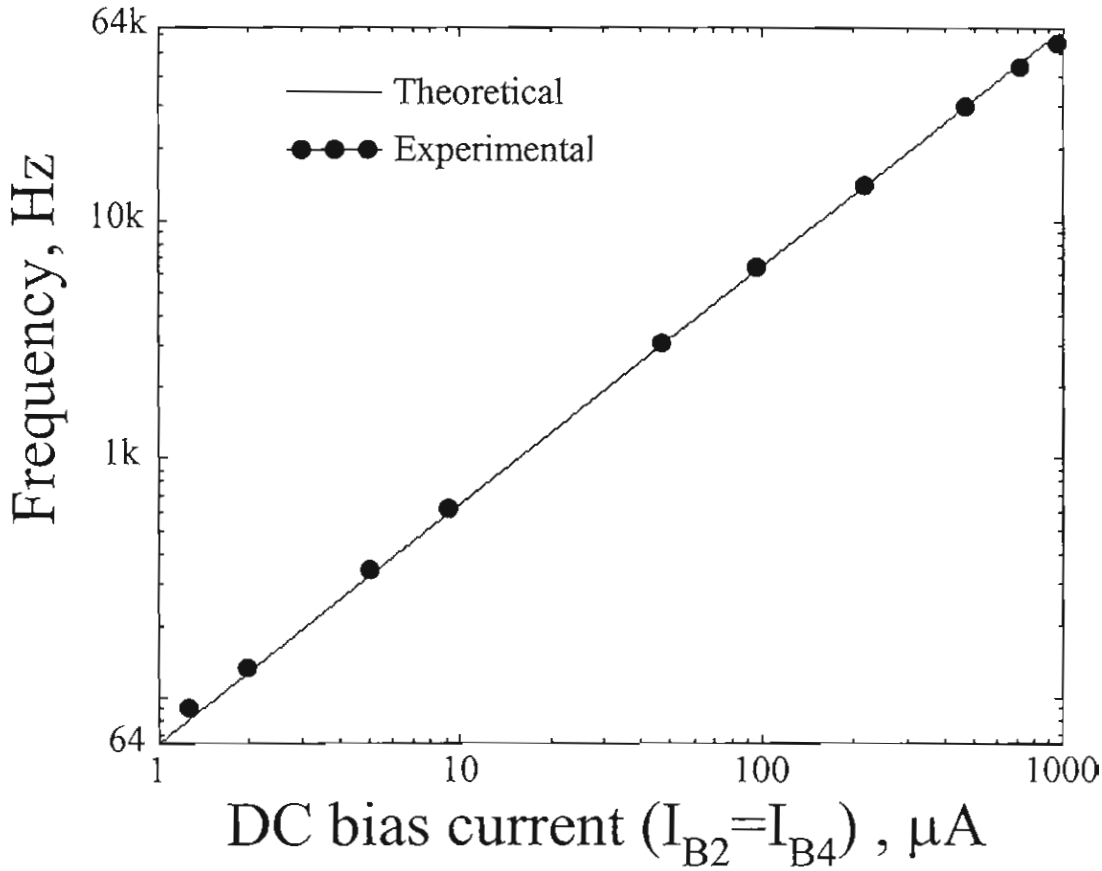

Figure 4 K.Kumwachara and W.Surakampontorn

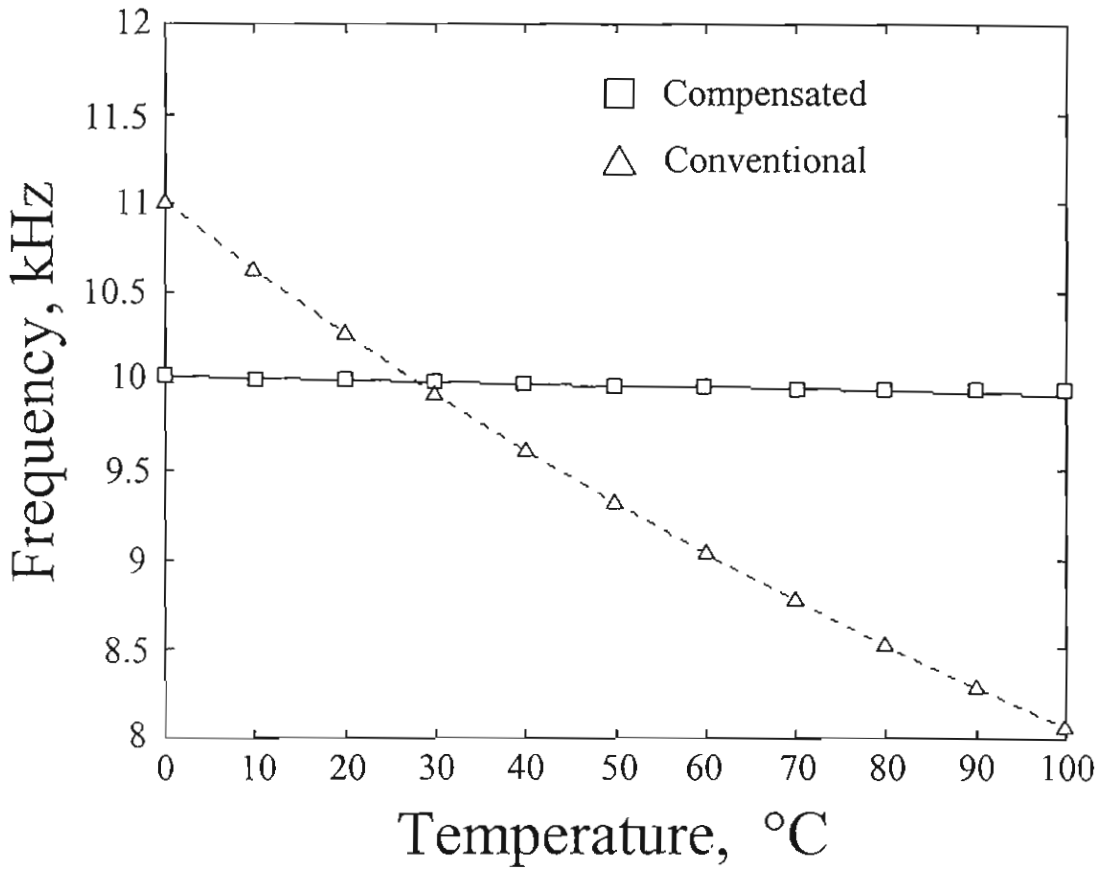

Figure 5 K.Kumwachara and W.Surakampontorn