รายงานวิจัยฉบับสมบูรณ์

โครงการ การพัฒนาและออกแบบวงจรกรองแถบผ่านแบบเชิงซ้อนที่อาศัยเทคนิควงจรสวิทช์-กระแสสำหรับระบบวิทยุระยะสั้น *Bluetooth*™

โดย อภิศักดิ์ วรพิเชฐ

10 สิงหาคม 2547

สัญญาเลขที่ TRG4580062

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อภิศักดิ์ วรพิเชฐ
มหาวิทยาลัยเทคโนโลยีมหานคร

สนับสนุนโดยสำนักงานกองทุนสนับสนุนงานวิจัย

(ความเห็นของรายงานนี้เป็นของผู้วิจัย สกว.ไม่จำเป็นต้องเห็นด้วยเสมอไป)

Abstract

Project Code : TRG4580062

Project Title : Design of switched-current (SI) complex filter for *Bluetooth*™ for short range radio link

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Traditionally, high performance channel filters for integrated wireless transceivers have employed class A operational amplifiers and passive resistors and capacitors. With the need to find solutions which work adequately in standard low voltage CMOS and with much lower power consumption, this research describes an alternative approach employing class AB switched-current sampled analogue techniques with non-cascode and cascode configuration. It is used to design a fifth order complex channel filter for a low-IF Bluetooth receiver. Various techniques have been incorporated to lower the filter's power consumption such as multi-rate design, dynamic element matching and analysis of optimum power budget. The designed prototypes achieve adequate performance in a 0.3μm standard CMOS process while operating at 2.0V supply and 2.7mA of current consumption. Finally, each of the filters occupies an area of 2.5x0.69mm^2.

Keywords : Bluetooth, filters, transceiver, switched-current, CMOS

บทคัดย่อ

รหัสโครงการ : **TRG4580062**

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ปรกติแล้ว วงจรกรองช่องสญญาณสำหรับระบบรับ-ส่งไร้สายแบบวงจรรวม จะอาศัยออปแอมป์ที่ทำงานแบบคลาสเอ ผนวกกับ อุปกรณ์พาสซีฟ คือ ตัวต้านทาน และ ตัวเก็บประจุ แต่ความต้องการด้านการกินกำลังงานต่ำมาก และความสามารถในการทำงานได้ที่ระดับไฟเลี้ยงต่ำในกระบวนการผลิตซีมอสในยุคปัจจุบัน ทำให้เราจำเป็นต้องหาเทคนิคการออกแบบวงจรกรองใหม่ที่เหมาะสมกว่า โดยงานวิจัยฉบับนี้ นำเสนอแนวทางการออกแบบโดยอาศัยวงจรกรองสุ่มสวิทช์กระแสแบบคลาสเอบี ทั้งแบบพื้นฐานและแบบคาสโคด สำหรับสร้างวงจรกรองช่องสัญญาณแบบเชิงซ้อนอันดับ 5 ตามมาตราฐาน Bluetooth และได้เพิ่มเทคนิคช่วยต่าง ๆ คือ การสุ่มแบบหลายอัตรา การเข้าคู่หน่วยวงจรแบบพลวัต และการวิเคราะห์แบ่งกำลังงานเพื่อให้วงจรรวมที่ได้มีการกินกำลังงานต่ำสุด จากผลการทดลองพบว่าวงจรที่ได้ออกแบบทั้ง 2 วงจร ในเทคโนโลยีการผลิตซีมอส 0.35 ไมครอน มีสมรรถนะเพียงพอกับความต้องการ โดยทำงานที่ระดับไฟเลี้ยง 2.0 โวลต์ มีการกินกระแส 2.7 มิลลิวัตต์ และอาศัยพื้นที่ชิฟในแต่ละวงจรเท่ากับ 2.5x0.69 ตารางมิลลิเมตร

คำหลัก : Bluetooth, filters, transceiver, switched-current, CMOS

1. Introduction

The low-IF (intermediate frequency) poly-phase or complex architecture has emerged as the preferred approach for achieving the required sensitivity in fully integrated wireless transceivers [1]. The industry is currently driving down the cost and power consumption by attempting standard CMOS solutions for applications such as Bluetooth [2] and ZigBee (HomeRF Lite) [3] and this is creating new challenges for the circuit designer.

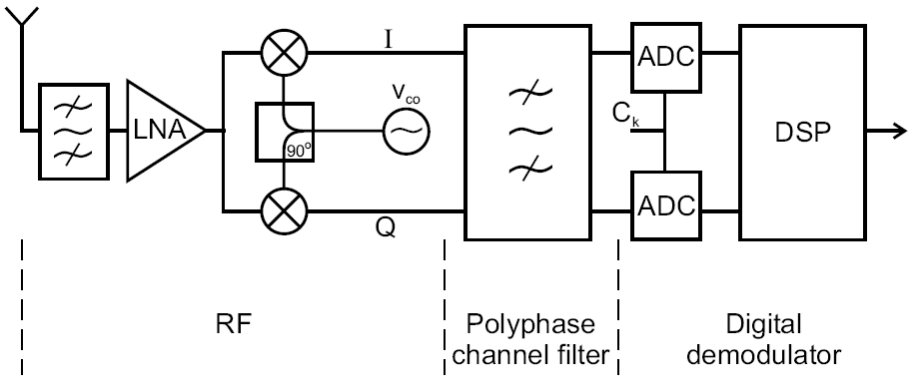


Figure 1.1: Typical low-IF receiver architecture

Figure 1.1 shows a typical low-IF receiver architecture. One of the keys to the success of this poly-phase approach has been the ability to integrate the channel filter. However, when solutions are required using the ever-lowering supply voltages demanded by standard CMOS, and with lower power consumption, conventional filter techniques using operational amplifiers with passive resistors and capacitors may prove inadequate. This is because, as supply voltage falls, the signal power falls faster than the power consumption, and also because headroom constraints to designing the operational amplifiers are aggravated. So, the motivation for this work was to develop a circuit style which better accommodates low supply voltage and which is therefore more 'future-proof'.

The approach adopted for this research is to make switched-current (SI) filters using class AB CMOS transconductors. While these can be expected to yield efficient solutions, they would not be expected to be as linear as the traditional approach using passive resistors and capacitors. So, a key aspect of using the SI technique is to demonstrate that suitable filters could be realized with lower power consumption and chip area, and with adequate inter-modulation performance.

In this report, we design a SI complex low-IF channel filter for Bluetooth. The class AB SI technique is reviewed and both real and complex bilinear z-transform integrators are developed. The performance of a filter for the Bluetooth specification is estimated and the complex SI filter is designed to meet the requirement using the developed cells. Simulated and experimental performances of the filter, including anti-alias filters and sample-and-holds, are presented. Finally, conclusions are drawn.

2. Class AB Switched-Current Techniques

The case for the switched-current (SI) technique, as opposed to the switched-capacitor (SC) technique, for analogue signal processors was outlined in [4]. In this, various performance vectors, signal-to-noise ratio (*SNR*), clock frequency (F_c) and power consumption (*P*), were analyzed and then combined to form a single figure-of-merit $FoM = \left(SNR \cdot F_c / P \right)$ to express overall performance. Using forecast process data for CMOS generations through the period 1991-2011, as summarized in Table 2.1, the *FoMs* of SC and SI were evaluated and these are shown in figure 2.1.

It is found that at the start of this period (1991), SC performed about ten times (10dB) better than class AB SI. However, as processing heads towards lower power supply voltage the performance of SC falls steadily while that of SI remains almost constant. During the course of the next decade, class AB SI can be expected to pass that of SC. This broadly reflects our experience with SI implementations through the earlier part of that period. It is justified rigorously in [4] and can be explained intuitively as follows.

Year	Technology (μm)	Process supply voltage(V)	Threshold voltage(V)
1991	0.80	5.0	0.80
1993	0.50	3.3	0.60
1995	0.35	3.3	0.50
1997	0.25	2.5	0.45
1999	0.18	1.8	0.35
2002	0.13	1.5	0.30
2005	0.10	1.2	0.25
2008	0.07	0.9	0.25
2011	0.05	0.6	0.20

Table 2.1: Forecast of CMOS technology generations

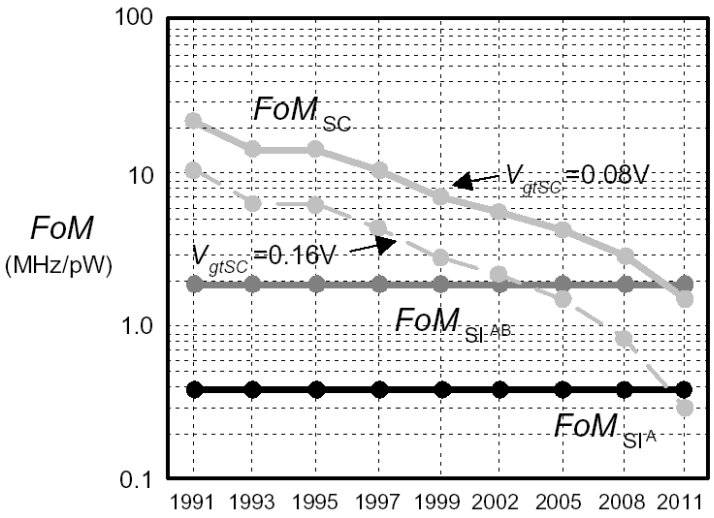


Figure 2.1: Figure-of-merits in SC and SI memory cells at different CMOS technology generations in Table 1

Consider a scenario in which V_{dd} falls but the supply current, (I_{dd}), and the total capacitance remain constant. With SC, the power consumption falls proportionally with V_{dd} but as the signal voltage swings must be reduced (to remain within the reduced V_{dd}), the signal power falls approximately as the square of the fall in V_{dd}. The transconductance of its OTA's is set to maximize the available voltage swing

and so remains unchanged as V_{dd} falls. So, the noise power and bandwidth are unchanged. The net result is that the *FoM* for SC falls proportionally with V_{dd}. With SI, the power consumption also falls proportionally with V_{dd} but there is no change to the signal current swings and so the signal power is constant. However, the reduced V_{dd} and constant I_{dd} necessitate the use of higher transconductance devices and this produces a noise power which increases with the square of the fall in V_{dd}. This is because capacitance has stayed constant and there is a proportional increase in bandwidth. The net result is that the *FoM* for SI stays constant despite falling V_{dd}.

Having described the rationale behind the use of SI techniques, we now review the operation of class AB SI building blocks which are the SI memory, the sample-and-hold and the integrator.

2.1 SI Memory Structure

Figure 2.2(a) shows the structure of the class AB SI memory cell [5]. It comprises a class AB transconductor (-*G*) with parasitic memory capacitance (C_g), a memory switch which closes on phase ϕ'_1, and input and output switches which close on phases ϕ_1 and ϕ_2 respectively. The clock phases are given in figure 2.2(b) and show that the phases ϕ_1 and ϕ_2 are in anti-phase but that phase ϕ'_1 falls fractionally before phase ϕ_1 to ensure that the memory switch opens before the input current is interrupted.

On the sampling phase, ϕ_1, the memory switch is closed and this closes the loop around the transconductor. The input current, *i*, initially charges the memory capacitance C_g but the voltage developed causes current to flow in the output of the transconductor. The loop settles with substantially all the input current owing at the transconductor output and a voltage $v_{in} = \frac{i}{G}$ held on C_g.

On the hold phase, ϕ_2, the memory switch is opened and v_{in} continues to be held on C_g and this sustains the current i_{out} = -*i* at the output terminal. So, the SI memory cell samples the input current at the end of phase ϕ_1 (actually on the falling edge of ϕ'_1) and makes it available on phase ϕ_2 with inversion of polarity.

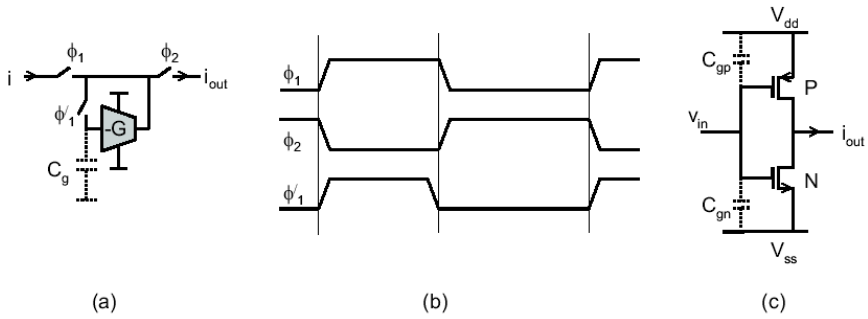


Figure 2.2: Basic class AB SI memory cell (a) memory cell (b) clock waveforms (c) transconductor

The class AB transconductor is shown in figure 2.2(c) and employs the PMOS/NMOS transistor pair previously described by Nauta and Seevinck in [6]. If the PMOS and NMOS transistors P and N have identical parameters (a simplifying assumption but not a requirement), then $g_{mp} = g_{mn} = g_m$ and the overall transconductance of this single-ended cell is -G where G=2g_m. Biasing the input at the mid-rail voltage $V_{dd}/2$ produces equal drain currents J in both P and N and the output current is zero. When the input voltage changes from its quiescent value $V_{dd}/2$ by v_{in}, the drain currents of P and N become unbalanced and a linearly related current, $i_{out} = -G \cdot v_{in}$, flows at the output. The transconductor is exceptionally efficient because it operates in class AB for peak output currents as high as $i_{out} = 4 \cdot J$. The precise value of G may be controlled by the supply voltage using a control circuit that will be described later. The parasitic memory capacitance C_g is given by the sum of the P and N gate capacitances, i.e., $C_g \approx C_{gn} + C_{gp}$.

On the sampling phase, ϕ_1, the drain currents, I_n and I_p, settle to:

$$I_{n,p} = J(1 \pm m)^2 \qquad -1 \le m \le +1 \tag{2.1}$$

where m is the signal modulation given by $m = \frac{i}{4J}$. The input voltage, v_{in}, settles to a value determined by the input current and the transconductance,

$$v_{in} = \frac{i}{g_{mn} + g_{mp}} = \frac{i}{G} \tag{2.2}$$

So, we see that the class AB transconductor gives the memory a signal-independent input conductance and, because C_g is also constant, the settling behavior is substantially signal-independent. This linear behavior occurs despite the square-law variation of the individual drain currents as shown in the simulation of figure 2.3.

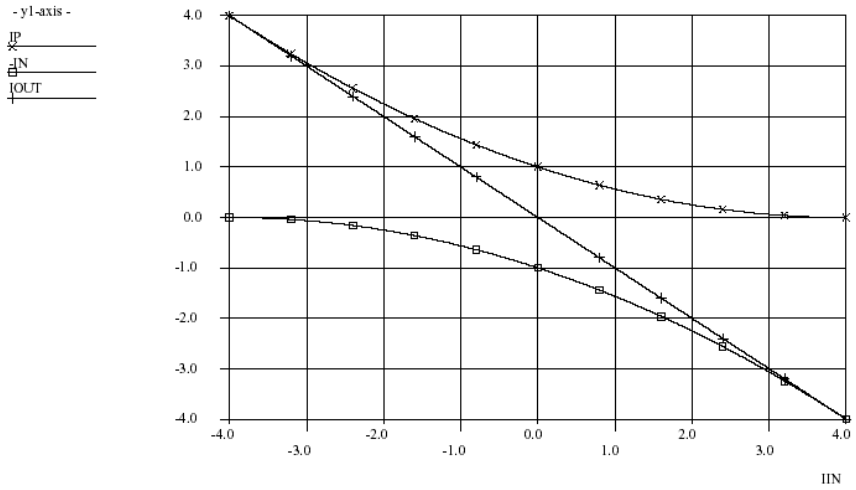


Figure 2.3: Normalized behavior (J=1) of an idealized class AB SI memory cell

The voltages that are developed when a first memory cell, N1 and P1, on its hold phase is connected to second memory, N1 and P1, on its sample phase, determine the dc design of the memory cell, as shown in figure 2.4(a).

For equal threshold voltages, V_t, all transistors stay in saturation over the whole signal range, $-1 \le m \le +1$, so long as the quiescent gate overdrive voltage is set to:

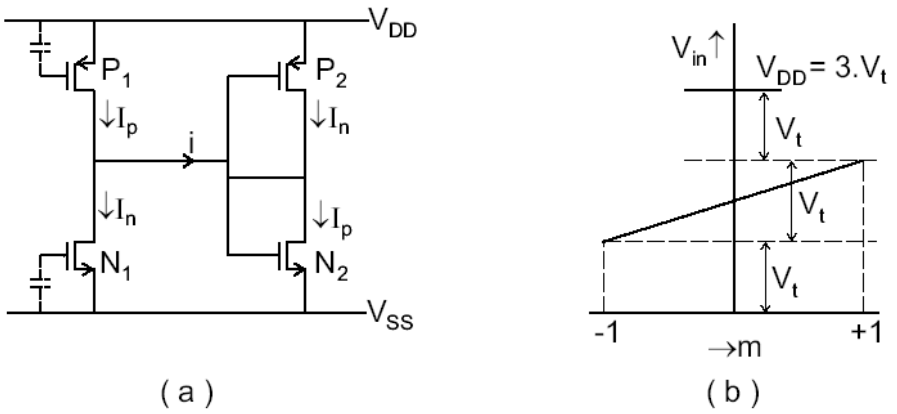


Figure 2.4: Transmission between primitive single-ended class AB SI memory cells (a) circuit arrangement (b) input voltage variation with signal for $\widehat{m}=1$

$$V_{gt} \le \frac{V_t}{2\widehat{m}} \tag{2.3}$$

where $\widehat{m}$ is the maximum signal modulation, and the supply voltage is set to:

$$V_{dd} = 2(V_{gt} + V_t) = V_t(2 + \frac{1}{\widehat{m}}) \tag{2.4}$$

So, for $\widehat{m}$ =1, we may design with:

$$V_{gt} = \frac{V_t}{2} \tag{2.5}$$

and:

$$V_{dd} = 3 \cdot V_t \tag{2.6}$$

For $\widehat{m}$ =1 and $V_t = 0.6\text{V}$, then $V_{gt} = 0.3\text{V}$, $V_{dd} = 1.8\text{V}$ and this will ensure saturated operation of all transistors of the basic memory cell. It can be shown that the signal-to-noise ratio of the SI memory is:

$$SNR_m = 10\log\left(\frac{V_{gt}^{\ 2}}{\frac{4\gamma kT_j}{3C_{tot}}}\right) \tag{2.7}$$

where C_{tot} is the total capacitance associated with the memory cell, *k* is Boltzmann's constant (1.38e-23), T_j is the junction temperature and γ is a parameter relating total memory noise (memory transistors and switches) to theoretical 'white' noise in the memory transistors.

Normally, the memory cells are used in balanced pairs for use in differential architectures. With such balanced pairs, designed for the same power consumption as their single-ended counterpart, the signal-to-noise ratio (SNR) is unchanged. Furthermore, it can be shown that the harmonic distortions resulting from the memory cell's finite output conductance effects is:

$$HD_1 = \frac{2G_{ds}}{G} + \frac{C_{dg}}{C_{dg} + C} \tag{2.8}$$

$$HD_2 = 0 \tag{2.9}$$

$$HD_3 = \frac{G_{ds}}{G} \cdot \frac{\hat{m}^2}{2} \tag{2.10}$$

where HD_1 is the linear gain error. Finite settling errors and charge injection errors produce linear gain errors but substantially no offset errors or harmonic distortion.

The effects of finite output conductance can be reduced by using cascoding as shown in figure 2.5. This arrangement uses separate P and N memory switches which should give better power supply noise rejection as the memory capacitances are better isolated on the hold phase. This option is also available in the basic memory even though figure 2.2(a) shows a memory configuration with a single memory switch. However, this diagramatic form (figure 2.2(a)) is adopted throughout this report purely to simplify the configurations of higher level blocks which may in practice use the double memory switch configuration.

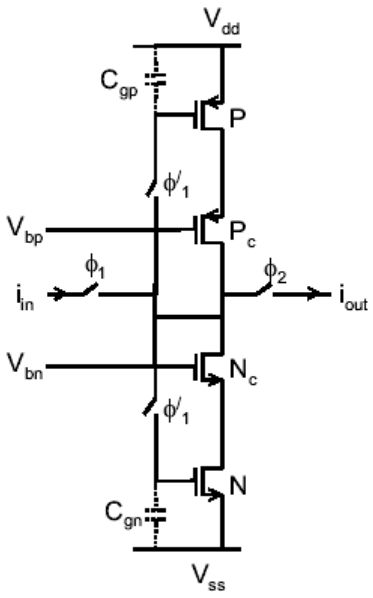


Figure 2.5: Cascoded switched-current memory cell

Following similar procedures to determine the dc design as given above for the basic (non-cascoded) memory cell it can be shown that the conditions for maintaining saturated operation of all transistors of the cascode memory cell are given by:

$$V_{gt} \le \frac{V_t - V_{gtc}}{2\hat{m}} \tag{2.11}$$

where V_{gtc} is the gate overdrive voltage of the cascode transistors, and the supply voltage is set to:

$$V_{dd} = \frac{V_t}{\hat{m}}(1 + 2\hat{m} + \frac{V_{gtc}}{V_t}) \tag{2.12}$$

So, if the same values are chosen for V_{gt} and V_{dd} that were used for the basic memory cell, saturated operation of all transistors in the cascoded memory cell can be sustained only by reducing $\hat{m}$ (for $V_t = 0.6\text{V}$ and $V_{gtc} = 0.2\text{V}$, then $V_{gt} = 0.3\text{V}$, $V_{dd} = 1.8\text{V}$ and $\hat{m} = 0.67$). However, this reduced

dynamic range may be unnecessary because larger modulation $(0.67 \le \widehat{m} \le 1)$ will only cause the cascode transistors to enter the triode region at the peaks of large amplitude signals and in this state the cascoded memory reverts to the basic memory.

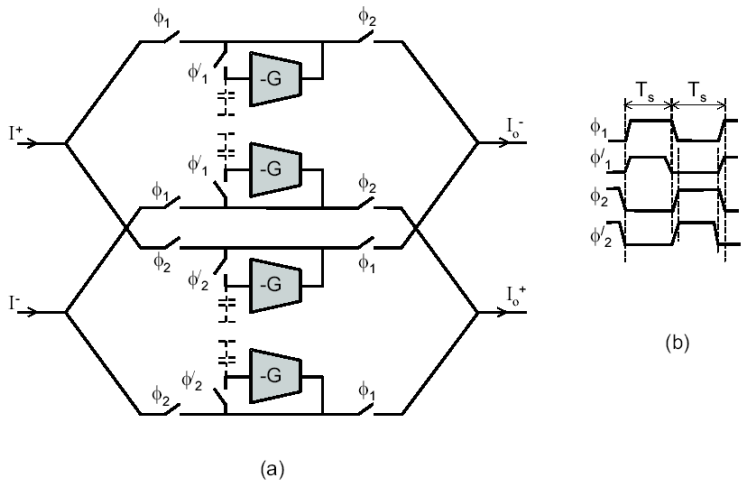


Figure 2.6: Balanced switched-current sample-and-hold

2.2 Balanced SI Sample-and-Hold

A balanced SI sample-and-hold is shown in figure 2.6 and comprises two multiplexed balanced memory cells. On phase ϕ_1, the upper pair samples the balanced input current while the lower pair is holding the balanced input current it sampled on the previous phase ϕ_2. On the next phase ϕ_2, the lower pair samples the balanced input current while the first pair is holding the balanced input current it sampled on the previous phase ϕ_1. Clearly, the cell is operating with an effective sampling period of $T_s = T_{ck}/2$, i.e., it samples the input signal and produces a sampled-and-held output on both ϕ_1 and ϕ_2 phases and so is said to be 'double-sampling'. Note that the balanced SI sample-and-hold cell has no common-mode rejection.

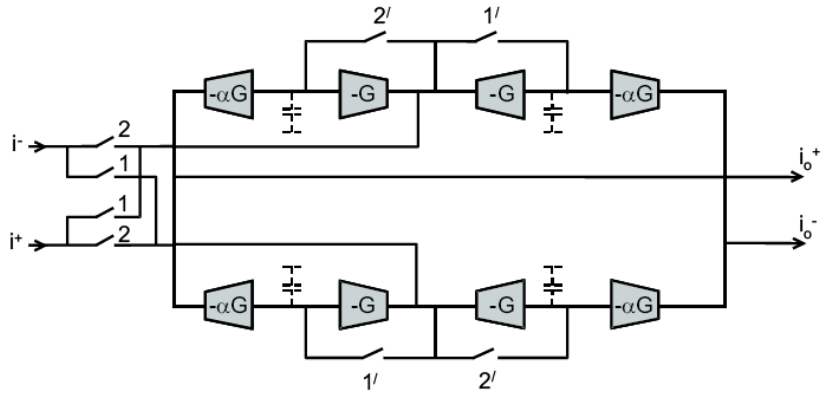


Figure 2.7: Balanced switched-current integrator

2.3 Balanced SI Integrator

The balanced SI integrator is shown in figure 2.7. It comprises two single-ended integrator cores each of which has a pair of anti-phased memory cells coupled back to back, a commutating switch arrangement at the balanced inputs, and balanced outputs which are produced by subtracting and scaling (by α) of the integrator core signals. The input commutating switch arrangement periodically reverses the polarity of the signal and because this is performed synchronously with the signal reversal in the integrator's memory cells, this produces a running summation of the input samples, i.e., it performs integration.

It can be shown [7] that, for a differential input signal, i, the differential output signal, $i_{out}(n)$, during sampling period (n) is given by:

$$i_{out}(n) = \alpha[i(n) + i(n-1)] + i_{out}(n-1) \tag{2.13}$$

Taking z-transforms and re-arranging, we have the transfer response as:

$$H(z) = \frac{i_{out}(z)}{i(z)} = \alpha \frac{1+z^{-1}}{1-z^{-1}} \tag{2.14}$$

For physical frequencies, $z \to e^{j\omega Ts}$, the response becomes:

$$\begin{aligned} H(\omega) &= \frac{\alpha}{j \tan \frac{\omega Ts}{2}} \\ &\approx \frac{\alpha}{j\omega \frac{Ts}{2}} \qquad\qquad \omega T_s \ll 1 \end{aligned} \tag{2.15}$$

Like the sample-and-hold cell, it is operating with an effective sampling period of $T_s = T_{ck}/2$, i.e., it samples the input signal and produces an integrated output on both ϕ_1 and ϕ_2 phases. As this demands no more bandwidth from its memory cells than with the single-sampling Euler integrators, it gives a further benefit to power consumption. The integrator creates no excess phase and has a time constant given by:

$$\tau = \frac{T_s}{2\alpha} \tag{2.16}$$

It is performing trapezoidal integration with the bilinear *z*-transform defined by:

$$s \to \frac{2}{Ts} \frac{1-z^1}{1+z^{-1}} \tag{2.17}$$

Any common-mode component of the input signal is not reversed by the input commutating switch and so is not integrated, merely transmitted with attenuation (α) to the outputs. Consequently, there is no need for common-mode feedback circuits in this integrator.

3. Complex Filter Synthesis

The function of the channel filter is to pass the wanted channel while rejecting neighboring channel interferers. As these interferers occur at frequencies on either side of the passband, image

responses must be suppressed and this requires using a bandpass filter with an asymmetric amplitude response, i.e., $|H(j\omega)| \neq |H(-j\omega)|$. Filters of this type require complex coefficients and these can be created by poly-phase or complex networks employing two paths driven by signals which are identical but in exact quadrature phase as supplied in the down-converted I- and Q-channels of a low-IF transceiver.

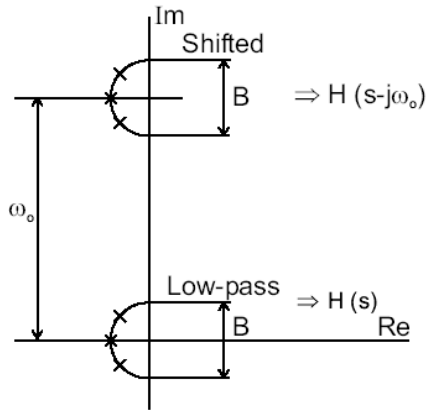


Figure 3.1: Complex filter basics

3.1 Complex Filters

The principle of the poly-phase or complex filter is illustrated in figure 3.1. Starting with a real lowpass filter (i.e., with real coefficients), the transformation $s \rightarrow s - j\omega_0$ is applied [8]. This shifts the poles up the imaginary axis by ω_0 and transforms the low-pass response (actually a bandpass response centered at $\omega = 0$) into an identical bandpass response centerd at $\omega = \omega_0$. The transformation preserves both amplitude and phase characteristics and produces the required feature of having no image response at negative frequency.

Synthesis of complex filters follows similar procedures to those for real filters except that it makes use of complex integrators.

3.2 Balanced Complex SI Integrators

The signal-flow graphs (SFG) for the real and complex integrators are shown in figure 3.2. In figure 3.2(a), we see the SFGs of the real integrator described in the last section. Starting with the continuous-time SFG, we first substitute $\tau = \frac{T_s}{2\alpha}$ and then perform the bilinear mapping $s \to \frac{2}{T_s}\frac{1-z^{-1}}{1+z^{-1}}$ to create the *z*-domain SFG of the real integrator.

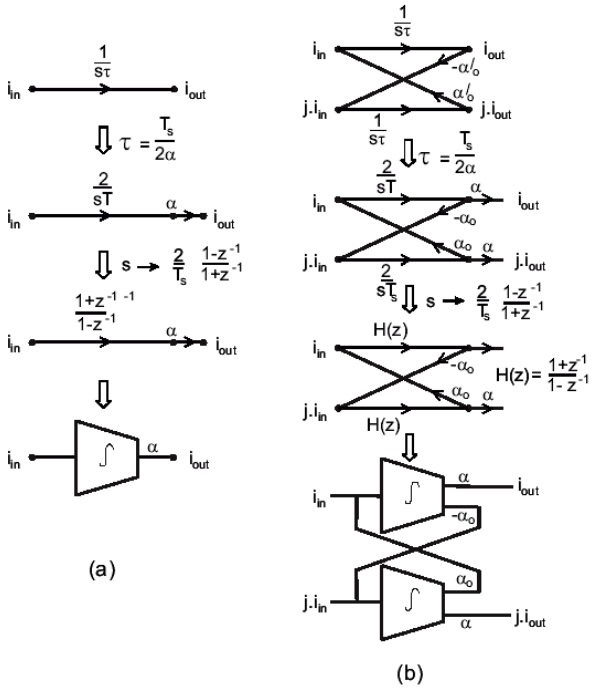


Figure 3.2: Integrator signal flow graphs (a) Real (b) Complex

In figure 3.2(b) we see the SFGs of the complex integrator. First, we create the SFG of the continuous-time complex integrator. It is easily shown that quadrature input signals produce quadrature output signals each with a transfer function given by:

$$H(s) = \frac{1}{(s\tau - j\alpha_0)} \tag{3.1}$$

For $\alpha_0 = \omega_0 \tau$, this becomes:

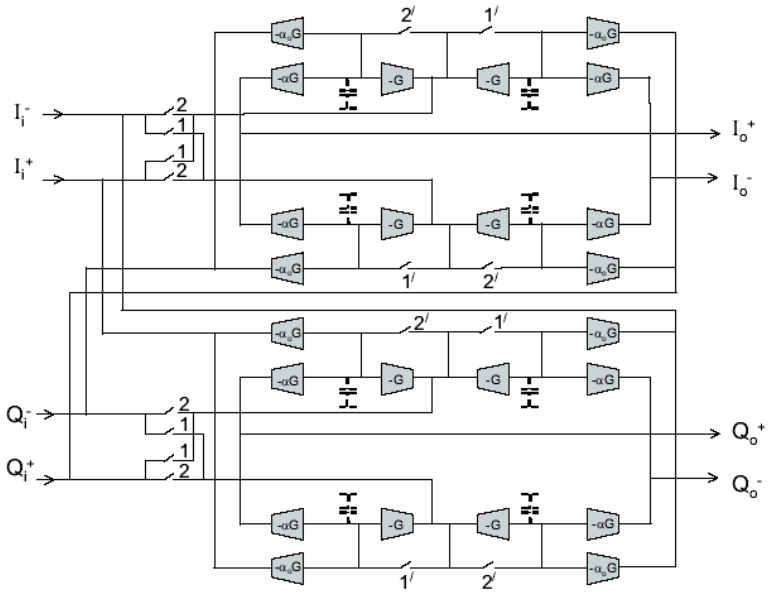


Figure 3.3: Complex integrator schematic

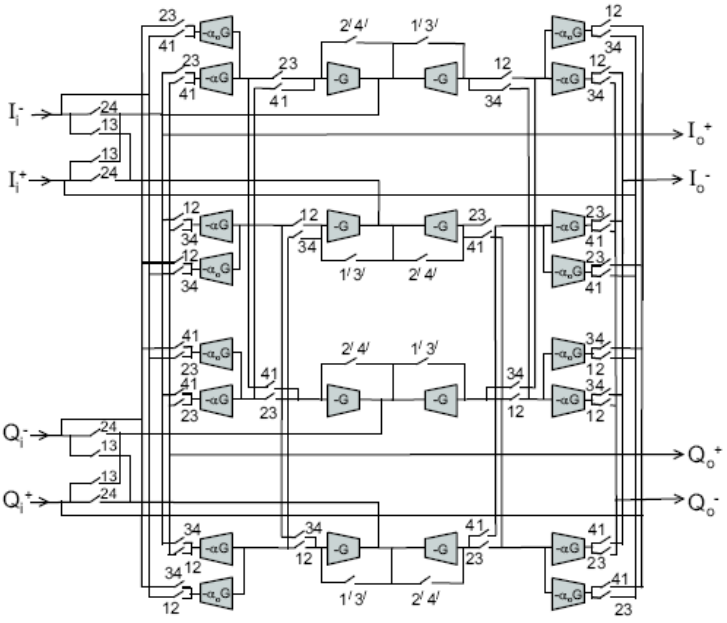


Figure 3.4: Complex integrator with dynamic element matching

$$H(s) = \frac{1}{(s - j\omega_0)\tau} \tag{3.2}$$

which demonstrates that the transformation, $s \to s - j\omega_0$, is being performed as required. Next, we substitute $\tau = \frac{T}{2\alpha}$ and then perform the bilinear mapping to create the *z*-domain SFG of the complex SI integrator. The block diagram shows that the complex integrator comprises a pair of real integrators each with normal outputs weighted α and extra outputs weighted α_0 and $-\alpha_0$ cross-coupled back to the inputs. These coefficients (α and α_0) are defined by the ratio of the transconductance of the output stage to that of the integrator core memories. As the transconductance is determined by the width of the MOS transistors (assuming constant length), there is complete freedom of choice subject to the process minimum feature size. The coefficients are set to:

$$\alpha = \frac{T_s}{2\tau} \tag{3.3}$$

$$\alpha_0 = \frac{\omega_0 T_s}{2} \tag{3.4}$$

By applying the bilinear z-transform $s \to (2/T_s)(1 - z^{-1})/(1 + z^{-1})$ to figure 3.2(b), the complex bilinear integrator circuit schematic is shown in figure 3.3 [9]. The output and cross-coupling signals are generated by the $-\alpha G$ and $-\alpha_0 G$ transconductors which are identical to the integrator core transconductors ($-G$) except that the widths of all transistors are scaled by α and α_0 respectively. This scaling reduces the bias current by the same factor and this maintains the voltage levels.

The success of the complex filter in rejecting image responses depends critically on the gain matching of the I- and Q-paths of the integrator. Unfortunately, this matching is determined by the matching of the coefficients ($-\alpha$ and $-\alpha_0$) which is determined by transistor matching. So, β and V_t mismatches will reduce the achievable image rejection.

The solution to this problem is to use 'dynamic element matching' as shown in figure 3.4. The arrangement periodically swaps the $-\alpha G$ and $-\alpha_0 G$ output transconductors between the I- and Q-paths so that each path experiences the same average values of coefficients. The switch sequence which

produces this swapping also ensures that the output transconductors stay connected to their respective memory transconductors $(-G)$ through both their sampling phase and the following hold phase. This ensures that no information from the I-path is transferred to the Q-path and vice versa.

3.3 Balanced Complex Filters

We can now proceed to synthesize the complex filter. First, we generate the lowpass real filter by traditional leapfrog methods and then the complex bandpass filter is created by shifting the real lowpass response to the required center frequency. We will create a fifth-order 0.5dB equi-ripple Chebyshev complex leapfrog channel filter suitable for Bluetooth (F_0 =1MHz, F_{bw} =1.2MHz), using the bilinear *z*-transform integrators described in the previous section. First, we will design the filter operating with a single sampling frequency of 13MHz (i.e., at the clock frequency = 6.5MHz).

3.3.1 Single-rate design

The synthesis starts with the 1rad/s, 1Ω lowpass LCR prototype of a 0.5dB equiripple Chebyshev response. This must be scaled to give the desired lowpass bandwidth $(\omega_{b\omega} = 2\pi \cdot 0.6\text{Mrad/s})$. Now, because we will use bilinear *z*-transform integrators, which produce a frequency distortion to the lowpass response and this response is further distorted in the frequency shifting operation, we must scale to a pre-warped bandwidth, ω_p, which anticipates both these distortions. The strategy we adopted is as follows. First, we define a pre-warped frequency for the lower band edge $(\omega_{col} = 2\pi \cdot 0.4\text{Mrad/s})$ as ω_{pl} where:

$$\omega_{pl} = \frac{2}{T_s}\tan\left(\frac{\omega_{col} \cdot T_s}{2}\right) \tag{3.5}$$

where T_s is the sampling period (T_s = 1/13MHz = 76.92ns). Next, we define the pre-warped frequency for the higher band edge $(\omega_{coh} = 2\pi \cdot 1.6\text{Mrad/s})$ as ω_{ph} where:

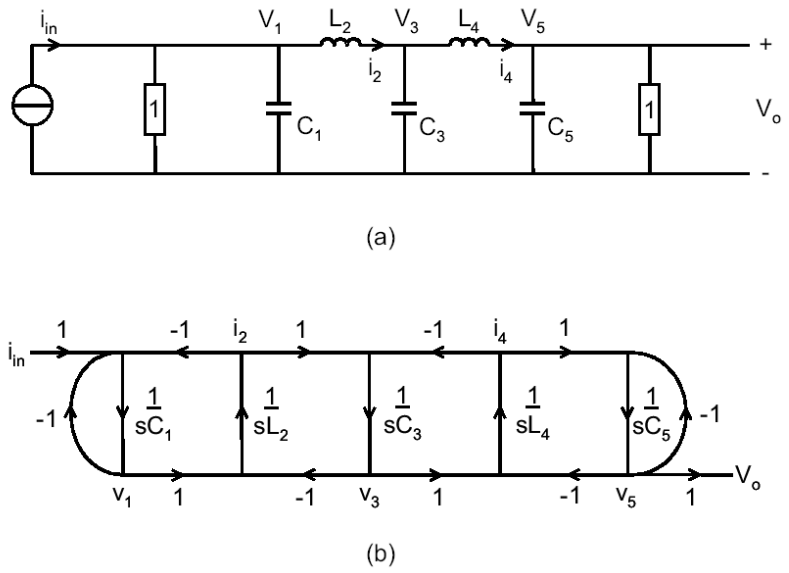


Figure 3.5: S-domain lowpass design (a) 5th-order lowpass prototype (b) SFG

$$\omega_{ph} = \frac{2}{Ts}\tan\left(\frac{\omega_{coh} \cdot T_s}{2}\right) \tag{3.6}$$

Then the pre-warping needed for the lowpass bandwidth (half the bandpass bandwidth) is given by ω_p where:

$$\omega_p = \frac{\omega_{ph} - \omega_{pl}}{2} \tag{3.7}$$

and the pre-warping needed for the frequency shift (the mid-band frequency) is given by ω_{p0} where:

$$\omega_{p0} = \frac{\omega_{ph} + \omega_{pl}}{2} \tag{3.8}$$

This gives $\omega_p = 4.0324\text{Mrad/s}$ (0.6418MHz) and $\omega_{p0} = 6.5536\text{Mrad/s}$ (1.0430MHz).

C_1	423.0nF
L_2	304.9nH
C_3	630.1nF
L_4	304.9nH
C_5	423.0nF

Table 3.1: Lowpass LCR prototype after scaling to pre-warped bandwidth

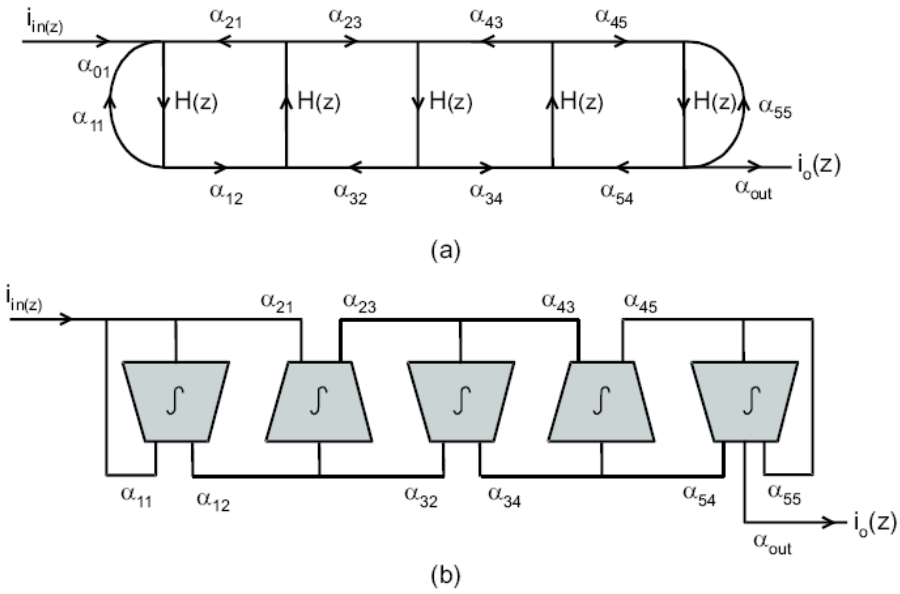


Figure 3.6: *z*-domain lowpass design (a) SFG (b) SI architecture

So, the lowpass LCR prototype is scaled to $\omega_p = 4.0324\text{Mrad/s}$ by dividing each capacitor and inductor of the 1rad/s prototype by ω_p and these are given in Table 3.1.

The scaled LCR prototype is shown in figure 3.5(a). Its nodal equations of the ladder network (R=1 in the prototype) are:

$$v_1 = \frac{1}{sC1}\left(i_{in} - \frac{v_1}{R} - i_2\right) \tag{3.9}$$

$$i_2 = \frac{1}{sL_2}\left(v_1 - v_3\right) \tag{3.10}$$

$$v_3 = \frac{1}{sC_3}\left(i_2 - i_4\right) \tag{3.11}$$

$$i_4 = \frac{1}{sL_4}\left(v_3 - v_{out}\right) \tag{3.12}$$

$$v_{out} = \frac{1}{sC_5}\left(i_4 - \frac{v_{out}}{R}\right) \tag{3.13}$$

These equations may be represented as a signal-flow graph (SFG) using state variables v_1, i_2, v_3, i_4 and v_5 as shown in figure 3.5(b). Each branch of the SFG corresponds to an integration.

Next, we translate this lowpass design into the *z*-domain by applying the bilinear mapping $s \to \frac{2}{T}\frac{1-z^{-1}}{1+z^{-1}}$ and then substituting,

$$\alpha_{01} = -\alpha_{11} = -\alpha_{21} = \frac{T_s}{2C_1} = 0.0909 \tag{3.14}$$

$$\alpha_{12} = -\alpha_{32} = \frac{T_s}{2L_2} = 0.1261 \tag{3.15}$$

$$\alpha_{23} = -\alpha_{43} = \frac{T_s}{2C_3} = 0.0610 \tag{3.16}$$

$$\alpha_{34} = -\alpha_{54} = \frac{T_s}{2L_4} = 0.1261 \tag{3.17}$$

$$\alpha_{45} = -\alpha_{55} = \frac{T_s}{2C_5} = 0.0909 \tag{3.18}$$

The resulting *z*-domain SFG of the lowpass design and the corresponding SI architecture are shown in figure 3.6(a) and (b).

Translating this lowpass design into its complex bandpass counterpart involves providing two paths, each containing the lowpass filter, and then replacing each pair of real integrators with a complex

integrator. This results in the SFG and SI architecture shown in figure 3.7(a) and (b). The cross-branch coefficient, α_0, for this design (F_0 = 1MHz) is given by:

$$\alpha_0 = \frac{\omega_{p0} T_s}{2} = 0.2521 \tag{3.19}$$

From figure 3.7(a), we see that as the currents owing at the first integrator's input $(\omega = 0)$ must sum to zero (and that each integrator output is derived from a pair of current mirrors), the input coefficient must be set to,

$$\alpha_{in} = 2\left(\alpha_{11} + \alpha_0 + \alpha_{21}\right) = 0.1406 \tag{3.20}$$

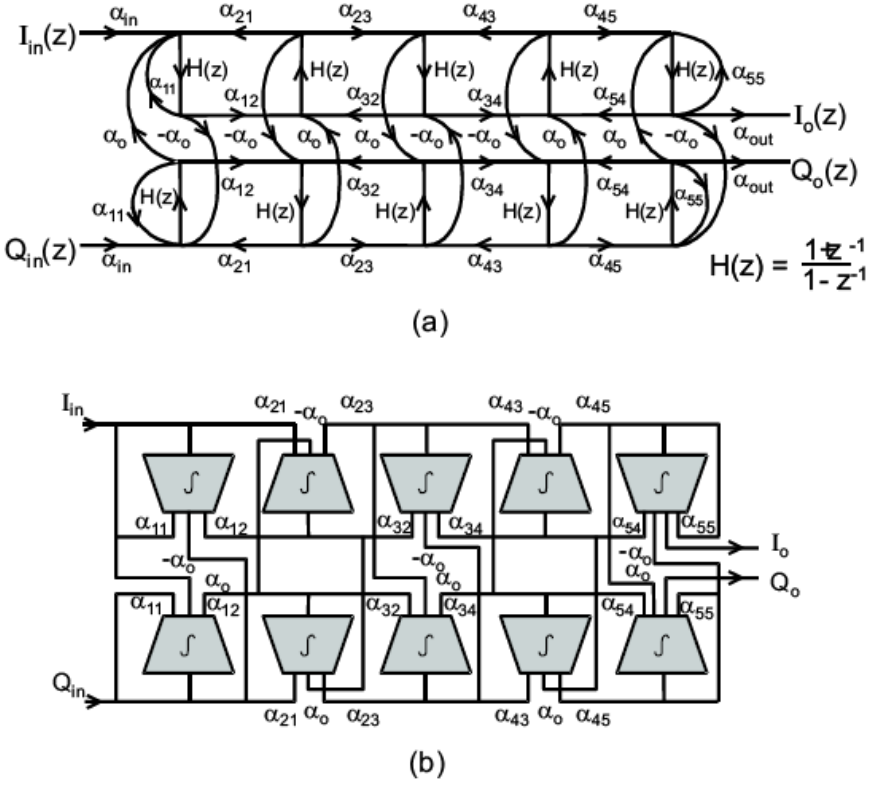


Figure 3.7: Single-rate complex filter structure (a) SFG (b) SI architecture

With $\alpha_{out} = 0.5$, the current gain at the centre of the passband is 0dB (instead of -6dB as in the prototype).

Behavioral models of the complex filter can be used to simulate the responses of each of the five complex integrator cores, as shown in figure 3.8(a). The first four integrators (I_1-I_4) have gains which peak above that of the output integrator (I_5) but have equal gain at the center of the passband. For some applications this would bring the risk of internal overload and would require internal gain redistribution to optimize the dynamic range. However, the Bluetooth spectral mask (figure 3.8(b)) falls rapidly at frequencies offset from the center and this safeguards against internal overload, making dynamic range optimization unnecessary.

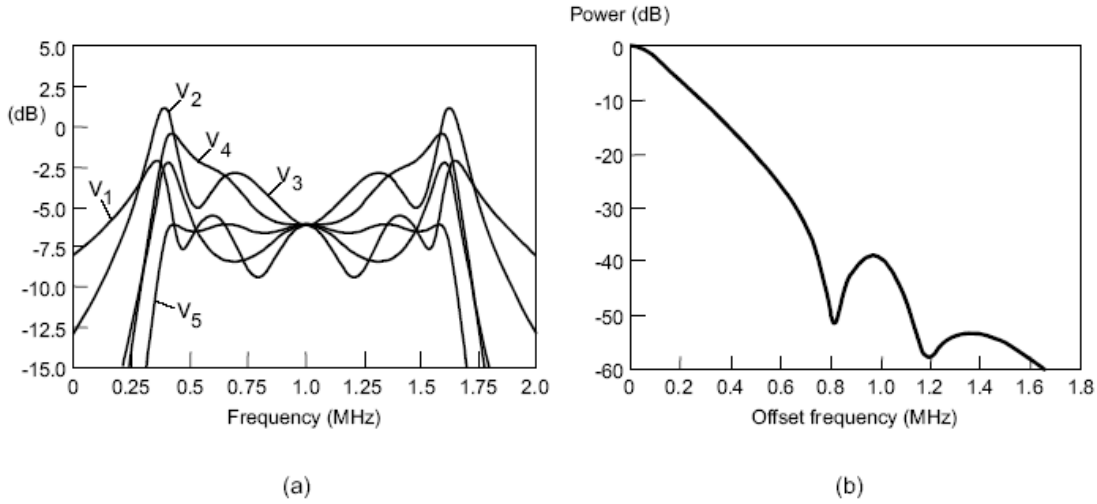


Figure 3.8: Internal signal responses (a) responses (b) GFSK spectral mask

3.3.2 Multi-rate design

All sampled-analogue signal processors require a continuous-time anti-alias pre-filter to prevent signals above the Nyquist frequency folding back to baseband. This filter is an overhead and should therefore be kept as simple as possible. When computed from Bluetooth specification, it should provide a

Butterworth response with at least 54dB attenuation at the sampling frequency and this problem is aggravated by the large spreads in IC time-constants. Even with a sampling frequency of 26MHz (i.e., twice the sampling frequency assumed in the last section), a third order lowpass Butterworth response is needed assuming $\pm 50\%$ spread in cut-off frequency. Unfortunately, doubling the sampling frequency to 26MHz would double the power consumption of the SI channel filter (SIF) while alternatively doubling the order of the anti-alias filter (AAF) creates unwarranted complexity.

The solution we have adopted is to use a multi-rate technique similar to that frequently adopted in SC [10]. In this technique, we place a decimator sampling at 26MHz between the AAF and the SIF which is sampling at F_s= 13MHz. As this decimation is only by a factor of two it can be created by a simple modification to the SIF input stage. The decimator is often called a 'cosine filter' because it adds an extra transfer response given by:

$$H_{dec}(e^{j\omega Ts}) = 2\left|\cos\left(\frac{\pi f}{2F_s}\right)\right| \tag{3.21}$$

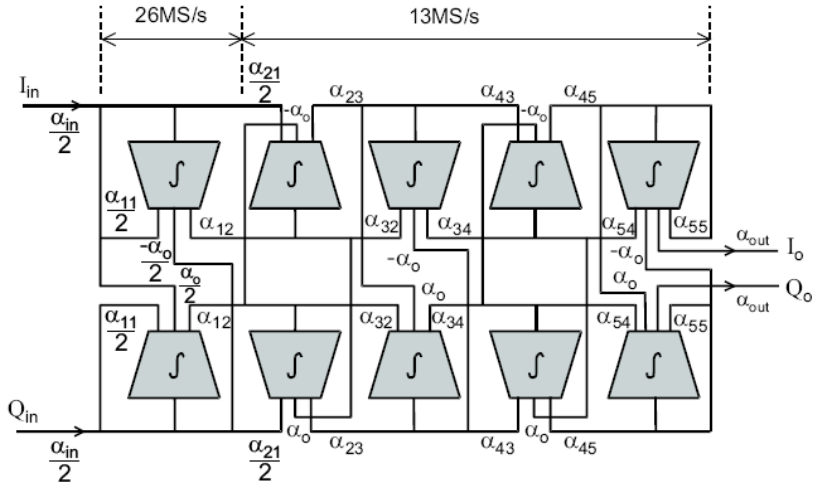


Figure 3.9: Multi-rate SIF architecture

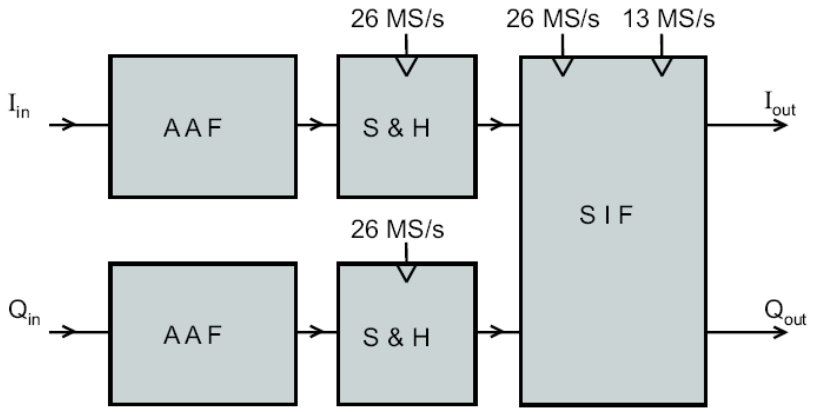


Figure 3.10: Architecture of multi-rate SI channel filter

This response has a peak amplitude of two at even multiples of F_s with nulls at odd multiples. Consequently, the decimator introduces a gain of 6dB and a small droop to the passband response.

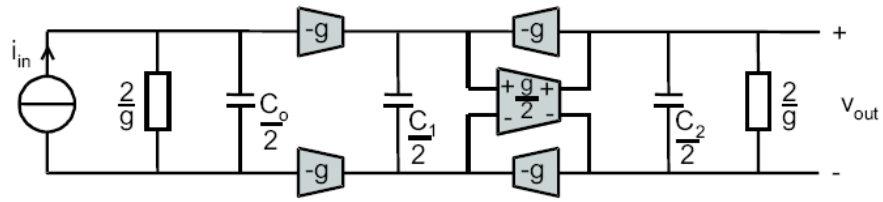


Figure 3.11: Anti-alias filter (AAF)

The changes to the SIF that introduce decimation are shown in figure 3.9. We see that the first complex integrator operates at 26MS/s while the remaining integrators operate at 13MS/s as before. Further, all coefficients connecting to the input are halved (to $\alpha_{in}/2$, $\alpha_{11}/2$, $\alpha_{21}/2$ and $\pm\alpha_0/2$) to maintain the gain at 0dB. The architecture of the total channel filter is shown in figure 3.10.

It is most convenient to use the Gm-C continuous-time technique for the AAF as similar transconductors to those of the SIF may be used. This allows the filter to operate from the same supplies and minimizes the SIF interfacing issues. Figure 3.11 shows a balanced 3rd order lowpass Gm-C filter. It comprises a first order section cascaded with a biquadratic section which uses both single-ended transconductors (g) and a balanced transconductor $(-g/2)$ which is needed to stabilize the feedback loop. The amplitude response is given by:

$$H(s)=\frac{v_{out}}{v_{in}}=\frac{A_0}{\left(1+s\frac{C_0}{g}\right)\left(1+s\frac{C_1}{g}+s^2\frac{C_1C_2}{g^2}\right)} \tag{3.22}$$

where A_0 is the low frequency gain defined by the relative transconductance of the first order section. The response of a 3rd order Butterworth is:

$$H(s)=\frac{A_0}{\left(1+\frac{s}{\omega_0}\right)\left(1+\frac{s}{\omega_0}+\frac{s^2}{\omega_0^2}\right)} \tag{3.23}$$

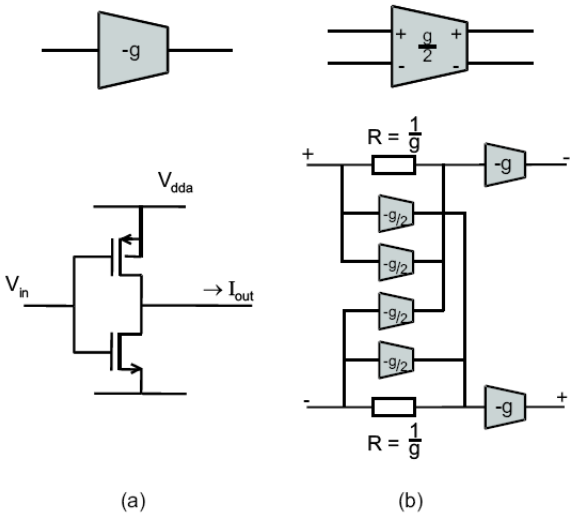


Figure 3.12: Transconductors used in AAF (a) single-ended (b) balanced

where ω_0 is the -3dB radian frequency which is to be set to $\omega_{co} = 2\pi \cdot 2\text{Mrad/s}$. Matching coefficients gives:

$$C_0 = C_1 = C_2 = \frac{g}{\omega_{co}} \tag{3.24}$$

The transconductors are similar to those used in [5] and are shown in figure 3.12. The single-ended transconductor is simply a pMOS/nMOS pair and produces linear transconductance, $g = 2g_m$ where $g_m = g_{mp} = g_{mn}$. The balanced transconductor is based on that proposed by Nauta and Seevinck and includes a pair of the same single-ended transconductors and a common-mode feedback arrangement of half-sized transconductors. The series resistors, R = 1/g, give the AAF common-mode rejection. Note that, as in the AAF, resistors and transconductors can be freely mixed because their relationship is preserved by the feedback arrangement used to regulate V_{dda}.

3.3.3 Combined anti-alias and sample-and-hold

Figure 3.13 shows the anti-alias filter connected to the sample-and-hold cell (S&H). The transconductors of the S&H are scaled by $\alpha_{in}/2$ so that it delivers the correct drive to the channel filter. As it has multiplexed operation, it presents a nearly constant differential input conductance of $\alpha_{in}G/4$. If the AAF output resistor is reduced to $2/\left(g - \alpha_{in}G/2\right)$ then the filter network remains correctly terminated.

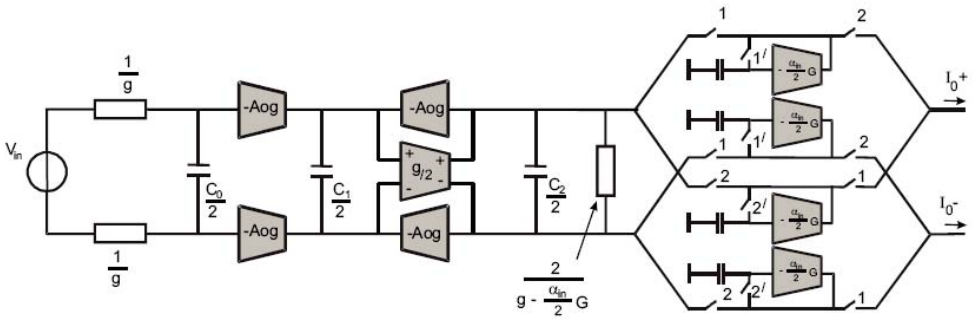


Figure 3.13: Combined anti-alias filter and sample-and-hold

3.3.4 Supply voltage regulation

One feature of the class AB transconductor cells is their sensitivity to the supply voltage. They are only practicable when operated from a regulated supply. One possible bias arrangement is shown in figure 3.14. The loop of transistors P_1, P_2, N_1, N_2 (P_1 has 4 times the width of P_2) adjusts its current until the transconductance of P_2 is $g_{m2} = 1/2R$. This current is mirrored via P_3 and summed with the current from N_3 which is a mirror of the current in the 'diode-connected' reference transconductor, P;N. If the current in N_3 is lower than that in P_3 then the charge pump is enabled and the gate of N_{reg} is pumped high. This raises V_{dda} until the currents become equal at which point the pump is disabled and the loop stabilizes. The resulting value of V_{dda} gives the reference transconductor, P;N a transconductance of $G = 1/R$ and as the rail also supplies the channel filter, its transconductors develop the same or scaled values of transconductance.

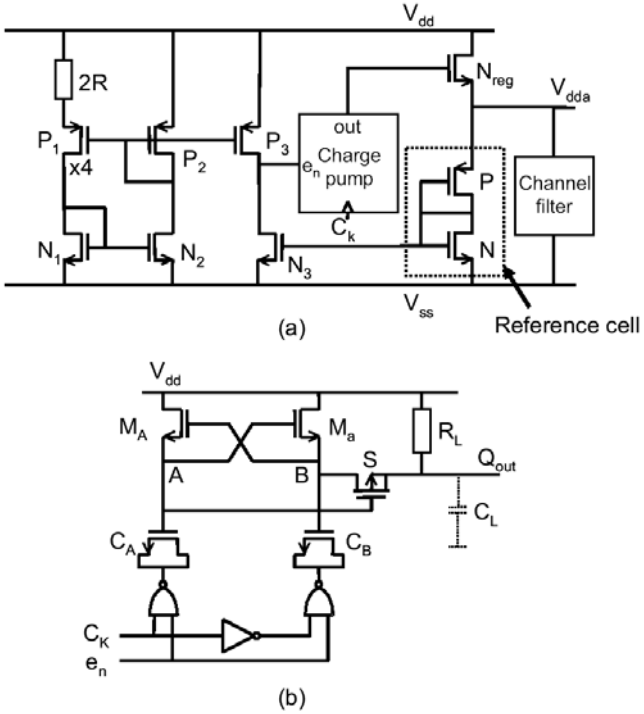


Figure 3.14: Supply voltage regulator

The sizing of the regulating transistor, N_{reg}, is a trade-off between power supply (both V_{dda} and V_{ss}) noise rejection which favors low W/L and output impedance which favors high W/L. Also, the regulating transistor may be a single transistor as shown or, as in this design, it may be segmented and distributed throughout the SI cells. This introduces a potential path mismatch error resulting from the random variations of individual regulator transistors but minimizes any crosstalk between the I- and Q-channels.

4. Electrical Filter Design

We have established an architecture for our channel filter which is to include an anti-alias filter (AAF) combined with a sample-and-hold (S&H) in each path and followed by the multi-rate complex SI filter (SIF) as shown in figure 4.1. The task of this section is to perform the transistor level design of the cells so that the required signal-to-noise ratio of the whole channel filter (SNR) of 65.3dB is achieved with minimum power consumption. This can be done by partitioning the power budget between the continuous-time block (AAF) and the sampled-analogue block (S&H and SIF). Then, given the required bandwidth, the SNR of the memory cells is designed. Finally, the transistor sizes and bias currents for the memory cells can be found via the procedure outlined in detail in [11].

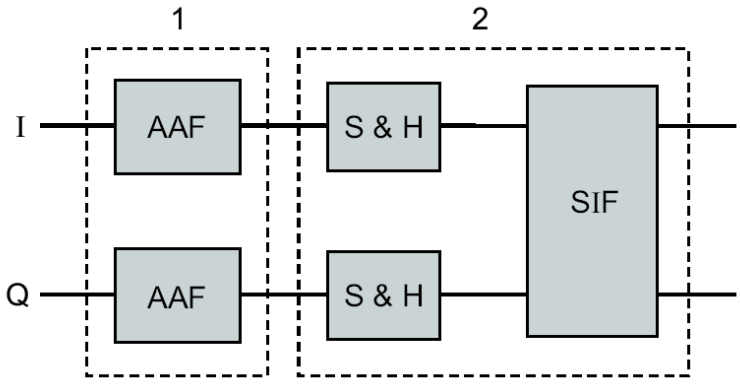


Figure 4.1: Partitioning for power optimization

If we consider the two main circuit blocks shown in figure 4.1, the optimum power partition between block 1 and block 2 is when *P/SNR* is minimized where *P* is the total power consumption of both blocks and *SNR* is the overall signal-to-noise ratio. We have:

$$\frac{1}{SNR} = \frac{1}{SNR_1} + \frac{1}{SNR_2} = \frac{A_1}{g} + \frac{A_2}{G} \tag{4.1}$$

where A_1 and A_2 are constants which may be determined empirically from simulations of each type of circuit. Also, the total power consumption, *P*, in terms of the separate power consumptions, P_1 and P_2, is given by:

$$P = P_1 + P_2 = B_1 g + B_2 G \tag{4.2}$$

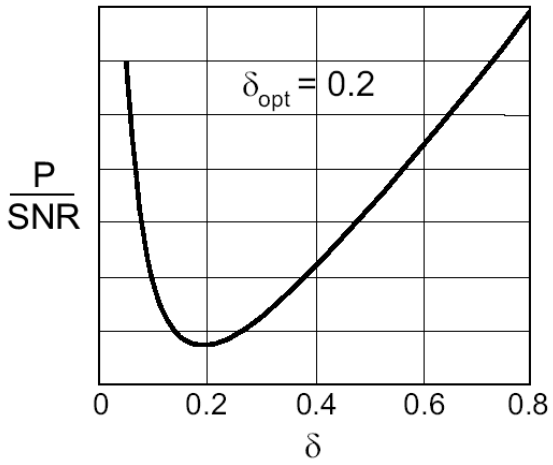


Figure 4.2: Optimisation of $\frac{P}{SNR}$

where B_1 and B_2 are also constants which may be determined empirically from simulations of each type of circuit. If we put $g = \delta \cdot G$ then it can be shown that:

$$\frac{P}{SNR}=\left(\frac{A_1}{\delta}+A_2\right)\left(\delta B_1+B_2\right) \tag{4.3}$$

The constants were evaluated experimentally for the process to be used and the function plotted as shown in figure 4.2.

This indicates a minimum at about $\delta=0.2$ but, as the slope of the curve below the minimum is rather steep, a more robust design value of $\alpha=0.3$ was used. So, for the SIF using a (single-ended) transconductance of G, the AAF used a transconductance of g=0.3G and the S&H used a transconductance of $\alpha_{in}G/2=\left(\alpha_{11}+\alpha_0+\alpha_{21}\right)G=0.0703G$. These transconductances are easily realised by linearly scaling the transistor widths with respect to the reference transconductor (G). With all cells operating from the same supply voltage, this linearly scales the transistor bias and signal currents but preserves the internal voltage swings throughout the design. Note that the first integrator of SIF samples at twice the rate (26MHz) of the other integrators and so is designed with the same transconductance (G) but half the total capacitance $\left(C_{tot}/2\right)$ to achieve memories with twice the bandwidth.

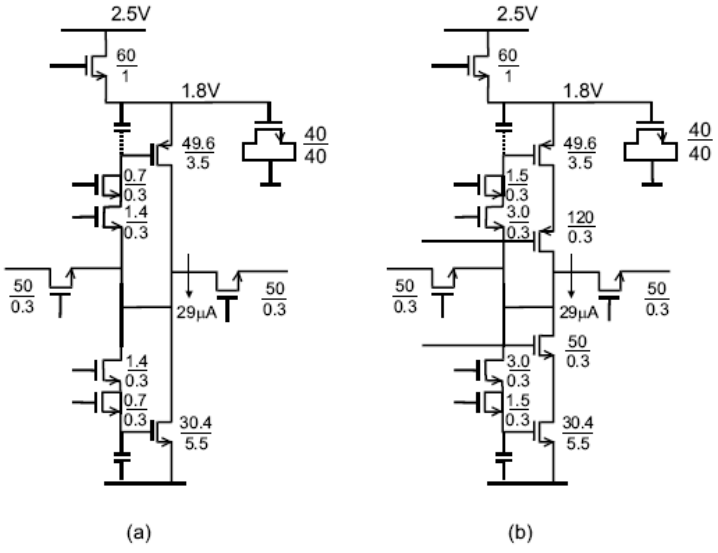


Figure 5.1: Reference memory cells (a) basic (b) cascaded versions

5. Simulated Performances

The multi-rate channel filter (AAF, S&H and SIF) with dynamic element matching (DEM) in the first integrator was designed in the AMS 0.35μm CMOS process with both the basic and cascoded memory designs (figure 5.1). The prototype filter designs were evaluated via simulations. The experimental results of the real silicon filter implementation will be given in the next section.

Figures 5.2 and 5.3 show the simulations of the overall amplitude response and the passband response of channel filter (AAF+S&H+SIF) using behavioural models for single-rate and multi-rate schemes. Note that the 1dB passband droop of the multi-rate response in figure 5.3 is due to the 'cosine' filtering of the decimation at the input of the first integrator.

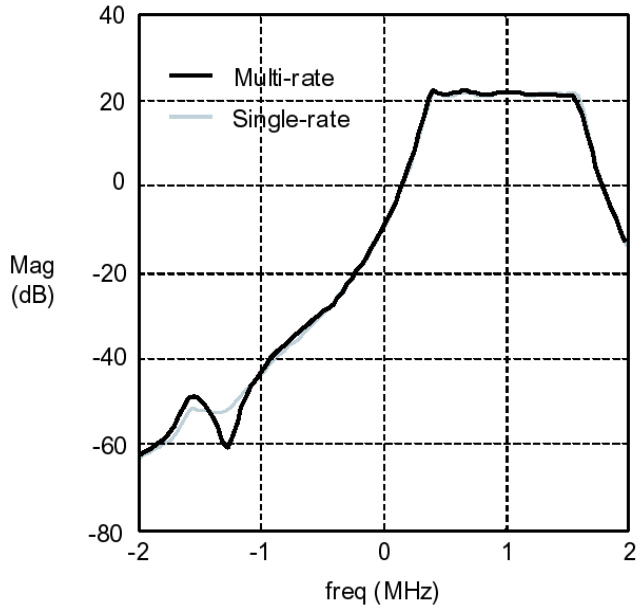


Figure 5.2: Behavioral simulation of channel filters' amplitude response for single-rate and multi-rate architectures

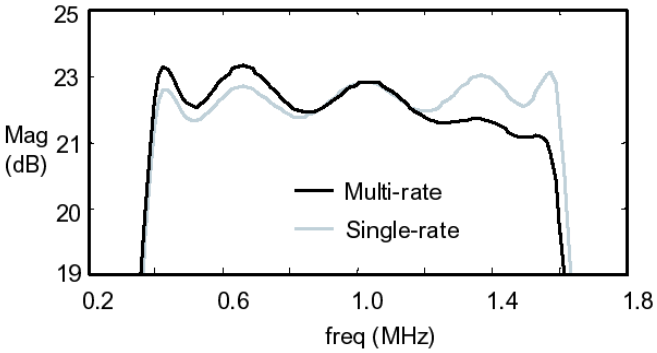


Figure 5.3: Behavioral simulation of channel filters' passband response for single-rate and multi-rate architectures

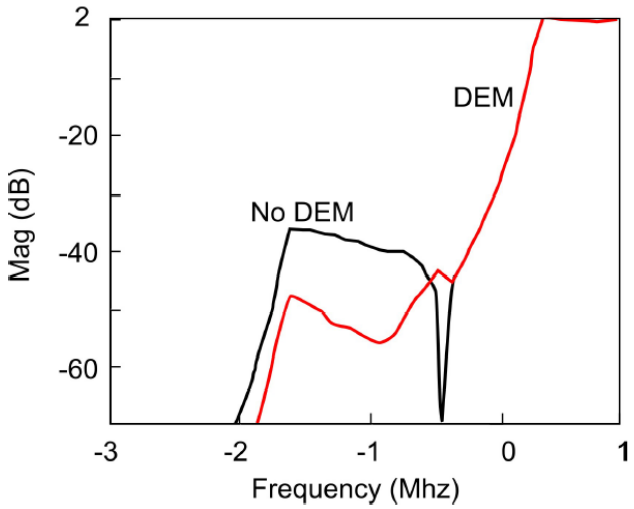


Figure 5.4: Behavioral simulation of channel filters' passband response with 5% path mismatch

Figure 5.4 shows the behavioural simulation of the channel filter response with 5% mismatch between the I-path and the Q-path with DEM both active and inactive. This shows that, without DEM, the path mismatch reduces the image band rejection (*IBR*) to about 35dB. However, with DEM active in the first integrator, this is increased by a further 15dB to about 50dB.

Figures 5.5 and 5.6 show the transistor-level simulation of the channel filters' overall and passband amplitude responses for extreme process corners and with both basic and cascoded memory designs. The cascode version shows a passband response which is nearly ideal with 0.5dB ripple and a gain of about 22.5dB with 2dB droop produced partly by the 'cosine' filtering of the multi-rate design and partly by the extra passband droop of the AAF. The band edges are very close to the specification for all process corners. The image response indicates a worsening but still adequate image band rejection (*IBR*) for slow processing ($\geq$ 42dB at 1MHz). The basic version shows a passband response with less gain (about 19.9dB), less passband ripple and rounded passband edges, all the result of finite drain resistances of the basic cell memory transistors. However, as the spectral mask of the GFSK modulation used in Bluetooth peaks at the centre of the passband the small loss of energy resulting from the degraded passband edges produces negligible loss of BER (confirmed by system simulation). The 1MHz *IBR* is about 46 dB.

The 1dB compression point occured with a peak differential amplitude of 50mVp at the filter inputs. This is because compression first occurs in the AAF which is common to both versions of the filter. Figures 5.7 shows the simulated output noise spectrum for the basic and cascode versions under typical, 40^{o}C conditions. The 1MHz noise densities are 35fV^2/Hz and 45fV^2/Hz respectively giving input refered noise densities of 18.9nV/$\sqrt{Hz}$ and 15.9nV/$\sqrt{Hz}$ and a *SNR* of 64.6dB and 66.1dB respectively.

Figure 5.8 shows the simulated output spectra of the basic and cascoded versions under typical, 40C conditions for differential inputs of 15mVp at frequencies of 4MHz and 7MHz producing a third order product at 1MHz. Using the formula,

$$IIP3 = \frac{3v_{in} + A_0 - v_{out}}{2} \tag{1}$$

where v_{in} and v_{out} are the amplitudes of the input sinusoids (-36.5dBVp at 4MHz and 7MHz) and output intermodulation product (at 1MHz), and A_0 is the mid-band voltage gain, *IIP3* is 4.2dBVp (basic) and 0.5dBVp (cascoded) for near blockers. The extra spurs at 6.5MHz and 0.5MHz in figure 5.8 are thought to be the result from clock feedthrough (6.5MHz for 13MHz double sampling) and mixing of the clock

with the 7MHz input signal respectively. The *IIP3* for more distant blockers (6MHz,11MHz) was expected to be higher because the AAF had greater attenuation at these higher frequencies but this was not the case. This indicates that most of the third-order distortion responsible for the disappointing *IIP3* is occuring in the AAF rather than the SIF and suggests that *IIP3* could be improved by redistributing the gain from the AAF to the SIF output stage.

The V_{dda} regulator maintained constant transconductance in the SI memory cells over process and temperature extremes through proper control of the memory bias currents. The bias current (J) was 44μA (slow, 0C), 29μA (typical, 40C) and 20.5μA (fast, 125C). Monte-Carlo dc simulation of the integrator core memories showed that the bias current stayed within 3% due to random process spreads.

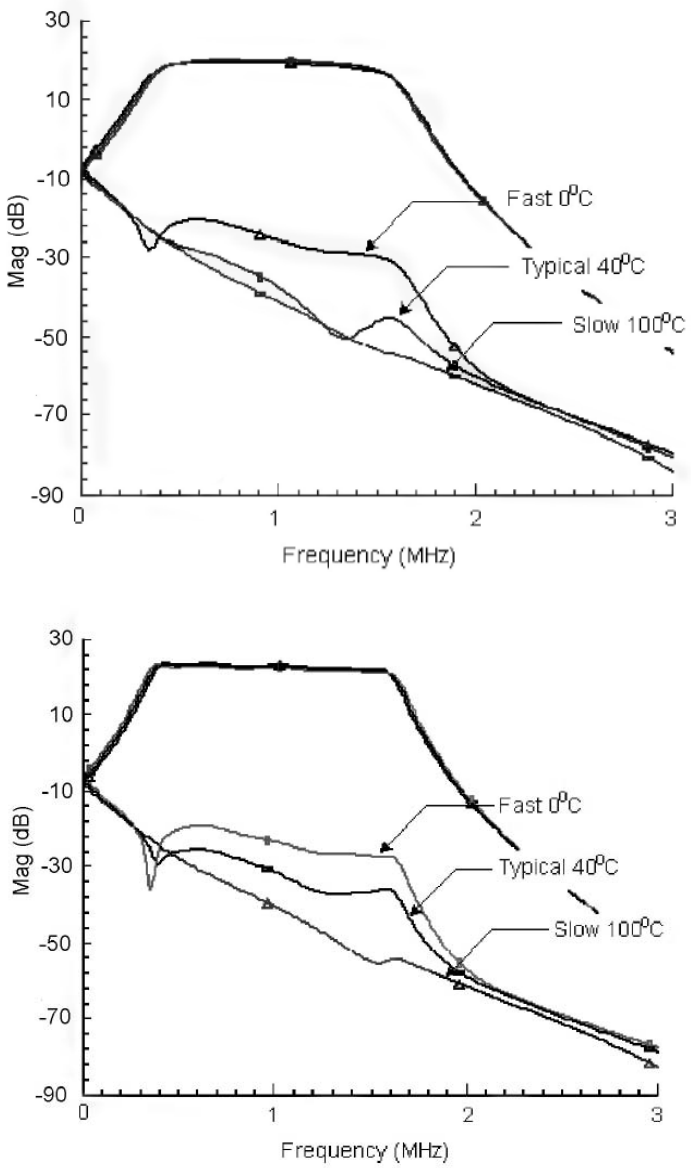


Figure 5.5: Transistor-level simulation of basic (upper) and cascode (lower) channel filter's amplitude response

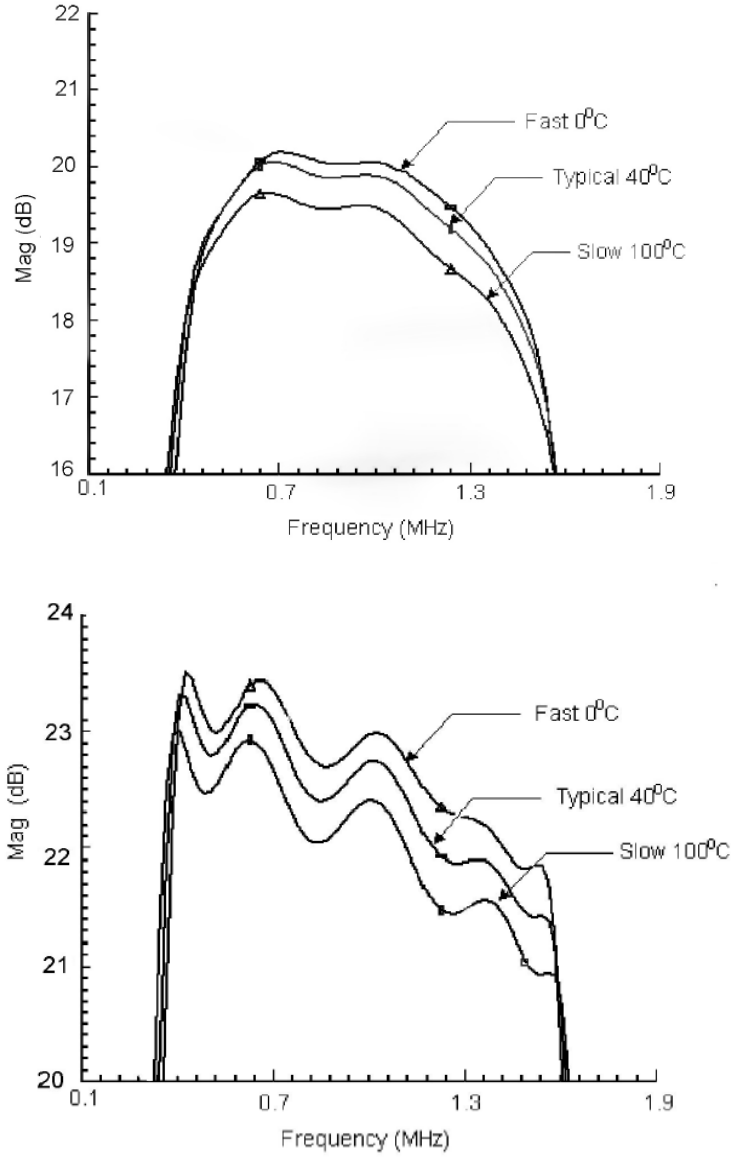


Figure 5.6: Transistor-level simulation of basic (upper) and cascode (lower) channel filter's passband response

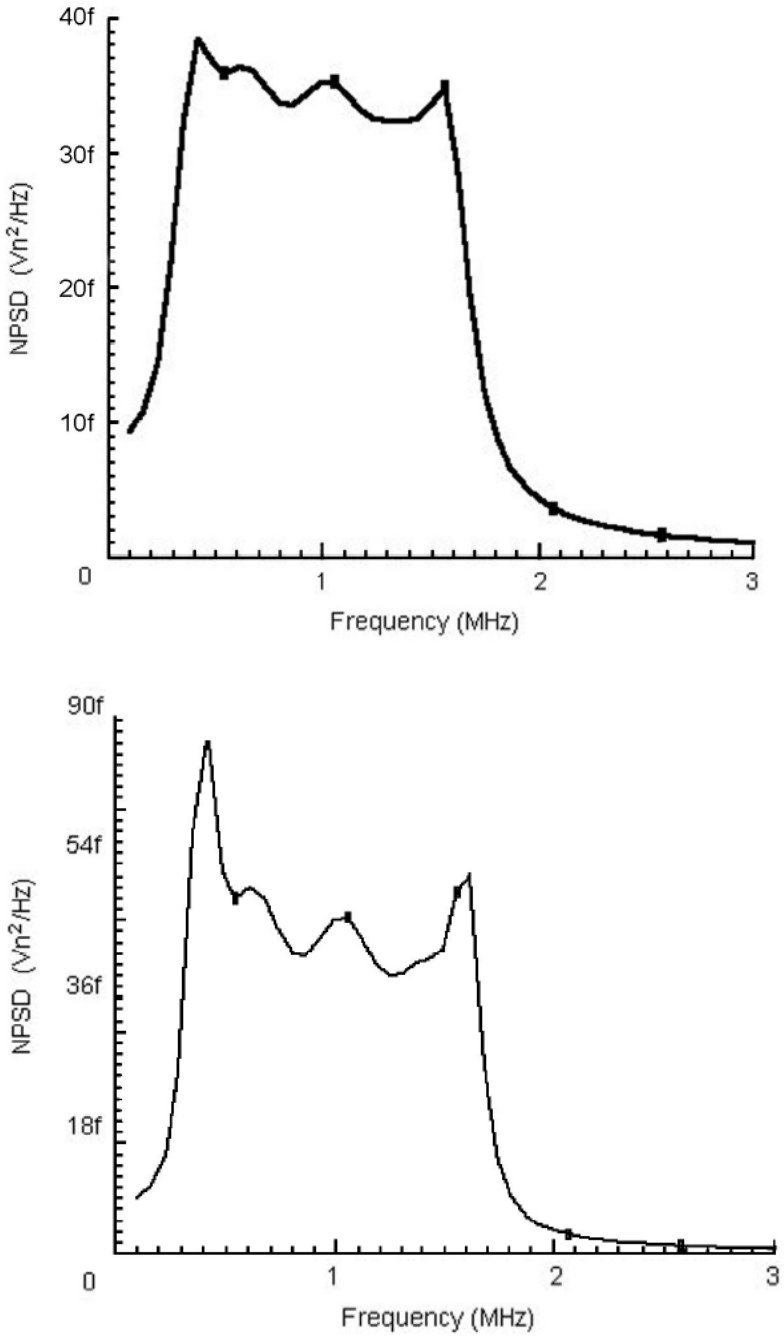


Figure 5.7: Simulated output noise of the basic (upper) and cascode (lower) channel filter with typical processing and 40C

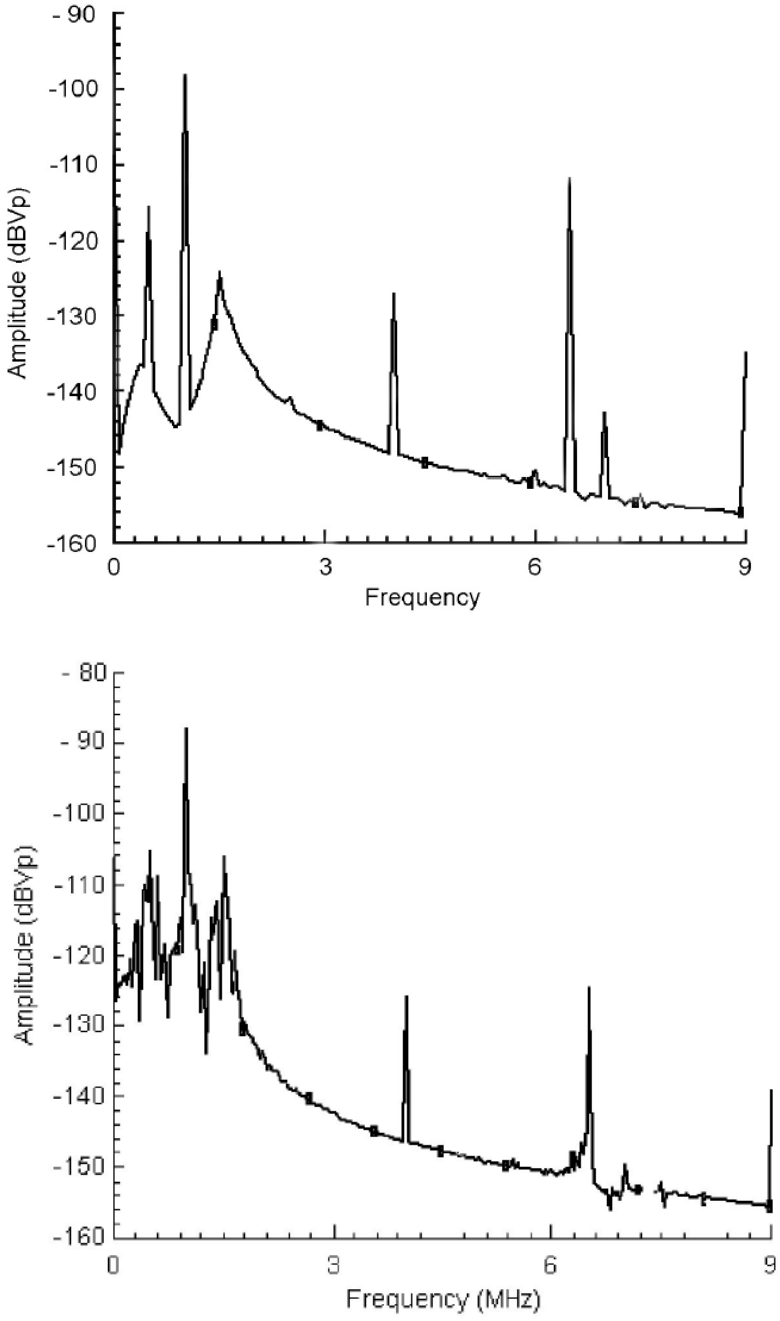


Figure 5.8: Simulated output spectrum of the basic (upper) and cascode (lower) channel filter for the *IIP3* test with typical processing and 40C

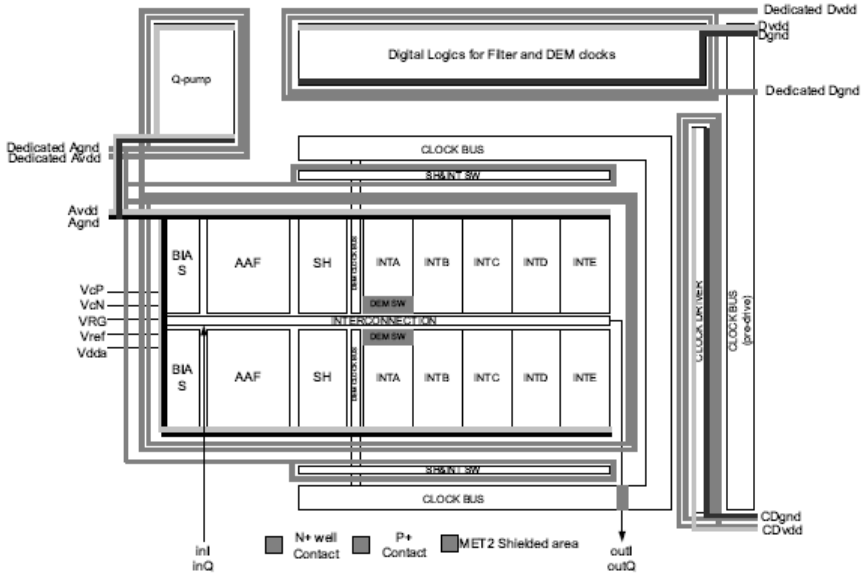


Figure 6.1: Chip floorplan of the SI filter

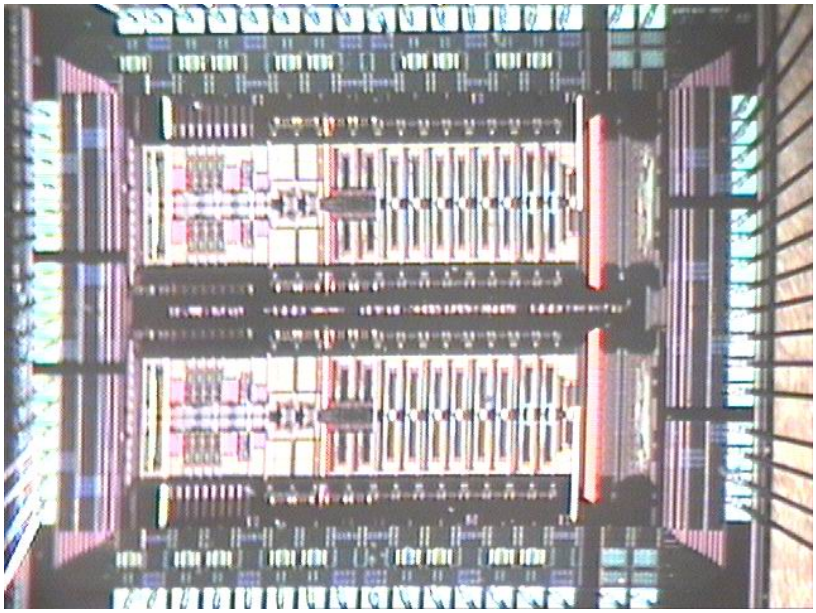


Figure 6.2: Chip micro photograph

6. Experimental Results

Figure 6.1 shows the chip floorplan for the basic and cascode SI filters. The chip microphotograph is given in figure 6.2 with the basic version at the top and the cascode version at the bottom part of the die. Note that the layout for the basic filter is derived from the cascode version without further compaction.

Figures 6.3 and 6.4 show the experimental results of the overall amplitude responses and the passband responses respectively of basic and cascode multi-rate SI channel filters (AAF+S&H+SIF). Notice the 2.5dB passband droop of the multi-rate responses in the figures as anticipated from simulation. Also, the basic version has more rounded passband edges due to a finite drain resistance. Both the cascode and basic filters show passband responses with less gain and less passband ripples compared to simulations. This is due to parasitic capacitance effects which was not taken into account during simulations. Again, due to parasitic capacitances, the gains of the filters at 1MHz are less than the simulated values, i.e. 20.4dB (from 22.5dB) for the cascode and 16.9dB (from 19.9dB) for the basic circuit. The image responses indicate adequate image band rejection (*IBR*) with 45dB for the cascode and 49dB for the basic version. Note that this level of image rejection is obtained without the need to activate the DEM, indicating good matching between the filters' I- and Q- paths as a result of careful layouts.

Figure 6.5 show the measured plots between input and output voltages at 1MHz frequency. The plots indicate differential input 1dB compression points at 48.5mVp (-29.3dBV$_{rms}$) for the basic and 44.6mVp (-30.1dBV$_{rms}$) for the cascode filters. The basic version exhibits a larger 1dB compression point because it has a smaller filter gain. Figures 6.6 shows the measured output noise spectrum for the basic and cascode versions where, at 1MHz noise, the differential noise densities are 16.48fV^2/Hz and 23.08fV^2/Hz respectively giving input referred noise densities of 15.1nV/$\sqrt{Hz}$ and 12.7nV/$\sqrt{Hz}$ and *SNR's* of 67.4dB and 67.03dB respectively.

Figure 6.7 shows the inter-modulation plots at frequencies of 4MHz and 7MHz which produces a third order product at 1MHz. It suggests almost identical third-order input intercept point (*IIP3*) of

1.5dBVp and 2dBVp for the basic and cascode filters respectively. This result confirms the assumption that most of the third-order distortion responsible for the *IIP3* is occuring in the AAF rather than the SIF. So, the *IIP3* could be improved by simply redistributing the gain from the AAF to the SIF's output stage.

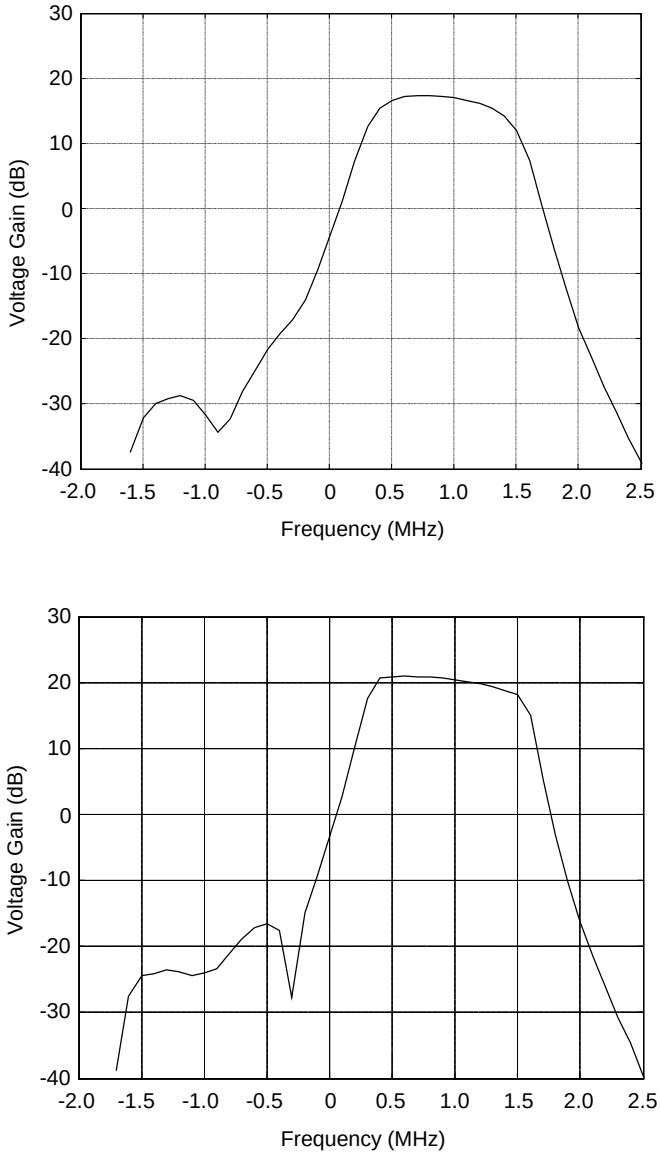


Figure 6.3: Measured results of basic (upper) and cascode (lower) channel filter's amplitude response

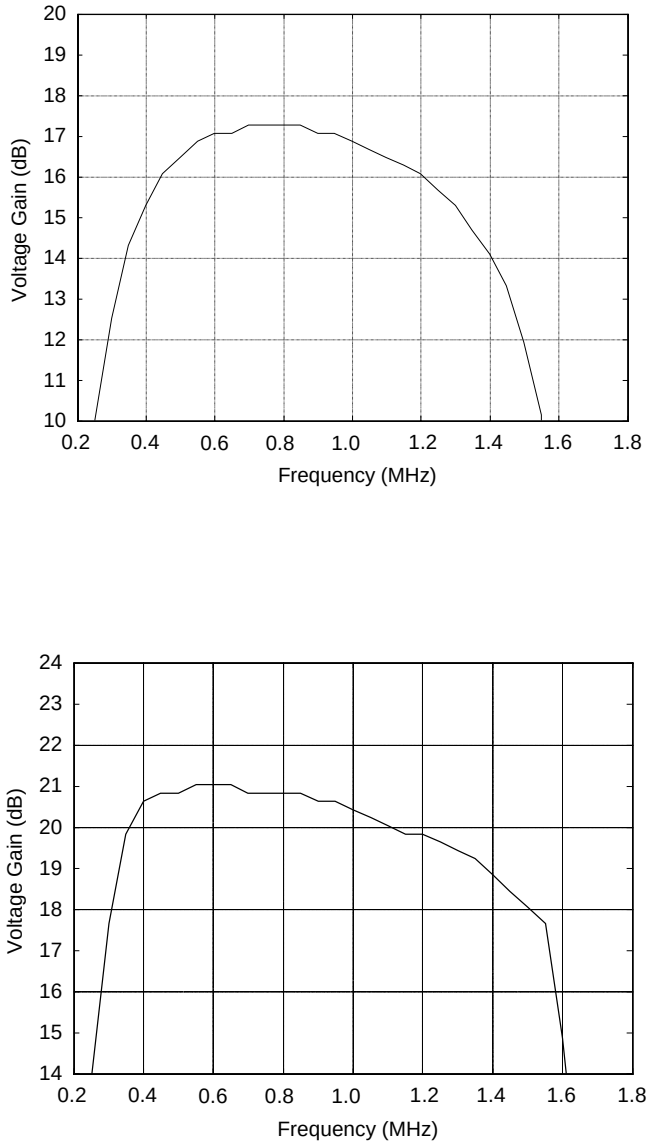


Figure 6.4: Measured results of basic (upper) and cascode (lower) channel filter's passband response

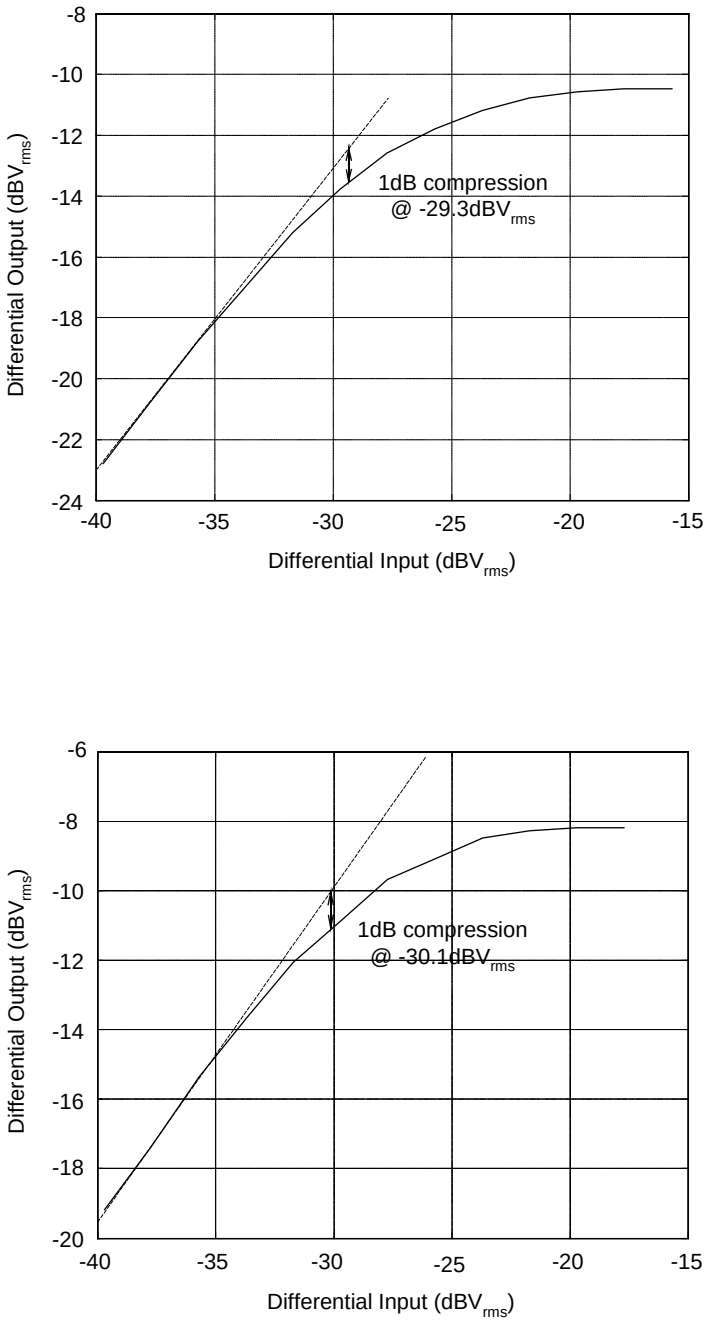
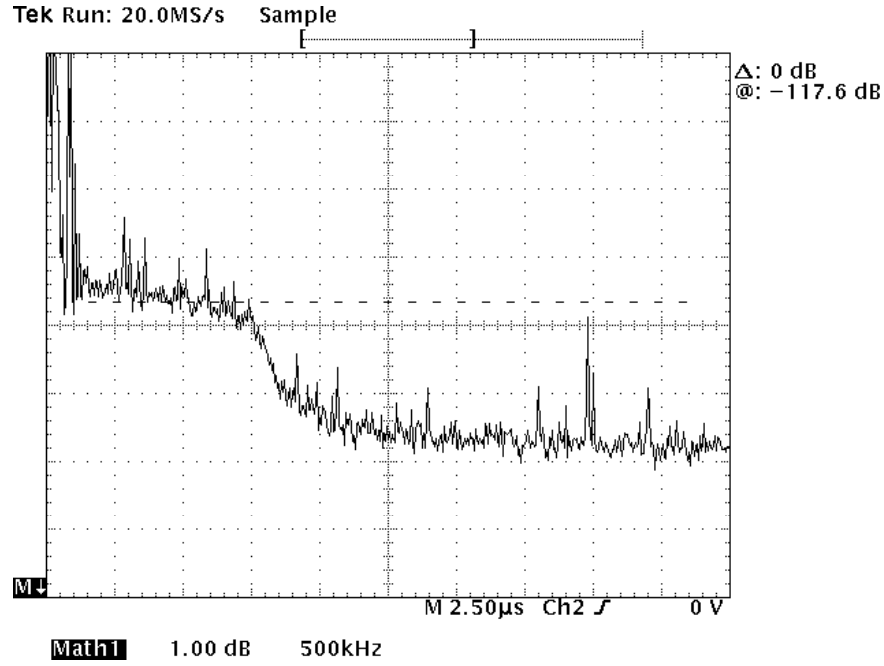


Figure 6.5: Measured 1dB compression plots of the basic (upper) and cascode (lower) channel filter.



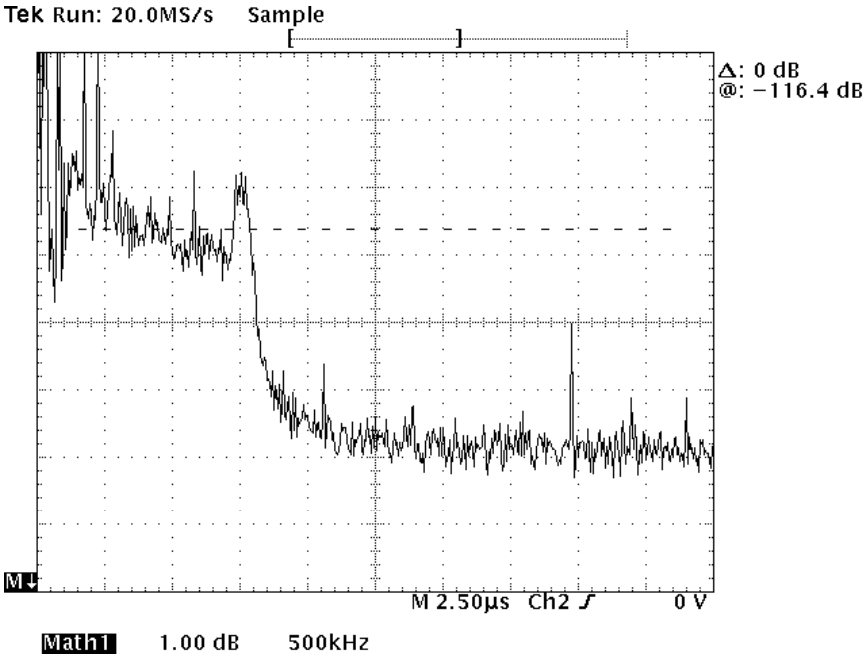
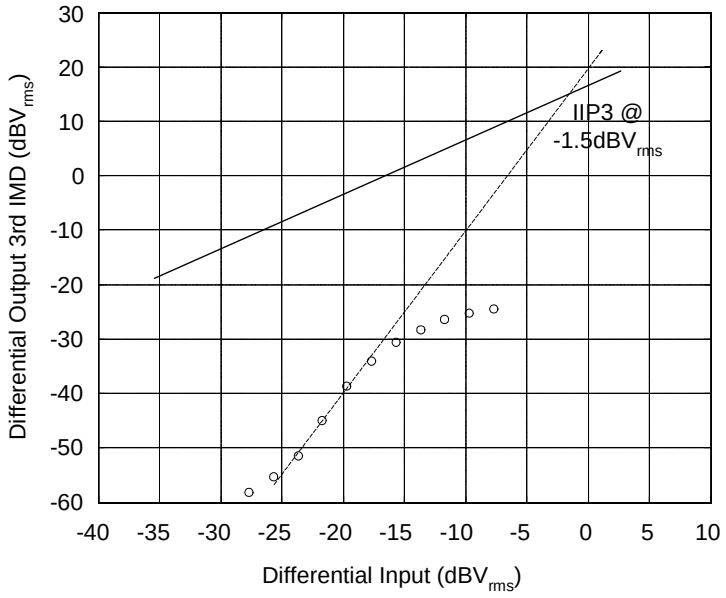


Figure 6.6: Measured output noises of the basic (upper) and cascode (lower) channel filter.



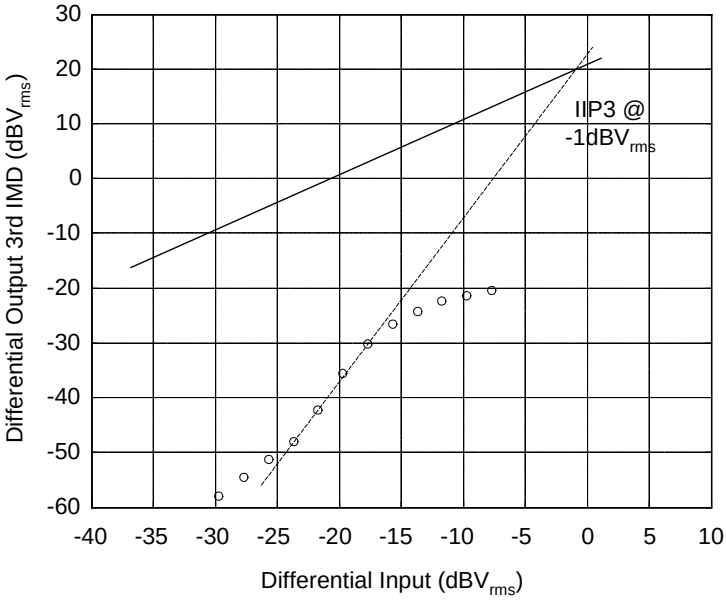


Figure 6.7: Measured third-order intercept point plots of the basic (upper) and cascode (lower) channel filter.

7. Conclusion

This research work has reported the investigation of a low voltage, low power channel select filter for Bluetooth using switched-current (SI) techniques in a digital CMOS process. It started with a resume of the rationale behind the use of SI for low voltage CMOS. This indicated that while alternative voltage mode circuit techniques (switched-capacitors or op-amp RC) lose performance in low voltage processes, SI maintains its overall performance and benefits are expected with CMOS processes operating at 1.5V and below.

Following a review of class AB SI cells, an SI complex bandpass channel select filter for Bluetooth (1MHz centre frequency and 1.2MHz bandwidth) was developed. The synthesis was based on the 'leapfrog' simulation of a double-terminated fifth-order 0.5dB Chebyshev LCR ladder prototype. The architecture used a third-order anti-alias Gm-C filter (AAF) and a double-sampling sample-and-hold (S&H) in each channel, followed by the complex SI bandpass filter (SIF). This SIF employed a multi-rate technique using a 26MHz clock for the first integrators and 13MHz in the others to produce 'cosine' filtering for easing the AAF specification. The S&H used balanced SI class AB memories in a double-sampling arrangement and the SIF used balanced SI double-sampling bilinear *z*-transform integrators, also using balanced SI class AB memories. To improve the degradation of image band rejection (*IBR*) resulting from path mismatch, the first integrators used 'dynamic element matching' (DEM).

The electrical design was then performed for a AMS 0.35μm digital CMOS process. The resulting filter was simulated using both behavioral and transistor-level models. These demonstrated that the filter design produced the correct response. With the cascoded cell design the transistor-level simulation of amplitude response was nearly ideal but with the basic cell design there was a noticeable rounding of the passband corners and an attenuation of the passband ripple. Neither of these defects is expected to be serious because the GFSK modulation used by Bluetooth has most of its spectral energy near the centre of the passband and so there is negligible impact on BER. With a path mismatch of 5%, the use of DEM increased the *IBR* by about 15dB given typical values of 46dB (basic) and 42dB (cascode). The signal-to-noise ratios were 64.6dB (basic) and 66.1dB (cascode) and the out-of-band third-

order intermodulation products for near interferers (4MHz/7MHz) were 4.2dBVp (basic) and 0.5dBVp (cascode). So, as cascode memories occupy more area and have worse *IIP3* and *IBR*, the basic version may be a better option. Nevertheless, the actual choice must be selected based upon experimental results.

The designed basic and cascode filters were also implemented in real silicon. The measured amplitude responses exhibit overall shapes similar to simulations but with attenuation of the passband gain and passband ripple in both of the filters. This is attributed to parasitic capacitances that were not taken into account in the reported simulation results. Also, as expected from simulation in the last section, the rounding of the passband corners and attenuation of the passband ripple are larger in the basic design. Again, neither of these defects is critical for Bluetooth radio. The realized filters exhibit *IBR* better than 49dB (basic) and 45dB (cascode). The signal-to-noise ratios were 67.4dB (basic) and 67.03dB (cascode) and the out-of-band third-order intermodulation products for near interferers (4MHz/7MHz) were 1.5dBVp (basic) and 2dBVp (cascode). Both filters consume 2.7mA of current at 2.0V supply voltage.

The summary of the filters' measured performances is given in Table 7.1 in compareison with the desired specifications. It can be seen that the overall performance of both the filters are almost equivalent except that the cascode version has the measured gain closer to specification of 22.5dB and so it is eventually seen as the preferred choice. Although the filter performance in terms of the *IIP3* is less than the requirement of 10dBVp, this can be easily dealt with by re-distributing the gain from the front anti-alas filter (AAF) to the SI filter output. Note that the input referred noise will be increased but this is completely feasible since the SNR performance is about 1.7dB more than the require specification.

	Specification	*Basic filter*	*Cascode filter*
Gain @1MHz	22.9dB	16.9dB	22.4dB
Input Refered Noise Density	-	$15.1\text{nV}/\sqrt{Hz}$	$12.7\text{nV}/\sqrt{Hz}$
Input Refered 1dB Compression	-	48.5mV_p	44.6mV_p
Signal-to-Noise-Ratio	65.3dB	67.4dB	67.03dB
IIP3 (4MHz, 7MHz)	10dBV_p	1.5dBV_p	2dBV_p
IBR @1MHz	>20dB	49dB	45dB
CMRR 1MHz	-	50dB	52dB
Supply Voltage	-	2.0V	2.0V
Supply Current	-	2.75mA	2.7mA
Chip Area	-	$2500\text{x}690\mu\text{m}^{2*}$	$2500\text{x}690\mu\text{m}^2$

* The layout for the basic filter is derived from the cascode version without further compaction.

Table 7.1 Summary of the filters' performances

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Output จากโครงการวิจัยที่ได้รับทุนจาก สกว.

1. ผลงานตีพิมพ์ในวารสารวิชาการนานาชาติ

   จะได้ทำการส่งต้นฉบับบทความ ชื่อ “A Low-voltage Multi-rate Switched-current Technqiues for Bluetooth Complex Channel-select Filter” ไปยังวารสาร IEEE Journal of Solid-state Circuits

2. การนำผลงานวิจัยไปใช้ประโยชน์
   - เชิงวิชาการ งานวิจัยในโครงการนี้ ก่อให้เกิดนักวิจัยใหม่ขึ้น คือ ดร.รังสิมันต์ สิทธิกร ซึ่งเป็นนักวิจัยผู้ช่วยของโครงการ

3. อื่นๆ คือผลงานตีพิมพ์ในที่ประชุมวิชาการในประเทศ ดังนี้
   - รังสิมันต์ สิทธิกร, อภิศักดิ์ วรพิเชฐ และ John B. Hughes, “วงจรกรองความถี่เชิงซ้อนชนิด ผ่านแถบมีอัตราการกินไฟต่ำโดยใช้โครงสร้างชนิดทรานส์คอนดักเตอร์-ตัวเก็บประจุสำหรับเครื่องรับส่งไร้สายชนิดไอเอฟต่ำ”, A Transconductor-Capacitor Based Low-Power Complex Bandpass Filter Structure For Low-IF Wireless Transceivers, การประชุมวิชาการทางวิศวกรรมไฟฟ้า ครั้งที่ 25 (EECON-25) มหาวิทยาลัยสงขลานครินทร์, หน้า 11-15, 21-22 พฤศจิกายน 2545.
   - R. Sittdhikorn, A. Worapishet and J.B. Hughes, "A Low-Power Multi-Rate Switched-Current Channel Filter with Dynamic Element Matching for Low-IF Bluetooth Wireless Receiver", การประชุมวิชาการทางวิศวกรรมไฟฟ้า ครั้งที่ 26 (EECON-26) สจพ., หน้า 1355-1358, 6-7 พฤศจิกายน 2546.